CDB44800

Evaluation Board For CS44800

Features

- Eight Output Channels
- Configurable for full-bridge or half-bridge operation, allowing evaluation of different output power levels and BOM options.
- Single Positive Voltage Supply for Amplified Audio Outputs
- CS4461 for Power Supply Rejection Feedback
- Header for External Serial Audio I/O
- Adjustable Power Supplies for Easy Configuration
- Software provided to configure the board.
- Demonstrates recommended layout and grounding arrangements.

Description

The CDB44800 demonstration board is an excellent means for evaluating the CS44800 eight-channel Class-D PWM modulator. Evaluation requires a digital audio signal source, analog audio analyzer, and power supplies.

Clocks and data can be provided to the CS44800 by the CS8416 S/PDIF receiver or by an I/O header. PWM output from the CS44800 is amplified using the Philips TDA8939 power stage. The CS4461 is used for power supply rejection. A line out and headphone driver are provided as well. A comprehensive GUI provides control over the functions of the CS44800, CS4461, CS8416, and Philips TDA8939.

ORDERING INFORMATION

CDB44800 Evaluation Board

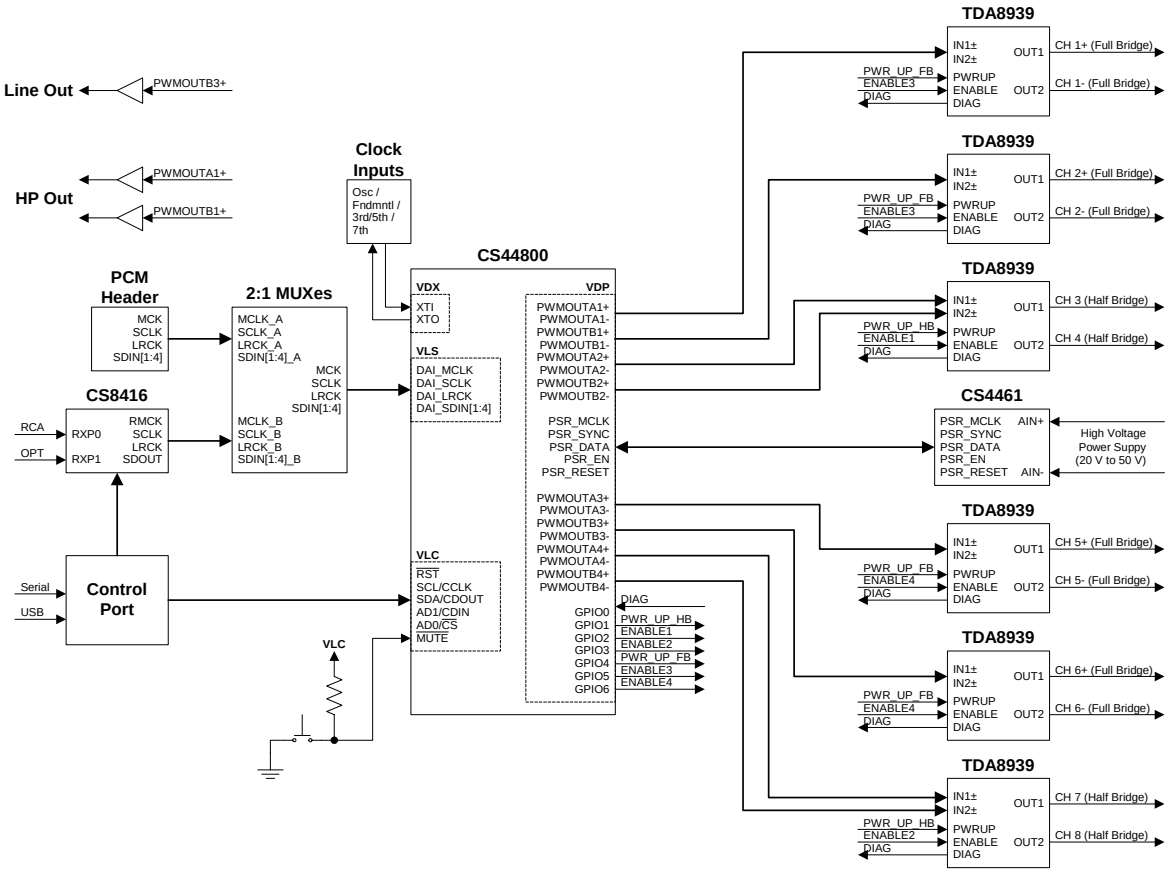


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. SYSTEM OVERVIEW

The CDB44800 demonstration board is an excellent means for evaluating the CS44800 eight-channel Class-D PWM modulator. It incorporates a digital audio interface, four full-bridge and 4 half-bridge configurations, and power supply rejection (PSR) circuitry, all on a two-layer board.

The CDB44800 schematic set is shown in Figures 4 through 12 and the board layout is shown in Figures 13 through 15.

1.1 CS44800 PWM Modulator

A complete description of the CS44800 is included in the CS44800 product data sheet.

The CS44800 converts linear PCM data to pulse width modulated (PWM) output. It uses an SRC to minimize jitter effects, resulting in high-quality sound output.

All supply voltages (VDX, VLS, VLC, and VDP) can be set using J30, J31, J32, and J28. A push button is provided for immediate muting of the PWMOUTxxx outputs. PCM data and clocks are input from either the CS8416 or J24 (PCM Input). J25 provides the SYS_CLK and J21 provides the PS_SYNC output clocks for system development.

1.2 CS4461 PSR Feedback ADC

A complete description of the CS4461 is included in the CS4461 product data sheet.

The CS4461 is connected to the CS44800 to provide power supply rejection (PSR) for the VP supply voltage connected to J17. Resistors R41 and R42 should be scaled for the supply voltage used. See the CS4461 data sheet for equations to determine the resistor values. The board comes initially populated with resistor values set for VP = 40 V.

1.3 TDA8939 Power Stage

A complete description of the Philips TDA8939 is included in the TDA8939 product data sheet.

The TDA8939 is a high-voltage PWM amplifier power stage. It integrates two half-bridge drivers and fault protection. With VP set to 40 V and R_{load} = 8 Ω, the TDA8939 can produce up to 65 W when set as a full-bridged output. With VP set to 40 V and R_{load} = 4 Ω, the TDA8939 can produce up to 35 W when set as a half-bridged output.

The supply voltage is set through J17 (VP) and should be between 20 V and 50 V. LEDs D1 - D6 (DIAG) indicate a fault condition with the corresponding power stage. These signals are OR'ed and input to GPIO0 pin on the CS44800. Speaker outputs are available from J1 - J16. Care should be taken to not connect the full bridge black speaker connectors to ground as these outputs are driven. The half bridge black speaker connectors can be connected directly to ground as these outputs are tied to ground on the board.

1.4 CS8416 Digital Audio Receiver

The operation of the CS8416 receiver and a discussion of the digital audio interface are included in the CS8416 data sheet.

The CS8416 converts the input S/PDIF data stream into PCM data for the CS44800. The CS8416 operates in master mode and can output either 128*Fs or 256*Fs from its RMCK pin. Digital Interface format selection of I²S (24-bit), Left Justified (24-bit), or Right Justified (16 or 24-bit) can be made.

D20 (RERR) indicates a receiver error, such as loss of lock.

S/PDIF input is through OPT1 or J33.

1.5 Line and Headphone Outputs

An example of line level and headphone driver outputs are provided on the board. J18/J19 and J20 must be in place to connect the PWM outputs to drive the headphone and line outputs.

1.6 Control Port Interface and GUI

The CS44800 is controlled through the provided control port interface. Connections to the control port can be made through J37 (RS-232 Serial) or J29 (External Control Header). A Windows based GUI provides control over all the individual registers of the CS44800 and the CS8416. To use the onboard control logic, J29 should be jumpered to “PC”. To use external control logic J29 should have all jumpers removed and external signal and ground can be input through the pins labeled “EXT”. All external control signal levels should be referenced to the VLC voltage setting of the board.

1.7 Power

Power must be supplied to the evaluation board through the +5.0 V binding post (J41). Onboard regulators supply +3.3 V and +2.5 V to the rest of the board. All voltage inputs must be referenced to the single black banana-type ground connector (J40).

WARNING:Please refer to the CS44800 datasheet for allowable voltage levels.

1.8 Grounding and Power Supply Decoupling

The CS44800 requires careful attention to power supply and grounding arrangements to optimize performance. The block diagram on page 1 provides an overview of the connections to the CS44800, Figure 13 shows the component placement, Figure 14 shows the top layout, and Figure 15 shows the bottom layout. The 0.1µF ceramic decoupling capacitors are located as close to the power pins of the CS44800 as possible and on the same side of the board as the CS44800. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

1.9 Critical Component Selection

The output filter of the half-bridge and full-bridge outputs have components that must be chosen carefully.

The output snubbing resistors, R17-R40, used to shape the switching PWM output edges, should be 5.6 Ω, ¼ W (VP = 30 V), ½ W (VP = 40 V), or 1 W (VP = 50 V) resistors. This board is populated with DALE CRCW20105R62F parts.

The output snubbing capacitors, C43-C56, used to shape the switching PWM output edges, should be 560 pF, C0G (NPO), with a voltage rating above the VP voltage. This board is populated with KEMET C0805C561K5GAC05R62F parts.

The output low-pass filter inductors, L1-L12, used to filter high frequency content from the speakers, should be chosen so that their saturation current rating is above that of the maximum output current. This board is populated with TRANSTEK MAGNETICS TMP50627CT and TMP50626CT parts.

The output low-pass filter capacitors, C13-C16, C18, C19, C21-C24, C26, and C27, used to filter high frequency content from the speakers, should be chosen to have a dielectric of metallized film, with a voltage rating above the VP voltage. This board is populated with PANASONIC ECQV1H474JL and ECQV1H105JL parts.

The half-bridge channels output high-pass filter capacitors, C17, C20, C25, and C28, used to filter DC frequency content from the speakers, should have a ripple current rating above the maximum peak output current and have a voltage rating above the maximum peak output voltage. This board is populated with PANASONIC ECA1HM102 parts. The capacitance value determines the cutoff frequency of the high-pass filter. The cutoff frequency (-3 dB point) on the board has been set for 26 Hz when used with a 6 Ω load.

The VP power supply bulk decoupling capacitors, C29-C32 and C57-C60 should be chosen to have a voltage rating above the VP voltage. The lower the capacitor's ESR rating at the working frequency, the better the noise attenuation. Low ESR decoupling capacitors will offer lower output speaker noise than high ESR capacitors. This board is populated with NICHICON UPW1J102MHH parts.

The Zoble filter network resistors, R1-R12, used to impedance match the speaker, should be chosen to have a power handling according to the following equation: $P = C * V^2 * f$. For this board, C = 0.22 μF, f = 20 kHz, and V = the RMS full-scale output voltage. This board is populated with 1 W DALE CRCW251222R1F parts.

CONNECTOR	Reference Designator	INPUT / OUTPUT	SIGNAL PRESENT
+5V	J36	Input	+5.0 V Power Supply
GND	J35	Input	Ground Reference
VDX	J30	Input	+2.5 V, +3.3 V, or +5.0 V Power Supply for VDX
VLS	J31	Input	+2.5 V, +3.3 V, or +5.0 V Power Supply for VLS
VLC	J32	Input	+2.5 V, +3.3 V, or +5.0 V Power Supply for VLC
VDP	J28	Input	+3.3 V or +5.0 V Power Supply for VDP
COAX IN	J33	Input	CS8416 digital audio input via coaxial cable
OPTICAL IN	OPT1	Input	CS8416 digital audio input via optical cable
PCM Input	J24	Input	Input for PCM Clocks and Data
HEADPHONE	J23	Output	Headphone Driver Output
LFE LINE OUT	J22	Output	Line Level Output for LFE Channel
SERIAL	J37	Input	Serial Control Port Interface
VP	J17	Input	+20 V to +50 V Power Supply for the TDA8939 Output Power Stages
FB_CHANNEL_1/L	J1 J2	Output Output	Positive and Negative Full Bridge Outputs for Channel 1 / Left
FB_CHANNEL_2/R	J3 J4	Output Output	Positive and Negative Full Bridge Outputs for Channel 2 / Right
HB_CHANNEL_3/LS	J5 J6	Output Output	Positive Half Bridge Output and Ground Reference for Channel 3 / Left Surround
HB_CHANNEL_4/RS	J7 J8	Output Output	Positive Half Bridge Output and Ground Reference for Channel 4 / Right Surround
FB_CHANNEL_5/C	J9 J10	Output Output	Positive and Negative Full Bridge Outputs for Channel 5 / Center
FB_CHANNEL_6/LFE	J11 J12	Output Output	Positive and Negative Full Bridge Outputs for Channel 6 / Low Frequency Effects (Subwoofer)
HB_CHANNEL_7/SBL	J13 J14	Output Output	Positive Half Bridge Output and Ground Reference for Channel 7 / Surround Back Left
HB_CHANNEL_8/SBR	J15 J16	Output Output	Positive Half Bridge Output and Ground Reference for Channel 8 / Surround Back Right

Table 1. System Connections

2. GUI CONTROL

The CDB44800 is shipped with a Microsoft Windows® based GUI, which allows control over the CS8416 and CS44800 registers. Interface to the CDB44800 control port is provided using an RS-232 serial cable. Once the appropriate cable is connected between the CDB44800 and the host PC, load the FlexLoader.exe from the CDB44800 directory. Once loaded, all registers are set to their default reset state. The GUI File menu provides the ability to save and restore (load) script files containing all of the register settings. Sample script files are provided for basic functionality.

2.1 CS44800 Dialog Tab

The CS44800 Dialog tab provides high level control over the CS44800's registers. Controls are provided to change volume, mute, power down, ramp, SAI input format, minimum pulse width, and channel delay.

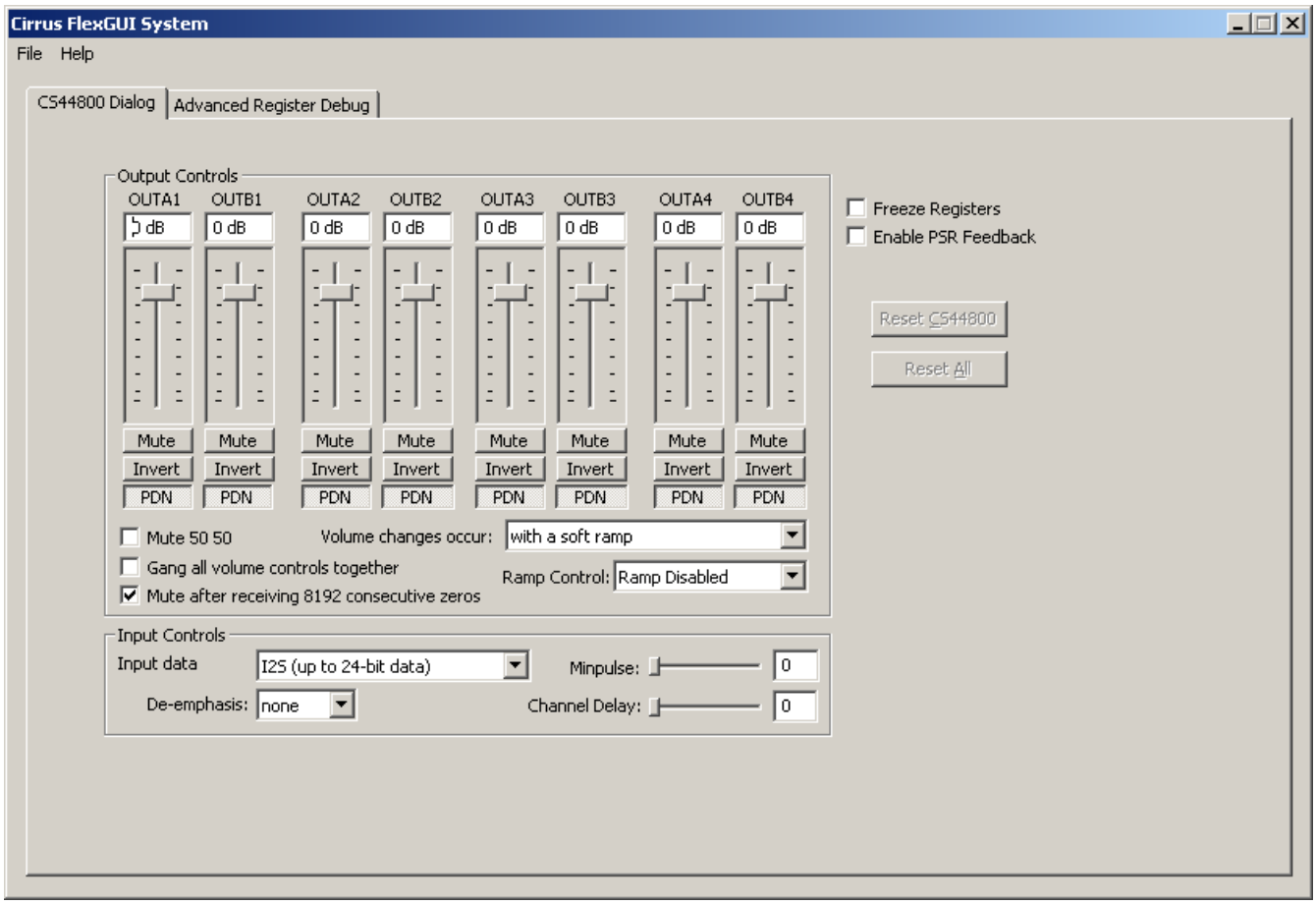
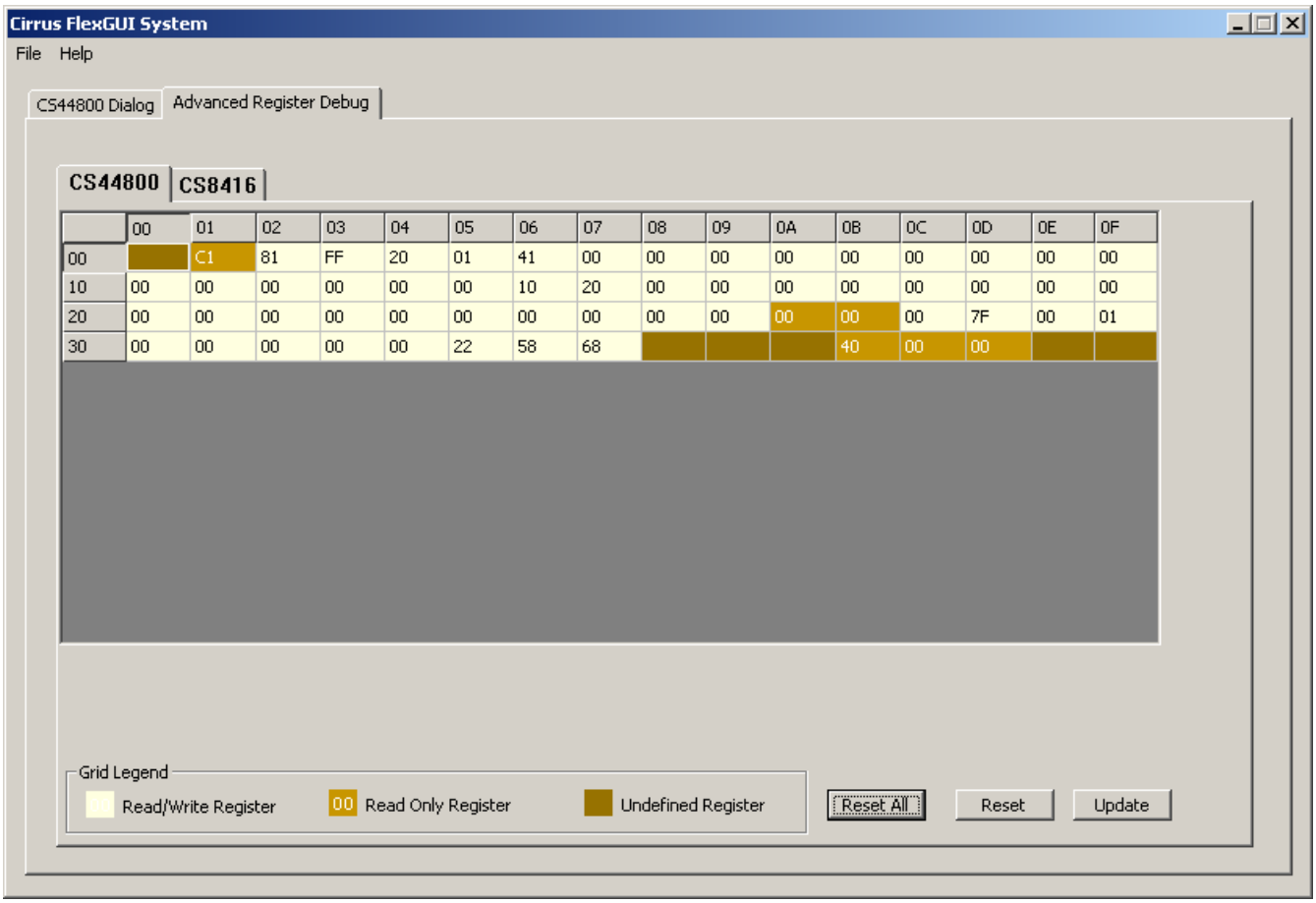


Figure 1. CS44800 Dialog Tab

2.2 Advanced Register Debug Tab

The Advanced Register Debug tab provides low level control over the CS44800 and CS8416 individual register settings. Each device is displayed on a separate tab. Register values can be modified bitwise or bytewise. For bitwise, click the appropriate push button for the desired bit. For bytewise, the desired hex value can be typed directly in the register address box in the register map.



	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
00		C1	81	FF	20	01	41	00	00	00	00	00	00	00	00	00
10	00	00	00	00	00	00	10	20	00	00	00	00	00	00	00	00
20	00	00	00	00	00	00	00	00	00	00	00	00	00	7F	00	01
30	00	00	00	00	00	22	58	68				40	00	00		

Figure 2. Advanced Register Debug Tab - CS44800

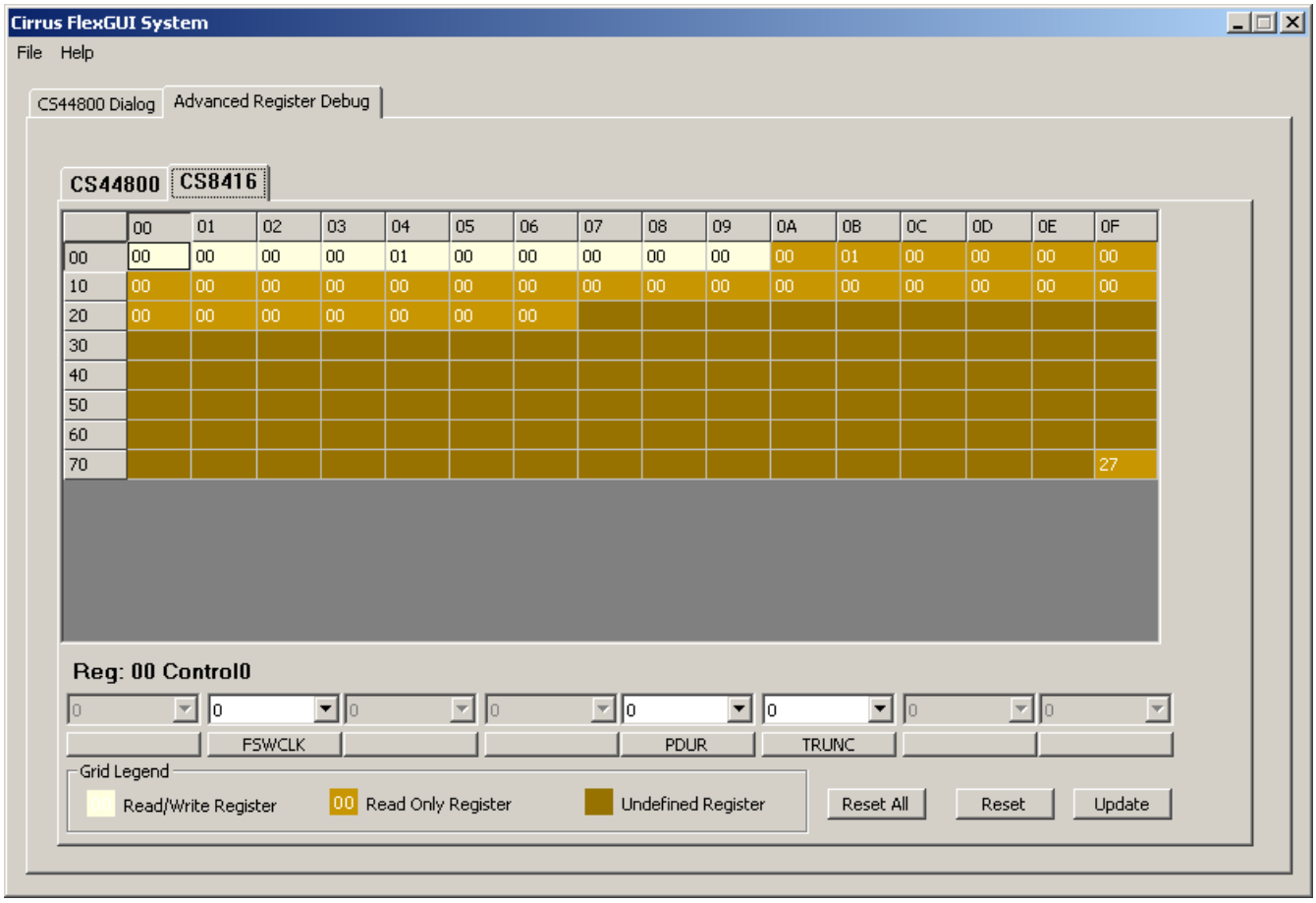


Figure 3. Advanced Register Debug Tab - CS8416

3. SCHEMATICS

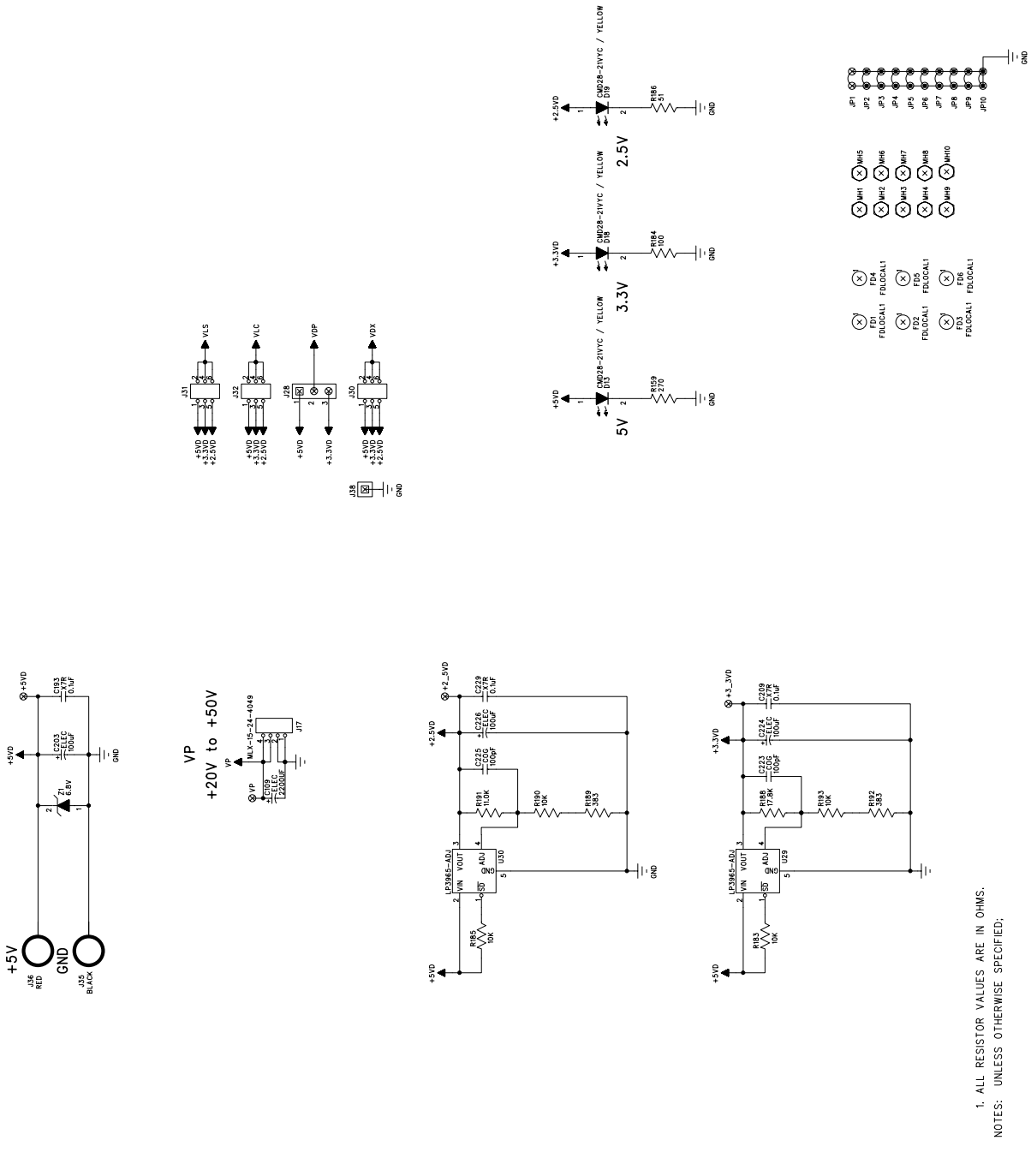


Figure 4. Power

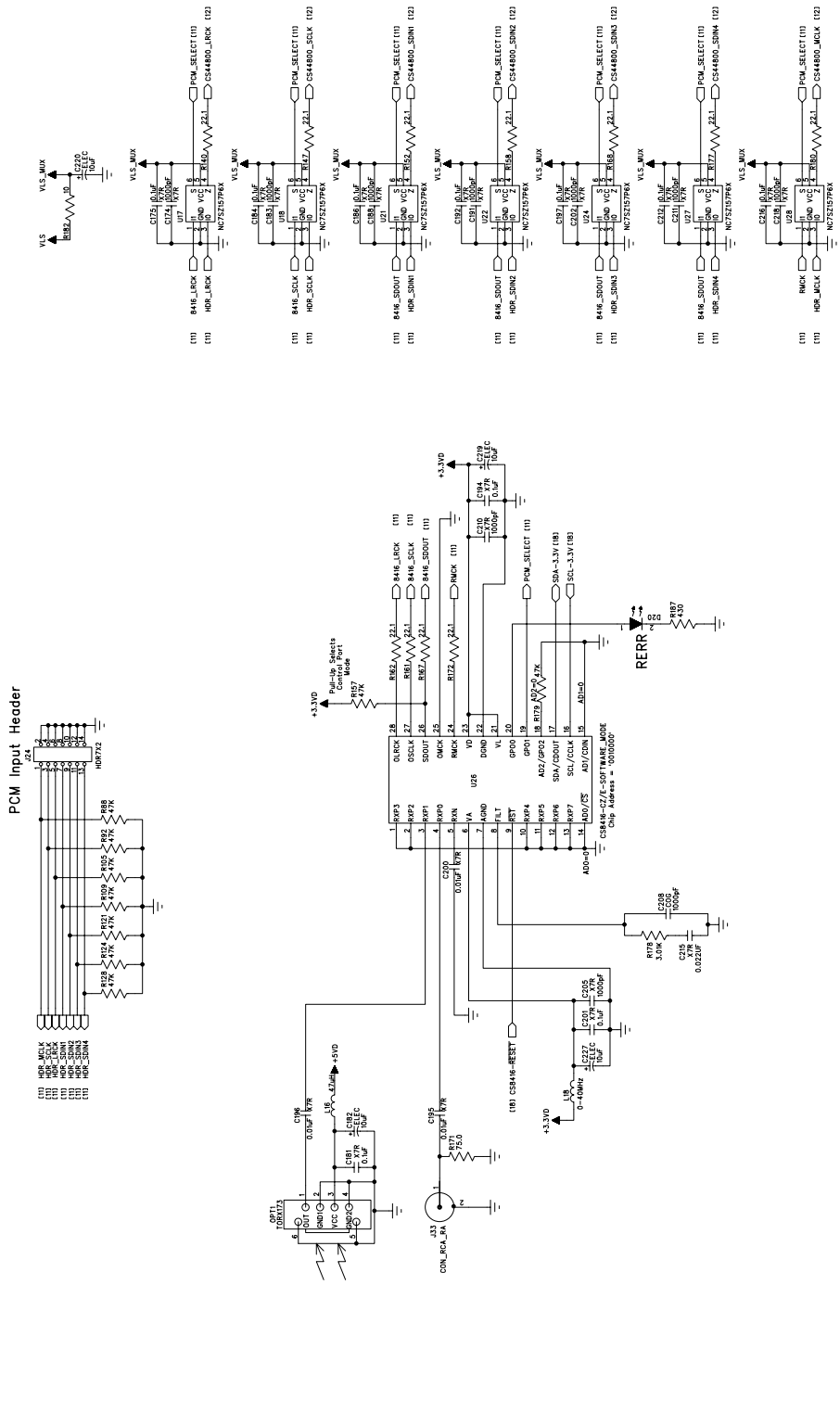


Figure 5. CS8416

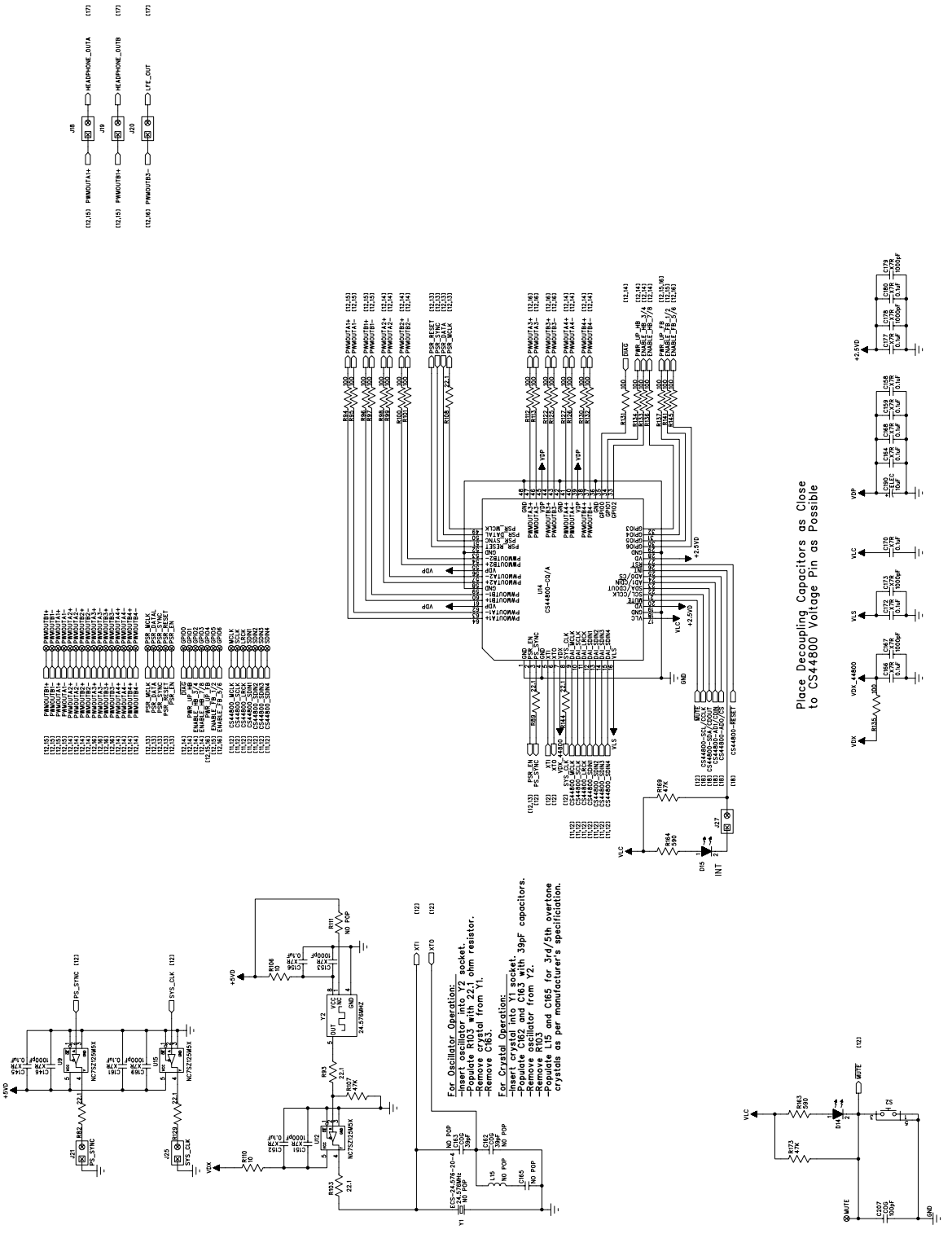


Figure 6. CS44800

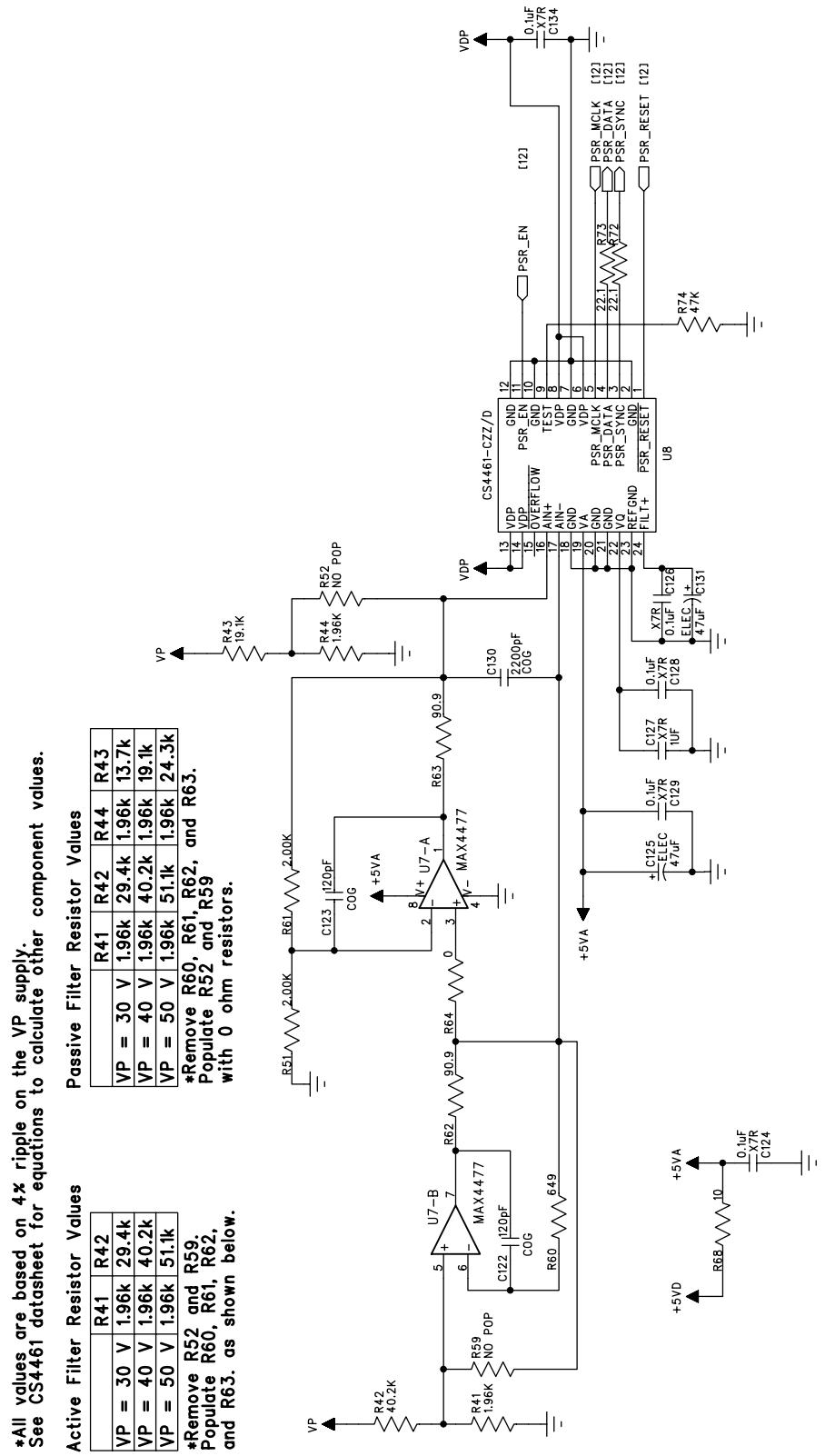


Figure 7. CS4461 PSR Feedback

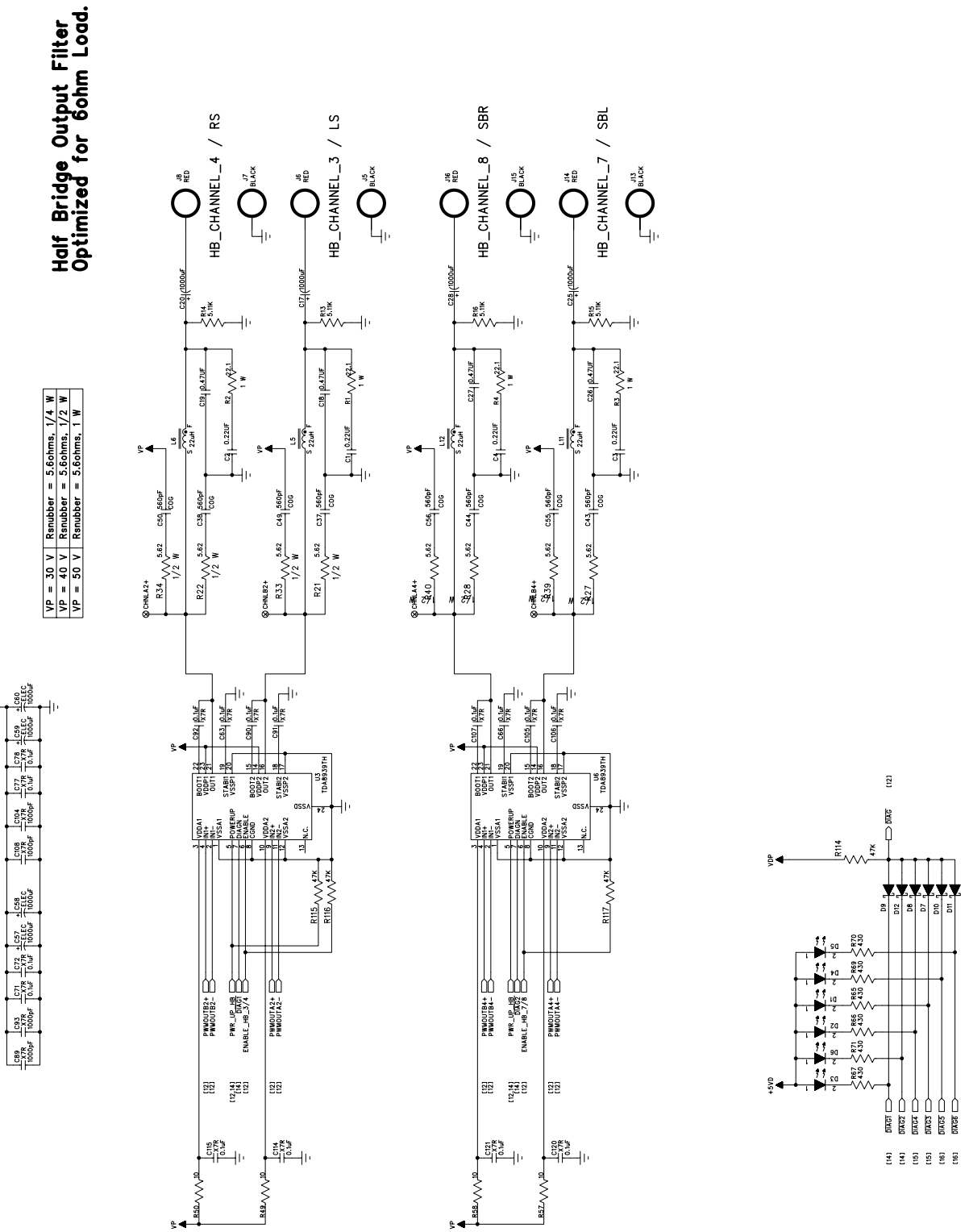


Figure 8. Half Bridge Channels

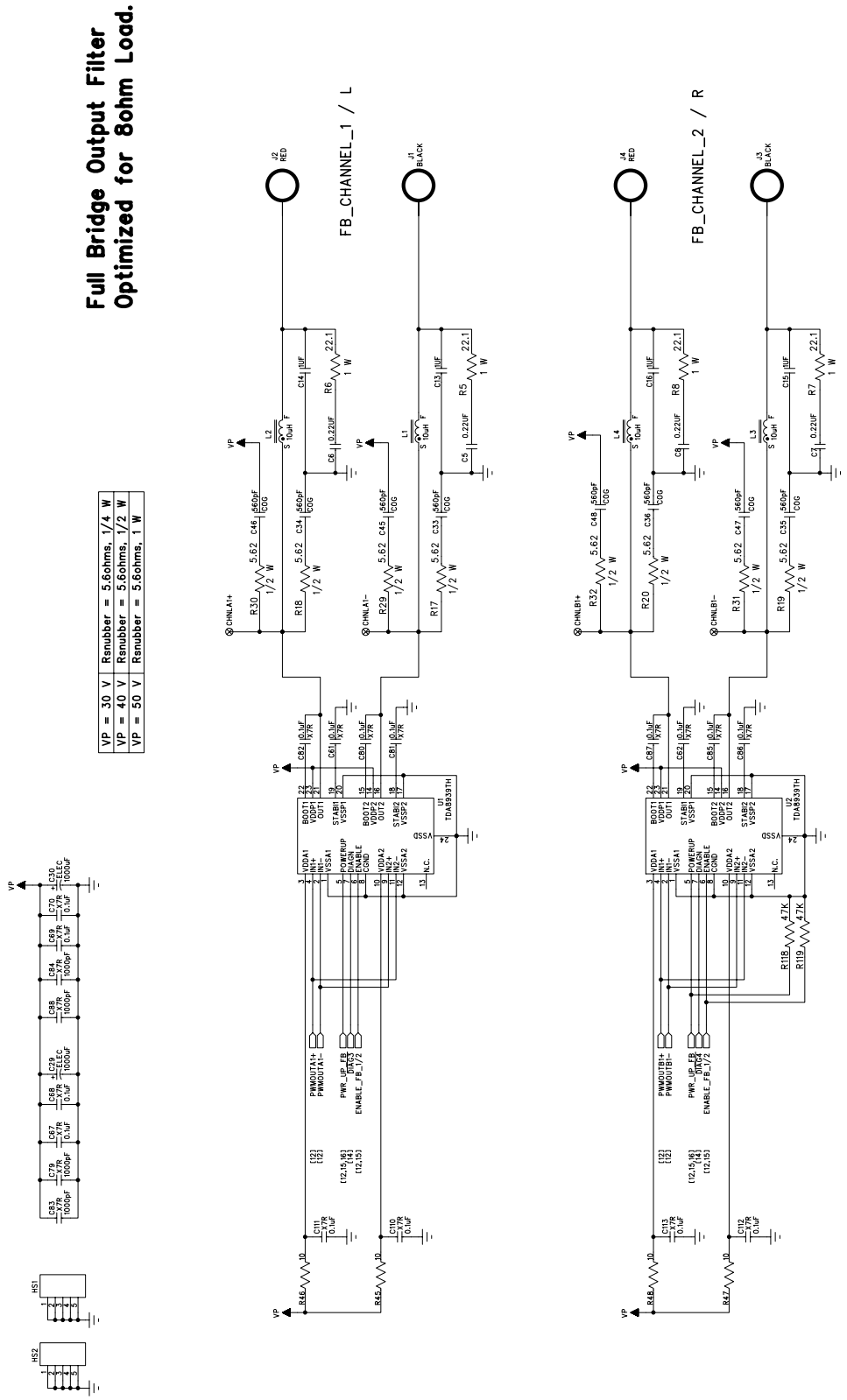


Figure 9. Full Bridge Channels 1

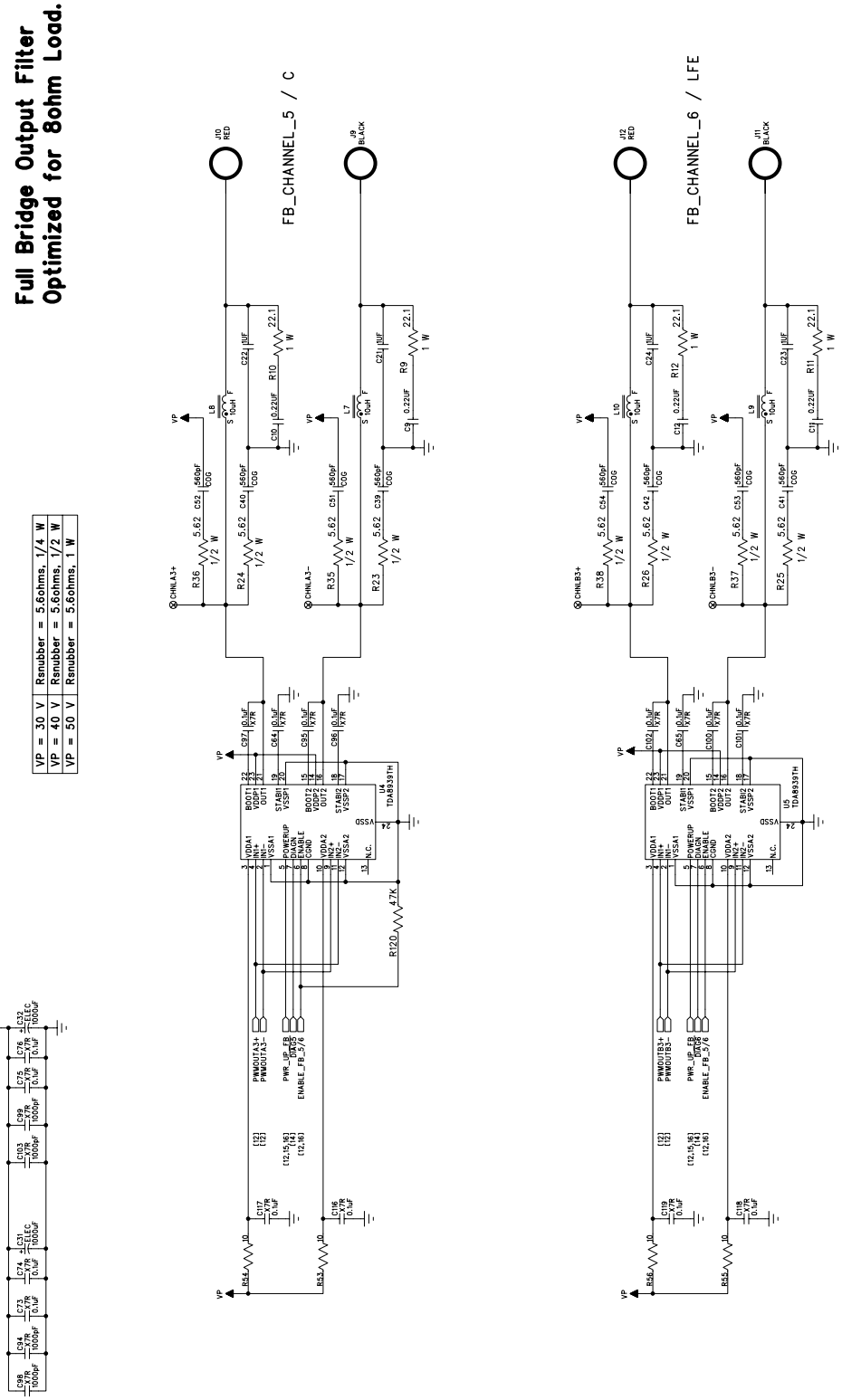


Figure 10. Full Bridge Channels 2

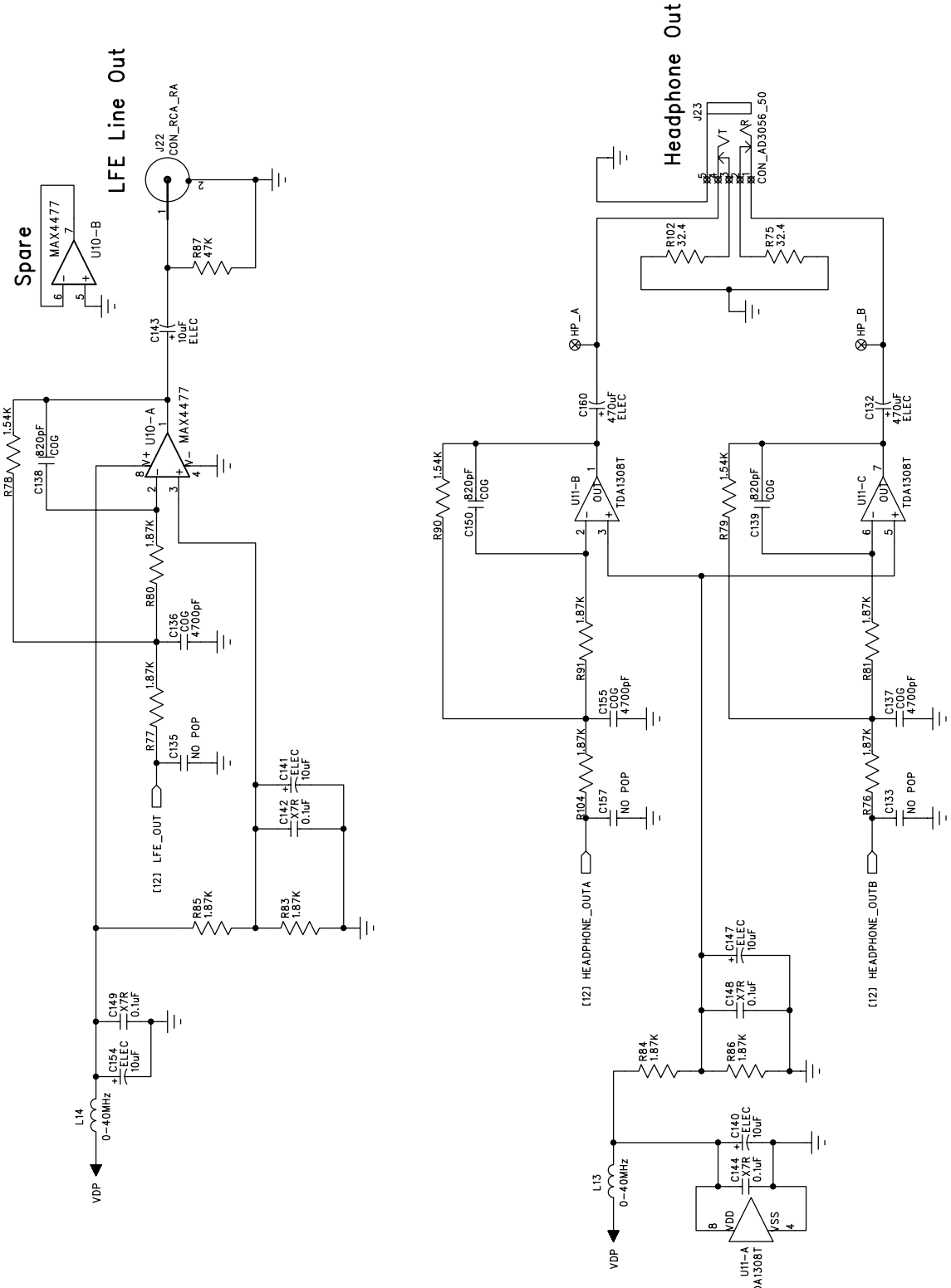


Figure 11. Analog Outputs

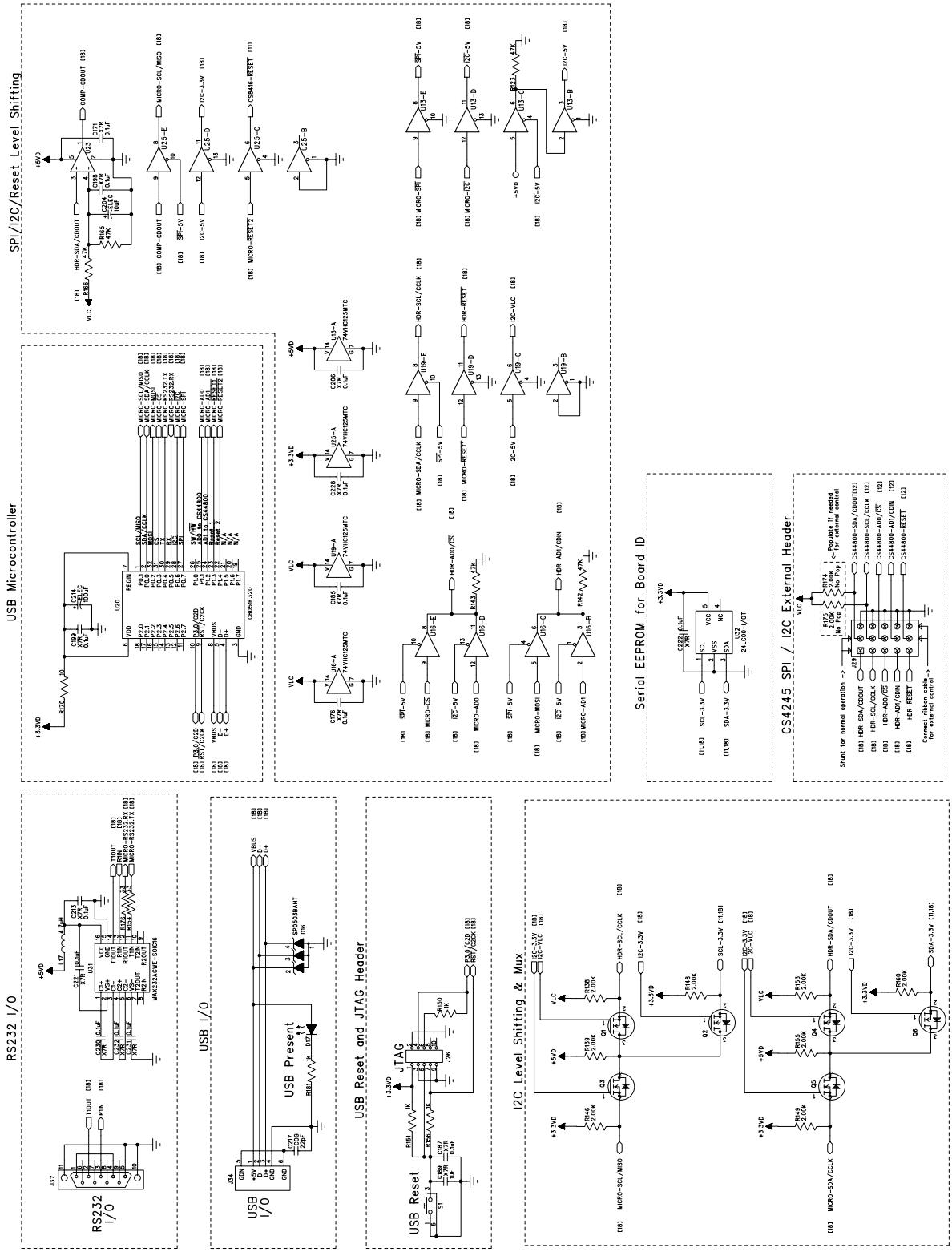


Figure 12. Control Port

4. LAYOUT

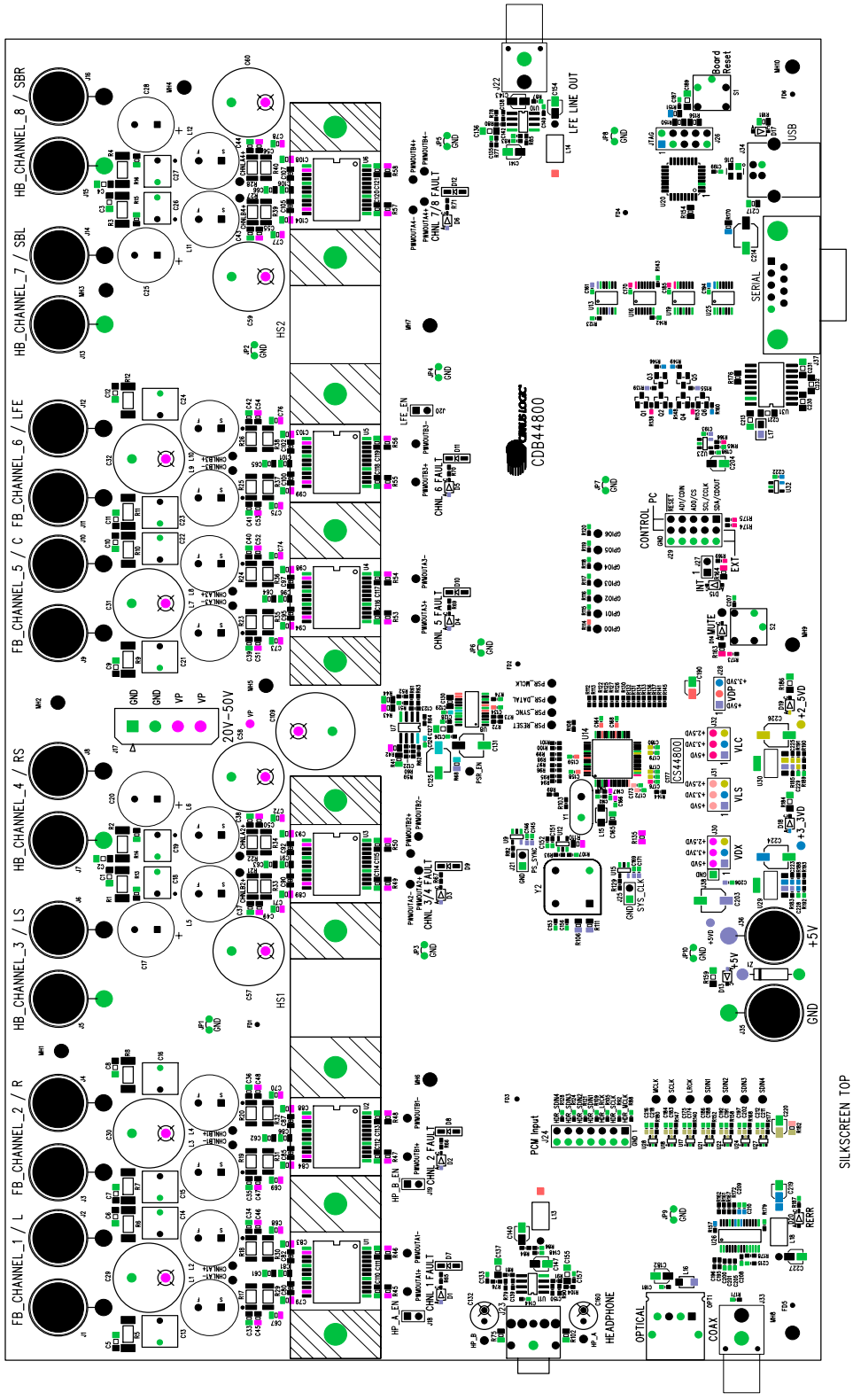


Figure 13. Silk Screen

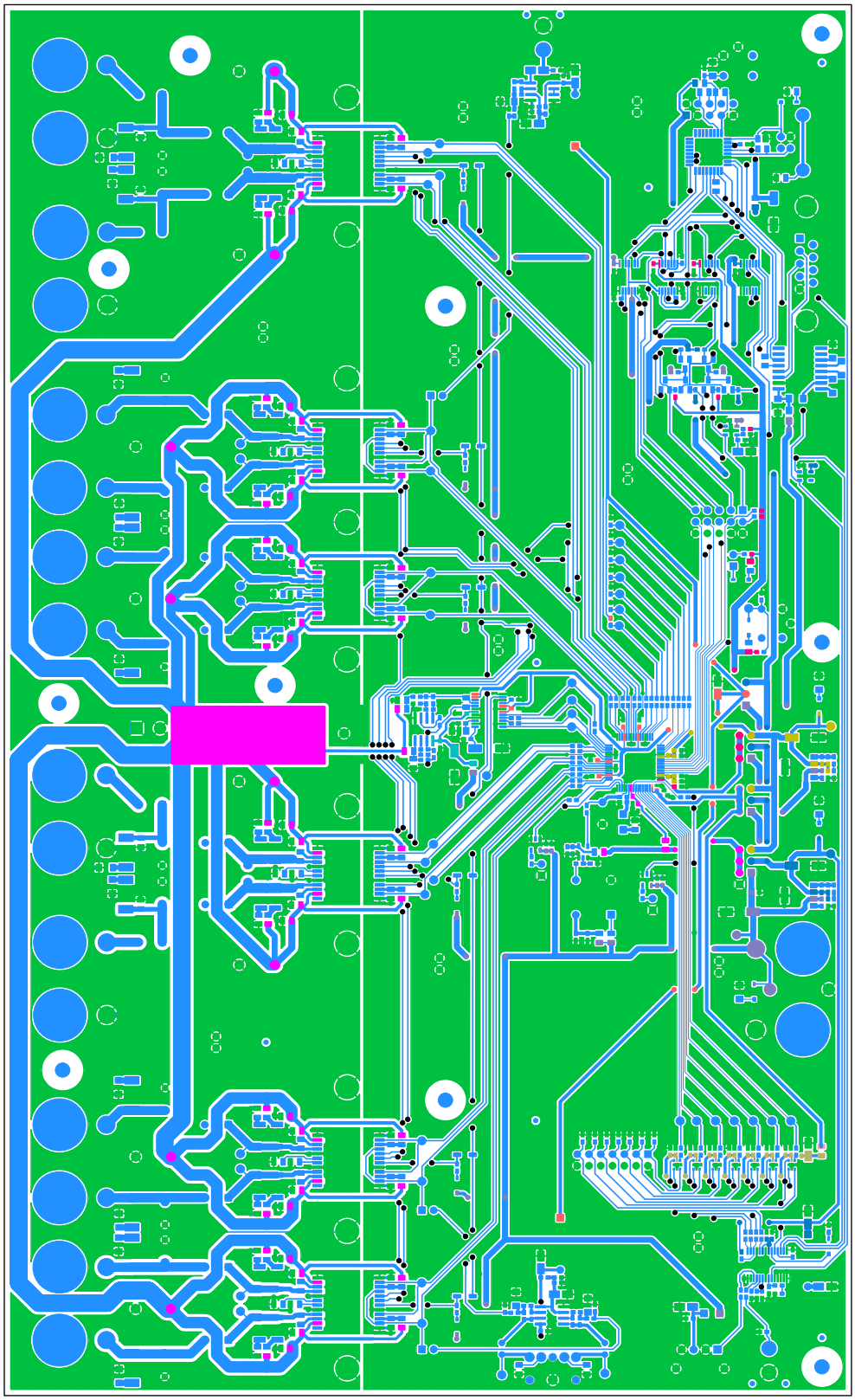


Figure 14. Topside Layer

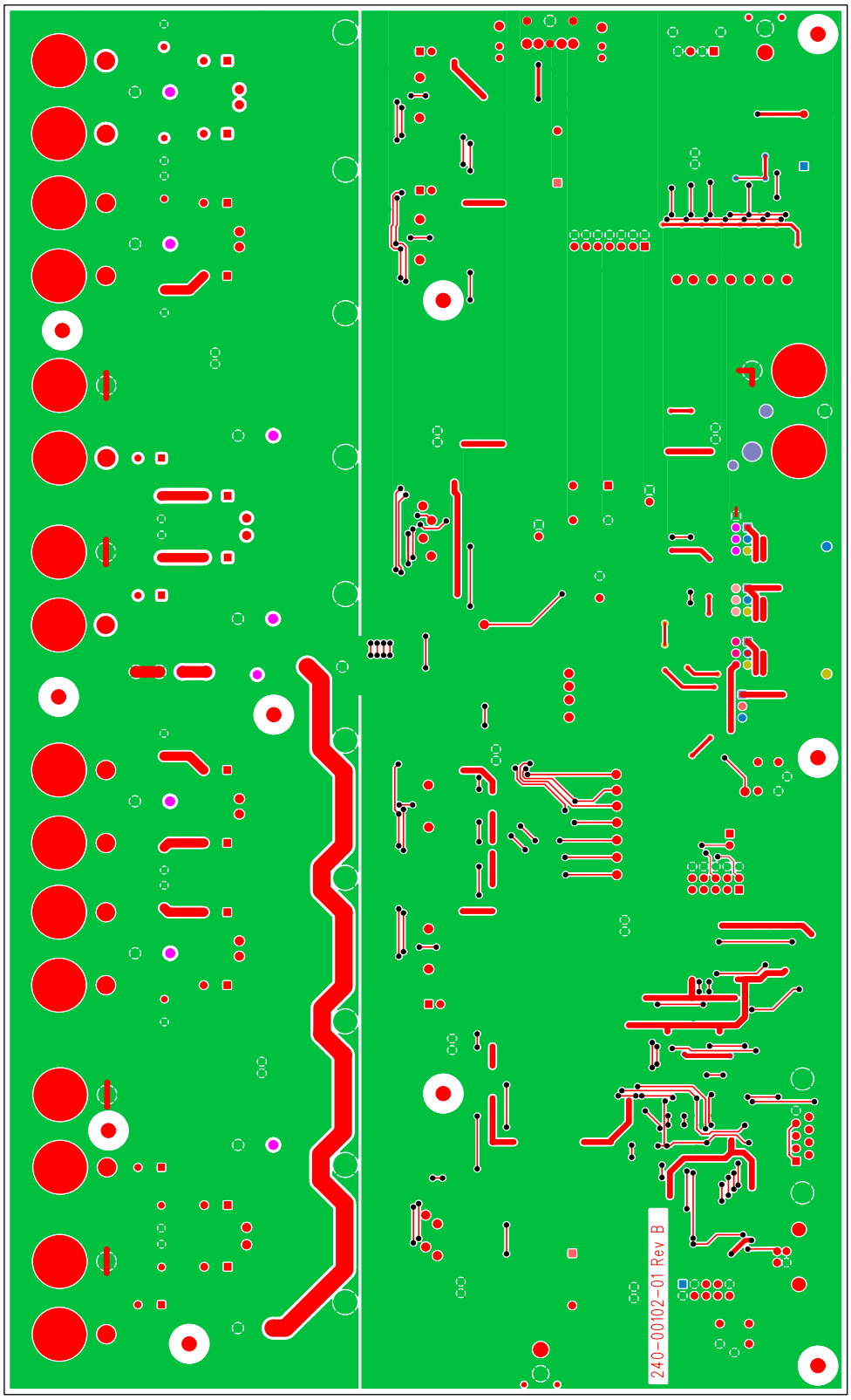


Figure 15. Bottomside Layer

5. REVISION HISTORY

Release	Date	Changes
DB1	June 2004	1st Release
DB2	October 2004	Updated sections to reflect board revision B changes: -Updated “CS44800 PWM Modulator” on page 3 -Updated “CS4461 PSR Feedback ADC” on page 3 -Updated “TDA8939 Power Stage” on page 3 -Updated “CS8416 Digital Audio Receiver” on page 3 -Updated “Line and Headphone Outputs” on page 4 -Updated “Control Port Interface and GUI” on page 4 -Added “Critical Component Selection” on page 4 -Updated Table 1 on page 6 -Updated “CS44800 Dialog Tab” on page 7 -Updated Figure 1 on page 7 -Updated Figure 2 on page 8 -Updated Figure 4 on page 10 -Updated Figure 5 on page 11 -Updated Figure 6 on page 12 -Updated Figure 7 on page 13 -Updated Figure 8 on page 14 -Updated Figure 9 on page 15 -Updated Figure 10 on page 16 -Updated Figure 11 on page 17 -Updated Figure 12 on page 18 -Updated Figure 13 on page 19 -Updated Figure 14 on page 20 -Updated Figure 15 on page 21

Table 2. Revision History

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **<http://www.cirrus.com/corporate/contacts/sales.cfm>**

AMEYA360
Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com