June 2014

FDM3622
N-Channel PowerTrench® MOSFET
100V, 4.4A, 60mΩ

Features

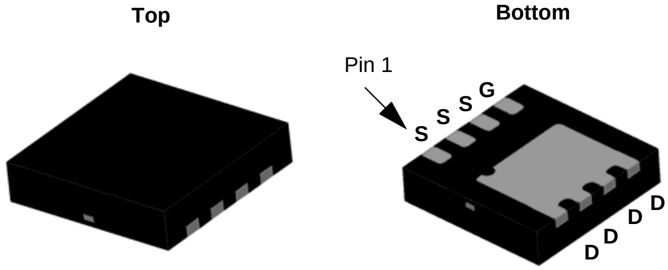
- Max $r_{DS(on)}$ = 60mΩ at V_{GS} = 10V, I_D = 4.4A
- Max $r_{DS(on)}$ = 80mΩ at V_{GS} = 6.0V, I_D = 3.8A
- Low Miller Charge
- Low QRR Body Diode
- Optimized efficiency at high frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)
- RoHS Compliant

General Description

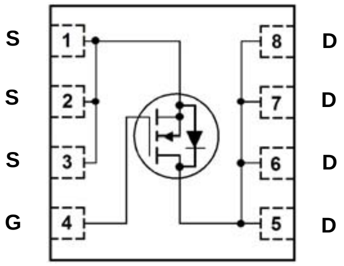
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

- Distributed Power Architectures and VRMs.
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier
- Formerly developmental type 82744



MLP 3.3x3.3



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		100	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current -Continuous	(Note 1a)	4.4	A
	-Pulsed		20	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	54	mJ
P_D	Power Dissipation	(Note 1a)	2.1	W
	Power Dissipation	(Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	60	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDM3622	FDM3622	MLP 3.3x3.3	13''	12 mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V	100			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80V, V_{GS} = 0V			1	µA
		T_J = 100°C			250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA	2		4	V
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 4.4A		44	60	mΩ
		V_{GS} = 6.0V, I_D = 3.8A		56	80	
		V_{GS} = 10V, I_D = 4.4A , T_J = 150°C		92	120	

Dynamic Characteristics

C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		820	1090	pF
C_{oss}	Output Capacitance			125	170	pF
C_{rss}	Reverse Transfer Capacitance			35	55	pF
Rg	Gate Resistance	V_{DS} = 15mV, f = 1MHz	0.1	3.1	6.2	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50V, I_D = 4.4A V_{GS} = 10V, R_{GEN} = 24Ω		11	20	ns
t_r	Rise Time			25	40	ns
$t_{d(off)}$	Turn-Off Delay Time			35	56	ns
t_f	Fall Time			26	42	ns
Q_g	Total Gate Charge	V_{GS} = 10V V_{DD} = 50V I_D = 4.4A		13	17	nC
Q_{gs}	Gate to Source Gate Charge			3.6		nC
Q_{gd}	Gate to Drain "Miller" Charge			3.4		nC

Drain-Source Diode Characteristics

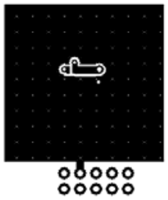
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 4.4A			1.25	V
		V_{GS} = 0V, I_S = 2.2A			1.0	V
t_{rr}	Reverse Recovery Time	I_F = 4.4A, di/dt = 100A/µs			56	ns
Q_{rr}	Reverse Recovery Charge				108	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

(a)$R_{\theta JA}$ = 60°C/W when mounted on a 1 in^2 pad of 2 oz copper, 1.5'x1.5'x0.062' thick PCB.

(b)$R_{\theta JA}$ = 135°C/W when mounted on a minimum pad of 2 oz copper.



a. 60°C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 135°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300µs, Duty cycle < 2.0%.

3: E_{AS} of 54 mJ is based on starting T_J = 25 C; N-ch: L = 3 mH, I_{AS} = 6 A, V_{DD} = 100 V, V_{GS}= 10 V.

Typical Characteristics T_J = 25°C unless otherwise noted

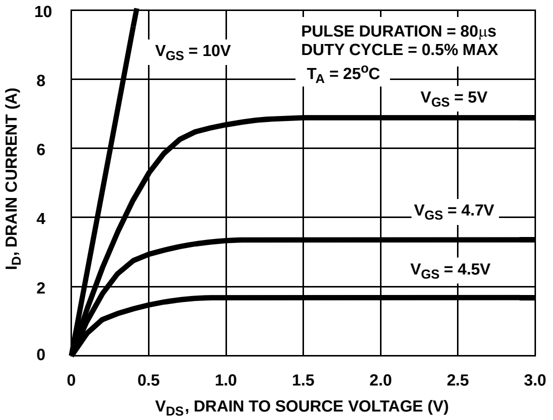


Figure 1. On-Region Characteristics

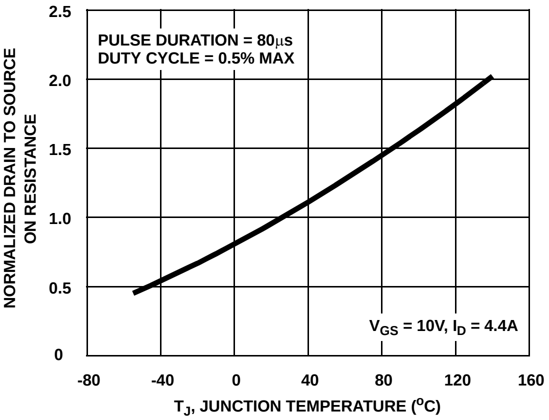


Figure 2. Normalized On-Resistance vs Junction Temperature

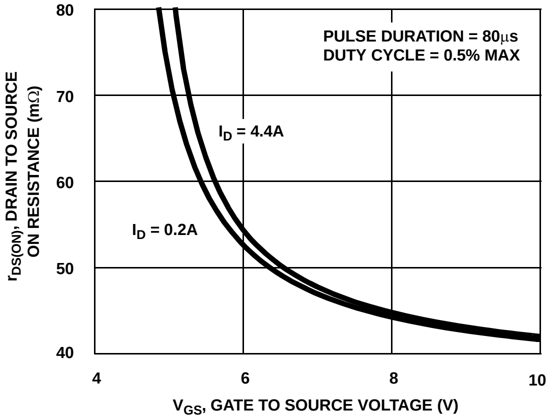


Figure 3. On-Resistance vs Gate to Source Voltage

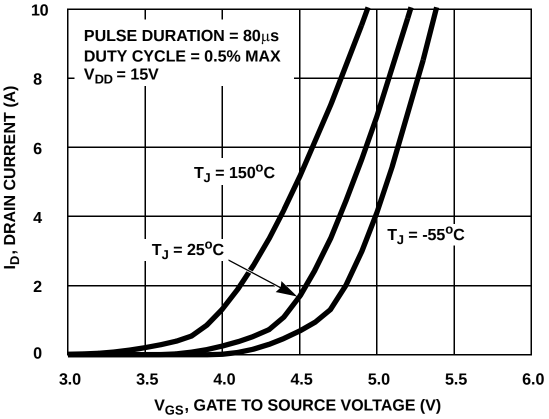


Figure 4. Transfer Characteristics

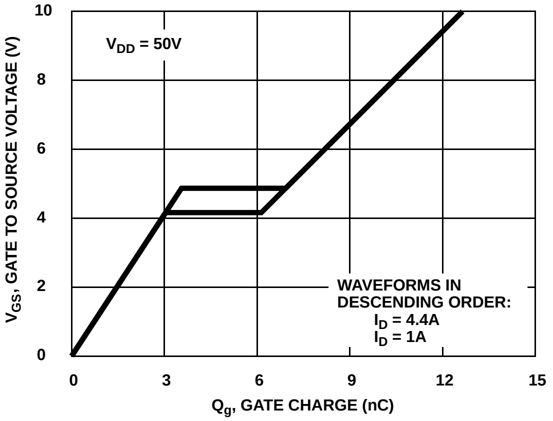


Figure 5. Gate Charge Characteristics

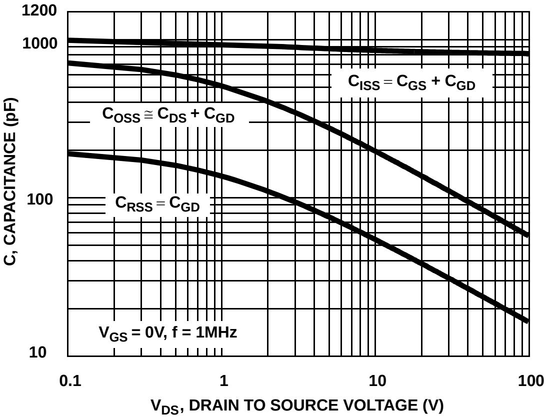


Figure 6. Capacitance vs Drain to Source Voltage

Typical Characteristics T_J = 25°C unless otherwise noted

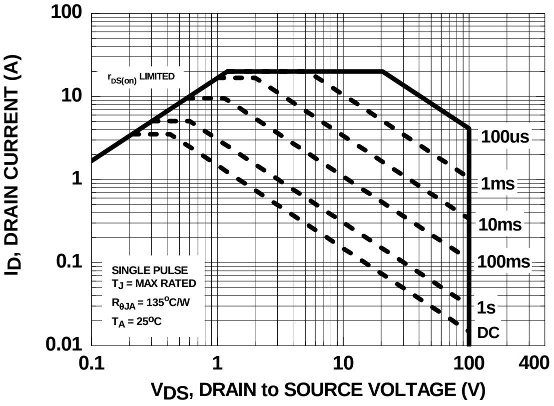


Figure 7. Forward Bias Safe Operating Area

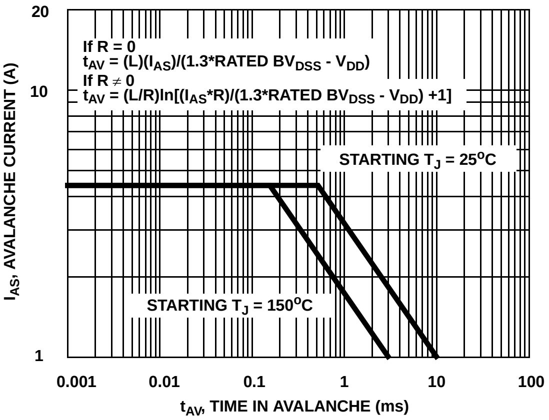


Figure 8. Uncalamped Inductive Switching Capability

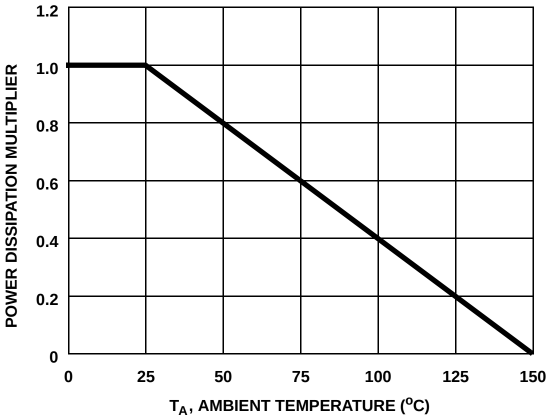


Figure 9. Normalized Power dissipation vs Ambient Temperature

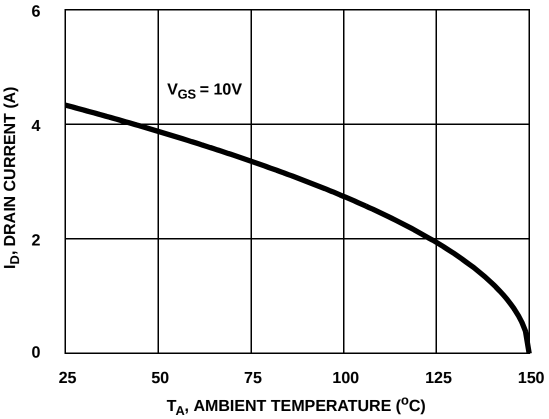


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

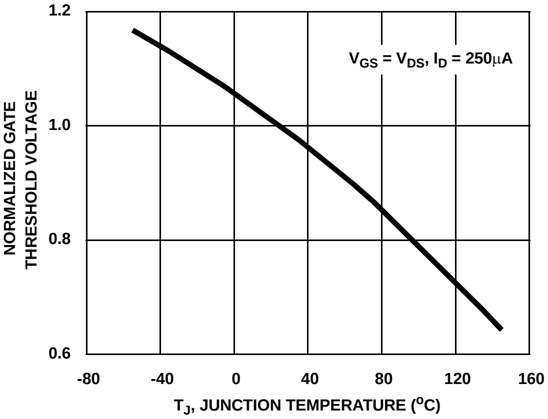


Figure 11. Normalized Gate Threshold voltage vs Junction Temperature

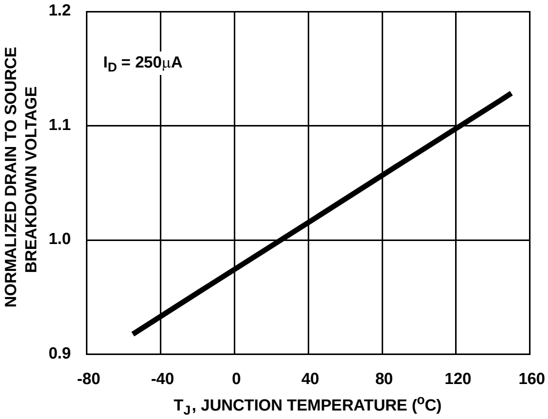


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

Typical Characteristics T_J = 25°C unless otherwise noted

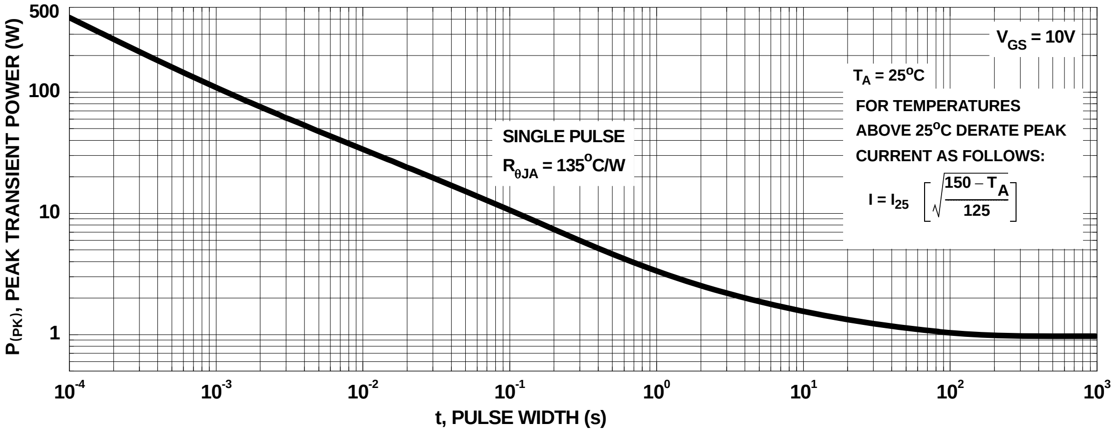


Figure 13. Peak Current Capability

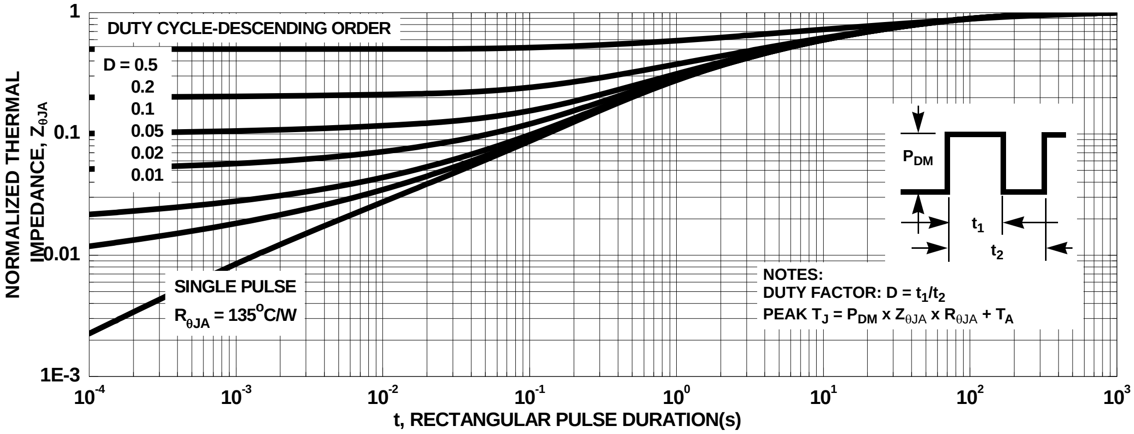
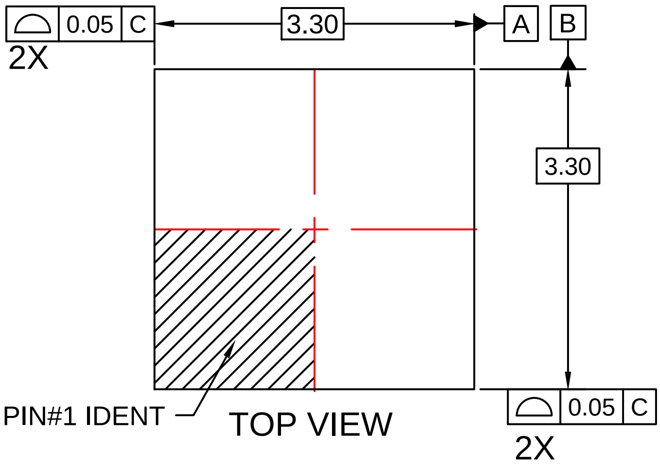
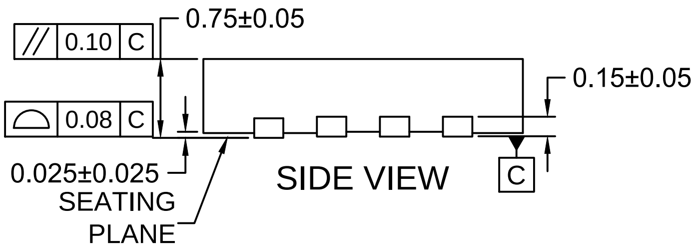


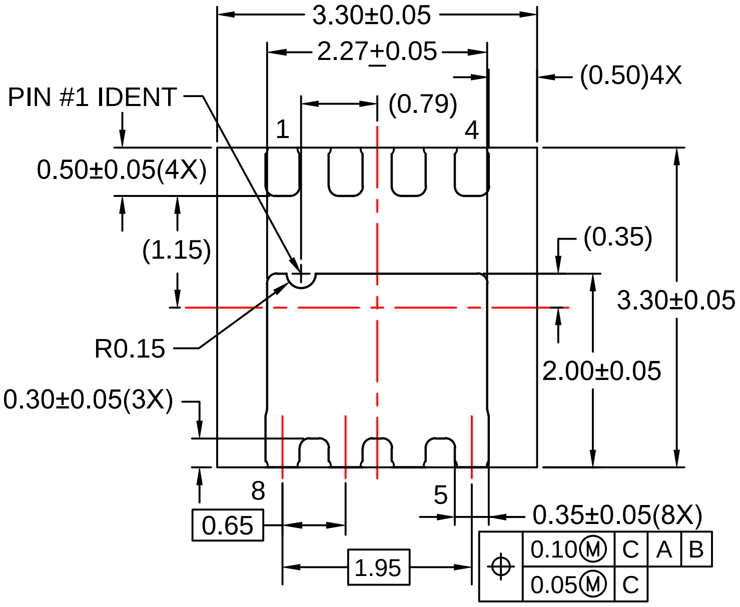
Figure 14. Transient Thermal Response Curve



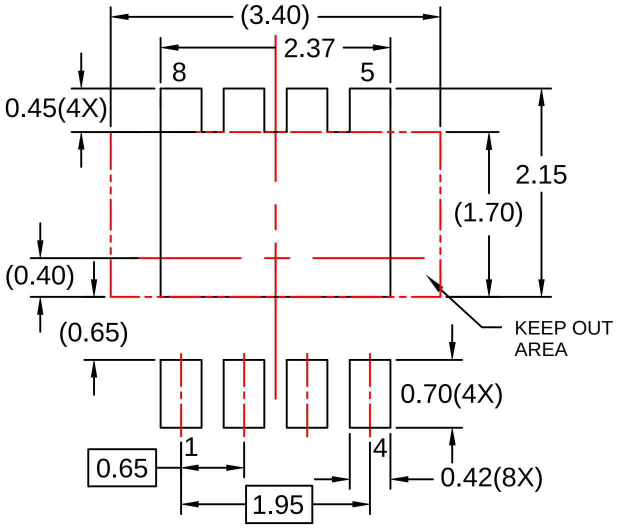
TOP VIEW



SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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