LM3477 High Efficiency High-Side N-Channel Controller for Switching Regulator

Check for Samples: LM3477

FEATURES

- **500kHz Switching Frequency**
- **Adjustable Current Limit**
- **1.5% Reference**
- **Thermal Shutdown**
- **Frequency Compensation Optimized with a Single Capacitor and Resistor**
- **Internal Softstart**
- **Current Mode Operation**
- **Undervoltage Lockout with Hysteresis**
- **8-lead (VSSOP-8) Package**

APPLICATIONS

- **Local Voltage Regulation**
- **Distributed Power**
- **Notebook and Palmtop Computers**
- **Internet Appliances**
- **Printers and Office Automation**
- **Battery operated Devices**
- **Cable Modems**
- **Battery Chargers**

DESCRIPTION

The LM3477/A is a high-side N-channel MOSFET switching regulator controller. It can be used in topologies requiring a high side MOSFET such as buck, inverting (buck-boost) and zeta regulators. The LM3477/A's internal push pull driver allows compatibility with a wide range of MOSFETs. This, the wide input voltage range, use of discrete power components and adjustable current limit allows the LM3477/A to be optimized for a wide variety of applications.

The LM3477/A uses a high switching frequency of 500kHz to reduce the overall solution size. Current-mode control requires only a single resistor and capacitor for frequency compensation. The current mode architecture also yields superior line and load regulation and cycle-by-cycle current limiting. A 5µA shutdown state can be used for power savings and for power supply sequencing. Other features include internal soft-start and output over voltage protection. The internal soft-start reduces inrush current. Over voltage protection is a safety feature to ensure that the output voltage stays within regulation.

The LM3477A is similar to the LM3477. The primary difference between the two is the point at which the device transitions into hysteretic mode. The hysteretic threshold of the LM3477A is one-third of the LM3477.

	Hysteretic Threshold(1)
LM3477	≅ 36% of programmed current limit
LM3477A	≅ 12% of programmed current limit

(1) See Hysteretic Threshold and PROGRAMMING THE CURRENT LIMIT/HYSTERETIC THRESHOLD for more information.

Typical Application Circuit

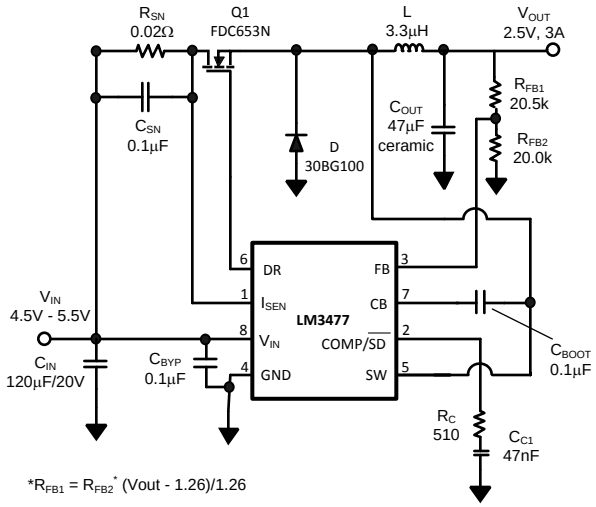


Figure 1. Typical High Efficiency Step-Down (Buck) Converter

Connection Diagram

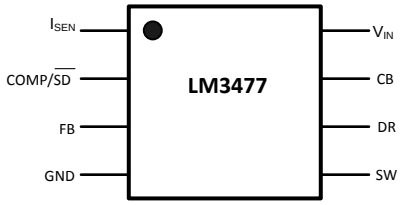


Figure 2. 8 Lead (VSSOP-8 Package)

PIN DESCRIPTION

Pin Name	Pin Number	Description
I_{SEN}	1	Current sense input pin. Voltage generated across an external sense resistor is fed into this pin.
COMP/$\overline{SD}$	2	Compensation pin. A resistor-capacitor combination connected to this pin provides compensation for the control loop. Pull this pin below 0.65V to shutdown.
FB	3	Feedback pin. The output voltage should be adjusted using a resistor divider to provide 1.270V at this pin.
GND	4	Ground pin.
SW	5	Switch Node. Source of the external MOSFET is connected to this node.
DR	6	Drive pin. The gate of the external MOSFET should be connected to this pin.
CB	7	Boot-strap pin. A capacitor must be connected between this pin and SW pin (pin 5) for proper operation. The voltage developed across this capacitor provides the gate drive for the external MOSFET.
V_{IN}	8	Power Supply Input pin.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Input Voltage	36V
Peak Driver Output Current (<10µs)	1.0A
CB Pin Voltage (3)	43V
I_{SEN} Pin Voltage	500mV
Power Dissipation	Internally Limited
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
ESD Susceptibilty (4) Human Body Model Machine Model	 2kV 200V
Lead Temperature for VSSOP Package Vapor Phase (60 sec.) Infared (15 sec.)	 215°C 220°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) The CB pin must not be higher than 8V above the V_{SW}.
(4) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is 200 pF capacitor discharged directly into each pin.

Operating Ratings (1)

Supply Voltage	$2.97V \le V_{IN} \le 35V$
Junction Temperature Range	$-40°C \le T_J \le +125°C$

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics(1)

Specifications in Standard type face are for T_J = 25°C, and in **bold type face** apply over the full **Operating Temperature Range**. Unless otherwise specified, V_{IN} = 12V.

Symbol	Parameter	Conditions	Typical	Limit	Units
V_{FB}	Feedback Voltage	V_{COMP} = 1.4V, $2.97V \le V_{IN} \le 36V$	1.270	 1.260/**1.252** 1.288/**1.290**	V V(min) V(max)
ΔV_{LINE}	Feedback Voltage Line Regulation	$2.97V \le V_{IN} \le 36V$	0.001		%/V
ΔV_{LOAD}	Output Voltage Load Regulation		±0.5		%/V (max)
V_{UVLO}	Input Undervoltage Lock-out		2.87	 **2.97**	V V(max)
$V_{UV(HYS)}$	Input Undervoltage Lock-out Hysteresis		180	 **130** **225**	mV mV (min) mV (max)
F_{SW}	Switching Frequency		500	 **435** **575**	kHz kHz(min) kHz(max)
$R_{DS1\ (ON)}$	Driver Switch On Resistance (top)	I_{DR} = 0.2A, V_{IN}= 5V	7		Ω
$R_{DS2\ (ON)}$	Driver Switch On Resistance (bottom)	I_{DR} = 0.2A	4		Ω
$(V_{CB}-V_{SW})_{max}$	Maximum Boot Voltage	V_{IN} < 7.2V	V_{IN}		V
		$V_{IN} \ge 7.2V$	7.2		
D_{max}	Maximum Duty Cycle		93	 88	% %(min)
T_{min} (on)	Minimum On Time		330	 **230** **495**	nsec nsec(min) nsec(max)

(1) All limits are ensured at room temperature (standard type face) and at **temperature extremes (bold type face)**. All room temperature limits are 100% tested. All limits at **temperature extremes** are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics[1] (continued)

Specifications in Standard type face are for T_J = 25°C, and in **bold type face** apply over the full **Operating Temperature Range**. Unless otherwise specified, V_{IN} = 12V.

Symbol	Parameter	Conditions	Typical	Limit	Units
I_{SUPPLY}	Supply Current (switching)	[2]	2.0	**3.0**	mA mA (max)
I_Q	Quiescent Current in Shutdown Mode	[3], V_{IN} = 5V	5	**8**	µA µA (max)
$V_{CL(O)}$	Current Limit Voltage at 0% Duty Cycle	LM3477	155	130/**125** 185/**190**	mV mV (min) mV (max)
		LM3477A	165	140/**135** 195/**200**	mV mV (min) mV (max)
$V_{CL(100)}$	Current Limit Voltage at 100% Duty Cycle	LM3477	74	50/**43** 98/**98**	mV mV (min) mV (max)
		LM3477A	65	41/**25** 89/**98**	mV mV (min) mV (max)
V_{SC}	Short-Circuit Current Limit Sense Voltage	V_{IN} = 5V, LM3477	350	**270** **420**	mV mV (min) mV (max)
		V_{IN} = 5V, LM3477A	310	**260** **380**	mV mV (min) mV (max)
V_{SL}	Internal Compensation Ramp Voltage Height	V_{IN} = 5V, LM3477	83		mV
		V_{IN} = 5V, LM3477A	103		
V_{OVP}	Output Over-voltage Protection (with respect to feedback voltage) [4]	V_{COMP} = 1.4V	50	32/**25** 78/**85**	mV mV(min) mV(max)
$V_{OVP(HYS)}$	Output Over-Voltage Protection Hysteresis[4]	V_{COMP} = 1.4V	60	**20** **110**	mV mV(min) mV(max)
Gm	Error Amplifier Transconductance	V_{COMP} = 1.4V I_{EAO} = 100µA (Source/Sink)	750	600/**365** 1000/**1265**	µmho µmho (min) µmho (max)
A_{VOL}	Error Amplifier Voltage Gain	V_{COMP} = 1.4V I_{EAO} = 100µA (Source/Sink)	38	**30** **42**	V/V V/V (min) V/V (max)
I_{EAO}	Error Amplifier Output Current (Source/ Sink)	Source, V_{COMP} = 1.4V, V_{FB} = 0V	100	75/**50** 130/**160**	µA µA (min) µA (max)
		Sink, V_{COMP} = 1.4V, V_{FB} = 1.4V	−140	−110/**−95** −170/**−180**	µA µA (min) µA (max)
V_{EAO}	Error Amplifier Output Voltage Swing	Upper Limit V_{FB} = 0V COMP Pin = Floating	2.2	**2.0** **2.35**	V V(min) V(max)
		Lower Limit V_{FB} = 1.4V	0.75	**0.5** **0.95**	V V(min) V(max)
T_{SS}	Internal Soft-Start Delay	V_{FB} = 1.2V, V_{COMP} = Floating	5		msec
T_r	Drive Pin Rise Time	C_{GS} = 3000pF, V_{DR} = 0 to 3V	25		ns
T_f	Drive Pin Fall Time	C_{GS} = 3000pF, V_{DR} = 0 to 3V	25		ns

(2) For this test, the COMP/$\overline{SD}$ pin must be left floating.
(3) For this test, the COMP/$\overline{SD}$ pin must be pulled low.
(4) The over-voltage protection is specified with respect to the feedback voltage. This is because the over-voltage protection tracks the feedback voltage. The overvoltage protection threshold is given by adding the feedback voltage, V_{FB} to the over-voltage protection specification.

Electrical Characteristics(1) (continued)

Specifications in Standard type face are for T_J = 25°C, and in **bold type face** apply over the full **Operating Temperature Range**. Unless otherwise specified, V_{IN} = 12V.

Symbol	Parameter	Conditions	Typical	Limit	Units
V_{SD}	Shutdown Threshold (5)	Output = High	1.15	**1.35**	V V (max)
		Output = Low	0.65	**0.3**	V V (min)
I_{SD}	Shutdown Pin Current	V_{SD} = 5V	−1		µA
		V_{SD} = 0V	+1		
TSD	Thermal Shutdown		165		°C
T_{SH}	Thermal Shutdown Hysteresis		10		°C
θ_{JA}	Thermal Resistance	MM Package	200		°C/W

(5) The COMP/$\overline{SD}$ pin should be pulled to ground to turn the regulator off. The voltage on the COMP/$\overline{SD}$ pin must be below the limit for Output = Low to keep the regulator off.

Typical Performance Characteristics

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C.

I_Q (Shutdown) vs Temperature & Supply Voltage

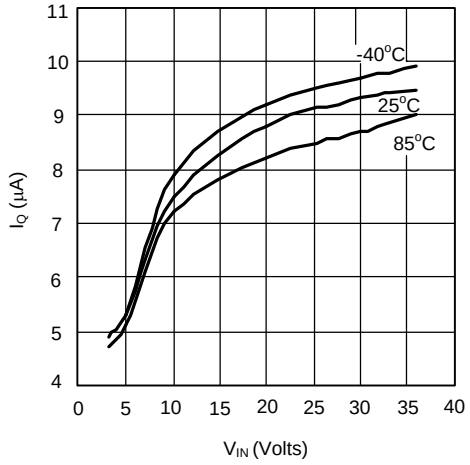


Figure 3.

I_{Supply} vs Temperature & Supply Voltage (Non-Switching)

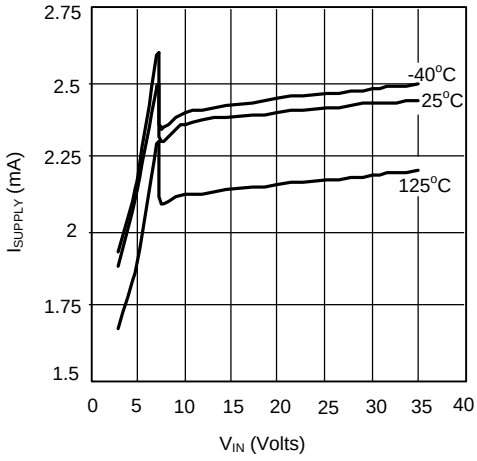


Figure 4.

I_{Supply} vs Temperature & Supply Voltage (Switching)

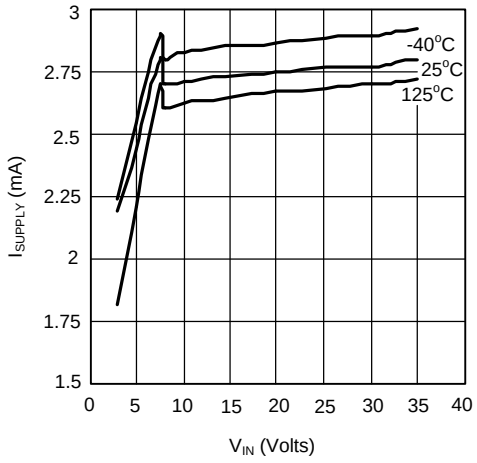


Figure 5.

Frequency vs Temperature

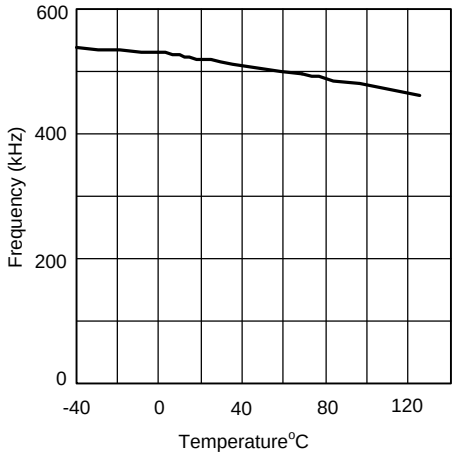


Figure 6.

V_{CB}–V_{SW} vs Supply Voltage

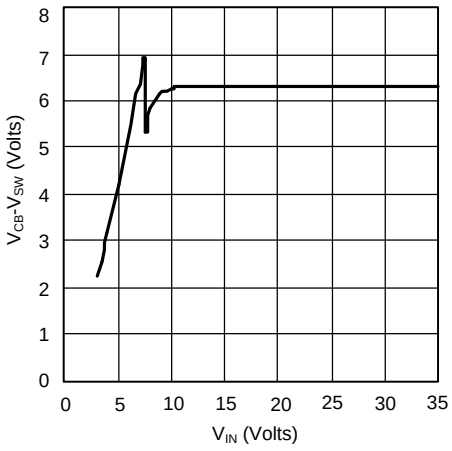


Figure 7.

COMP Pin Voltage vs Load Current

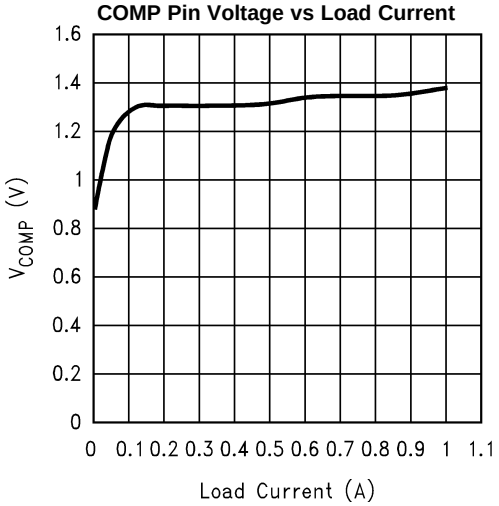


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C.

Efficiency vs Load Current (V_{IN} = 24V, V_{OUT} = 12V)

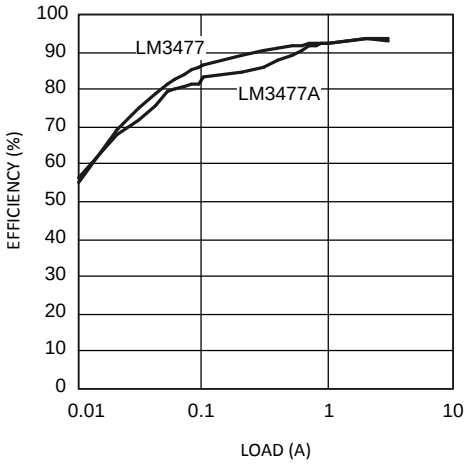


Figure 9.

Efficiency vs Load Current (V_{IN} = 5V, $_{OUT}$ = 3.3V)

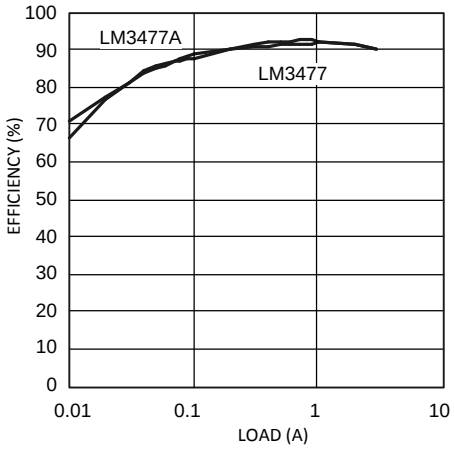


Figure 10.

Efficiency vs Load Current (V_{IN} = 12V, V_{OUT} = 3.3V)

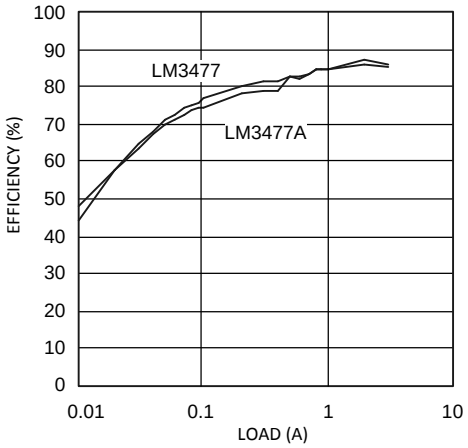


Figure 11.

Error Amplifier Gain

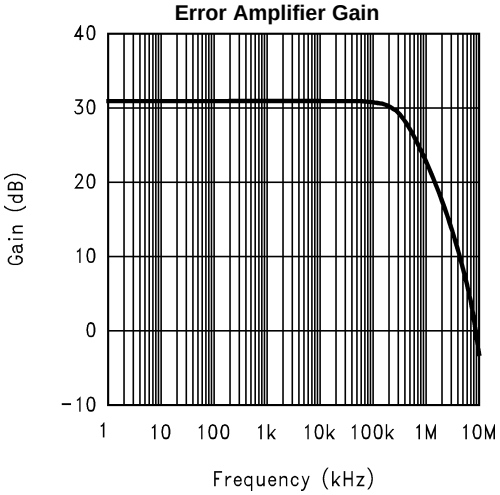


Figure 12.

Error Amplifier Phase Shift

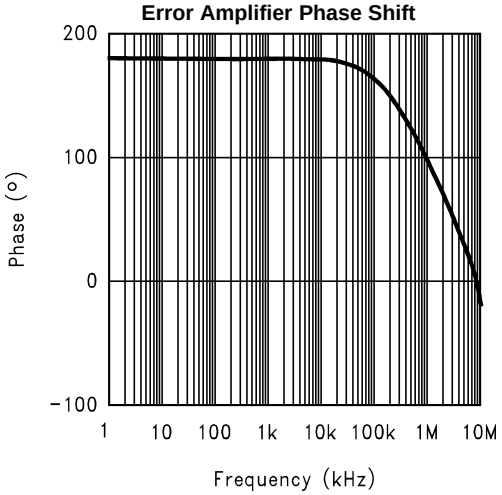


Figure 13.

COMP Pin Source Current vs Temperature

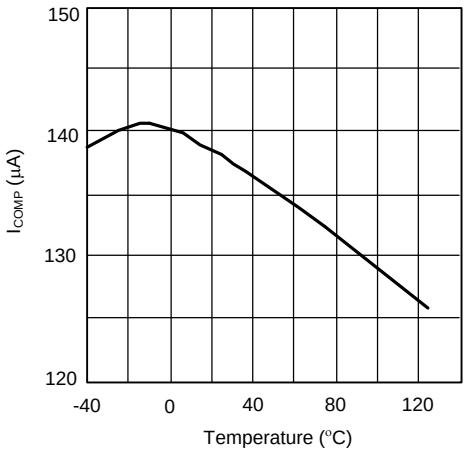


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C.

Short Circuit vs Temperature

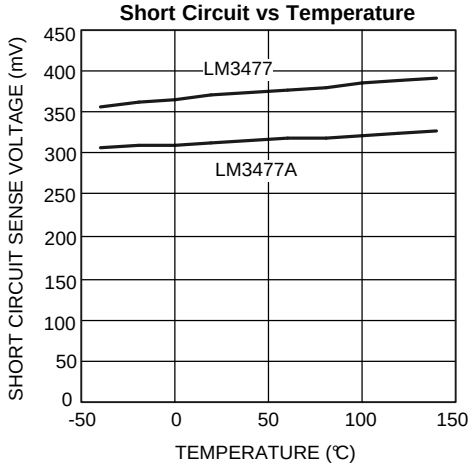


Figure 15.

Slope Compensation Ramp vs Slope Compensation Resistor

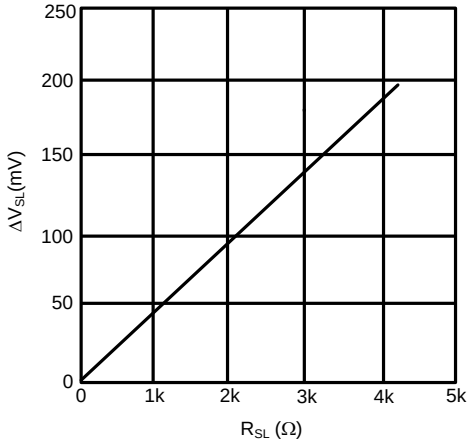


Figure 16.

Shutdown Threshold Hysteresis vs Temperature

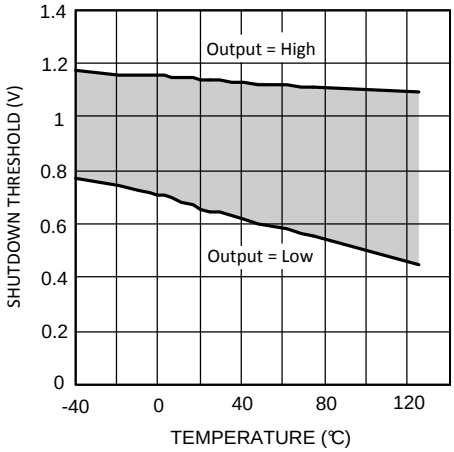


Figure 17.

Current Sense Voltage vs Duty Cycle

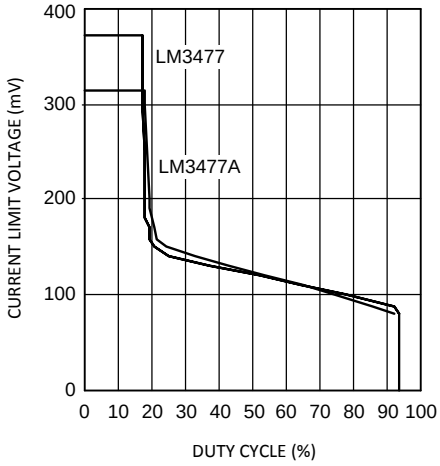
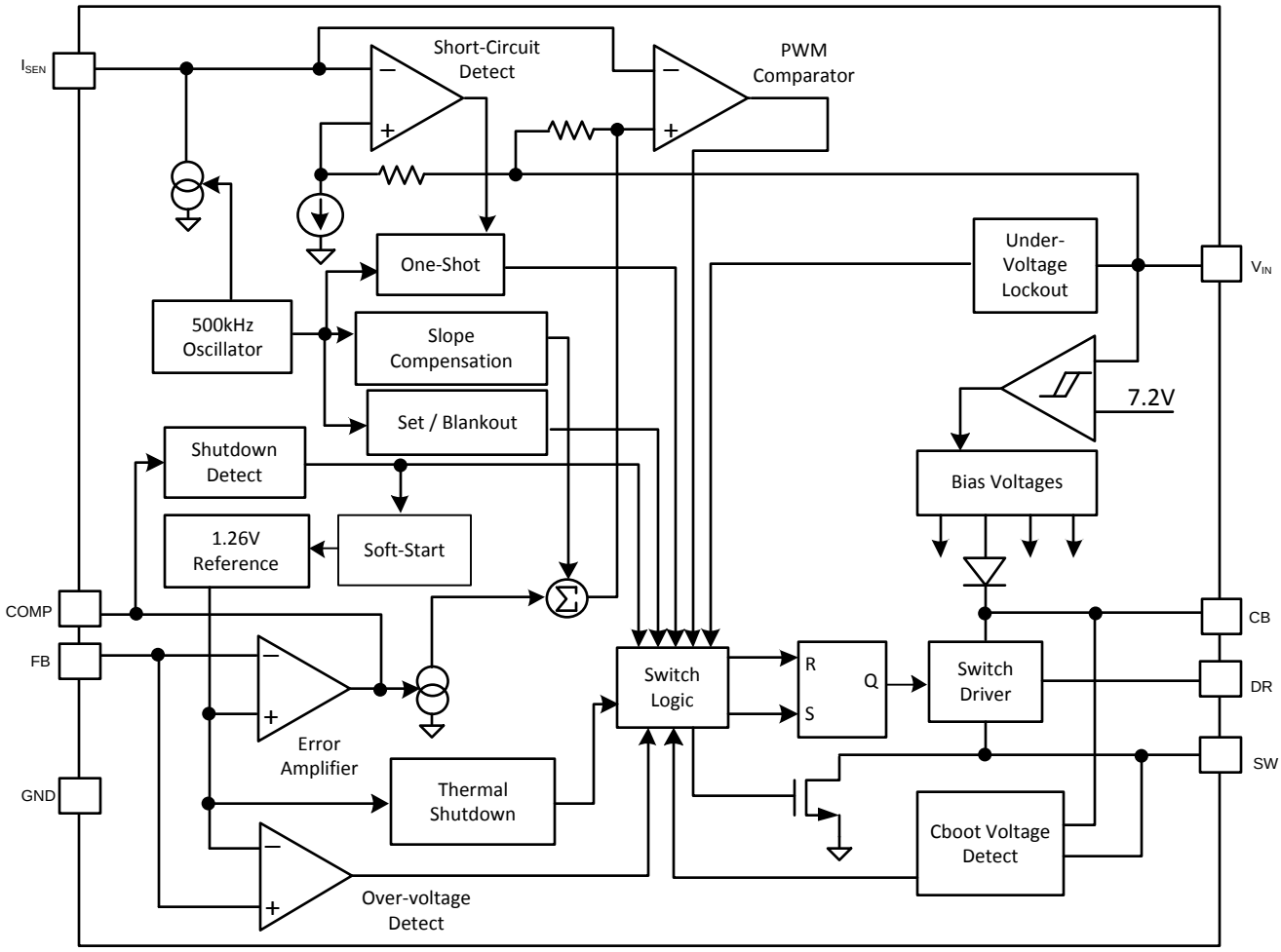


Figure 18.

Functional Block Diagram



FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION

The LM3477/A is a switching regulator controller for topologies incorporating a high side switch. The most common of these topologies is the step-down, or buck, converter. Other topologies such as the inverting (buck-boost) and inverse SEPIC (zeta) converters can be realized. This datasheet will focus on buck converter applications.

The LM3477/A employs current mode control architecture. Among the many benefits of this architecture are superior line and load regulation, cycle-by-cycle current limiting, and simple loop compensation. The LM3477/A features a patented adjustable slope compensation scheme to enable flexible inductor selection. The LM3477/A has a combination of features that allow its use in a wide variety of applications. The input voltage can range from 2.97V to 35V, with the output voltage being positive or negative depending on the topology. The current limit can be scaled to safely drive a wide range of loads. An internal soft-start is provided to limit initial in-rush current. Output over voltage and input under voltage protection ensure safe operation of the LM3477/A.

REGIONS OF OPERATION

Pulse width modulation (PWM) is the normal mode of operation. In PWM, the output voltage is well regulated and has a ripple frequency equal to the switching frequency (500kHz). In low load conditions, the part operates in hysteretic mode. In this mode, the output voltage is regulated between a high and low value that results in a higher ripple magnitude and lower ripple frequency than in PWM mode (see OVER VOLTAGE PROTECTION).

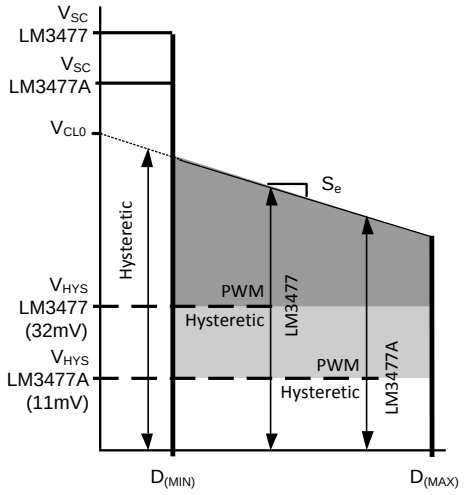


Figure 19. Operating Regions of the LM3477/A

The important differences between the LM3477 and the LM3477A are summarized in Figure 19. The voltages in Figure 19 can be referred to the switch current by dividing through by R_{SN}. The LM3477A has a lower hysteretic threshold voltage V_{HYS}, and thus will operate in PWM mode for a larger load range than the LM3477. Typically, V_{HYS} = 32mV for the LM3477, while V_{HYS} = 11mV for the LM3477A. The difference in area between the shaded regions give a graphical representation of this. The lightly shaded region is the extra PWM operating area gained by using the LM3477A. Thus the benefits of operating in PWM mode such as a well regulated output voltage with low noise ripple are extended to a larger load range when the LM3477A is used. While less significant, the other noteworthy difference between the two parts is in the short circuit current limit V_{SC}.

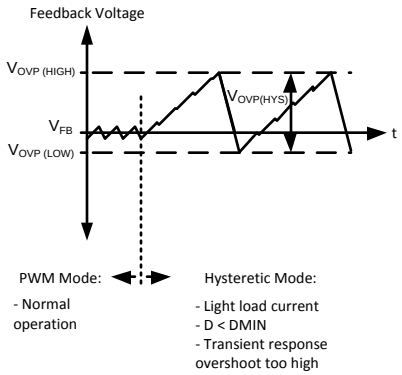
V_{SC} is a ceiling limit for the peak sense voltage V_{SNpk} (see SHORT CIRCUIT PROTECTION). V_{SC} is lower in the LM3477A than in the LM3477 (see the Electrical Characteristics for limits).

OVER VOLTAGE PROTECTION

The LM3477/A has over voltage protection (OVP) for the output voltage. OVP is sensed at and is in respect to the feedback pin (pin 3). If at anytime the voltage at the feedback pin rises to V_{FB} + V_{OVP}, OVP is triggered. See Electrical Characteristics for limits on V_{FB} and V_{OVP}.

OVP will cause the drive pin to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. The LM3477/A will begin switching again when the feedback voltage reaches V_{FB} + (V_{OVP} - $V_{OVP(HYS)}$). See Electrical Characteristics for limits on $V_{OVP(HYS)}$.

OVP can be triggered by any event that causes the output voltage to rise out of regulation. There are several common circumstances in which this can happen, and it is beneficial for a designer to be aware of these for debugging purposes, since the mode of operation changes from the normal Pulse Width Modulation (PWM) mode to the hysteretic mode. In the hysteretic mode the output voltage is regulated between a high and low value that results in a higher ripple magnitude and lower ripple frequency than in the PWM mode, see Figure 20.



See different Ripple Components in PWM and Hysteretic Modes.

Figure 20. The Feedback Voltage is related to the Output Voltage

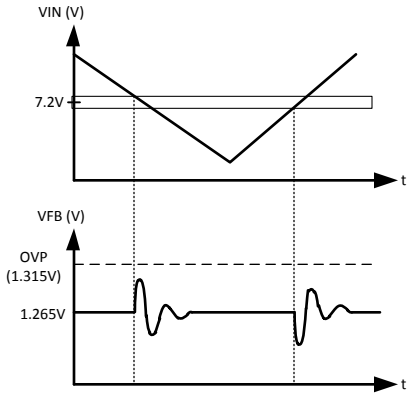
If the load current becomes too low, the LM3477/A will increase the duty cycle, causing the voltage to rise and trigger the OVP. The reasons for this involve the way the LM3477/A regulates the output voltage, using a control waveform at the pulse width modulator. This control waveform has upper and lower bounds.

Another way OVP can be tripped is if the input voltage rises higher than the LM3477/A is able to regulate in pulse width modulation (PWM) mode. The output voltage is related to the input voltage by the duty cycle as: $V_{OUT} = V_{IN}$*D. The LM3477/A has a minimum duty cycle of 16.5% (typical), due to the blank-out timing, TMIN. If the input voltage increases such that the duty cycle wants to be less than D_{MIN}, the duty cycle will hold at D_{MIN} and the output voltage will increase with the input voltage until it trips OVP.

It is useful to plot the operational boundaries in order to illustrate the point at which the device switches into hysteretic mode. In Figure 19, the limits shown are with respect to the peak voltage across the sense resistor R_{SN}, (V_{SNpk}); they can be referred to the peak inductor current by dividing through by R_{SN}. V_{SNpk} is bound to the shaded regions. In normal circumstances V_{SNpk} is required to be in the shaded region, and the LM3477/A will operate in the PWM mode. If operating conditions are chosen such that V_{SNpk} would not normally fall in the shaded regions, then the mode of operation is changed so that V_{SNpk} will be in the shaded region, and the part will operate in the hysteretic mode. What actually happens is that the LM3477/A will not allow V_{SNpk} to be outside of the shaded regions, so the duty cycle is adjusted.

The output voltage transient response overshoot can also trigger OVP. As discussed in Output Capacitor Selection, if the capacitance is too low or ESR too high, the output voltage overshoot will rise high enough to trigger OVP. However, as long as there is room for the duty cycle to adjust (the converter is not near D_{MIN} or D_{MAX}), the LM3477/A will return to PWM mode after a few cycles of hysteretic mode operation.

There is one last way that OVP can be triggered. If the unregulated input voltage crosses 7.2V, the output voltage will react as shown in Figure 21. The internal bias of the LM3477/A switches supplies at 7.2V. When this happens, a sudden small change in bias voltage is seen by all the internal blocks of the LM3477/A. The control voltage, VC, shifts because of the bias change, the PWM comparator tries to keep regulation. To the PWM comparator, the scenario is identical to step change in the load current, so the response at the output voltage is the same as would be observed in a step load change. Hence, the output voltage overshoot here can also trigger OVP. The LM3477/A will regulate in hysteretic mode for several cycles, or may not recover and simply stay in hysteretic mode until the load current drops. Note that the output voltage is still regulated in hysteric mode. Predicting whether or not the LM3477/A will come out of hysteretic mode in this scenario is a difficult task, however it is largely a function of the output current and the output capacitance. Triggering hysteretic mode in this way is only possible at higher load currents. The method to avoid this is to increase the output capacitance.



The Feedback Voltage Experiences an Oscillation if the Input Voltage Crosses the 7.2V Internal Bias Threshold

Figure 21.

DEFAULT/ADJUSTABLE SLOPE COMPENSATION

The LM3477/A uses a current mode control scheme. There are many advantages in a current mode architecture including inherent cycle-by-cycle current limiting and simple compensation of the control loop. However, there are consequences to using current mode control that one must be aware of while selecting circuit components. One of these consequences is the inherent possibility of subharmonic oscillations in the inductor current. This is a form of instability and should be avoided.

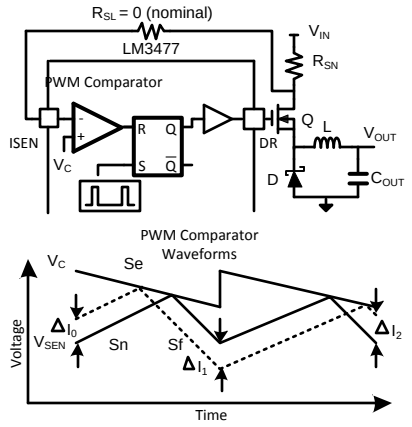


Figure 22. The Current Sensing Loop and Corresponding Waveforms

As a brief explanation, consider Figure 22. A lot of information is shown here. The top portion shows a schematic of the current sensing loop. The bottom portion shows the pulse width modulation (PWM) comparator waveforms for two switching cycles. The two solid waveforms shown are the waveforms compared at the internal pulse width modulator, used to generate the MOSFET drive signal. The top waveform with the slope S_e is the internally generated control waveform V_C. The bottom waveform with slopes S_n and S_f is the sensed inductor current waveform V_{SEN}. These signals are compared at the PWM comparator. There is a feedback loop involved here. The inductor current is sensed and fed back to the PWM comparator, where it is compared to V_C. The output of the comparator in combination with the R/S latch determine if the MOSFET is on or off, which effectively controls the amount of current the inductor receives. While V_C is higher than V_{SEN}, the PWM comparator outputs a high signal, driving the external power MOSFET on. When MOSFET is on, the inductor current rises at a constant slope, generating the sensed voltage V_{SEN}. When V_{SEN} equals V_C, the PWM comparator signals to drive the MOSFET off, and the sensed inductor current decreases with a slope S_f. The process begins again when R_S latch is set by an internal oscillator.

The subharmonic oscillation phenomenon is realized when a load excursion is experienced. The way it is analyzed is to calculate how the inductor current settles after such an excursion. Take for example the case when the inductor current experiences a step increase in its average current, shown as the dotted line in Figure 22. In the switching period that the excursion occurs, the inductor current will change by ΔI_0. In the following switching period, the inductor current will have a difference ΔI_1 from its original starting value. The original excursion is being propagated each switching cycle. What is desired is to find out if this propagation is converging or diverging. It is apparent that the difference in the inductor current from one cycle to the next is a function of S_n, S_f, and S_e, as follows:

$$\Delta I_n = \frac{S_f - S_e}{S_n + S_e} \Delta I_{n-1} \tag{1}$$

Hence, if the quantity $(S_f - S_e)/(S_n + S_e)$is greater than 1, the inductor current diverges and subharmonic oscillations result. Notice that as S_e increases, the factor decreases. Also, when the duty cycle is greater than 50%, as the inductance become less, the factor increases.

The LM3477/A internally generates enough slope compensation S_e to allow for the use of reasonable inductances. The height of the compensation slope ramp V_{SL} can be found in the Electrical Characteristics. The LM3477/A incorporates a patented scheme to increase S_e if there is need to use a smaller inductor. With the use of a single resistor R_{SL}, Se can be increased indefinitely. R_{SL} increases the compensation slope Se by the amount:

$$\Delta S_e = 50 \times 10^{-6} \times f_S \times R_{SL} \left(\frac{V}{\mu s}\right) \tag{2}$$

Therefore,

$$S_e = f_S (V_{SL} + 50 \times 10^{-6} \times R_{SL}) \left(\frac{V}{\mu s}\right) \tag{3}$$

When excursions of the inductor current are divergent, the current sensing control loop is unstable and produces a subharmonic oscillation in the inductor current. This oscillation is viewed as a resonance in the outer voltage control loop at half the switching frequency. In POWER INDUCTOR SECTION, calculations for minimum inductance and necessary slope resistance R_{SL} are carried out based on this resonant peaking.

START-UP/SOFT-START

The LM3477/A incorporates an internal soft-start during start-up. The soft-start forces the inductor current to rise slowly and smoothly as it increases towards the steady-state current. This technique is used to reduce the input inrush current during soft-start. The soft-start functionality is effective for approximately the first 5ms of start-up.

NOTE

The LM3477/A will not start-up if the output voltage is biased by more than 200mV above ground.

NOTE

If the slope resistor R_{SL} is used, the hysteretic threshold will be lowered. Therefore, the LM3477/A may require up to 100mA of pre-load to successfully start up.

SHORT CIRCUIT PROTECTION

When the voltage across the sense resistor (measured as the $V_{IN} - I_{SEN}$ differential voltage) exceeds V_{SC}, short-circuit current limit gets activated. In the short-circuit protection mode, the external MOSFET is turned off. When the short is removed, the external MOSFET is turned on after five cycles. The short circuit protection voltage V_{SC} is specified in the Electrical Characteristics. V_{SC} is lower in the LM3477A than in the LM3477.

SHUTDOWN

The compensation pin (Pin 2) of LM3477/A also functions as a shutdown pin. If a low signal (refer to the Electrical Characteristics for definition of low signal) appears on the COMP/$\overline{SD}$ pin, the LM3477/A stops switching and goes into a low supply current mode. The total supply current of the IC reduces to less than 10µA under these conditions. Figure 23 shows different implementations of the shutdown function.

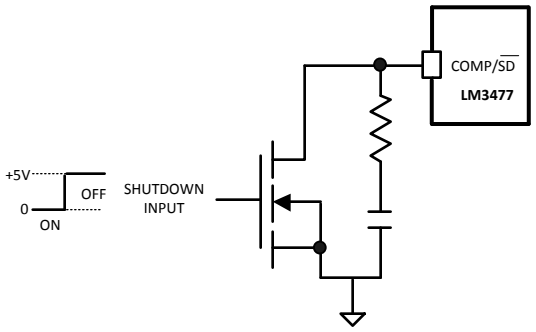


Figure 23. Implementing Shutdown in LM3477

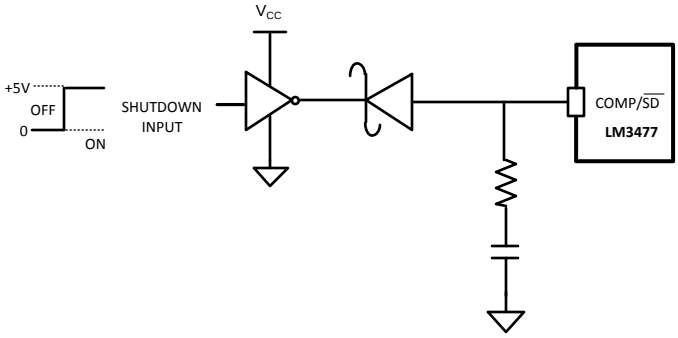


Figure 24. Implementing Shutdown in LM3477

Design Section

GENERAL

Power supply design involves making tradeoffs. To achieve performance specifications, limitations will be set on component selection. The LM3477/A provides many degrees of flexibility in choosing external components to accommodate various performance/component selection optimizations. For example, the internal slope compensation can be externally increased to allow smaller inductances to be used. The design procedures that follow provide instruction on how to select the external components in a typical LM3477/A buck circuit in continuous conduction mode, as well as aid in the optimization of performance and/or component selection. See Figure 25 for component reference and typical circuit. The LM3477/A may also be designed to operate in discontinuous conduction mode.

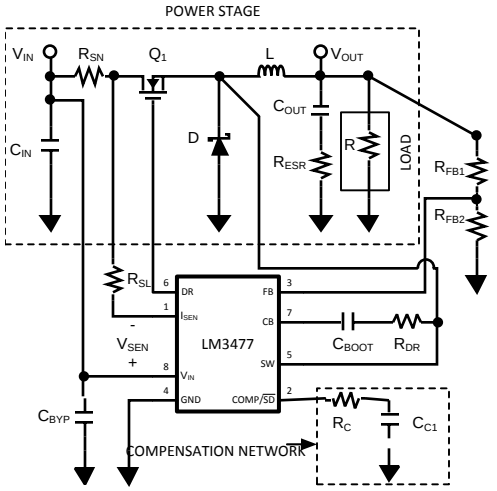


Figure 25. LM3477 Buck Converter Reference Schematic

PROGRAMMING THE OUTPUT VOLTAGE

The output voltage can be programmed using a resistor divider between the output and the feedback pins, as shown in Figure 25. The resistors are selected such that the voltage at the feedback pin is 1.27V. R_{FB1} and R_{FB2} can be selected using the equation:

$$V_{OUT} = 1.27*(1+ R_{FB1}/R_{FB2}) \quad (4)$$

CALCULATING THE DUTY CYCLE

In buck converter applications, the duty cycle of the LM3477/A may be calculated as:

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_Q - V_{SEN}} \approx \frac{V_{OUT}}{V_{IN}} \quad (5)$$

Where

V_D = forward drop of the power diode ≅ 0.5V

$V_Q = V_{DS}$ of the MOSFET when it is conducting ≅ $I_{OUT}*R_{DSON}$

V_{SEN} = Voltage across the sense resistor = I_{OUT} x R_{SN}

This is the fraction of the switching period that the switch is on. The switch is off for the remainder of the period. This fraction is expressed as:

$$D' = 1 - D \quad (6)$$

The LM3477/A has limits for the maximum and minimum duty cycle (see Electrical Characteristics). The maximum duty cycle of 93% (typical) will limit how low the input voltage may drop while maintaining a regulated output voltage (the dropout voltage). In situations where a very low dropout voltage is required, it is necessary to include V_D, V_Q and V_{SN} losses in the maximum duty cycle calculation. Voltage drops in the inductor will lower the dropout voltage as well.

The LM3487 provides the FET drive voltage through the voltage developed across Cboot, which is charged when the SW pin goes low. If Cboot cannot fully recharge, the device will automatically restart when the Cboot voltage falls below approximately 2V. Therefore, a Cboot value of at least 0.1uF is recommended to ensure normal operation at high duty cycles.

The minimum duty cycle of the LM3477/A corresponds to the minimum on time, or blank out time (see Electrical Characteristics).

$$D_{MIN} = T_{MIN}* f_s \quad (7)$$

This will not limit how high the input voltage can rise, however the LM3477/A will operate in hysteretic mode once the operating duty cycle decreases to the minimum duty cycle.

PROGRAMMING THE CURRENT LIMIT/HYSTERETIC THRESHOLD

Definitions

Current Limit: The current limit is the point at which the LM3477/A begins to limit the peak switch current. The current limit in the LM3477/A varies with duty cycle, which is a function of the V_{IN} − V_{OUT} differential.

Hysteric Threshold: Hysteretic threshold is the current at which the LM3477/A enters the hysteretic mode of operation (see OVER VOLTAGE PROTECTION). The hysteretic threshold is with respect to the peak switch current.

SETTING CURRENT LIMIT AND HYSTERETIC THRESHOLD

The adjustable current limit of the LM3477/A is set by the sense resistor R_{SN}. The voltage across R_{SN} is compared to an internal control voltage V_C. The onset of current limiting is when $V_{SEN(peak)}$ equals $V_{C(max)}$, or V_{CL}. V_{SEN} is defined here as the differential voltage from the V_{IN} pin to the I_{SEN} pin. V_{CL} decreases as the duty cycle increases, as shown in Figure 26. Therefore, it is important to know both $V_{SEN(peak)}$ and $V_{CL(min)}$ at the maximum operating duty cycle, or lowest V_{IN} condition.

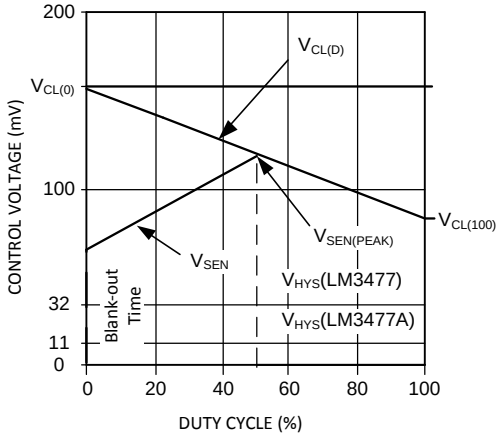


Figure 26. Current Limit and Hysteretic Threshold vs Duty Cycle

$$V_{SEN(PEAK)} = R_{SN}(I_{OUT(MAX)} + \frac{V_{OUT}(1-D_{MAX})}{2 \times L \times f_S}) \text{ (V)}, R_{SL} = 0$$

$$\approx R_{SN} \times I_{OUT(MAX)}(1+ 0.15) \text{ (V)} \quad (8)$$

$$V_{CL(MIN)} = V_{CL(0)(MIN)} - D_{(MAX)} (V_{CL(0)(MIN)} - V_{CL(100)(MIN)}) \quad (9)$$

where D_{MAX} is the duty cycle at the lowest V_{IN} condition.

To avoid current limit,

$$V_{SEN(peak)} < V_{CL(MIN)} \quad (10)$$

Therefore,

$$R_{SN(MAX)} = \frac{V_{CL(0)(MIN)} - D_{MAX} (V_{CL(0)(MIN)} - V_{CL(100)(MIN)})}{I_{OUT(MAX)} + \frac{V_{OUT}(1-D_{MAX})}{2 \times L \times f_S}}$$

$$\approx \frac{V_{CL(0)(MIN)} - D_{MAX} (V_{CL(0)(MIN)} - V_{CL(100)(MIN)})}{1.15 \times I_{OUT(MAX)}} \quad (11)$$

Example: $V_{IN(MIN)}$ = 4.5V, V_{OUT} = 2.5V, $I_{OUT(MAX)}$ = 3A

$$R_{SN(MAX)} = \frac{0.135 - 0.6 (0.135 - .025)}{1.15 (3)} = 0.02\Omega \quad (12)$$

The hysteretic threshold is derived in a similar manner, the only difference being that $V_{SEN(peak)}$ is compared $V_{C(min)}$ (V_{HYS}). Notice that V_{HYS} does not vary with the duty cycle. The hysteretic threshold is predetermined by the selection of R_{SN} above. The hysteretic threshold is:

$$I_{HYS} = \frac{V_{HYS}}{R_{SN}} = \frac{0.032}{R_{SN}} \text{ (A), LM3477}$$
$$= \frac{0.011}{R_{SN}} \text{ (A), LM3477A} \quad (13)$$

Continuing with the example above,

$$I_{HYS} = \frac{0.032}{0.02} = 1.6\text{A, LM3477}$$
$$= \frac{0.011}{0.02} \approx 0.55\text{A, LM3477A} \quad (14)$$

If the **peak switch current** decreases below this threshold, the LM3477/A will operate in hysteretic mode (see OVER VOLTAGE PROTECTION). In some designs, it will be desired to use R_{SL} so that lower valued inductors can be used (see DEFAULT/ADJUSTABLE SLOPE COMPENSATION and POWER INDUCTOR SECTION). Using R_{SL} will lower the current limit and the hysteretic threshold. See Figure 27. R_{SL} effectively adds an additional slope to the existing slope of the V_C waveform.

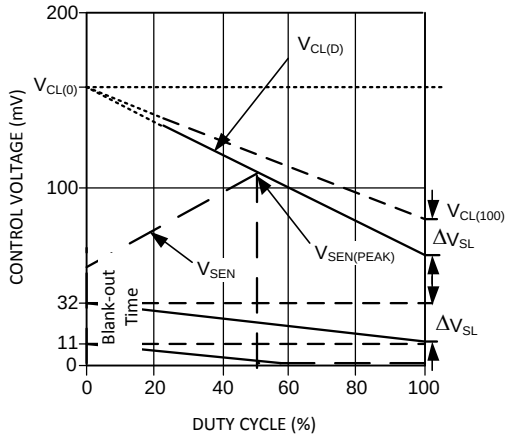


Figure 27. Current Limit and Hysteretic Threshold vs Duty Cycle with R_{SL}

When R_{SL} is used, the following equations apply:

$$R_{SN(MAX)} = \frac{V_{CL(0)(MIN)} - D_{MAX}\left(V_{CL(0)(MIN)} - \left(V_{CL(100)(MIN)} - 50 \times 10^{-6} \times R_{SL}\right)\right)}{I_{OUT} + \frac{V_{OUT}(1-D_{MAX})}{2 \times L \times f_S}}$$
$$\approx \frac{V_{CL(0)(MIN)} - D_{MAX}\left(V_{CL(0)(MIN)} - \left(V_{CL(100)(MIN)} - 50 \times 10^{-6} \times R_{SL}\right)\right)}{1.15 \times I_{OUT}} \quad (15)$$

$$I_{HYS} = \frac{MAX\left(V_{HYS} - 50 \times 10^{-6} \times R_{SL} \times D_{MAX}, 0\right)}{R_{SN}} \text{ (A)} \quad (16)$$

where $MAX(V_{HYS} - 50x10^{-6} \times R_{SL} \times D_{MAX}, 0)$ is the smaller of the two values in the parenthesis and V_{HYS} is 0.032V and 0.011V for the LM3477 and LM3477A, respectively. R_{SL} can be used creatively to intentionally lower the hysteretic threshold, allowing for better performance at lower loads. However, when R_{SL} is used, there may be a minimum load requirement (see START-UP/SOFT-START).

POWER INDUCTOR SECTION

The LM3477/A operates at a high switching frequency of 500kHz, which allows the use of small inductors. This is made apparent in the following set of equations used to calculate the output voltage ripple.

$$\Delta V_{OUT(Pk\text{-}Pk)} \cong \Delta i_{L(Pk\text{-}Pk)} \times R_{ESR} \text{ (V)} \tag{17}$$

$$\Delta i_{L(Pk\text{-}Pk)} = \frac{V_{OUT}\,(1\text{-}D)}{L \times f_S} \text{ (A)} \tag{18}$$

As the switching frequency fs increases, the inductance required for a given output voltage ripple decreases. The equations above for ΔV_{OUT} and Δi_L provide criteria for choosing the inductance. The maximum voltage ripple in steady-state, PWM operation can be controlled by limiting Δi_L which in turn is set by the inductance value. Alternatively, one can simply choose Δi_L as a percentage of the maximum output current. Clearly, the size of the output capacitor ESR, R_{ESR}, will have an affect on which criteria is used to choose the inductance. When the ESR is relatively low (less than 100mΩ), such as in ceramic, OSCON, and some low ESR tantalum capacitors, it is convenient to choose the inductance based on setting Δi_L to 30% of Iout(max). If the ESR is high, then it may be necessary to restrict Δi_L to a lower value so that the output voltage ripple is not too high. Generally speaking, the former suggestion of setting Δi_L to 30% of $I_{OUT(MAX)}$ is recommended.

The inductance also affects the stability of the converter. The slopes S_n and S_f in Figure 22 are functions of the inductance, while the compensation ramp, S_e, is fixed by default. Therefore if the inductance is too small, the converter may experience sub-harmonic oscillations. The LM3477/A provides sufficient internal slope compensation to allow for inductances chosen according to the $\Delta i_L = 0.3 \times I_{OUT}$ guideline in most cases. Still, one should check to make sure the inductance is not too low before continuing the design process. If it is found that the selected inductance is too low, a patented scheme to increase the compensation ramp, S_e, is provided in the LM3477/A (see DEFAULT/ADJUSTABLE SLOPE COMPENSATION). In the calculations that follow, if it is found that the chosen inductance is too small, R_{SL} can be used to increase Se so that the inductance can be used.

In a current mode control architecture, there is an inherent resonance at half the switching frequency (see DEFAULT/ADJUSTABLE SLOPE COMPENSATION). A convenient indicator of how much resonance exists is the quality factor Q. If Q is too high, subharmonic oscillations could occur, if Q is too low, the current mode architecture begins to act like a voltage mode architecture and the necessary compensation becomes more complex. This is discussed in more detail in Compensation, but here it is important to calculate Q to be sure the selected inductance will not cause problems to the stability of the converter. The calculations below call for an inductance that results in Q between 0.15 and 2. See Compensation if the chosen inductance enforces Q to be out of this range. By default, no extra slope compensation is needed, so R_{SL} = 0. In general, a Q between 0.5 and 1 is optimal.

$$Q = \frac{1}{\pi\,(m_c \times D' - 0.5)} \tag{19}$$

Where,

$$D' = 1 - D \tag{20}$$

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_Q - V_{SEN}} \approx \frac{V_{OUT}}{V_{IN}} \tag{21}$$

$$m_c = 1 + \frac{S_e}{S_n} = 1 + \frac{f_S L (V_{SL} + 50 \times 10^{-6} \times R_{SL})}{1.8 R_{SN} V_{IN}\, D' - V_Q - V_{SEN}} \approx 1 + \frac{f_S L (V_{SL} + 50 \times 10^{-6} \times R_{SL})}{1.8 R_{SN} V_{IN}\, D'} \tag{22}$$

$V_Q = V_{DS}$ of the MOSFET when it is conducting $I_{OUT} * R_{DS(ON)}$.

1.8 = voltage gain of the current sense amp.

V_{SEN} = Voltage across the sense resistor ≅ $I_{OUT} \times R_{SN}$

Back solving for L gives a range for acceptable inductances based on a range for Q:

$$\frac{V_{IN} 1.8 R_{SN} \left(\frac{1}{\pi Q_{MAX}} + D\text{-}0.5\right)}{f_S (V_{SL} + 50 \times 10^{-6} \times R_{SL})} \le L \le \frac{V_{IN} 1.8 R_{SN} \left(\frac{1}{\pi Q_{MIN}} + D\text{-}0.5\right)}{f_S (V_{SL} + 50 \times 10^{-6} \times R_{SL})} \tag{23}$$

It is recommended that:

Q(max) = 2, and

Q(min) = 0.15

Values for V_{SL} can be found in the Electrical Characteristics.

Note: Adding slope compensation with R_{SL} will decrease the current limit. An iterative process may be needed to meet current limit and stability requirements, see PROGRAMMING THE CURRENT LIMIT/HYSTERETIC THRESHOLD.

Output Capacitor Selection

A capacitance between 47µF - 100µF is typically used. Skip to CALCULATIONS FOR THE OUTPUT CAPACITOR for minimum capacitance calculations.

TYPE OF OUTPUT CAPACITORS

Different type of capacitors often have different combinations of capacitance, equivalent series resistance (ESR), and voltage ratings. High-capacitance multi-layer ceramic capacitors (MLCCs) have a very low ESR, typically 12mΩ, but also relatively low capacitance and low voltage ratings. Tantalum capacitors can have fairly low ESR, such as 18mΩ, and high capacitance (up to 1mF) at higher voltage ratings than MLCCs. Aluminum capacitors offer high capacitance and relatively low ESR and are available in high voltage ratings. OSCON capacitors can achieve ESR values that are even lower than those of MLCCs and with higher capacitance, but the voltage ratings are low. Other tradeoffs in capacitor technology include temperature stability, surge current capability, and capacitance density (physical size vs. capacitance).

OUTPUT CAPACITOR CONSIDERATIONS

Skip to CALCULATIONS FOR THE OUTPUT CAPACITOR if a quick design is desired. While it is generally desired to use as little output capacitance as possible to keep costs down, the output capacitor should be chosen with care as it directly affects the ripple component of the output voltage as well as other components in the design. The output voltage ripple is directly proportional to the ESR of the output capacitor (see POWER INDUCTOR SECTION). Therefore, designs requiring low output voltage ripple should have an output capacitor with low ESR. Choosing a capacitor with low ESR has the additional benefit of requiring one less component in the compensation network, as discussed in Compensation.

In addition to the output voltage ripple, the output capacitor directly affects the output voltage overshoot in a load transient. Two transients are possible: an unloading transient and a loading transient. An unloading transient occurs when the load current transitions to a higher current, and charge is unloaded from the output capacitor. A loading transient is when the load transitions to a lower current, and charge is loaded to the output capacitor. How the output voltage reacts during these transitions is known as the transient response. Both the capacitance and the ESR of the output capacitor will affect the transient response.

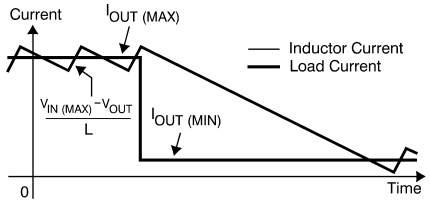


Figure 28. A Loading Transient

The control loop of the LM3477/A can be made fast enough to saturate the duty cycle when the worst case lode transient occurs. This means the duty cycle jumps to D_{MIN} or D_{MAX}, depending on the type of load transient. In a loading transient, as shown in Figure 28, the duty cycle drops to D_{MIN} while the inductor current falls to match the load current. During this time, the regulator is heavily dependent on the output capacitors to handle the load transient. The initial overshoot is caused by the ESR of the output capacitors. How the output voltage recovers after that initial excursion depends on how fast the inductor current falls and how large the output capacitance is. See Figure 29.

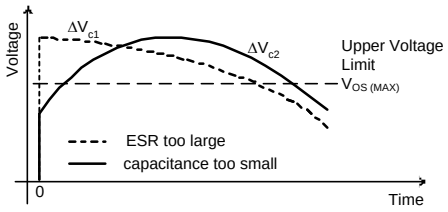


Figure 29. Output Voltage Overshoot Violation

The ESR and the capacitance of the output capacitor must be carefully chosen so that the output voltage overshoot is within the design's specification $V_{OS(MAX)}$. If the total combined ESR of the output capacitors is not low enough, the initial output voltage excursion will violate the specification, see ΔV_{C1}. If the ESR is low enough, but there is not enough output capacitance, the output voltage will travel outside the specification window due to the extra charge being dumped into the capacitor, see ΔV_{C2}. The LM3477/A has output over voltage protection (OVP) which could trigger if the transient overshoot is high enough. If this happens, the controller will operate in hysteretic mode (see OVER VOLTAGE PROTECTION) for a few cycles before the output voltage settles to its steady state. If this behavior is not desired, substitute V_{OVP} (referred to the output) for $V_{OS(MAX)}$ (V_{OVP} is found in the Electrical Characteristics) to find the minimum capacitance and maximum ESR of the output capacitor.

CALCULATIONS FOR THE OUTPUT CAPACITOR

During a loading transient, the delta output voltage ΔV_c has two changing components. One is the voltage difference across the ESR (ΔV_r), the other is the voltage difference caused by the gained charge (ΔV_q). This gives:

$$\Delta V_c = \Delta V_r + \Delta V_q \tag{24}$$

The design objective is to keep ΔV_c lower than some maximum overshoot ($V_{OS(MAX)}$). $V_{OS(MAX)}$ is chosen based on the output load requirements.

Both voltages ΔV_r and ΔV_qwill change with time. For ΔV_r the equation is:

$$\Delta V_r = R_{ESR}(\Delta I_{OUT(MAX)} - \frac{V_{OUT} \cdot D_{MIN} V_{IN}}{L} t)\,(V) \tag{25}$$

where,

R_{ESR} = the output capacitor ESR

ΔI_{OUT} = the difference between the load current change $I_{OUT(MAX)} - I_{OUT(MIN)}$

D_{MIN} = Minimum duty cycle of device (0.165 typical)

Evaluating this equation at t = 0 gives $\Delta V_{r(max)}$. Substituting $V_{OS(MAX)}$ for $\Delta V_{r(MAX)}$ and solving for R_{ESR} gives:

$$R_{ESR(MAX)} = \frac{V_{OS(MAX)}}{\Delta I_{OUT(MAX)}}\,\Omega \tag{26}$$

The expression for ΔV_q is:

$$\Delta V_q = \frac{\Delta I_{OUT(MAX)}}{C_{OUT}} t - \frac{V_{OUT} \cdot D_{MIN} V_{IN}}{2 \times L \times C_{OUT}} t^2\,(V) \tag{27}$$

From Figure 30 it can be told that ΔV_C will reach its peak value at some point in time and then decrease. The larger the output capacitance is, the earlier the peak will occur. To find the peak position, let the derivative of ΔV_C go to zero, and the result is:

$$t_{peak} = \frac{\Delta I_{OUT(MAX)} \times L}{V_{OUT} - D_{MIN} V_{IN}} - C_{OUT} R_{ESR} \tag{28}$$

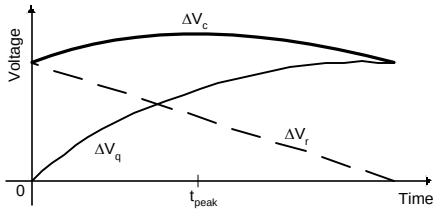


Figure 30. Output Voltage Overshoot Peak

The intention is to find the capacitance value that will yield, at t_{peak}, a ΔV_C that equals $V_{OS(max)}$. Substituting tpeak for t and equating ΔV_C to $V_{OS(max)}$ gives the following solution for $C_{OUT(MIN)}$:

$$C_{OUT(MIN)} = \frac{L\left(V_{OS(MAX)} - \sqrt{V_{OS(MAX)}^2 - (\Delta I_{OUT(MAX)} \times R_{ESR})^2}\right)}{(V_{OUT})\, R_{ESR}^2} (F) \quad (29)$$

The chosen output capacitance should not be less than 47µF, even if the solution for $C_{OUT(MIN)}$ is less than 47µF. Notice it is already assumed that the total ESR is no greater than $R_{ESR(MAX)}$, otherwise the term under the square root will be a negative number.

Power Mosfet Selection

The drive pin of LM3477/A must be connected to the gate of an external MOSFET. In a buck topology, the drain of the external N-Channel MOSFET is connected to the input and the source is connected to the inductor. The C_B pin voltage provides the gate drive needed for an external N-Channel MOSFET. The gate drive voltage depends on the input voltage (see Typical Performance Characteristics). In most applications, a logic level MOSFET can be used. For very low input voltages, a sub-logic level MOSFET should be used.

The selected MOSFET directly controls the efficiency. The critical parameters for selection of a MOSFET are:

1. Minimum threshold voltage, V_{TH}(MIN)
2. On-resistance, R_{DS}(ON)
3. Total gate charge, Q_g
4. Reverse transfer capacitance, C_{RSS}
5. Maximum drain to source voltage, $V_{DS(MAX)}$

The off-state voltage of the MOSFET is approximately equal to the input voltage. $V_{DS(MAX)}$ of the MOSFET must be greater than the input voltage. The power losses in the MOSFET can be categorized into conduction losses and ac switching or transition losses. $R_{DS(ON)}$ is needed to estimate the conduction losses. The conduction loss, P_{COND}, is the I^2R loss across the MOSFET. The maximum conduction loss is given by:

$$P_{COND(MAX)} = I^2 D_{MAX}\left[1 + \frac{1}{12}\left(\frac{\Delta i_{(PK-PK)}}{I}\right)^2\right] R_{DS(ON)} \quad (30)$$

where D_{MAX} is the maximum operating duty cycle:

$$D_{max} \approx \frac{V_{OUT}}{V_{IN(MIN)}} \quad (31)$$

The turn-on and turn-off transition times of a MOSFET from the MOSFET specifications require tens of nano-seconds. C_{RSS} and Q_g are needed from the MOSFET specifications to estimate the large instantaneous power loss that occurs during these transitions.

The average amount of gate current required to turn the MOSFET on can be calculated using the formula:

$$I_G = Q_g.F_S \quad (32)$$

The required gate drive power to turn the MOSFET on is equal to the switching frequency times the energy required to deliver the charge to bring the gate charge voltage to V_{DR} (see Electrical Characteristics and Typical Performance Characteristics for the drive voltage specification).

$$P_{Drive} = F_S.Q_g.V_{DR} \quad (33)$$

It is sometimes helpful or necessary to slow down the turn on transition of the FET so that less switching noise appears at the I_{SEN} pin. This can be done by inserting a drive resistor R_{DR} in series with the boot-strap capacitor (see Figure 25). This can help reduce sensing noise that may be preventing designs from operating at or near the LM3477/A's minimum duty cycle limit. Gate drive resistors from 2.2Ω to 51Ω are recommended.

Power Diode Selection

The output current commutates through the diode when the external MOSFET turns off. The three most important parameters for the diode are the peak current, peak inverse voltage, and average power dissipation. Exceeding these ratings can cause damage to the diode. The average current through the diode is given by:

$$I_{D(AVG)} = I_{OUT} \times (1-D) \quad (34)$$

where D is the duty cycle and I_{OUT} is the output current. The diode must be rated to handle this current.

The off-state voltage across the diode in a buck converter is approximately equal to the input voltage. The peak inverse voltage rating of the diode must be greater than the off-state voltage of the diode. To improve efficiency, a low forward drop schottky diode is recommended.

Input Capacitor Selection

In a buck converter, the high side switch draws large ripple currents from the input capacitor. The input capacitor must be rated to handle this RMS current.

$$I_{RMS\_CIN} = I_{OUT} \sqrt{\frac{V_{OUT}(V_{IN}-V_{OUT})}{V_{IN}}} \quad (35)$$

The power dissipated in the input capacitor is given by:

$P_{D(CIN)}=I_{RMS\_CIN}{}^2 R_{ESR\_CIN}$,

where R_{ESR_CIN} is the ESR of the input capacitor. The input capacitor must be selected to handle the rms current and must be able to dissipate the power. $P_{D(CIN)}$ must be lower than the rated power dissipation of the selected input capacitor. In many cases, several capacitors have to be paralleled to handle the rms current. In that case, the power dissipated in each capacitor is given by:

$P_{D(CIN)} = (I^2_{RMS\_CIN} R_{ESR\_CIN})/n^2$, where n is the total number of capacitors paralled at the input.

A 0.1µF or 1µF ceramic bypass capacitor is also recommended on the V_{IN} pin (pin 8) of the IC. This capacitor must be connected very close to pin 8.

Compensation

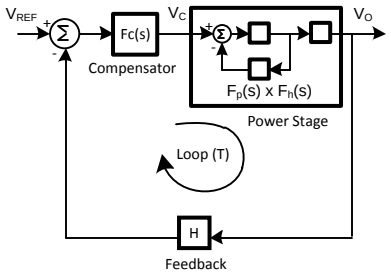


Figure 31. Control Block Diagram of a Current Mode Controlled Buck Converter

The LM3477/A is a current mode controller, therefore the control block diagram representation involves 2 feedback loops (see Figure 31). The inner feedback loop derives its feedback from the sensed inductor current, while the outer loop monitors the output voltage. This section will not give a rigorous analysis of current mode control, but rather a simplified but accurate method to determine the compensation network. The first part reveals the results of the model, giving expressions for solving for component values in the compensation network.

The compensation network is designed around the power components, or the power stage. An isolated schematic of the error amplifier and the various compensation components is shown in Figure 32. The error amplifier in conjunction with the compensation network makes up the compensator block in Figure 31. The purpose of the compensator block is to stabilize the control loop and achieve high performance in terms of the transient response, audio susceptibility and output impedance.

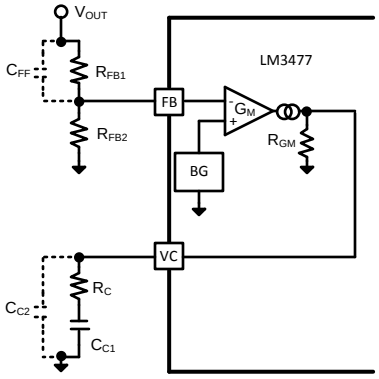
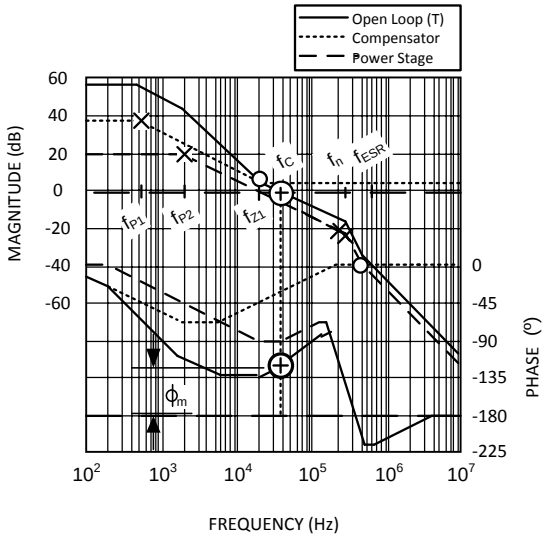


Figure 32. LM3477 Compensation Components

Figure 33 shows a bode plot of a typical current mode buck regulator. It is an estimate of the actual plot using the asymptotic approach. The three plots shown are of the compensator, powerstage, and loop gain, which is the product of the power stage, compensator, and feedback gain. The loop gain determines both static and dynamic performance of the converter. The power stage response is fixed by the selection of the power components, therefore the compensator is designed around the powerstage response to achieve a good loop response. Specifically, the compensator is added to increase low frequency magnitude, extend the 0dB frequency (crossover frequency), and improve the phase characteristic.



Poles, Zeros and Important Measurements are Labeled

Figure 33. Typical Open Loop, Compensator, and Power Stage Bode Plots for LM3477 Buck Circuits

There are several different types of compensation that can be used to improve the frequency response of the control loop. To determine which compensation scheme to use, some information about the power stage is needed.

Use $V_{IN} = V_{IN(MIN)}$ and $R = R_{MIN}$ ($I_{OUT(MAX)}$) when calculating compensation components.

$$H = \text{feedback gain} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \quad (36)$$

$$A_{DC} = \frac{R}{1.8R_{SN}} \frac{1}{1+\frac{R}{f_S L}\left[m_c \times D' - 0.5\right]} \quad (37)$$

$$m_c = 1+\frac{S_e}{S_n} \quad (38)$$

$$S_e = f_S(V_{SL} + 50x10^{-6} R_{SL}) \quad (39)$$

$$S_n = \frac{V_{IN}D' \times 1.8R_{SN}}{L} \quad (40)$$

$$f_{p1} = \frac{1}{2\pi}\left[\frac{1}{C_{OUT}R} + \frac{1}{f_s L C_{OUT}}(m_c \times D' - 0.5)\right] (Hz) \quad (41)$$

$$f_{ESR} = \frac{1}{2\pi C_{OUT} R_{ESR}} (Hz) \quad (42)$$

$$Q = \frac{1}{\pi (m_c \times D' - 0.5)} \quad (43)$$

With the power stage known, a compensator can be designed to achieve improved performance and stability. The LM3477/A will typically require only a single resistor and capacitor for compensation, but depending on the power stage it could require three or four external components.

It is a good idea to check that Q is between 0.15 and 2, if it was not already done when selecting the inductor. If Q is less than 0.15 or greater than 2, skip to SAMPLING POLE QUALITY FACTOR before continuing with the compensator design.

First, a target crossover frequency (f_c) for the loop gain must be selected. The crossover frequency is the bandwidth of the converter. A higher bandwidth generally corresponds to faster response times and lower overshoots to load transients. However, the bandwidth should not be much higher than 1/10 the switching frequency. The LM3477/A operates with a 500kHz switching frequency, so it is recommended to choose a crossover frequency between 10kHz - 50kHz.

The schematic of the LM3477/A compensator is shown in Figure 32. The default design uses R_c and C_{C1} to form a lag (type 2) compensator. The C_{C2} capacitor can be added to form an additional pole that is typically used to cancel out the esr zero of the output capacitor. Finally, if extra phase margin is needed, the Cff capacitor can be added (this does not help at low output voltages, see below).

The strategy taken here for choosing R_c and C_{C1} is to set the crossover frequency with R_c, and set the compensator zero with C_{C1}. Using the selected target crossover frequency, f_C, set R_C to:

$$R_C = \frac{f_C \times R_{GM}}{A_{DC} \times GM \times R_{GM} \times H \times f_{P1} - f_C} \Omega \quad (44)$$

f_C = Crossover frequency in Hertz (20kHz - 50kHz is recommended)

$R_{GM} = 50x10^3\Omega$

$GM = 1000x10^{-6}$ A/V

The compensator zero, f_{Z1}, is set with C_{C1}. When fast transient responses are desired, f_{Z1} should be placed as high as possible, however it should not be higher than the selected crossover frequency f_C. The guideline proposed here is to choose C_{C1} such that f_{Z1} falls somewhere between the power pole f_{P1} and ½ decade before the selected crossover frequency fc:

$$\frac{3.16}{2\pi f_C R_C} \leq C_{C1} \leq \frac{1}{2\pi f_{p1} R_C} \quad (45)$$

In this compensation scheme, the pole created by C_{C2} is used to cancel out the zero created by the ESR of the output capacitor. In other schemes such as the methods discussed in SAMPLING POLE QUALITY FACTOR, the ESR zero is used. For the typical case, use C_{C2} if:

$$f_{ESR} < \frac{f_S}{2} \quad (46)$$

$$C_{C2} = \frac{R_{GM} + R_C}{2\pi f_{ESR} R_{GM} R_C} \text{ (F)} \quad (47)$$

PLOTTING THE OPEN LOOP RESPONSE

The open loop response is expressed as:

$T = A_{DC} \times A_{CM} \times H \times F_p(s) \times F_c(s)$

Where A_{DC} and H are given above and

$A_{CM} = GM \times R_{GM}$

$$F_{P(S)} = \frac{1 + \frac{s}{2\pi f_{ESR}}}{1 + \frac{s}{2\pi f_{p1}}} \quad (48)$$

$$F_h(s) = \frac{1}{s^2\left(\frac{1}{\pi f_s}\right)^2 + s\left(\frac{1}{\pi f_s Q}\right) + 1} \quad (49)$$

$$F_C(s) = \frac{(sC_{C1}R_C + 1)}{sC_{C1}R_{GM}(R_{GM} + R_C) + 1}, \; C_{C2} \text{ not used} \quad (50)$$

$$F_C(s) = \frac{(sC_{C1}R_C + 1)}{s^2 C_{C1}C_{C2}R_C R_{GM} + s(C_{C2}R_{GM} + C_{C1}(R_{GM} + R_C)) + 1}, \; C_{C2} \text{ used} \quad (51)$$

One can plot the magnitude and phase of the open loop response to analyze the frequency response.

EXAMPLE: COMPENSATION DESIGN

$4.5V \le V_{IN} \le 5.5V$

$V_{OUT} = 2.5V$

$I_{OUT} = 3A$ (R = 0.83Ω)

$R_{SN} = 0.02\Omega$

$L = 3.3\mu H$

$R_{SL} = 0\Omega$

$C_{OUT} = 100\mu F$

$R_{ESR} = 0.01\Omega$

First, calculate the power stage parameters using $V_{IN(MIN)}$ and $R_{(MAX)}$:

$$\text{H = feedback gain} = \frac{1.27}{2.5} = 0.508 \quad (52)$$

$$A_{DC} = \frac{0.83}{1.8 \times 0.02} \; \frac{1}{1 + \frac{0.83}{(500 \times 10^3)(3.3 \times 10^{-6})} \; [(3.36)(0.44) - 0.5]} = 15.5 \quad (53)$$

$$f_{p1} = \frac{1}{2\pi}\left(\frac{1}{(100 \times 10^{-6})(0.83)} + \frac{1}{(500 \times 10^3)(3.3 \times 10^{-6})(100 \times 10^{-6})} \left[\,(3.36)(0.44) - 0.5\,\right]\right) = 2.86 \text{ kHz} \quad (54)$$

$$f_{ESR} = \frac{1}{2\pi(100 \times 10^{-6})(0.01)} = 159\text{kHz} \quad (55)$$

$$Q = \frac{1}{\pi[(3.36)(0.44) - 0.5]} = 0.33 \quad (56)$$

In this example, a crossover frequency of 20kHz is chosen, so: $f_C = 20000$. R_C is now calculated using the power stage information and the target crossover frequency f_C:

$$R_C = \frac{(20 \times 10^3)(50 \times 10^3)}{(15.5)(0.001)(50 \times 10^3)(0.508)(2.86 \times 10^3) - (20 \times 10^3)}$$

$$= 904\Omega \quad (57)$$

This sets the high frequency gain of the compensator such that a crossover frequency of f_C is obtained. The capacitor C_{C1} sets the compensator zero, f_{Z2}. Set f_{Z2} between the power pole f_{P1} and the ½ decade before the target crossover frequency f_C:

$$\frac{3.16}{2\pi(20 \times 10^3)(900)} \leq C_{C1} \leq \frac{1}{2\pi(2.86 \times 10^3)(900)}$$

$$28\ nF \leq C_{C1} \leq 62\ nF \quad (58)$$

Choosing $C_{C1} = 62 \times 10^{-9}$ F will set $f_{Z2} = f_{P1}$, canceling out the power pole and insuring a −20dB/decade slope in the low frequency magnitude response. In other words, the phase margin below the crossover frequency will always be higher than the phase margin at the crossover frequency.

If better transient response times are desired, a second method is to set f_{Z2} between f_{P1} and ½ decade before f_C, the target crossover frequency. This trades more low frequency gain for less phase margin, which translates to faster but more oscillatory step responses. We pick C_{C1} = 47nF.

If the esr zero of the output capacitor (f_{ESR}) is too low or if more phase margin is required, additional components may be added to increase the flexibility of the compensator.

Use C_{C2} if $f_{ESR} < ½\ f_S$, that is if:

$$\frac{1}{2\pi C_{OUT} R_{ESR}} < 250kHz \quad (59)$$

For this example, f_{ESR} = 159 kHz, so use C_{C2}.

$$C_{C2} = \frac{50 \times 10^3 + 900}{2\pi\ (.159 \times 10^3)\ (50 \times 10^3)\ (900)}$$

$$= 1.1\ nF \quad (60)$$

The equations used here for R_C, C_{C1}, and C_{C2} are approximations valid when $C_{C2} << C_{C1}$. For exact equations, see PLOTTING THE OPEN LOOP RESPONSE. In some cases, the desired inductance is several times higher than the optimal inductance set by the internal slope compensation. This results in a Q lower than 0.15, in which case additional methods of compensating are presented (see SAMPLING POLE QUALITY FACTOR).

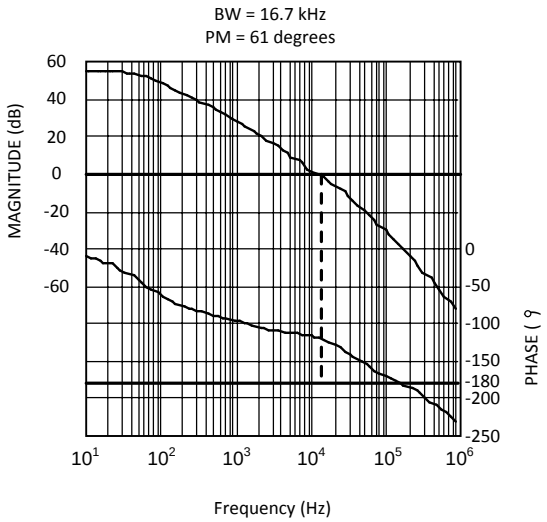
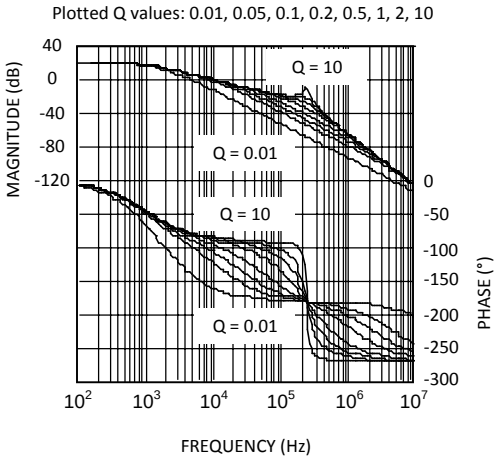


Figure 34. Open Loop Frequency Response for LM3477 Compensation Design Example

SAMPLING POLE QUALITY FACTOR

In a current mode control architecture, there is an inherent resonace at half the switching frequency. The LM3477/A internally compensates for this by adding a negative slope to the PWM control waveform (see DEFAULT/ADJUSTABLE SLOPE COMPENSATION). The factor in the power stage equations above, Q, describes how much resonance will be observed. Q is a function of duty cycle and m_c. Figure 35 shows how the power stage bode plot is affected as Q is varied from 0.01 to 10. The resonance is caused by two complex poles at half the switching frequency. If m_c is too low, the resonant peaking could become severe coinciding with subharmonic oscillations in the inductor current. If m_c is too high, the two complex poles split and the converter begins to act like a voltage mode converter and the compensation scheme used above should be changed.



The Quality Factor Q of the Two Complex Poles is used to qualify how much resonant peaking is observed in the Power Stage Bode Plot

Figure 35.

If Q>2, the sampling poles are imaginary and are approaching the right half of the imaginary plane (the system is becoming unstable). In this case, Q must be decreased by either increasing the inductance, or more preferably, adding more slope compensation through the R_{SL} resistor (see DEFAULT/ADJUSTABLE SLOPE COMPENSATION).

If Q<0.15, it means that one of the sampling poles is decreasing in frequency towards the dominant power pole, f_{p1}. There are three ways to compensate for this. Decrease the crossover frequency, add a phase lead network, or use the output capacitor's ESR to cancel out the low frequency sampling pole.

One option is to decrease the crossover frequency so that the phase margin is not as severely decreased by the sampling pole. Decreasing the crossover frequency to between 1kHz to 10kHz is advisable here. As a result, there will be a decrease in transient response performance.

Another option is the use of the feed-forward capacitor, Cff. This will provide a positive phase shift (lead) which can be used to increase phase margin. However, it is important to note that the effectiveness of Cff decreases with output voltage. This is due to the fact that the frequencies of the zero f_{zff} and pole f_{pff} get closer together as the output voltage is reduced.

The frequency of the feed-forward zero and pole are:

$$f_{zff} = \frac{1}{2\pi R_{FB1} C_{ff}} (Hz) \quad (61)$$

$$f_{pff} = \frac{1}{2\pi R_{FB1} C_{ff}} \frac{R_{FB1} + R_{FB2}}{R_{FB2}} = f_{zff} \frac{V_{OUT}}{V_{FB}} (Hz) \quad (62)$$

A third option is to strategically place the ESR zero f_{ESR} of the output capacitor to cancel out the sampling pole. In this case, the capacitor C_{C2} will not be used to cancel out f_{ESR}. f_{ESR} should be placed around the crossover frequency f_c, but this will depend on how low Q is.

REVISION HISTORY

Changes from Revision J (March 2013) to Revision K	Page
• Changed layout of National Data Sheet to TI format	27

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3477AMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S13A	Samples
LM3477AMMX	NRND	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 125	S13A	
LM3477AMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S13A	Samples
LM3477MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	S13B	
LM3477MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S13B	Samples
LM3477MMX	NRND	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 125	S13B	
LM3477MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S13B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

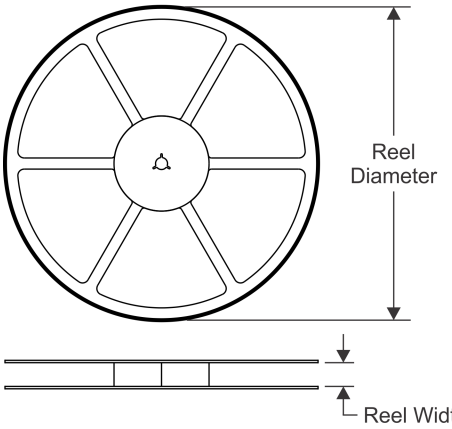
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

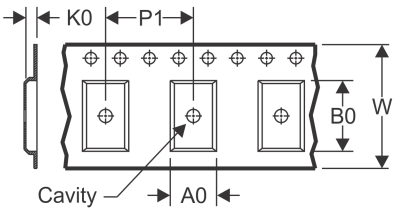
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

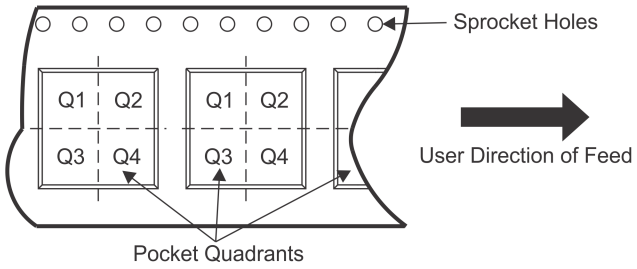


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

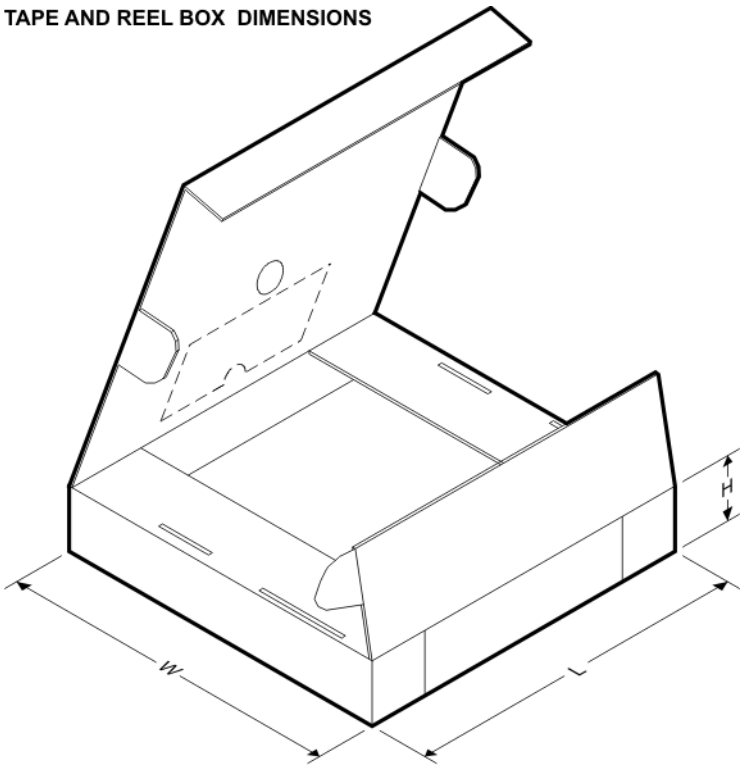
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3477AMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3477AMMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3477AMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3477MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3477MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3477MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3477MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

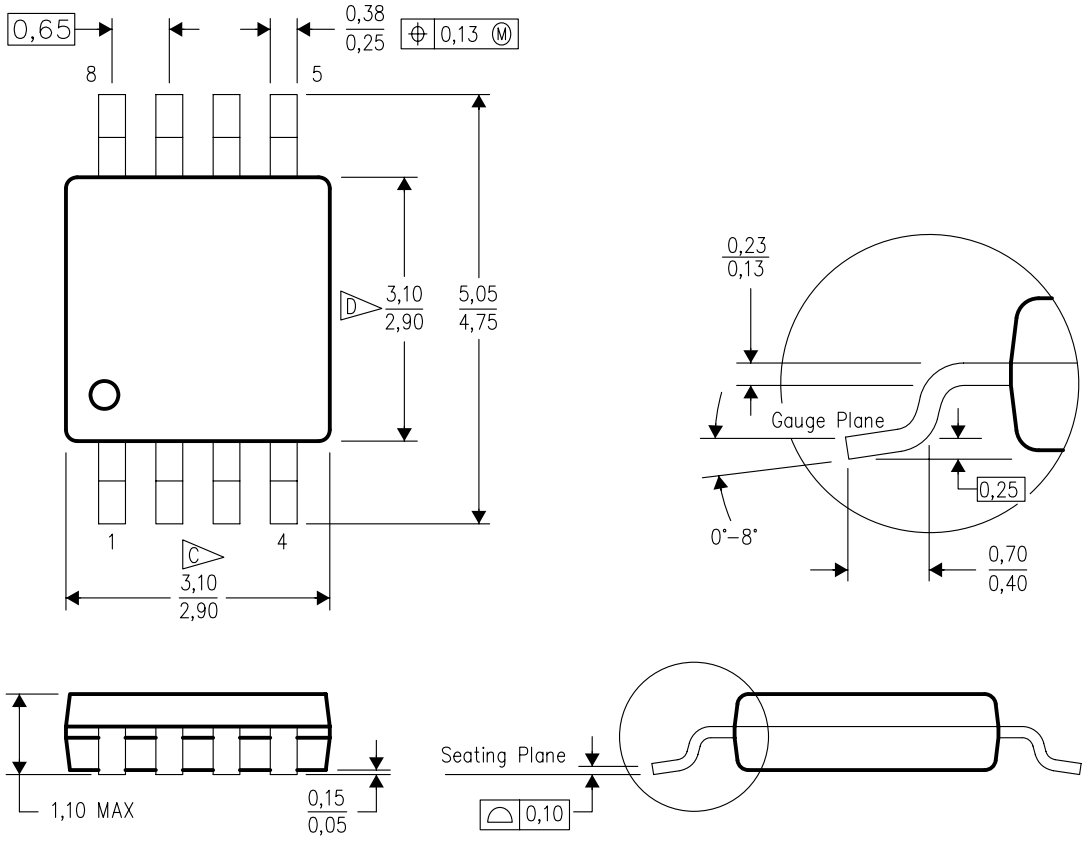
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3477AMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM3477AMMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM3477AMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM3477MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM3477MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM3477MMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM3477MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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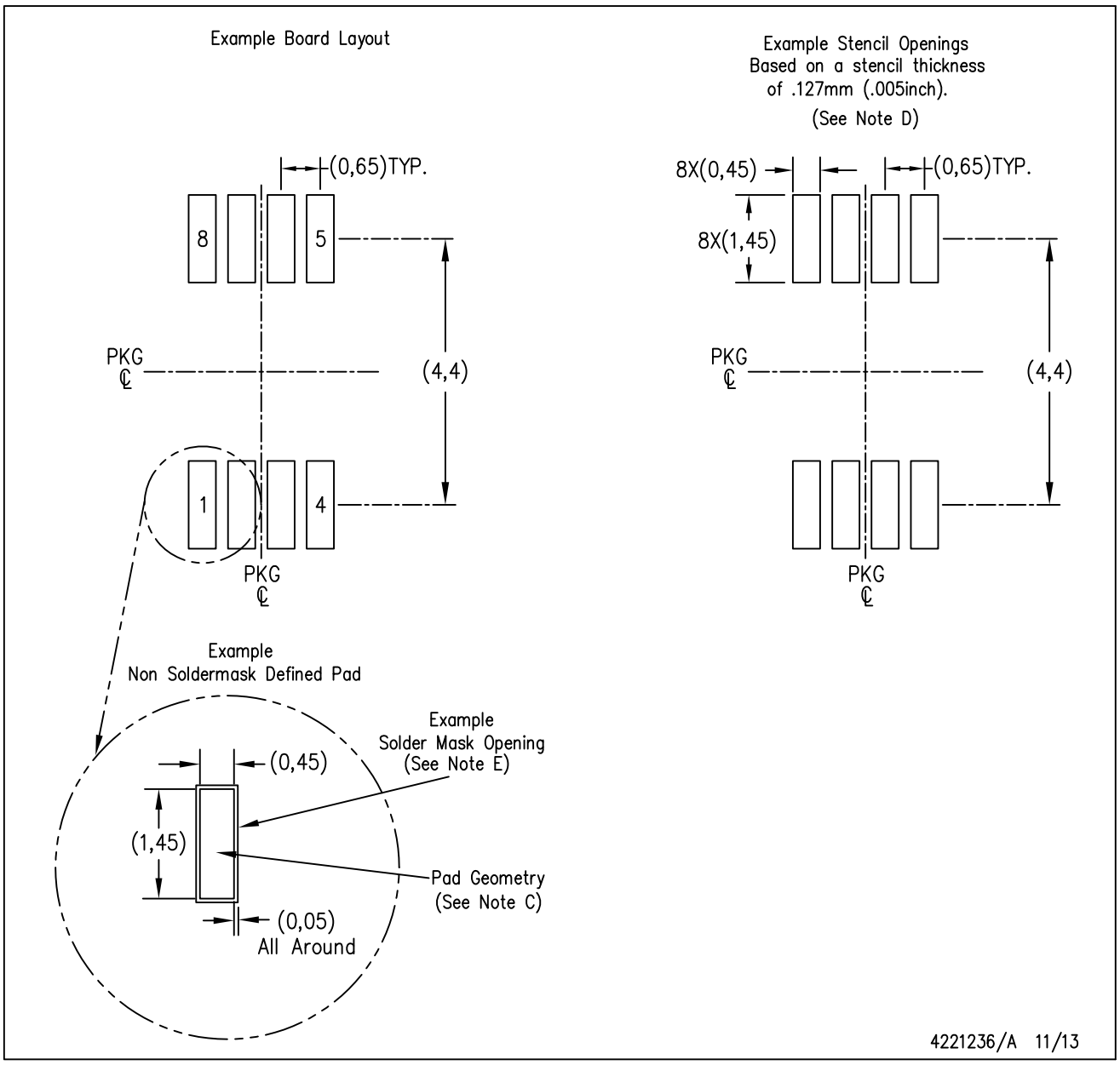
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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