FAIRCHILD SEMICONDUCTOR®

January 2010

FDC655BN

Single N-Channel, Logic Level, PowerTrench® MOSFET

30 V, 6.3 A, 25 mΩ

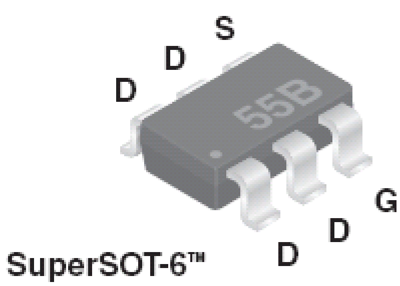
Features

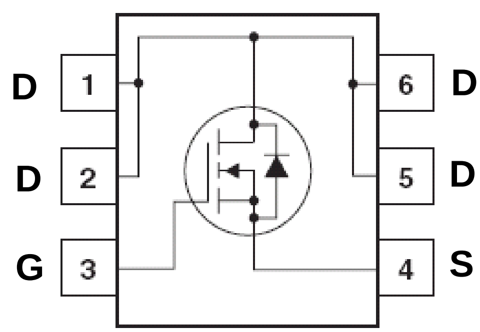
- Max $r_{DS(on)}$ = 25 mΩ at V_{GS} = 10 V, I_D = 6.3 A
- Max $r_{DS(on)}$ = 33 mΩ at V_{GS} = 4.5 V, I_D = 5.5 A
- Fast switching
- Low gate charge
- High performance trchnology for extremely low $r_{DS(on)}$
- Termination is Lead-free and RoHS Compliant

General Description

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applicatoins where low in-line power loss and fast switching are required.





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	-Continuous T_A = 25°C (Note 1a)	6.3	A
	-Pulsed	20	
P_D	Power Dissipation (Note 1a)	1.6	W
	Power Dissipation (Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to + 150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.55B	FDC655BN	SSOT-6™	7 ”	8 mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0 V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25°C		25		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25°C		-5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 6.3 A		21	25	mΩ
		V_{GS} = 4.5 V, I_D = 5.5 A		26	33	
		V_{GS} = 10 V, I_D = 6.3 A, T_J = 125°C		30	36	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 6.3 A		35		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1MHz		470	620	pF
C_{oss}	Output Capacitance			100	130	pF
C_{rss}	Reverse Transfer Capacitance			60	90	pF
R_g	Gate Resistance			3.0		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		6	11	ns
t_r	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			15	26	ns
t_f	Fall Time			2	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 15 V, I_D = 6.3 A		9	13	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 5 V; V_{DD} = 15 V, I_D = 6.3 A		5	7	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 15 V, I_D = 6.3 A		1.4		nC
Q_{gd}	Gate to Drain “Miller” Charge			1.6		nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain-Source Diode Forward Current				1.3	A
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 6.3 A, di/dt = 100 A/µs		15	26	ns
Q_{rr}	Reverse Recovery Charge			4	10	nC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a. 78 °C/W when mounted on a 1 in^2 pad of 2 oz copper on FR-4 board.
b. 156 °C/W when mounted on a minimum pad.

2: Pulse Test: Pulse Width<300 us, Duty Cycle<2.0%.

Typical Characteristics T_J = 25°C unless otherwise noted

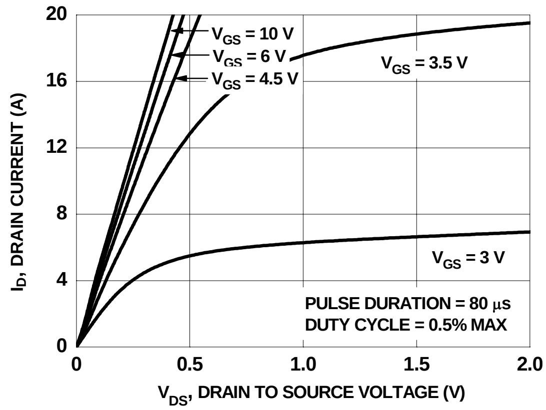


Figure 1. On Region Characteristics

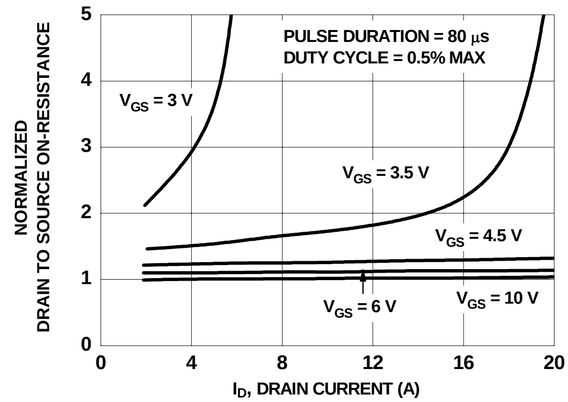


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

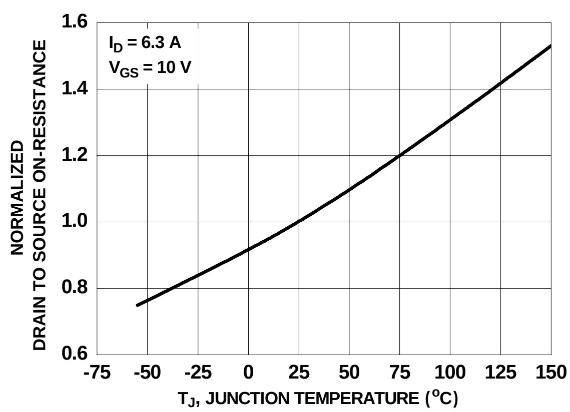


Figure 3. Normalized On Resistance vs Junction Temperature

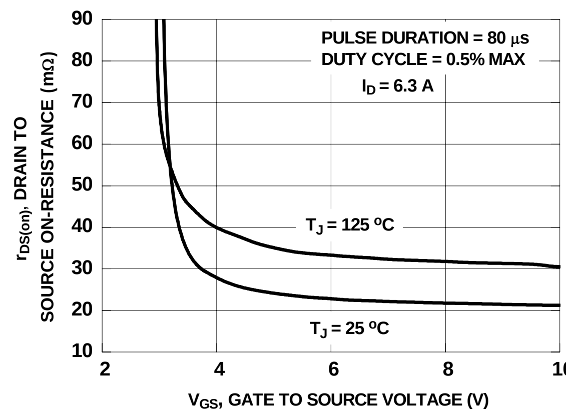


Figure 4. On-Resistance vs Gate to Source Voltage

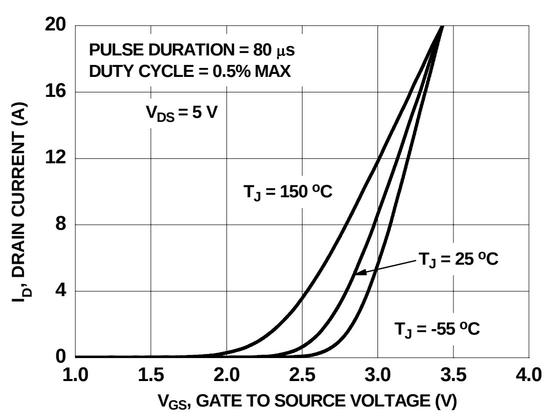


Figure 5. Transfer Characteristics

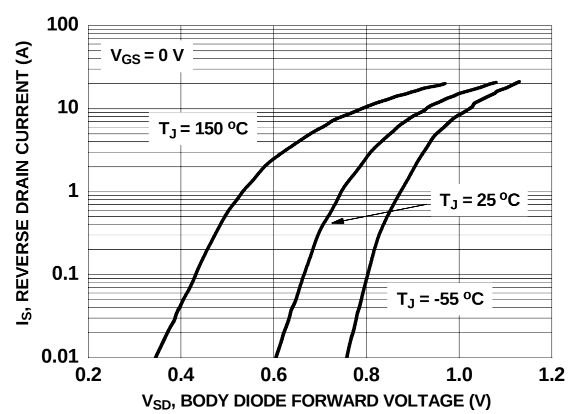


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

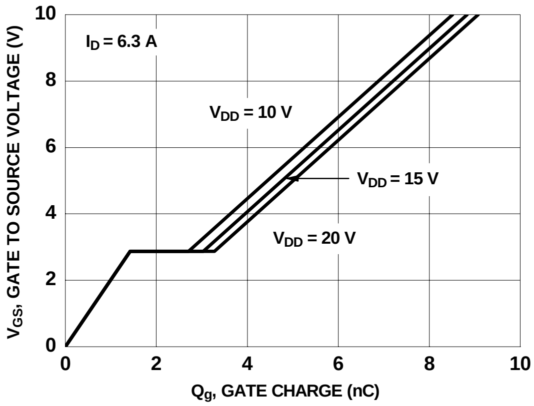


Figure 7. Gate Charge Characteristics

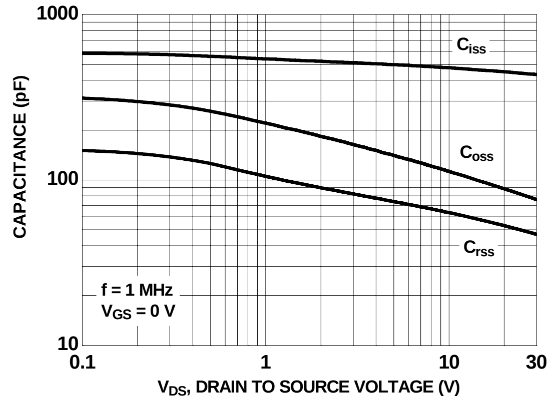


Figure 8. Capacitance vs Drain to Source Voltage

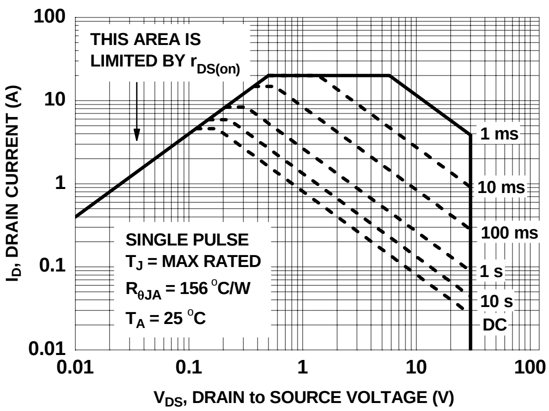


Figure 9. Forward Bias Safe Operating Area

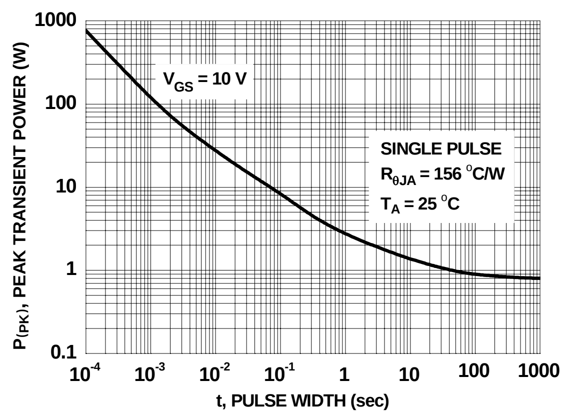


Figure 10. Single Pulse Maximum Power Dissipation

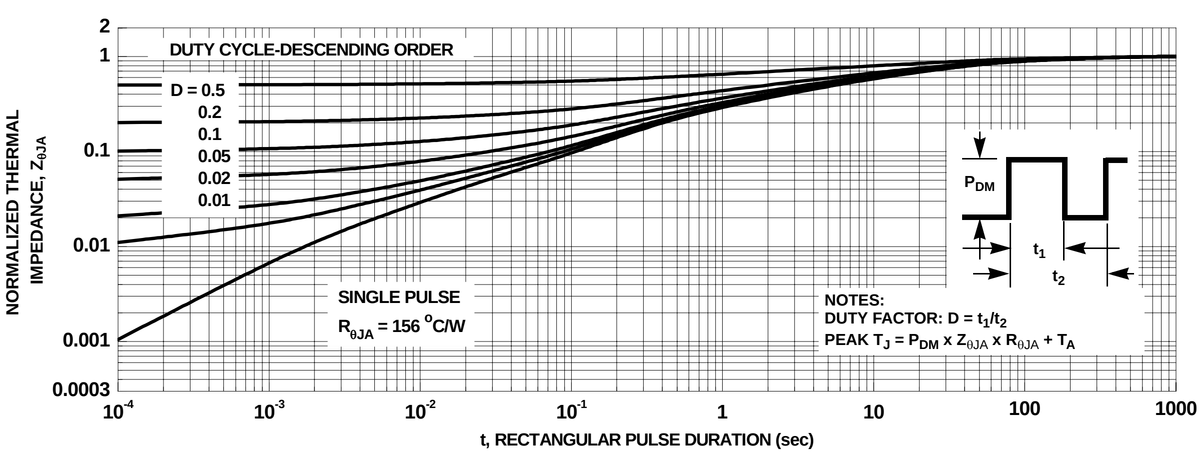


Figure 11. Junction-to-Ambient Transient Thermal Response Curve

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