NUD3124, SZNUD3124

Automotive Inductive Load Driver

This micro−integrated part provides a single component solution to switch inductive loads such as relays, solenoids, and small DC motors without the need of a free−wheeling diode. It accepts logic level inputs, thus allowing it to be driven by a large variety of devices including logic gates, inverters, and microcontrollers.

Features

- Provides Robust Interface between D.C. Relay Coils and Sensitive Logic
- Capable of Driving Relay Coils Rated up to 150 mA at 12 Volts
- Replaces 3 or 4 Discrete Components for Lower Cost
- Internal Zener Eliminates Need for Free−Wheeling Diode
- Meets Load Dump and other Automotive Specs
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These are Pb−Free Devices

Typical Applications

- Automotive and Industrial Environment
- Drives Window, Latch, Door, and Antenna Relays

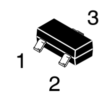
Benefits

- Reduced PCB Space
- Standardized Driver for Wide Range of Relays
- Simplifies Circuit Design and PCB Layout
- Compliance with Automotive Specifications

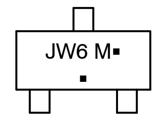
ON Semiconductor®

http://onsemi.com

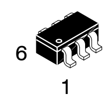
MARKING DIAGRAMS



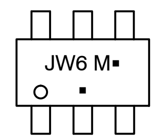
SOT−23
CASE 318
STYLE 21



JW6 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)



SC−74
CASE 318F
STYLE 7



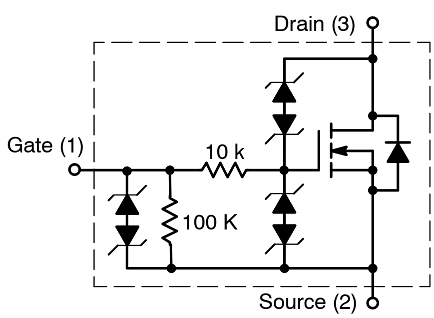
JW6 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

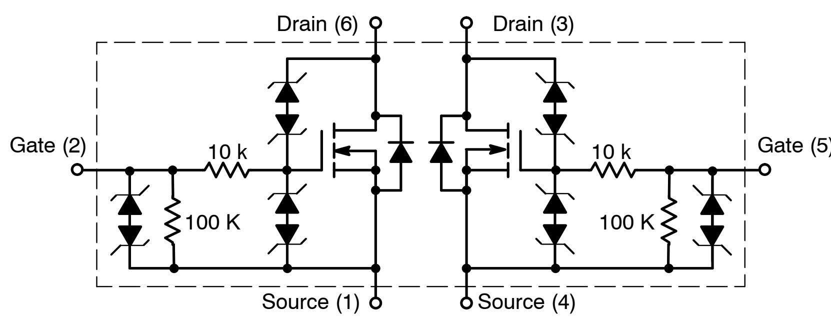
Device	Package	Shipping†
NUD3124LT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel
SZNUD3124LT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel
NUD3124DMT1G	SC−74 (Pb−Free)	3000 / Tape & Reel
SZNUD3124DMT1G	SC−74 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

INTERNAL CIRCUIT DIAGRAMS



CASE 318



CASE 318F

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MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Symbol	Rating	Value	Unit
V_{DSS}	Drain−to−Source Voltage – Continuous (T_J = 125°C)	28	V
V_{GSS}	Gate−to−Source Voltage – Continuous (T_J = 125°C)	12	V
I_D	Drain Current – Continuous (T_J = 125°C)	150	mA
E_Z	Single Pulse Drain−to−Source Avalanche Energy (For Relay's Coils/Inductive Loads of 80 Ω or Higher) (T_J Initial = 85°C)	250	mJ
P_{PK}	Peak Power Dissipation, Drain−to−Source (Notes 1 and 2) (T_J Initial = 85°C)	20	W
E_{LD1}	Load Dump Suppressed Pulse, Drain−to−Source (Notes 3 and 4) (Suppressed Waveform: V_s = 45 V, R_{SOURCE} = 0.5 Ω, T = 200 ms) (For Relay's Coils/Inductive Loads of 80 Ω or Higher) (T_J Initial = 85°C)	80	V
E_{LD2}	Inductive Switching Transient 1, Drain−to−Source (Waveform: R_{SOURCE} = 10 Ω, T = 2.0 ms) (For Relay's Coils/Inductive Loads of 80 Ω or Higher) (T_J Initial = 85°C)	100	V
E_{LD3}	Inductive Switching Transient 2, Drain−to−Source (Waveform: R_{SOURCE} = 4.0 Ω, T = 50 μs) (For Relay's Coils/Inductive Loads of 80 Ω or Higher) (T_J Initial = 85°C)	300	V
Rev−Bat	Reverse Battery, 10 Minutes (Drain−to−Source) (For Relay's Coils/Inductive Loads of 80 Ω or more)	−14	V
Dual−Volt	Dual Voltage Jump Start, 10 Minutes (Drain−to−Source)	28	V
ESD	Human Body Model (HBM) According to EIA/JESD22/A114 Specification	2,000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Nonrepetitive current square pulse 1.0 ms duration.
2. For different square pulse durations, see Figure 2.
3. Nonrepetitive load dump suppressed pulse per Figure 3.
4. For relay's coils/inductive loads higher than 80 Ω, see Figure 4.

THERMAL CHARACTERISTICS

Symbol	Rating		Value	Unit
T_A	Operating Ambient Temperature		−40 to 125	°C
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		−65 to 150	°C
P_D	Total Power Dissipation (Note 5) Derating above 25°C	SOT−23	225 1.8	mW mW/°C
P_D	Total Power Dissipation (Note 5) Derating above 25°C	SC−74	380 3.0	mW mW/°C
$R_{\theta JA}$	Thermal Resistance Junction−to−Ambient (Note 5)	SOT−23 SC−74	556 329	°C/W

5. Mounted onto minimum pad board.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain to Source Sustaining Voltage (I_D = 10 mA)	V_{BRDSS}	28	34	38	V
Drain to Source Leakage Current (V_{DS} = 12 V, V_{GS} = 0 V) (V_{DS} = 12 V, V_{GS} = 0 V, T_J = 125°C) (V_{DS} = 28 V, V_{GS} = 0 V) (V_{DS} = 28 V, V_{GS} = 0 V, T_J = 125°C)	I_{DSS}	 – – – –	 – – – –	 0.5 1.0 50 80	μA
Gate Body Leakage Current (V_{GS} = 3.0 V, V_{DS} = 0 V) (V_{GS} = 3.0 V, V_{DS} = 0 V, T_J = 125°C) (V_{GS} = 5.0 V, V_{DS} = 0 V) (V_{GS} = 5.0 V, V_{DS} = 0 V, T_J = 125°C)	I_{GSS}	 – – – –	 – – – –	 60 80 90 110	μA
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{GS} = V_{DS}, I_D = 1.0 mA) (V_{GS} = V_{DS}, I_D = 1.0 mA, T_J = 125°C)	$V_{GS(th)}$	 1.3 1.3	 1.8 –	 2.0 2.0	V
Drain to Source On−Resistance (I_D = 150 mA, V_{GS} = 3.0 V) (I_D = 150 mA, V_{GS} = 3.0 V, T_J = 125°C) (I_D = 150 mA, V_{GS} = 5.0 V) (I_D = 150 mA, V_{GS} = 5.0 V, T_J = 125°C)	$R_{DS(on)}$	 – – – –	 – – – –	 1.4 1.7 0.8 1.1	Ω
Output Continuous Current (V_{DS} = 0.25 V, V_{GS} = 3.0 V) (V_{DS} = 0.25 V, V_{GS} = 3.0 V, T_J = 125°C)	$I_{DS(on)}$	 150 140	 200 –	 – –	mA
Forward Transconductance (V_{DS} = 12 V, I_D = 150 mA)	g_{FS}	–	500	–	mmho
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 12 V, V_{GS} = 0 V, f = 10 kHz)	Ciss	–	32	–	pf
Output Capacitance (V_{DS} = 12 V, V_{GS} = 0 V, f = 10 kHz)	Coss	–	21	–	pf
Transfer Capacitance (V_{DS} = 12 V, V_{GS} = 0 V, f = 10 kHz)	Crss	–	8.0	–	pf
SWITCHING CHARACTERISTICS					
Propagation Delay Times: High to Low Propagation Delay; Figure 1, (V_{DS} = 12 V, V_{GS} = 3.0 V) Low to High Propagation Delay; Figure 1, (V_{DS} = 12 V, V_{GS} = 3.0 V) High to Low Propagation Delay; Figure 1, (V_{DS} = 12 V, V_{GS} = 5.0 V) Low to High Propagation Delay; Figure 1, (V_{DS} = 12 V, V_{GS} = 5.0 V)	 t_{PHL} t_{PLH} t_{PHL} t_{PLH}	 – – – –	 890 912 324 1280	 – – – –	ns
Transition Times: Fall Time; Figure 1, (V_{DS} = 12 V, V_{GS} = 3.0 V) Rise Time; Figure 1, (V_{DS} = 12 V, V_{GS} = 3.0 V) Fall Time; Figure 1, (V_{DS} = 12 V, V_{GS} = 5.0 V) Rise Time; Figure 1, (V_{DS} = 12 V, V_{GS} = 5.0 V)	 t_f t_r t_f t_r	 – – – –	 2086 708 556 725	 – – – –	ns

TYPICAL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)

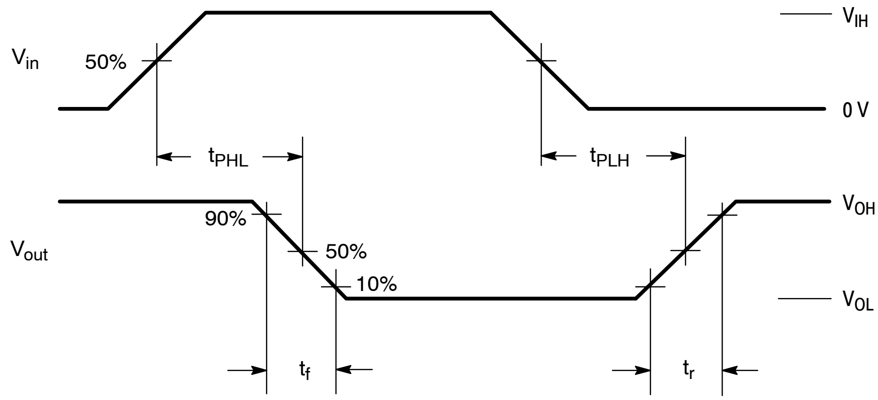


Figure 1. Switching Waveforms

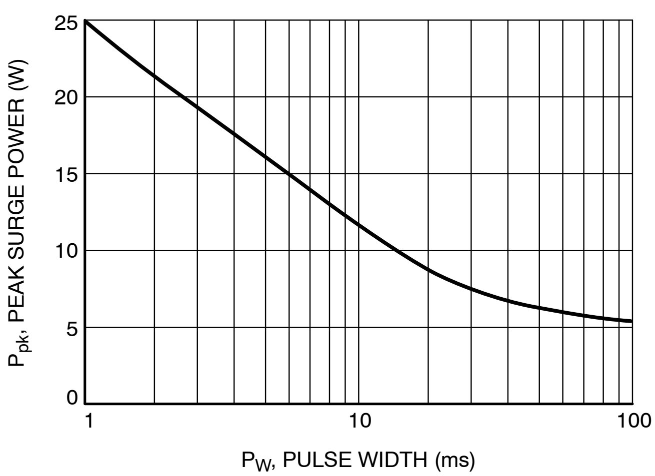


Figure 2. Maximum Non−repetitive Surge Power versus Pulse Width

Load Dump Pulse Not Suppressed:

V_R = 13.5 V Nominal ±10%
V_S = 60 V Nominal ±10%
T = 300 ms Nominal ±10%
T_R = 1 − 10 ms ±10%

Load Dump Pulse Suppressed:

NOTE: Max. Voltage DUT is exposed to is approximately 45 V.
V_S = 30 V ±20%
T = 150 ms ±20%

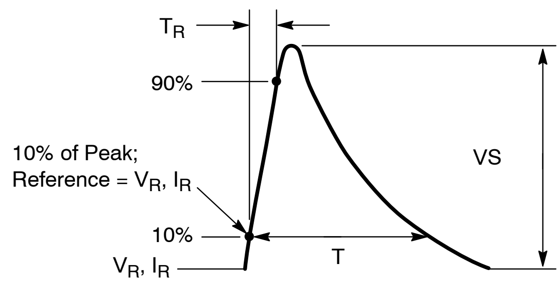


Figure 3. Load Dump Waveform Definition

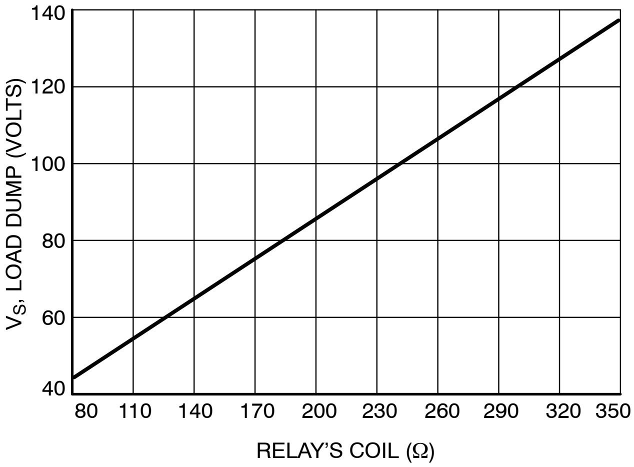


Figure 4. Load Dump Capability versus Relay's Coil dc Resistance

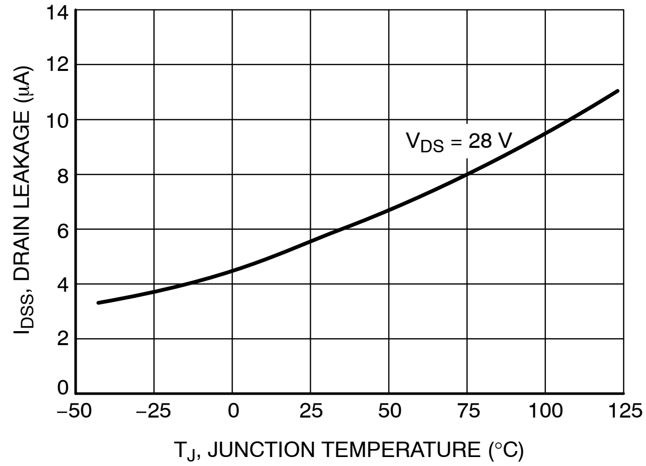


Figure 5. Drain−to−Source Leakage versus Junction Temperature

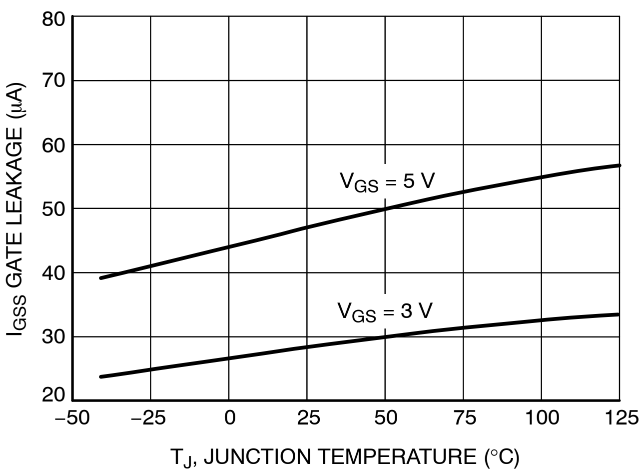


Figure 6. Gate−to−Source Leakage versus Junction Temperature

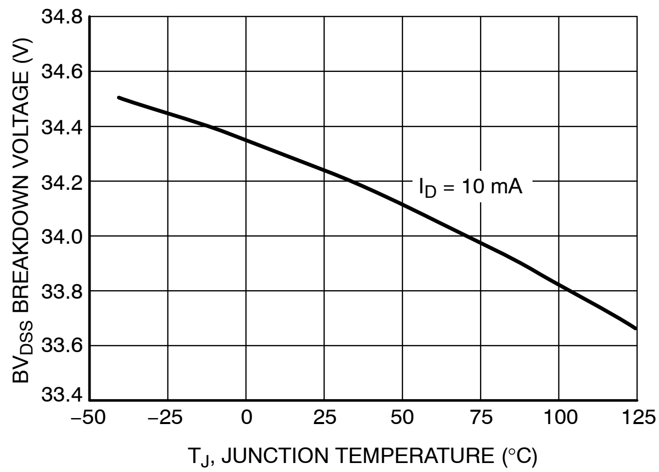


Figure 7. Breakdown Voltage versus Junction Temperature

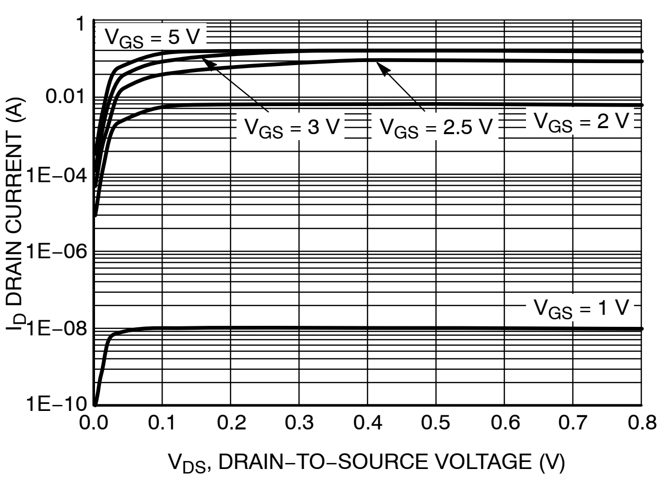


Figure 8. Output Characteristics

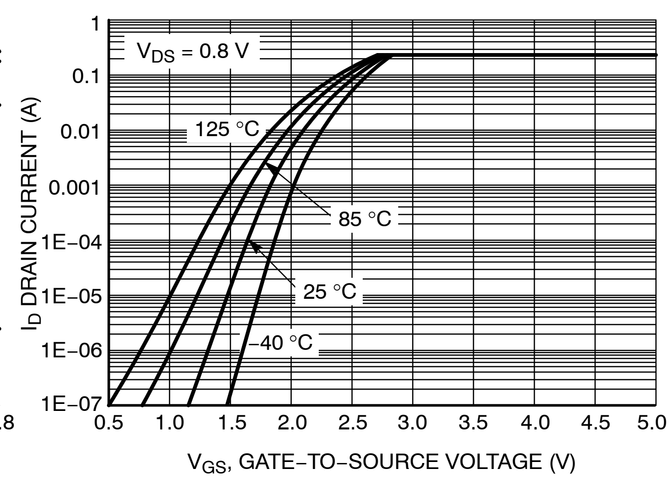


Figure 9. Transfer Function

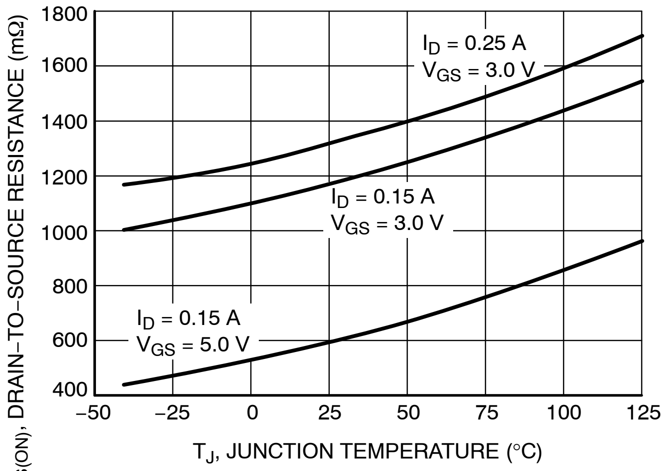


Figure 10. On Resistance Variation versus Junction Temperature

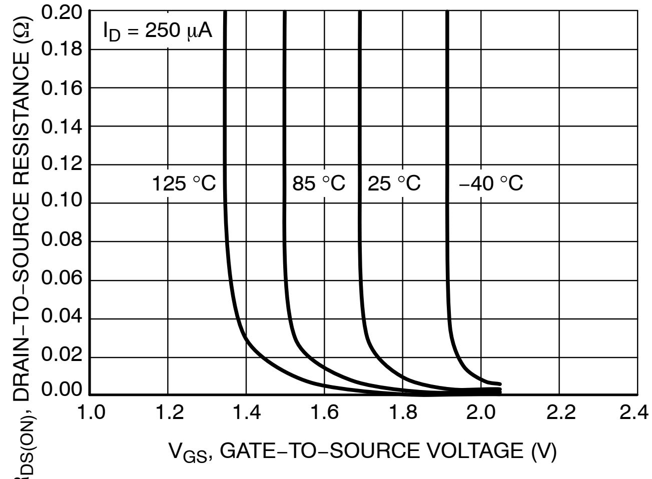


Figure 11. On Resistance Variation versus Gate−to−Source Voltage

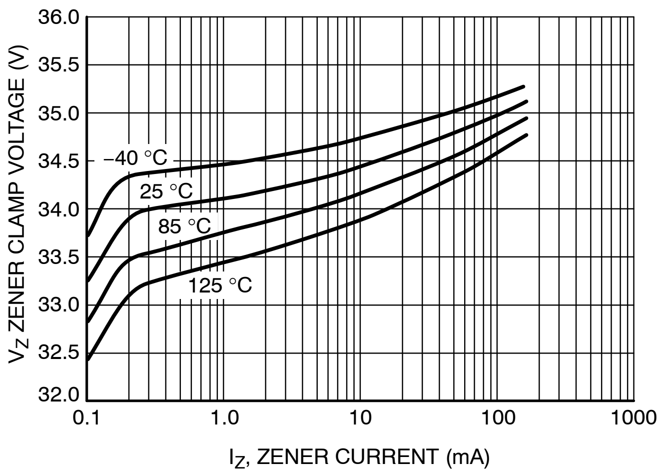


Figure 12. Zener Clamp Voltage versus Zener Current

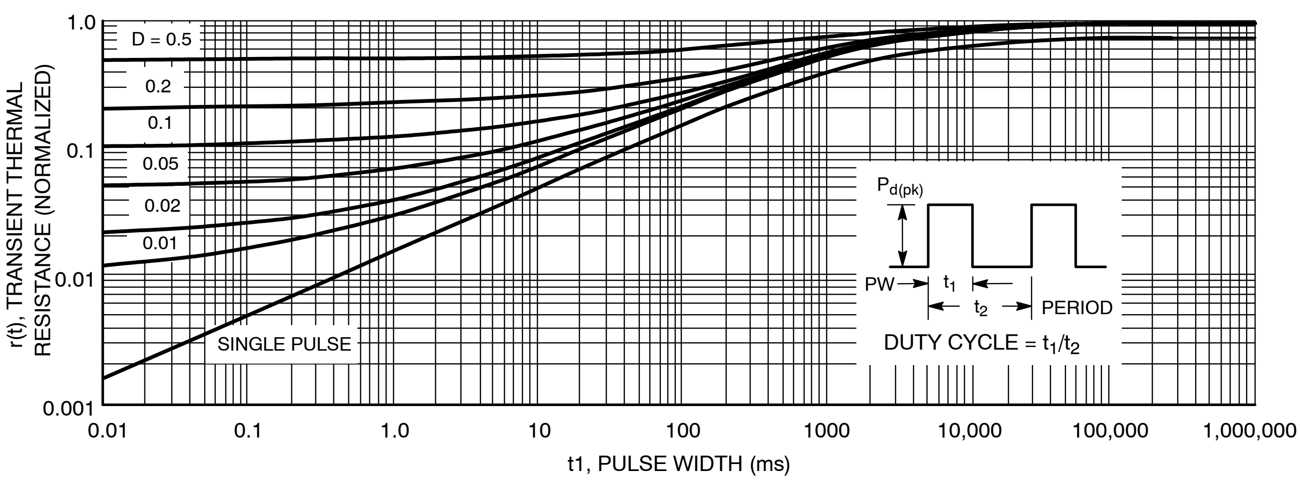


Figure 13. Transient Thermal Response for NUD3124LT1G

APPLICATIONS INFORMATION

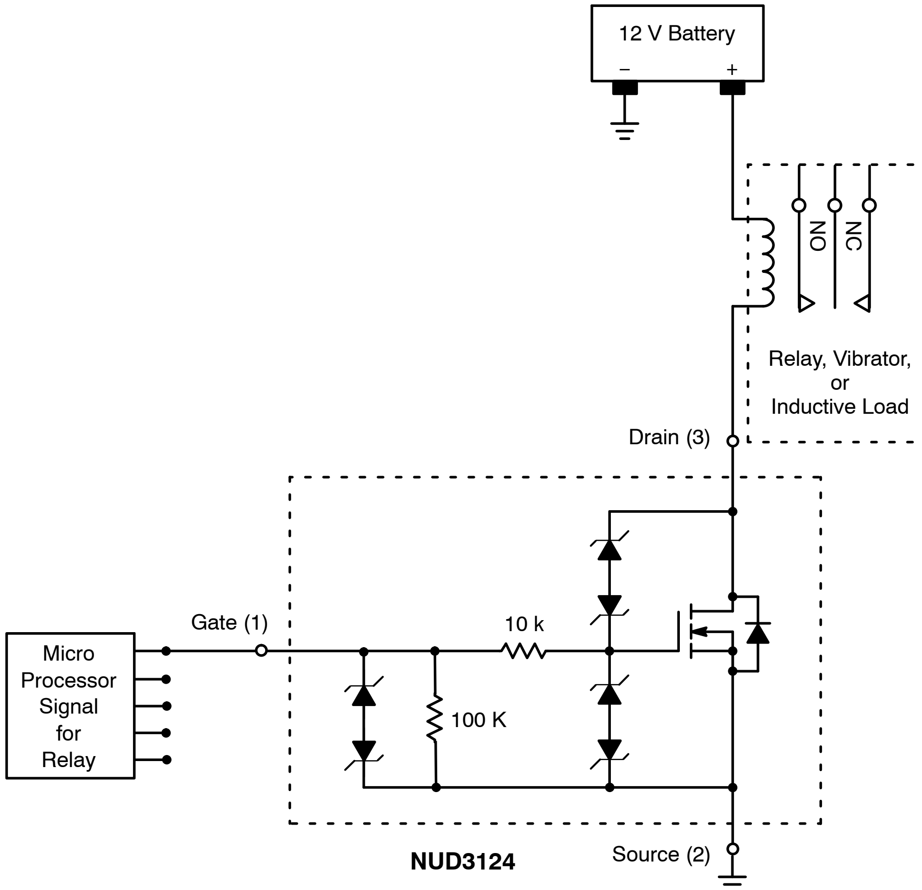
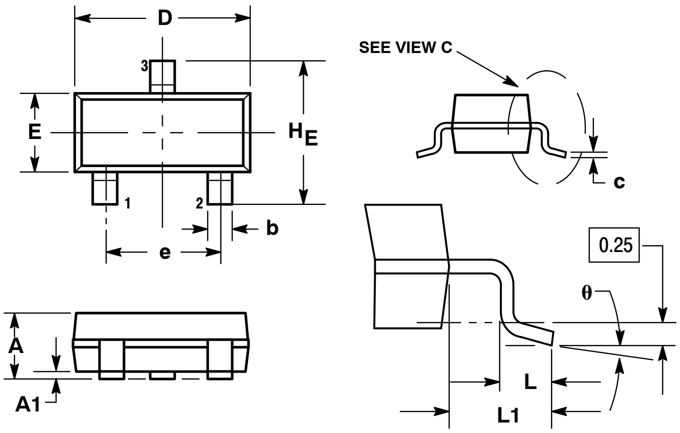


Figure 14. Applications Diagram

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AP



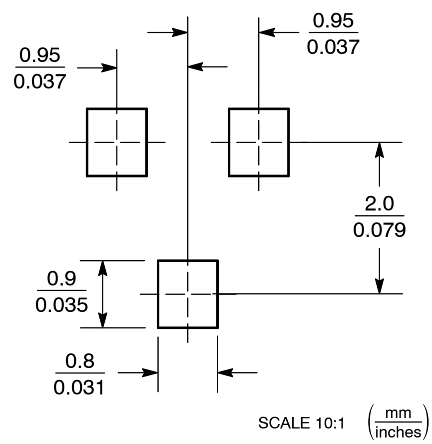
VIEW C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	−−−	10°	0°	−−−	10°

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

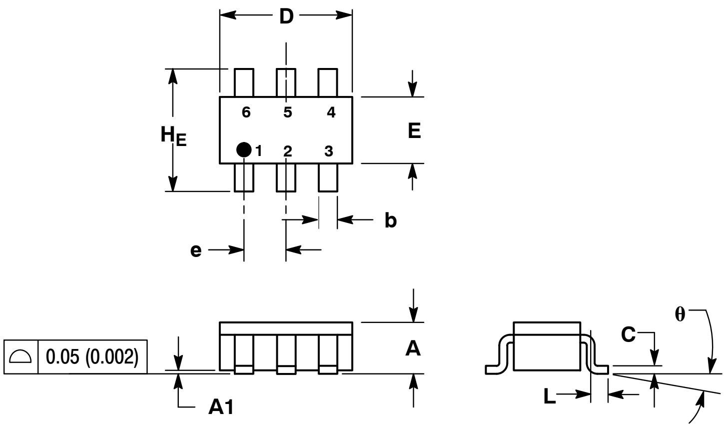
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SC−74
CASE 318F−05
ISSUE M

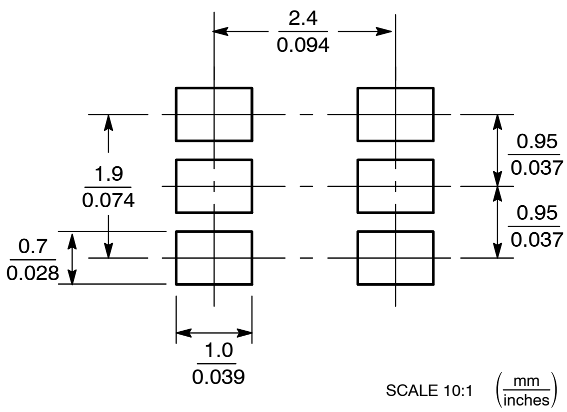


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01, −02, −03, −04 OBSOLETE. NEW STANDARD 318F−05.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	–	10°	0°	–	10°

STYLE 7:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

SOLDERING FOOTPRINT*



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