

### FEATURES

- 4.7  $\Omega$  maximum on resistance @ 25°C
- 0.5  $\Omega$  on resistance flatness
- Fully specified at  $\pm 15$  V/ $+12$  V/ $\pm 5$  V
- 3 V logic-compatible inputs
- Up to 115 mA continuous current per channel
- Rail-to-rail operation
- Break-before-make switching action
- 16-/20-lead TSSOP and 4 mm  $\times$  4 mm LFCSP\_VQ packages

### APPLICATIONS

- Relay replacement
- Audio and video routing
- Automatic test equipment
- Data acquisition systems
- Temperature measurement systems
- Avionics
- Battery-powered systems
- Communication systems
- Medical equipment

### GENERAL DESCRIPTION

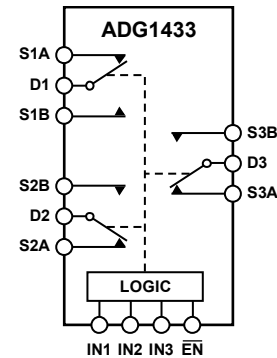
The ADG1433 and ADG1434 are monolithic industrial CMOS (*i*CMOS®) analog switches comprising three independently selectable single-pole, double-throw (SPDT) switches and four independently selectable SPDT switches, respectively.

All channels exhibit break-before-make switching action that prevents momentary shorting when switching channels. An  $\overline{EN}$  input on the ADG1433 (LFCSP and TSSOP packages) and ADG1434 (LFCSP package only) is used to enable or disable the device. When disabled, all channels are switched off.

The *i*CMOS modular manufacturing process combines high voltage, complementary metal-oxide semiconductor (CMOS), and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage parts has been able to achieve. Unlike analog ICs using a conventional CMOS process, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

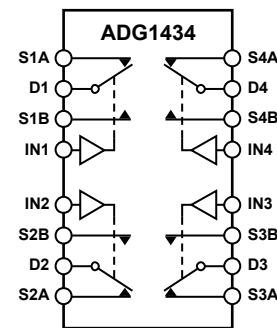
The ultralow on resistance and on resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications, where low distortion is critical. *i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

### FUNCTIONAL BLOCK DIAGRAMS



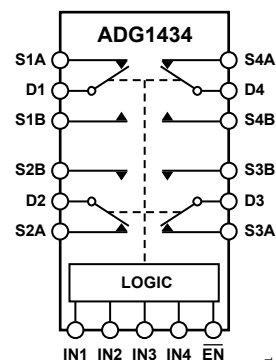
SWITCHES SHOWN FOR  
A 1 INPUT LOGIC.

Figure 1. ADG1433 TSSOP and LFCSP\_VQ



SWITCHES SHOWN FOR  
A 1 INPUT LOGIC.

Figure 2. ADG1434 TSSOP



SWITCHES SHOWN FOR  
A 1 INPUT LOGIC.

Figure 3. ADG1434 LFCSP\_VQ

### Rev. C

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## REVISION HISTORY

### 6/09—Rev. B to Rev. C

|                                  |    |
|----------------------------------|----|
| Updated Outline Dimensions ..... | 16 |
| Changes to Ordering Guide .....  | 17 |

### 3/09—Rev. A to Rev. B

|                                             |    |
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| Change to $I_{DD}$ Parameter, Table 1 ..... | 4  |
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| Updated Outline Dimensions, Figure 39 ..... | 17 |

### 6/08—Rev. 0 to Rev. A

|                                                               |    |
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| Added Continuous Current per Channel Parameter, Table 1 ..... | 4  |
| Added Continuous Current per Channel Parameter, Table 2 ..... | 5  |
| Added Continuous Current per Channel Parameter, Table 3 ..... | 6  |
| Changes to Table 4 .....                                      | 7  |
| Changes to Figure 30 .....                                    | 13 |
| Updated Outline Dimensions .....                              | 16 |
| Changes to Ordering Guide .....                               | 17 |

### 10/06—Revision 0: Initial Version

# SPECIFICATIONS

## ±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ , GND = 0 V, unless otherwise noted.

Table 1.

| Parameter                                             | +25°C       | –40°C to +85°C | –40°C to +125°C <sup>1</sup> | Unit              | Test Conditions/Comments                                                      |
|-------------------------------------------------------|-------------|----------------|------------------------------|-------------------|-------------------------------------------------------------------------------|
| <b>ANALOG SWITCH</b>                                  |             |                |                              |                   |                                                                               |
| Analog Signal Range                                   |             |                | $V_{SS}$ to $V_{DD}$         | V                 | $V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 25               |
| On Resistance, $R_{ON}$                               | 4           |                |                              | $\Omega$ typ      |                                                                               |
|                                                       | 4.7         | 5.7            | 6.7                          | $\Omega$ max      | $V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$                         |
| On Resistance Match Between Channels, $\Delta R_{ON}$ | 0.5         |                |                              | $\Omega$ typ      | $V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$                               |
|                                                       | 0.78        | 0.85           | 1.1                          | $\Omega$ max      |                                                                               |
| On Resistance Flatness, $R_{FLAT(ON)}$                | 0.5         |                |                              | $\Omega$ typ      | $V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$                               |
|                                                       | 0.72        | 0.77           | 0.92                         | $\Omega$ max      |                                                                               |
| <b>LEAKAGE CURRENTS</b>                               |             |                |                              |                   |                                                                               |
| Source Off Leakage, $I_S$ (Off)                       | $\pm 0.04$  |                |                              | nA typ            | $V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$                         |
|                                                       | $\pm 0.3$   | $\pm 0.6$      | $\pm 3$                      | nA max            | $V_D = \pm 10\text{ V}$ , $V_S = \pm 10\text{ V}$ ; see Figure 26             |
| Drain Off Leakage, $I_D$ (Off)                        | $\pm 0.04$  |                |                              | nA typ            | $V_D = \pm 10\text{ V}$ , $V_S = \pm 10\text{ V}$ ; see Figure 26             |
|                                                       | $\pm 0.3$   | $\pm 0.6$      | $\pm 3$                      | nA max            |                                                                               |
| Channel On Leakage, $I_D$ , $I_S$ (On)                | $\pm 0.05$  |                |                              | nA typ            | $V_S = V_D = \pm 10\text{ V}$ ; see Figure 27                                 |
|                                                       | $\pm 0.4$   | $\pm 0.8$      | $\pm 8$                      | nA max            |                                                                               |
| <b>DIGITAL INPUTS</b>                                 |             |                |                              |                   |                                                                               |
| Input High Voltage, $V_{IH}$                          |             |                | 2.0                          | V min             | $V_{IN} = V_{GND}$ or $V_{DD}$                                                |
| Input Low Voltage, $V_{IL}$                           |             |                | 0.8                          | V max             |                                                                               |
| Input Current, $I_{IL}$ or $I_{IH}$                   | $\pm 0.005$ |                |                              | $\mu\text{A}$ typ |                                                                               |
|                                                       |             |                | $\pm 0.1$                    | $\mu\text{A}$ max |                                                                               |
| Digital Input Capacitance, $C_{IN}$                   | 3           |                |                              | pF typ            |                                                                               |
| <b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>            |             |                |                              |                   |                                                                               |
| Transition Time, $t_{TRANS}$                          | 140         |                |                              | ns typ            | $R_L = 100\ \Omega$ , $C_L = 35\text{ pF}$                                    |
|                                                       | 170         | 200            | 230                          | ns max            | $V_S = 10\text{ V}$ , see Figure 28                                           |
| Break-Before-Make Time Delay, $t_D$                   | 40          |                |                              | ns typ            | $R_L = 100\ \Omega$ , $C_L = 35\text{ pF}$                                    |
|                                                       |             |                | 30                           | ns min            | $V_{S1} = V_{S2} = 10\text{ V}$ , see Figure 29                               |
| $t_{ON}(\overline{EN})$                               | 140         |                |                              | ns typ            | $R_L = 100\ \Omega$ , $C_L = 35\text{ pF}$                                    |
|                                                       | 170         | 200            | 230                          | ns max            | $V_S = 10\text{ V}$ , see Figure 30                                           |
| $t_{OFF}(\overline{EN})$                              | 60          |                |                              | ns typ            | $R_L = 100\ \Omega$ , $C_L = 35\text{ pF}$                                    |
|                                                       | 75          | 85             | 90                           | ns max            | $V_S = 10\text{ V}$ , see Figure 30                                           |
| Charge Injection                                      | –50         |                |                              | pC typ            | $V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , see Figure 31  |
| Off Isolation                                         | –70         |                |                              | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , see Figure 32 |
| Channel-to-Channel Crosstalk                          | –70         |                |                              | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , see Figure 34 |
| Total Harmonic Distortion, THD + N                    | 0.025       |                |                              | % typ             | $R_L = 110\ \Omega$ , 15 V p-p, $f = 20\text{ Hz}$ to 20 kHz, see Figure 35   |
| –3 dB Bandwidth                                       | 200         |                |                              | MHz typ           | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , see Figure 33                      |
| Insertion Loss                                        | 0.24        |                |                              | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , see Figure 33 |
| $C_S$ (Off)                                           | 12          |                |                              | pF typ            | $f = 1\text{ MHz}$                                                            |
| $C_D$ (Off)                                           | 22          |                |                              | pF typ            | $f = 1\text{ MHz}$                                                            |
| $C_D$ , $C_S$ (On)                                    | 72          |                |                              | pF typ            | $f = 1\text{ MHz}$                                                            |

# ADG1433/ADG1434

| Parameter                                   | +25°C | −40°C to +85°C | −40°C to +125°C <sup>1</sup> | Unit                                   | Test Conditions/Comments                              |
|---------------------------------------------|-------|----------------|------------------------------|----------------------------------------|-------------------------------------------------------|
| POWER REQUIREMENTS                          |       |                |                              |                                        | $V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ |
| $I_{DD}$                                    | 0.001 |                | 1                            | $\mu\text{A typ}$<br>$\mu\text{A max}$ | Digital inputs = 0 V or $V_{DD}$                      |
| $I_{DD}$                                    | 260   |                | 475                          | $\mu\text{A typ}$<br>$\mu\text{A max}$ | Digital inputs = 5 V                                  |
| $I_{SS}$                                    | 0.001 |                | 1                            | $\mu\text{A typ}$<br>$\mu\text{A max}$ | Digital inputs = 0 V, 5 V, or $V_{DD}$                |
| $V_{DD}/V_{SS}$                             |       |                | $\pm 4.5/\pm 16.5$           | V min/max                              | GND = 0 V                                             |
| Continuous Current per Channel <sup>2</sup> |       |                |                              |                                        | $V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$ |
| ADG1433                                     | 115   | 75             | 40                           | mA max                                 |                                                       |
| ADG1434                                     | 100   | 65             | 40                           | mA max                                 |                                                       |

<sup>1</sup> Temperature range for Y version: −40°C to +125°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

**12 V SINGLE SUPPLY**

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 2.**

| Parameter                                             | +25°C       | −40°C to +85°C | −40°C to +125°C <sup>1</sup> | Unit                                   | Test Conditions/Comments                                                        |
|-------------------------------------------------------|-------------|----------------|------------------------------|----------------------------------------|---------------------------------------------------------------------------------|
| <b>ANALOG SWITCH</b>                                  |             |                |                              |                                        |                                                                                 |
| Analog Signal Range                                   |             |                | 0 to $V_{DD}$                | V                                      |                                                                                 |
| On Resistance, $R_{ON}$                               | 6           |                |                              | $\Omega$ typ                           | $V_S = 0\text{ V}$ to $10\text{ V}$ , $I_S = -10\text{ mA}$ , see Figure 25     |
|                                                       | 8           | 9.5            | 11.2                         | $\Omega$ max                           | $V_{DD} = 10.8\text{ V}$ , $V_{SS} = 0\text{ V}$                                |
| On Resistance Match Between Channels, $\Delta R_{ON}$ | 0.55        |                |                              | $\Omega$ typ                           | $V_S = 0\text{ V}$ to $10\text{ V}$ , $I_S = -10\text{ mA}$                     |
|                                                       | 0.82        | 0.85           | 1.1                          | $\Omega$ max                           |                                                                                 |
| On Resistance Flatness, $R_{FLAT(ON)}$                | 1.5         |                |                              | $\Omega$ typ                           | $V_S = 0\text{ V}$ to $10\text{ V}$ , $I_S = -10\text{ mA}$                     |
|                                                       | 2.5         | 2.5            | 2.8                          | $\Omega$ max                           |                                                                                 |
| <b>LEAKAGE CURRENTS</b>                               |             |                |                              |                                        | $V_{DD} = 13.2\text{ V}$                                                        |
| Source Off Leakage, $I_S$ (Off)                       | $\pm 0.04$  |                |                              | nA typ                                 | $V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ , see Figure 26 |
|                                                       | $\pm 0.3$   | $\pm 0.6$      | $\pm 3$                      | nA max                                 |                                                                                 |
| Drain Off Leakage, $I_D$ (Off)                        | $\pm 0.04$  |                |                              | nA typ                                 | $V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ , see Figure 26 |
|                                                       | $\pm 0.3$   | $\pm 0.6$      | $\pm 3$                      | nA max                                 |                                                                                 |
| Channel On Leakage, $I_D$ , $I_S$ (On)                | $\pm 0.06$  |                |                              | nA typ                                 | $V_S = V_D = 1\text{ V}$ or $10\text{ V}$ , see Figure 27                       |
|                                                       | $\pm 0.4$   | $\pm 0.8$      | $\pm 8$                      | nA max                                 |                                                                                 |
| <b>DIGITAL INPUTS</b>                                 |             |                |                              |                                        |                                                                                 |
| Input High Voltage, $V_{IH}$                          |             |                | 2.0                          | V min                                  |                                                                                 |
| Input Low Voltage, $V_{IL}$                           |             |                | 0.8                          | V max                                  |                                                                                 |
| Input Current, $I_{IL}$ or $I_{IH}$                   | $\pm 0.005$ |                | $\pm 0.1$                    | $\mu\text{A}$ typ<br>$\mu\text{A}$ max | $V_{IN} = V_{GND}$ or $V_{DD}$                                                  |
| Digital Input Capacitance, $C_{IN}$                   | 4           |                |                              | pF typ                                 |                                                                                 |
| <b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>            |             |                |                              |                                        |                                                                                 |
| Transition Time, $t_{TRANS}$                          | 200         |                |                              | ns typ                                 | $R_L = 100\ \Omega$ , $C_L = 35\text{ pF}$                                      |
|                                                       | 255         | 310            | 350                          | ns max                                 | $V_S = 8\text{ V}$ , see Figure 28                                              |
| Break-Before-Make Time Delay, $t_D$                   | 80          |                |                              | ns typ                                 | $R_L = 100\ \Omega$ , $C_L = 35\text{ pF}$                                      |
|                                                       |             |                | 55                           | ns min                                 | $V_{S1} = V_{S2} = 8\text{ V}$ , see Figure 29                                  |
| $t_{ON}(\overline{EN})$                               | 210         |                |                              | ns typ                                 | $R_L = 100\ \Omega$ , $C_L = 35\text{ pF}$                                      |
|                                                       | 270         | 320            | 360                          | ns max                                 | $V_S = 8\text{ V}$ , see Figure 30                                              |
| $t_{OFF}(\overline{EN})$                              | 70          |                |                              | ns typ                                 | $R_L = 100\ \Omega$ , $C_L = 35\text{ pF}$                                      |
|                                                       | 86          | 95             | 105                          | ns max                                 | $V_S = 8\text{ V}$ , see Figure 30                                              |
| Charge Injection                                      | -10         |                |                              | pC typ                                 | $V_S = 6\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , see Figure 31    |
| Off Isolation                                         | -70         |                |                              | dB typ                                 | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , see Figure 32   |
| Channel-to-Channel Crosstalk                          | -70         |                |                              | dB typ                                 | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , see Figure 34   |
| -3 dB Bandwidth                                       | 135         |                |                              | MHz typ                                | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , see Figure 33                        |
| Insertion Loss                                        | 0.5         |                |                              | dB typ                                 | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , see Figure 33   |
| $C_S$ (Off)                                           | 25          |                |                              | pF typ                                 | $f = 1\text{ MHz}$                                                              |
| $C_D$ (Off)                                           | 45          |                |                              | pF typ                                 | $f = 1\text{ MHz}$                                                              |
| $C_D$ , $C_S$ (On)                                    | 80          |                |                              | pF typ                                 | $f = 1\text{ MHz}$                                                              |
| <b>POWER REQUIREMENTS</b>                             |             |                |                              |                                        | $V_{DD} = 13.2\text{ V}$                                                        |
| $I_{DD}$                                              | 0.002       |                |                              | $\mu\text{A}$ typ                      | Digital inputs = $0\text{ V}$ or $V_{DD}$                                       |
|                                                       |             |                | 1                            | $\mu\text{A}$ max                      |                                                                                 |
| $I_{DD}$                                              | 260         |                |                              | $\mu\text{A}$ typ                      | Digital inputs = $5\text{ V}$                                                   |
|                                                       |             |                | 475                          | $\mu\text{A}$ max                      |                                                                                 |
| $V_{DD}$                                              |             |                | 5/16.5                       | V min/max                              | $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$                                      |
| Continuous Current per Channel <sup>2</sup>           |             |                |                              |                                        | $V_{DD} = +10.8\text{ V}$ , $V_{SS} = 0\text{ V}$                               |
| ADG1433                                               | 100         | 65             | 40                           | mA max                                 |                                                                                 |
| ADG1434                                               | 85          | 60             | 35                           | mA max                                 |                                                                                 |

<sup>1</sup> Temperature range for Y version:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

<sup>2</sup> Guaranteed by design, not subject to production test.

# ADG1433/ADG1434

## ±5 V DUAL SUPPLY

$V_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = -5\text{ V} \pm 10\%$ , GND = 0 V, unless otherwise noted.

Table 3.

| Parameter                                                | +25°C  | −40°C to +85°C | −40°C to +125°C <sup>1</sup> | Unit              | Test Conditions/Comments                                                             |
|----------------------------------------------------------|--------|----------------|------------------------------|-------------------|--------------------------------------------------------------------------------------|
| <b>ANALOG SWITCH</b>                                     |        |                |                              |                   |                                                                                      |
| Analog Signal Range                                      |        |                | $V_{SS}$ to $V_{DD}$         | V                 |                                                                                      |
| On Resistance ( $R_{ON}$ )                               | 7      |                |                              | $\Omega$ typ      | $V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$ , see Figure 25                     |
|                                                          | 9      | 10.5           | 12                           | $\Omega$ max      | $V_{DD} = +4.5\text{ V}$ , $V_{SS} = -4.5\text{ V}$                                  |
| On Resistance Match Between Channels ( $\Delta R_{ON}$ ) | 0.55   |                |                              | $\Omega$ typ      | $V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$                                     |
|                                                          | 0.78   | 0.91           | 1.1                          | $\Omega$ max      |                                                                                      |
| On Resistance Flatness, $R_{FLAT(ON)}$                   | 1.5    |                |                              | $\Omega$ typ      | $V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$                                     |
|                                                          | 2.5    | 2.5            | 3                            | $\Omega$ max      |                                                                                      |
| <b>LEAKAGE CURRENTS</b>                                  |        |                |                              |                   |                                                                                      |
| Source Off Leakage, $I_S$ (Off)                          | ±0.02  |                |                              | nA typ            | $V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$                                  |
|                                                          | ±0.3   | ±0.6           | ±3                           | nA max            | $V_D = \pm 4.5\text{ V}$ , $V_S = \pm 4.5\text{ V}$ , see Figure 26                  |
| Drain Off Leakage, $I_D$ (Off)                           | ±0.02  |                |                              | nA typ            | $V_D = \pm 4.5\text{ V}$ , $V_S = \pm 4.5\text{ V}$ , see Figure 26                  |
|                                                          | ±0.3   | ±0.6           | ±3                           | nA max            |                                                                                      |
| Channel On Leakage, $I_D$ , $I_S$ (On)                   | ±0.04  |                |                              | nA typ            | $V_S = V_D = \pm 4.5\text{ V}$ , see Figure 27                                       |
|                                                          | ±0.4   | ±0.8           | ±8                           | nA max            |                                                                                      |
| <b>DIGITAL INPUTS</b>                                    |        |                |                              |                   |                                                                                      |
| Input High Voltage, $V_{IH}$                             |        |                | 2.0                          | V min             |                                                                                      |
| Input Low Voltage, $V_{IL}$                              |        |                | 0.8                          | V max             |                                                                                      |
| Input Current, $I_{IL}$ or $I_{IH}$                      | ±0.005 |                |                              | $\mu\text{A}$ typ | $V_{IN} = V_{GND}$ or $V_{DD}$                                                       |
|                                                          |        |                | ±0.1                         | $\mu\text{A}$ max |                                                                                      |
| Digital Input Capacitance, $C_{IN}$                      | 4      |                |                              | pF typ            |                                                                                      |
| <b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>               |        |                |                              |                   |                                                                                      |
| Transition Time, $t_{TRANS}$                             | 315    |                |                              | ns typ            | $R_L = 100\ \Omega$ , $C_L = 35\text{ pF}$                                           |
|                                                          | 430    | 480            | 550                          | ns max            | $V_S = 5\text{ V}$ , see Figure 28                                                   |
| Break-Before-Make Time Delay, $t_D$                      | 90     |                |                              | ns typ            | $R_L = 100\ \Omega$ , $C_L = 35\text{ pF}$                                           |
|                                                          |        |                | 55                           | ns min            | $V_{S1} = V_{S2} = 5\text{ V}$ , see Figure 29                                       |
| $t_{ON}(\overline{EN})$                                  | 325    |                |                              | ns typ            | $R_L = 100\ \Omega$ , $C_L = 35\text{ pF}$                                           |
|                                                          | 425    | 490            | 545                          | ns max            | $V_S = 5\text{ V}$ , see Figure 30                                                   |
| $t_{OFF}(\overline{EN})$                                 | 150    |                |                              | ns typ            | $R_L = 100\ \Omega$ , $C_L = 35\text{ pF}$                                           |
|                                                          | 200    | 225            | 240                          | ns max            | $V_S = 5\text{ V}$ , see Figure 30                                                   |
| Charge Injection                                         | −10    |                |                              | pC typ            | $V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , see Figure 31         |
| Off Isolation                                            | −70    |                |                              | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , see Figure 32        |
| Channel-to-Channel Crosstalk                             | −70    |                |                              | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , see Figure 34        |
| Total Harmonic Distortion, THD + N                       | 0.06   |                |                              | % typ             | $R_L = 110\ \Omega$ , 5 V p-p, $f = 20\text{ Hz}$ to $20\text{ kHz}$ , see Figure 35 |
| −3 dB Bandwidth                                          | 145    |                |                              | MHz typ           | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , see Figure 33                             |
| Insertion Loss                                           | 0.5    |                |                              | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , see Figure 33        |
| $C_S$ (Off)                                              | 18     |                |                              | pF typ            | $f = 1\text{ MHz}$                                                                   |
| $C_D$ (Off)                                              | 32     |                |                              | pF typ            | $f = 1\text{ MHz}$                                                                   |
| $C_D$ , $C_S$ (On)                                       | 80     |                |                              | pF typ            | $f = 1\text{ MHz}$                                                                   |
| <b>POWER REQUIREMENTS</b>                                |        |                |                              |                   |                                                                                      |
| $I_{DD}$                                                 | 0.002  |                |                              | $\mu\text{A}$ typ | $V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$                                  |
|                                                          |        |                | 1                            | $\mu\text{A}$ max | Digital inputs = 0 V, 5 V, or $V_{DD}$                                               |
| $I_{SS}$                                                 | 0.001  |                |                              | $\mu\text{A}$ typ | Digital inputs = 0 V, 5 V, or $V_{DD}$                                               |
|                                                          |        |                | 1                            | $\mu\text{A}$ max |                                                                                      |
| $V_{DD}/V_{SS}$                                          |        |                | ±4.5/±16.5                   | V min/max         | GND = 0 V                                                                            |
| Continuous Current per Channel <sup>2</sup>              |        |                |                              |                   | $V_{DD} = +4.5\text{ V}$ , $V_{SS} = -4.5\text{ V}$                                  |
| ADG1433                                                  | 95     | 60             | 35                           | mA max            |                                                                                      |
| ADG1434                                                  | 85     | 55             | 35                           | mA max            |                                                                                      |

<sup>1</sup> Temperature range for Y version: −40°C to +125°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 4.**

| Parameter                                                     | Rating                                                                              |
|---------------------------------------------------------------|-------------------------------------------------------------------------------------|
| $V_{DD}$ to $V_{SS}$                                          | 35 V                                                                                |
| $V_{DD}$ to GND                                               | −0.3 V to +25 V                                                                     |
| $V_{SS}$ to GND                                               | −25 V to +0.3 V                                                                     |
| Analog Inputs, Digital Inputs <sup>1</sup>                    | $V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first |
| Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum) | 250 mA                                                                              |
| Continuous Current, S or D <sup>2</sup>                       | Data + 15%                                                                          |
| Operating Temperature Range                                   |                                                                                     |
| Industrial (Y Version)                                        | −40°C to +125°C                                                                     |
| Storage Temperature Range                                     | −65°C to +150°C                                                                     |
| Junction Temperature                                          | 150°C                                                                               |
| Reflow Soldering Peak Temperature (Pb-Free)                   | 260 (+ 0 to −5)°C                                                                   |

<sup>1</sup> Overvoltages at A,  $\overline{\text{EN}}$ , S, or D pins are clamped by internal diodes. Current should be limited to the maximum ratings given.

<sup>2</sup> See data given in the Specifications section (see Table 1 to Table 3).

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 5.**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|--------------|---------------|---------------|------|
| TSSOP        | 150.4         | 50            | °C/W |
| LFCSP_VQ     | 30.4          | N/A           | °C/W |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# ADG1433/ADG1434

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

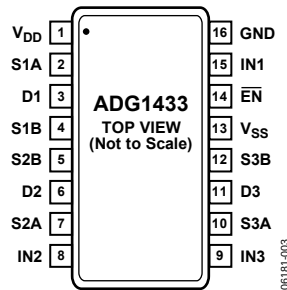
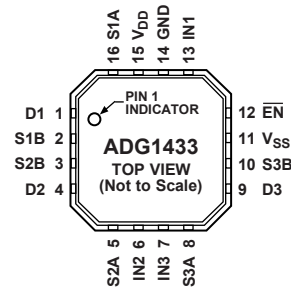


Figure 4. ADG1433 TSSOP Pin Configuration



NOTES  
1. EXPOSED PAD IS TIED TO SUBSTRATE,  $V_{SS}$ .

Figure 5. ADG1433 LFCSP\_VQ Pin Configuration

Table 6. ADG1433 Pin Function Descriptions

| Pin No. |          | Mnemonic        | Description                                                                                                                                 |
|---------|----------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| TSSOP   | LFCSP_VQ |                 |                                                                                                                                             |
| 1       | 15       | $V_{DD}$        | Most Positive Power Supply Potential.                                                                                                       |
| 2       | 16       | S1A             | Source Terminal 1A. Can be an input or an output.                                                                                           |
| 3       | 1        | D1              | Drain Terminal 1. Can be an input or an output.                                                                                             |
| 4       | 2        | S1B             | Source Terminal 1B. Can be an input or an output.                                                                                           |
| 5       | 3        | S2B             | Source Terminal 2B. Can be an input or an output.                                                                                           |
| 6       | 4        | D2              | Drain Terminal 2. Can be an input or an output.                                                                                             |
| 7       | 5        | S2A             | Source Terminal 2A. Can be an input or an output.                                                                                           |
| 8       | 6        | IN2             | Logic Control Input 2.                                                                                                                      |
| 9       | 7        | IN3             | Logic Control Input 3.                                                                                                                      |
| 10      | 8        | S3A             | Source Terminal 3A. Can be an input or an output.                                                                                           |
| 11      | 9        | D3              | Drain Terminal 3. Can be an input or an output.                                                                                             |
| 12      | 10       | S3B             | Source Terminal 3B. Can be an input or an output.                                                                                           |
| 13      | 11       | $V_{SS}$        | Most Negative Power Supply Potential. In single-supply applications, it can be connected to ground.                                         |
| 14      | 12       | $\overline{EN}$ | Active Low Digital Input. When high, the device is disabled and all switches are off. When low, INx logic inputs determine the on switches. |
| 15      | 13       | IN1             | Logic Control Input 1.                                                                                                                      |
| 16      | 14       | GND             | Ground (0 V) Reference.                                                                                                                     |

Table 7. ADG1433 Truth Table

| EN | INx | SxA | SxB |
|----|-----|-----|-----|
| 1  | X   | Off | Off |
| 0  | 0   | Off | On  |
| 0  | 1   | On  | Off |



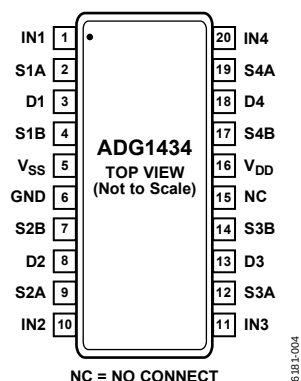


Figure 6. ADG1434 TSSOP Pin Configuration

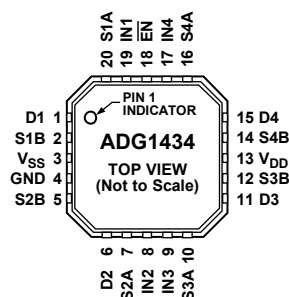


Figure 7. ADG1434 LFCSP\_VQ Pin Configuration

Table 8. ADG1434 Pin Function Descriptions

| Pin No. |          | Mnemonic        | Description                                                                                                                                 |
|---------|----------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| TSSOP   | LFCSP_VQ |                 |                                                                                                                                             |
| 1       | 19       | IN1             | Logic Control Input 1.                                                                                                                      |
| 2       | 20       | S1A             | Source Terminal 1A. Can be an input or an output.                                                                                           |
| 3       | 1        | D1              | Drain Terminal 1. Can be an input or an output.                                                                                             |
| 4       | 2        | S1B             | Source Terminal 1B. Can be an input or an output.                                                                                           |
| 5       | 3        | V <sub>SS</sub> | Most Negative Power Supply Potential. In single-supply applications, it can be connected to ground.                                         |
| 6       | 4        | GND             | Ground (0 V) Reference.                                                                                                                     |
| 7       | 5        | S2B             | Source Terminal 2B. Can be an input or an output.                                                                                           |
| 8       | 6        | D2              | Drain Terminal 2. Can be an input or an output.                                                                                             |
| 9       | 7        | S2A             | Source Terminal 2A. Can be an input or an output.                                                                                           |
| 10      | 8        | IN2             | Logic Control Input 2.                                                                                                                      |
| 11      | 9        | IN3             | Logic Control Input 3.                                                                                                                      |
| 12      | 10       | S3A             | Source Terminal 3A. Can be an input or an output.                                                                                           |
| 13      | 11       | D3              | Drain Terminal 3. Can be an input or an output.                                                                                             |
| 14      | 12       | S3B             | Source Terminal 3B. Can be an input or an output.                                                                                           |
| 15      | N/A      | NC              | No Connect.                                                                                                                                 |
| 16      | 13       | V <sub>DD</sub> | Most Positive Power Supply Potential.                                                                                                       |
| 17      | 14       | S4B             | Source Terminal 4B. Can be an input or an output.                                                                                           |
| 18      | 15       | D4              | Drain Terminal 4. Can be an input or an output.                                                                                             |
| 19      | 16       | S4A             | Source Terminal 4A. Can be an input or an output.                                                                                           |
| 20      | 17       | IN4             | Logic Control Input 4.                                                                                                                      |
| N/A     | 18       | EN              | Active Low Digital Input. When high, the device is disabled and all switches are off. When low, INx logic inputs determine the on switches. |

Table 9. ADG1434 TSSOP Truth Table

| INx | SxA | SxB |
|-----|-----|-----|
| 0   | Off | On  |
| 1   | On  | Off |

Table 10. ADG1434 LFCSP\_VQ Truth Table

| EN | INx | SxA | SxB |
|----|-----|-----|-----|
| 1  | X   | Off | Off |
| 0  | 0   | Off | On  |
| 0  | 1   | On  | Off |

## TYPICAL PERFORMANCE CHARACTERISTICS

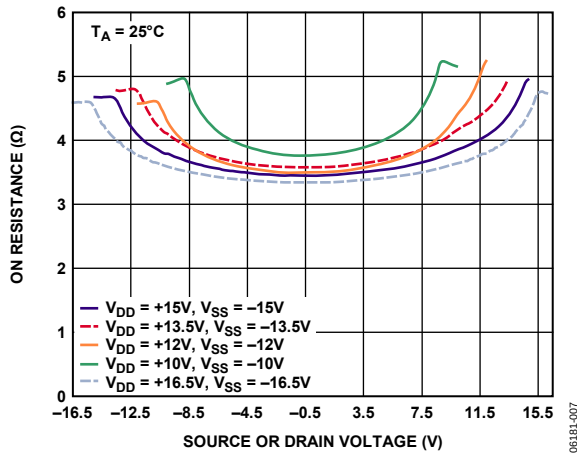


Figure 8. On Resistance as a Function of  $V_D$  ( $V_S$ ), Dual Supply

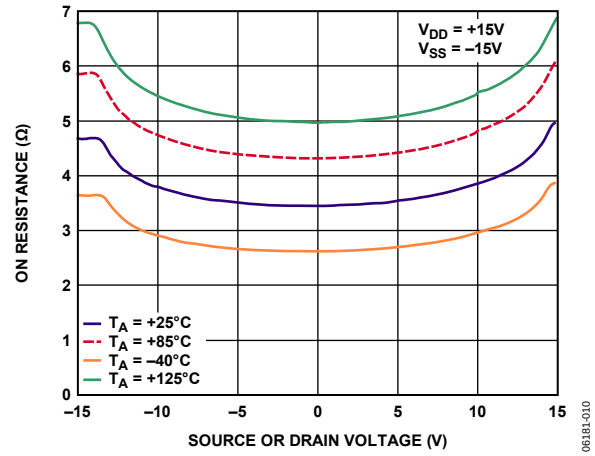


Figure 11. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures,  $\pm 15$  V Dual Supply

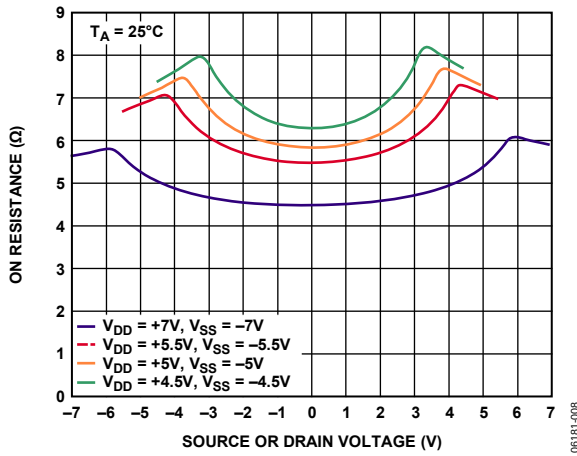


Figure 9. On Resistance as a Function of  $V_D$  ( $V_S$ ), Dual Supply

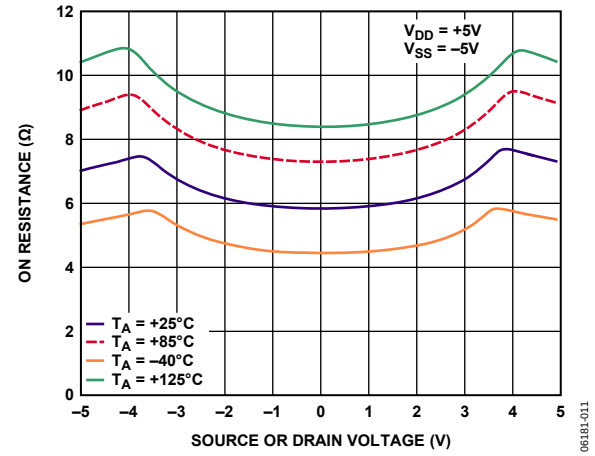


Figure 12. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures,  $\pm 5$  V Dual Supply

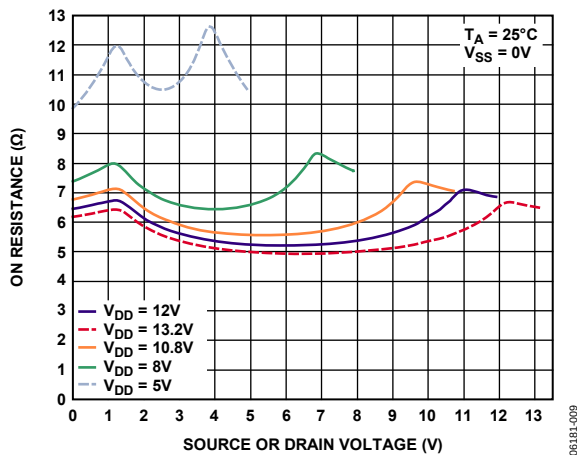


Figure 10. On Resistance as a Function of  $V_D$  ( $V_S$ ), Single Supply

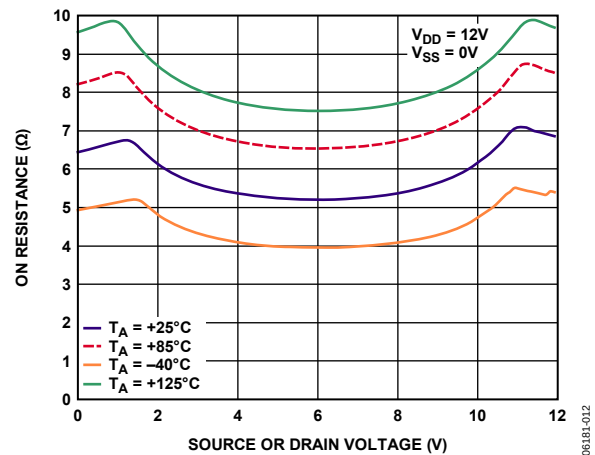


Figure 13. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, 12 V Single Supply

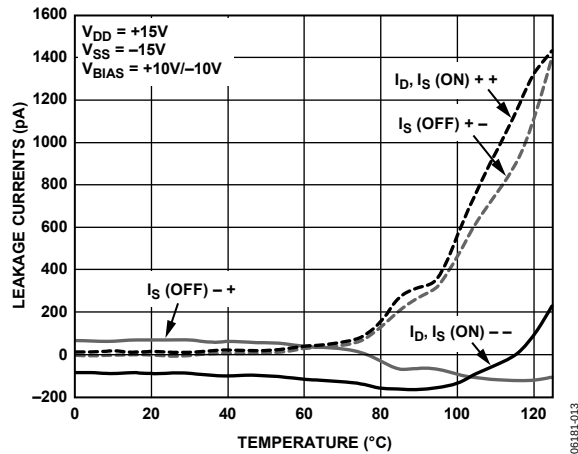


Figure 14. Leakage Currents as a Function of Temperature, ±15 V Dual Supply

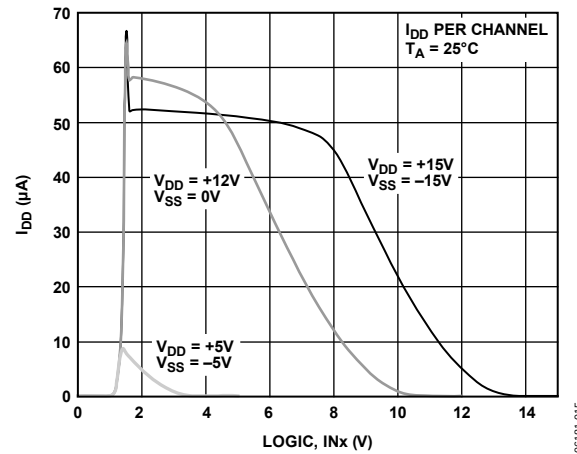


Figure 17.  $I_{DD}$  vs. Logic Level

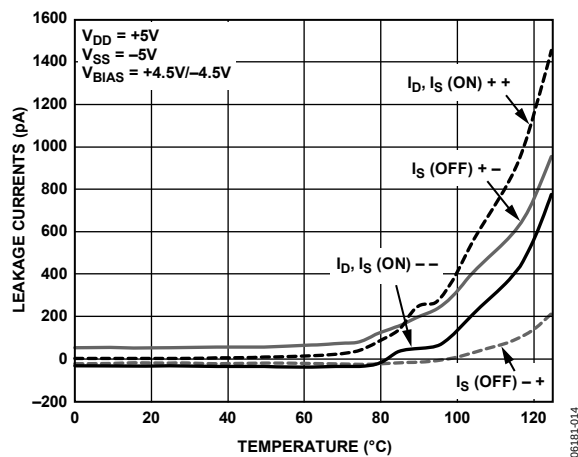


Figure 15. Leakage Currents as a Function of Temperature, ±5 V Dual Supply

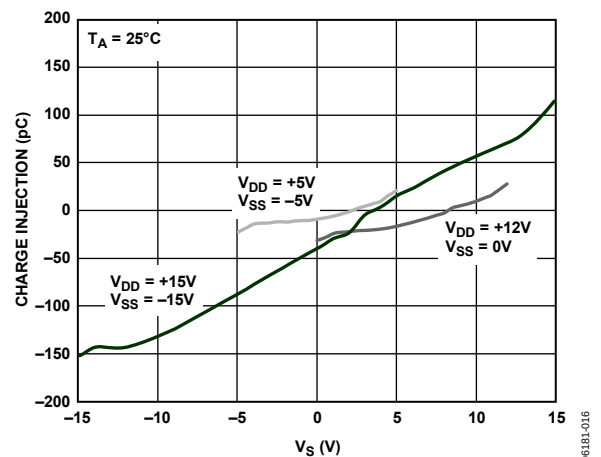


Figure 18. Charge Injection vs. Source Voltage

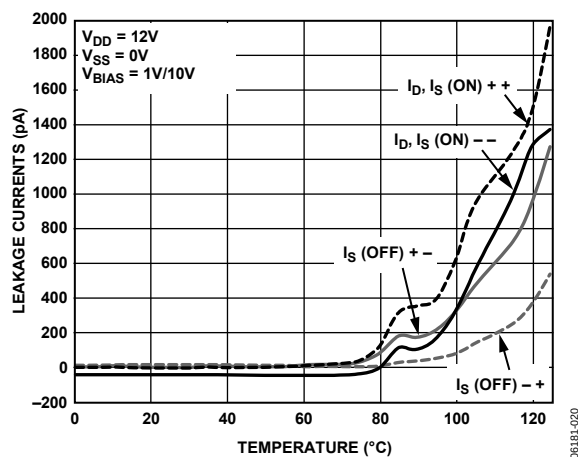


Figure 16. Leakage Currents as a Function of Temperature, 12 V Single Supply

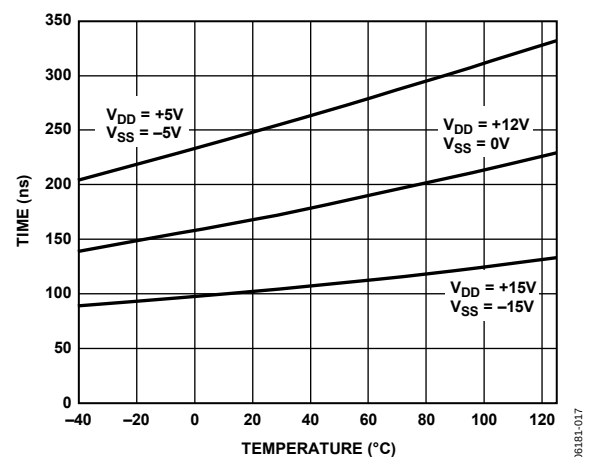


Figure 19. Transition Time vs. Temperature

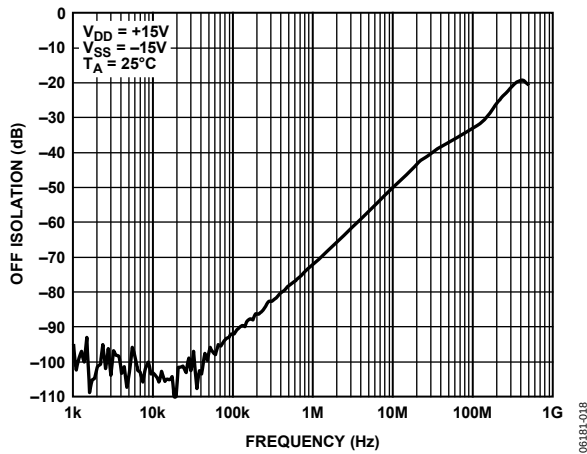


Figure 20. Off Isolation vs. Frequency

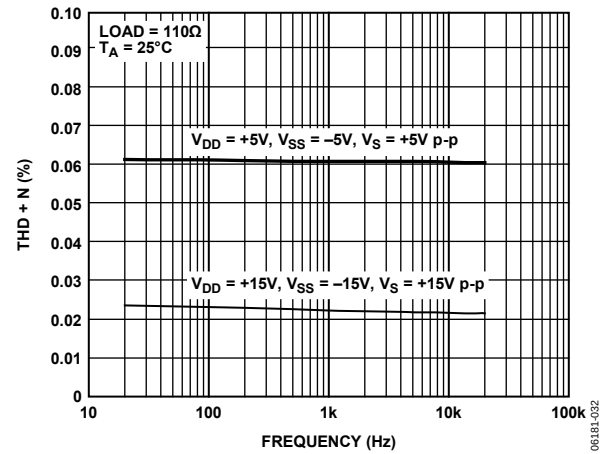


Figure 23. THD + N vs. Frequency

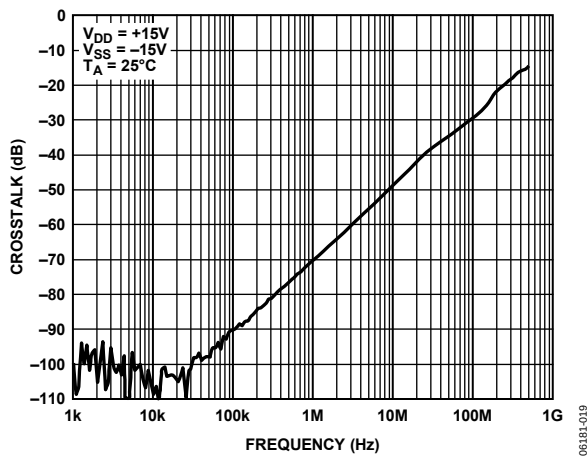


Figure 21. Crosstalk vs. Frequency

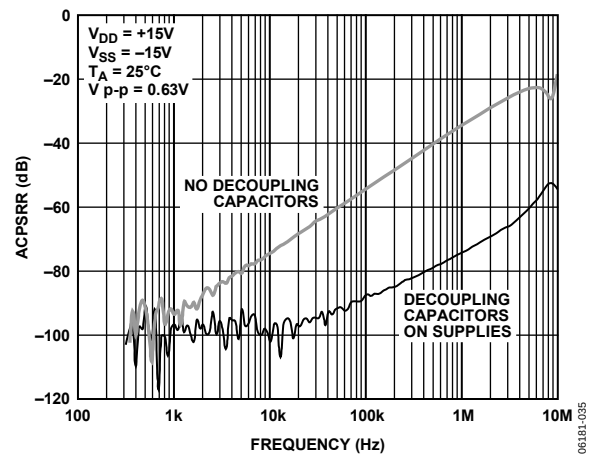


Figure 24. ACPSRR vs. Frequency

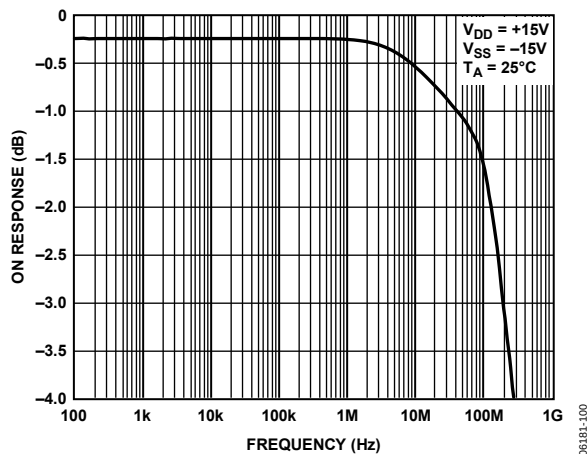


Figure 22. On Response vs. Frequency

## TEST CIRCUITS

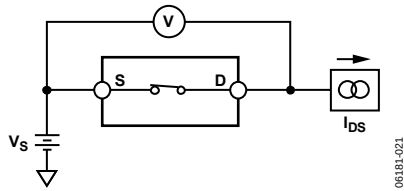


Figure 25. On Resistance

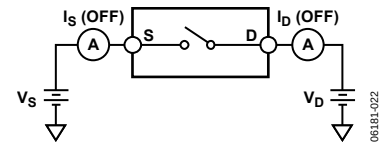


Figure 26. Off Leakage

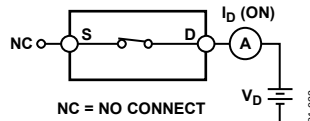


Figure 27. On Leakage

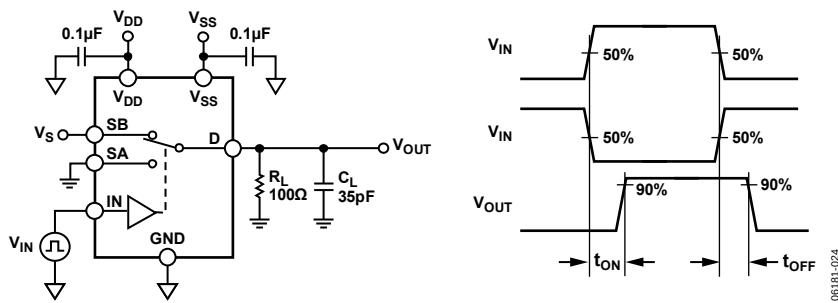


Figure 28. Switching Timing

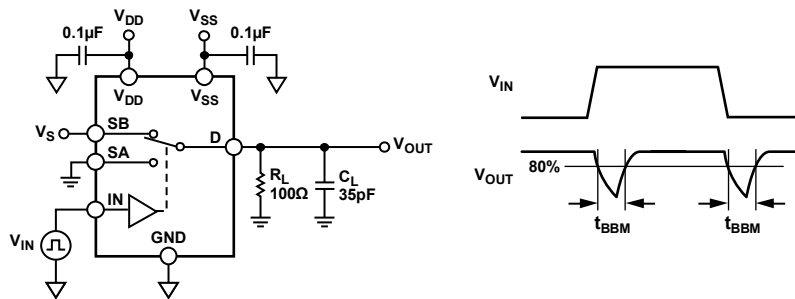


Figure 29. Break-Before-Make Delay,  $t_D$

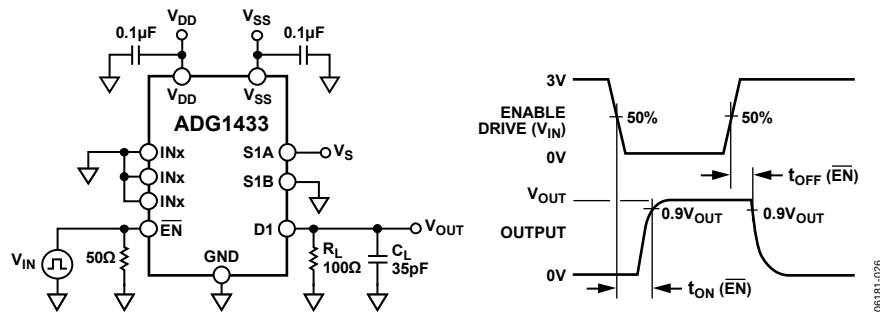


Figure 30. Enable Delay,  $t_{ON}(\overline{EN})$ ,  $t_{OFF}(\overline{EN})$

# ADG1433/ADG1434

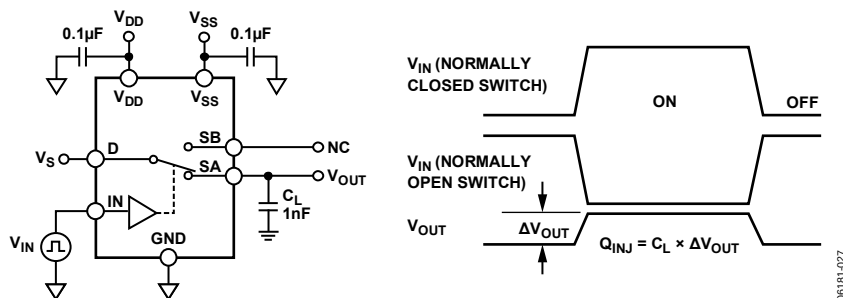


Figure 31. Charge Injection

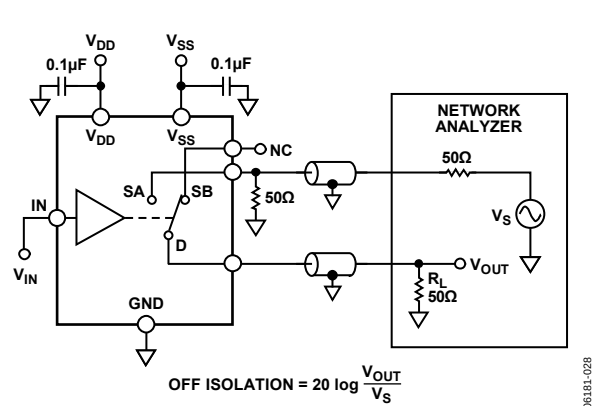


Figure 32. Off Isolation

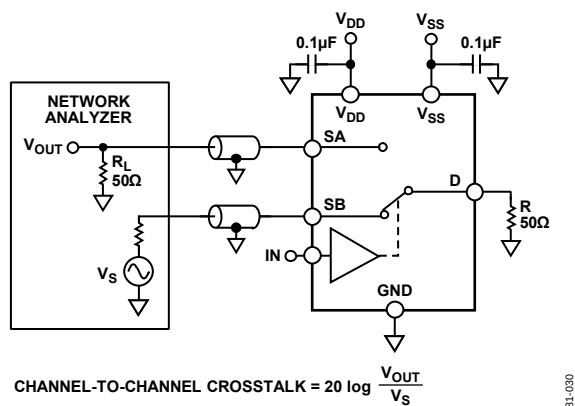


Figure 34. Channel-to-Channel Crosstalk

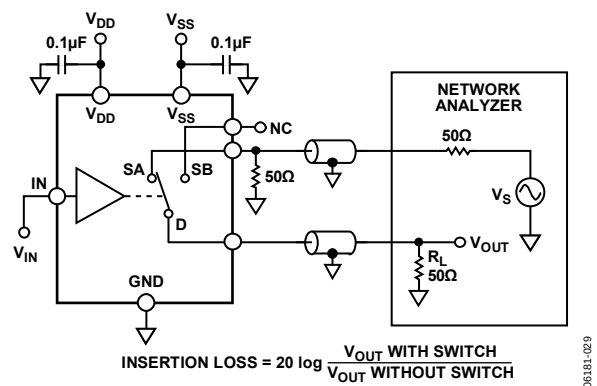


Figure 33. Bandwidth

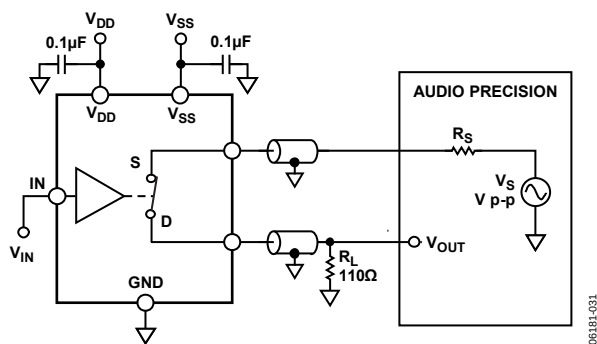


Figure 35. THD + Noise

## TERMINOLOGY

### $R_{ON}$

Ohmic resistance between Terminal D and Terminal S.

### $\Delta R_{ON}$

The difference between the  $R_{ON}$  of any two channels.

### $R_{FLAT(ON)}$

The difference between the maximum and minimum value of on resistance as measured.

### $I_S$ (Off)

Source leakage current when the switch is off.

### $I_D$ (Off)

Drain leakage current when the switch is off.

### $I_D, I_S$ (On)

Channel leakage current when the switch is on.

### $V_D$ ( $V_S$ )

Analog voltage on Terminal D and Terminal S.

### $C_S$ (Off)

Channel input capacitance for off condition.

### $C_D$ (Off)

Channel output capacitance for off condition.

### $C_D, C_S$ (On)

On switch capacitance.

### $C_{IN}$

Digital input capacitance.

### $t_{ON}$ ( $\overline{EN}$ )

Delay time between the 50% and 90% points of the digital input and switch on condition.

### $t_{OFF}$ ( $\overline{EN}$ )

Delay time between the 50% and 90% points of the digital input and switch off condition.

### $t_{TRANS}$

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

### $t_{BBM}$

Off time measured between the 80% point of both switches when switching from one address state to another.

### $V_{IL}$

Maximum input voltage for Logic 0.

### $V_{IH}$

Minimum input voltage for Logic 1.

### $I_{IL}$ ( $I_{IH}$ )

Input current of the digital input.

### $I_{DD}$

Positive supply current.

### $I_{SS}$

Negative supply current.

### Off Isolation

A measure of unwanted signal coupling through an off channel.

### Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

### Bandwidth

The frequency at which the output is attenuated by 3 dB.

### On Response

The frequency response of the on switch.

### Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

### AC Power Supply Rejection Ratio (ACPSRR)

A measure of the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

## OUTLINE DIMENSIONS

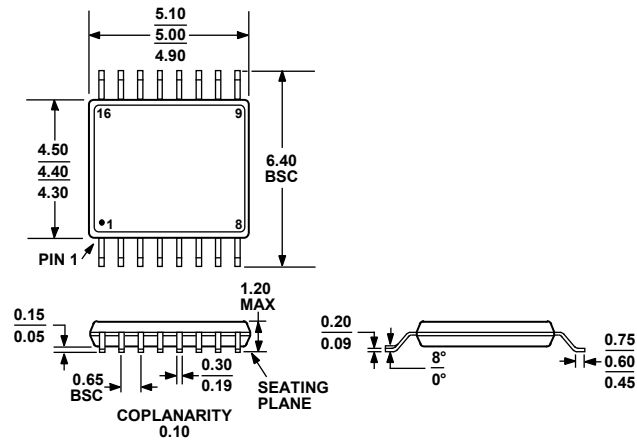


Figure 36. 16-Lead Thin Shrink Small Outline Package [TSSOP]  
(RU-16)  
Dimensions shown in millimeters

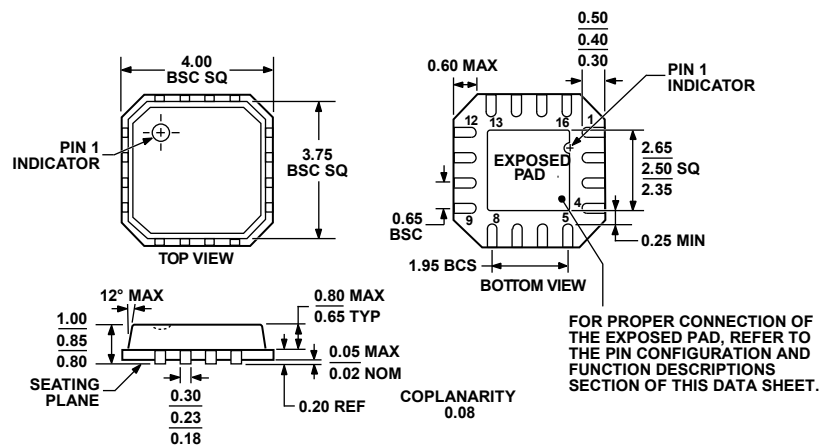


Figure 37. 16-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]  
4 mm x 4 mm Body, Very Thin Quad  
(CP-16-13)  
Dimensions shown in millimeters

031006-A



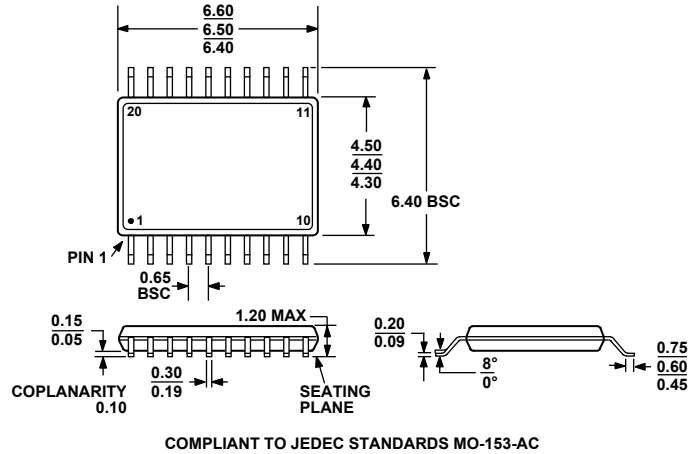


Figure 38. 20-Lead Thin Shrink Small Outline Package [TSSOP]  
(RU-20)  
Dimensions shown in millimeters

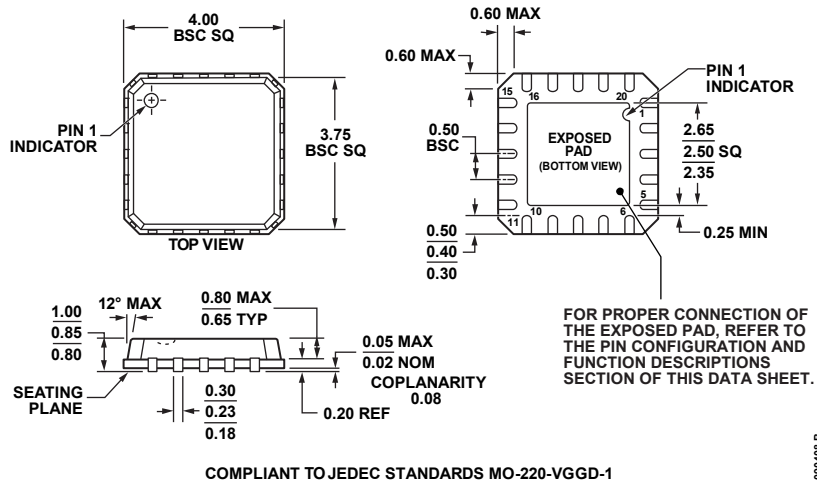


Figure 39. 20-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]  
4 mm × 4 mm Body, Very Thin Quad  
(CP-20-4)  
Dimensions shown in millimeters

## ORDERING GUIDE

| Model                          | Temperature Range | Description                                       | EN Pin | Package Option |
|--------------------------------|-------------------|---------------------------------------------------|--------|----------------|
| ADG1433YRUZ <sup>1</sup>       | −40°C to +125°C   | 16-Lead Thin Shrink Small Outline Package [TSSOP] | Yes    | RU-16          |
| ADG1433YRUZ-REEL <sup>1</sup>  | −40°C to +125°C   | 16-Lead Thin Shrink Small Outline Package [TSSOP] | Yes    | RU-16          |
| ADG1433YRUZ-REEL7 <sup>1</sup> | −40°C to +125°C   | 16-Lead Thin Shrink Small Outline Package [TSSOP] | Yes    | RU-16          |
| ADG1433YCPZ-REEL <sup>1</sup>  | −40°C to +125°C   | 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]  | Yes    | CP-16-13       |
| ADG1433YCPZ-REEL7 <sup>1</sup> | −40°C to +125°C   | 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]  | Yes    | CP-16-13       |
| ADG1434YRUZ <sup>1</sup>       | −40°C to +125°C   | 20-Lead Thin Shrink Small Outline Package [TSSOP] | No     | RU-20          |
| ADG1434YRUZ-REEL <sup>1</sup>  | −40°C to +125°C   | 20-Lead Thin Shrink Small Outline Package [TSSOP] | No     | RU-20          |
| ADG1434YRUZ-REEL7 <sup>1</sup> | −40°C to +125°C   | 20-Lead Thin Shrink Small Outline Package [TSSOP] | No     | RU-20          |
| ADG1434YCPZ-REEL <sup>1</sup>  | −40°C to +125°C   | 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]  | Yes    | CP-20-4        |
| ADG1434YCPZ-REEL7 <sup>1</sup> | −40°C to +125°C   | 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]  | Yes    | CP-20-4        |

<sup>1</sup> Z = RoHS Compliant Part.

**ADG1433/ADG1434**

**NOTES**

NOTES

## NOTES

# AMEYA360

Components Supply Platform

Authorized Distribution Brand :



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