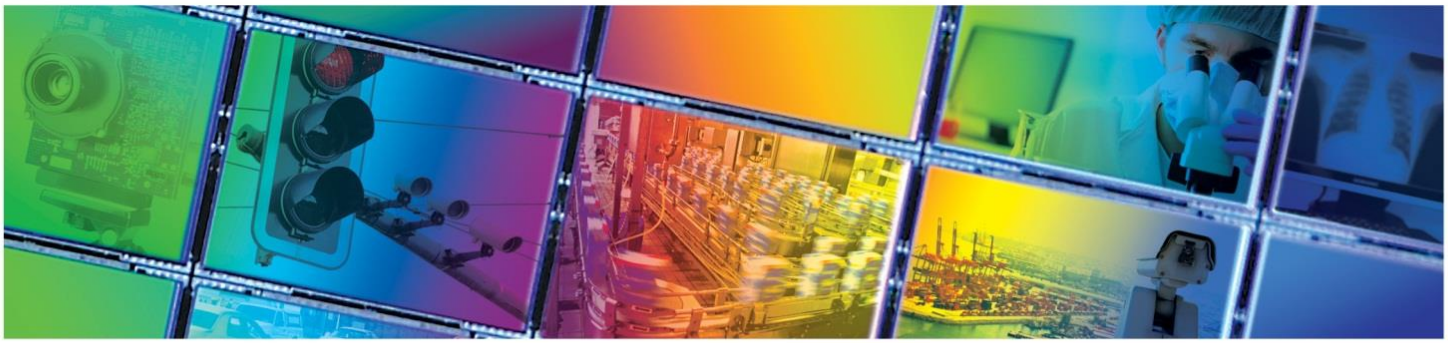
ON Semiconductor®

KAF-16803 IMAGE SENSOR

4096 (H) X 4096 (V) FULL FRAME CCD IMAGE SENSOR



JUNE 24, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.1 PS-0040

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KAF-16803 Image Sensor

DESCRIPTION

The KAF-16803 image sensor is a redesigned version of the popular KAF-16801 image sensor (4096 x 4096 pixel resolution), with enhancements that specifically target the needs of high performance digital radiography applications. Improvements include enhanced quantum efficiency for improved DQE at higher spatial frequencies, lower noise for improved contrast in areas of high density, and anti-blooming protection to prevent image bleed from over exposure in regions outside the patient.

The sensor utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode, as well as microlenses to maximize light sensitivity. When combined with large imaging area and small pixel size, the KAF-16803 provides the sensitivity, resolution and contrast necessary for high quality digital radiographs.

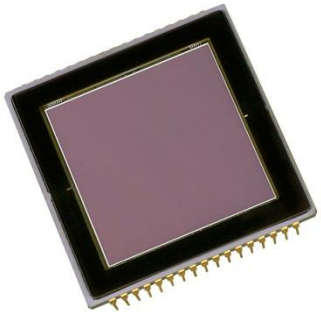
To simplify device integration, the KAF-16803 image sensor uses the same pin-out and package as the KAF-16801 image sensor.

KEY FEATURES

- TRUESENSE Transparent Gate Electrode for high sensitivity
- High Resolution
- Large Image Area
- High Quantum Efficiency
- Low Noise Architecture
- Broad Dynamic Range

APPLICATIONS

- Medical
- Scientific



Parameter	Typical Value
Architecture	Full Frame CCD; Square Pixels
Total Number of Pixels	4145 (H) x 4128 (V) = 17.1 Mp
Number of Effective Pixels	4127 (H) x 4128 (V) = 17.0 Mp
Number of Active Pixels	4096 (H) x 4096 (V) = 16.8 Mp
Pixel Size	9 µm (H) x 9 µm (V)
Active Image Size	36.8 mm (H) x 36.8 mm (V) 52.1 mm Diagonal
Aspect Ratio	1:1
Horizontal Outputs	1
Saturation Signal	100 ke$^-$
Output Sensitivity	22 µV/e$^-$
Quantum Efficiency (550nm)	60%
Responsivity (550 nm)	28.7 V/µJ/cm^2
Read Noise (f = 4 MHz)	9 e$^-$
Dark Signal (T = 25 °C)	3 e/pix/sec
Dark Current Doubling Temperature	6.3 °C
Linear Dynamic Range (f = 4 MHz, T = 25 °C)	80 dB
Blooming Protection (4 ms exposure time)	> 100 X saturation exposure
Maximum Data Rate	10 MHz
Package	CERDIP (Sidebrazed, CuW)
Cover Glass	AR coated, 2 sides and Taped Clear

All parameters above are specified at T = 25 °C, unless noted otherwise

Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H2053	KAF-16803-ABA-DD-BA	Monochrome, Microlens, CERDIP Package (sidebrazed, CuW), AR coated 2 sides, Standard grade	KAF-16803-ABA (Serial Number)
4H0863	KAF-16803-ABA-DD-AE	Monochrome, Microlens, CERDIP Package (sidebrazed, CuW), AR coated 2 sides, Engineering sample	
4H2054	KAF-16803-ABA-DP-BA	Monochrome, Microlens, CERDIP Package (sidebrazed, CuW), Taped clear coverglass, Standard grade	
4H0865	KAF-16803-ABA-DP-AE	Monochrome, Microlens, CERDIP Package (sidebrazed, CuW), Taped clear coverglass, Engineering sample	

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

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Rochester, New York 14615

Phone: (585) 784-5500
E-mail: info@truesenseimaging.com

Device Description

ARCHITECTURE

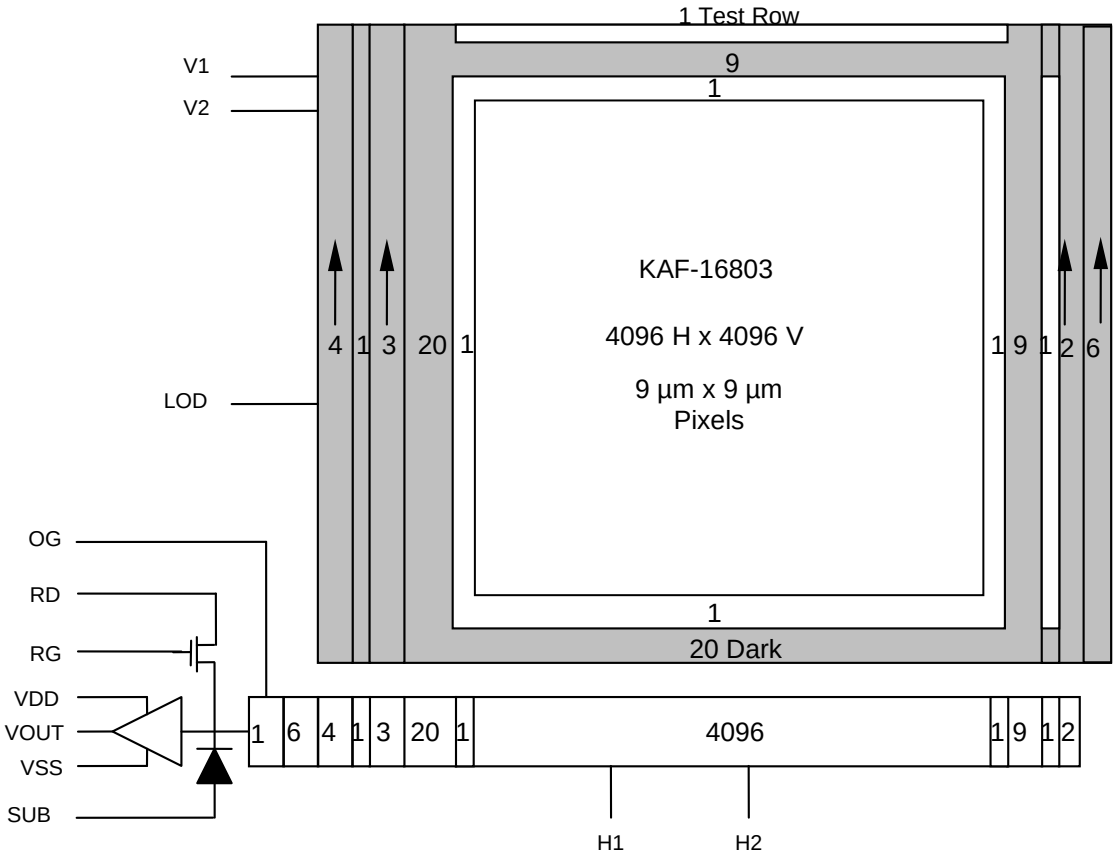

Figure 1: Block Diagram

Each line is composed of dummy pixels, internal test pixels, active buffer pixels, and valid photoactive pixels.

Dummy Pixels

Within each horizontal shift register the first pixels are 11 dummy pixels and should not be used to determine a dark reference level.

Internal Test

The next 4 pixels are introduced into the design to facilitate production testing. These behave differently than the buffer and dark pixels and should not be used to establish a dark reference. The last three pixels in each line are also internal test pixels and should not be used to establish a dark reference.

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region, exist light shielded pixels that include 20 leading dark pixels on every line. There are also 20 full dark lines at the start and 9 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a dark reference.

Active Buffer Pixels

There is 1 photoactive buffer row and column adjacent to the valid photoactive pixels. These may have signals levels different from those in the imaging array and are not counted in the active pixel count.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

Charge Transport

The integrated charge from each pixel is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCDs to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented a new line on the falling edge of V2 while H1 is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion.

HORIZONTAL REGISTER

Output Structure

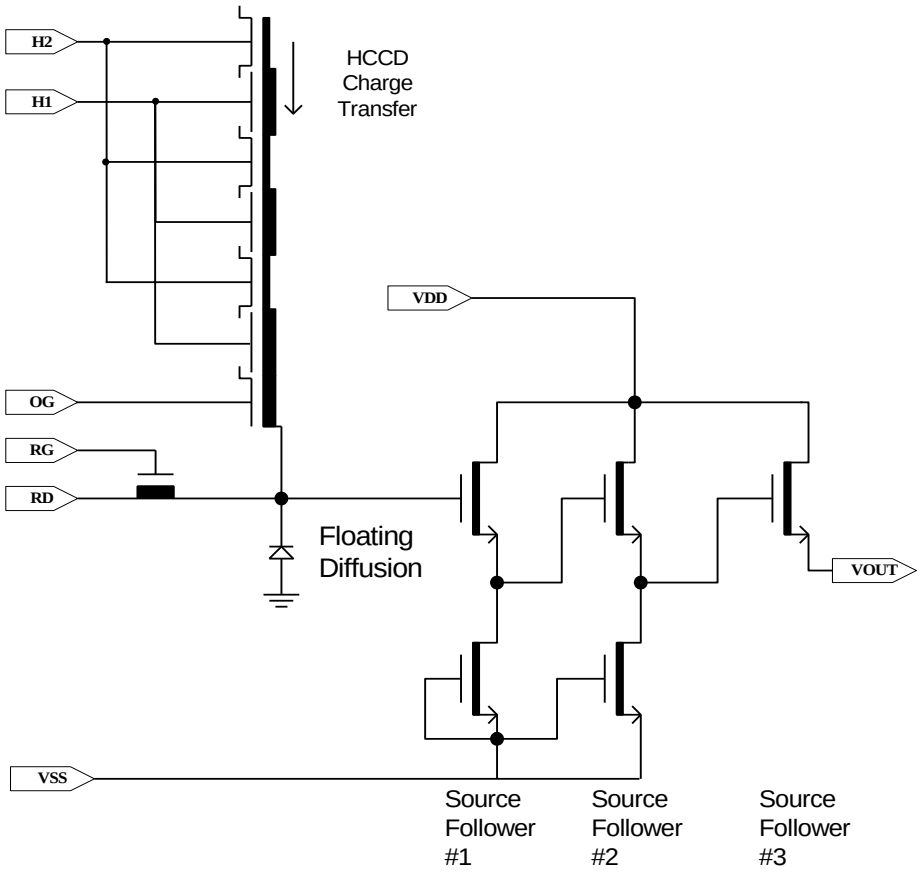

Figure 2: Output Architecture

The output consists of a floating diffusion capacitance connected to a three-stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip current source must be added to the VOUT pin of the device. See Figure 3.

Output Load

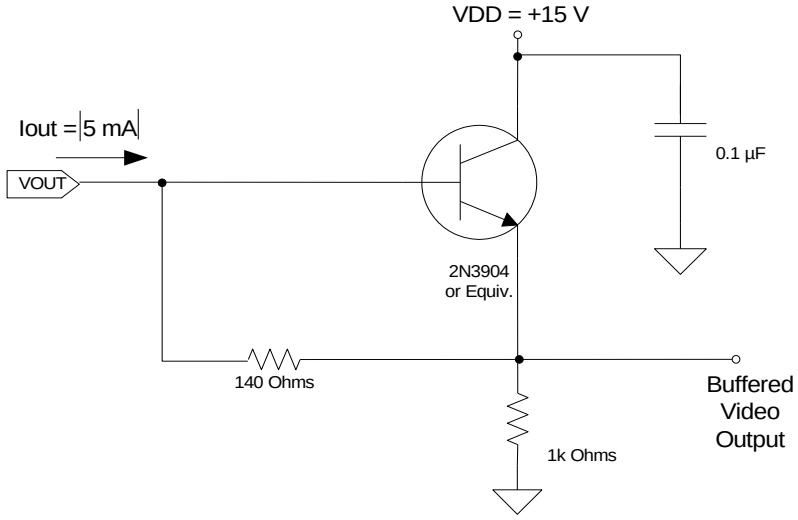

Figure 3: Recommended Output Structure Load Diagram.

Note:

Component values may be revised based on operating conditions and other design considerations.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

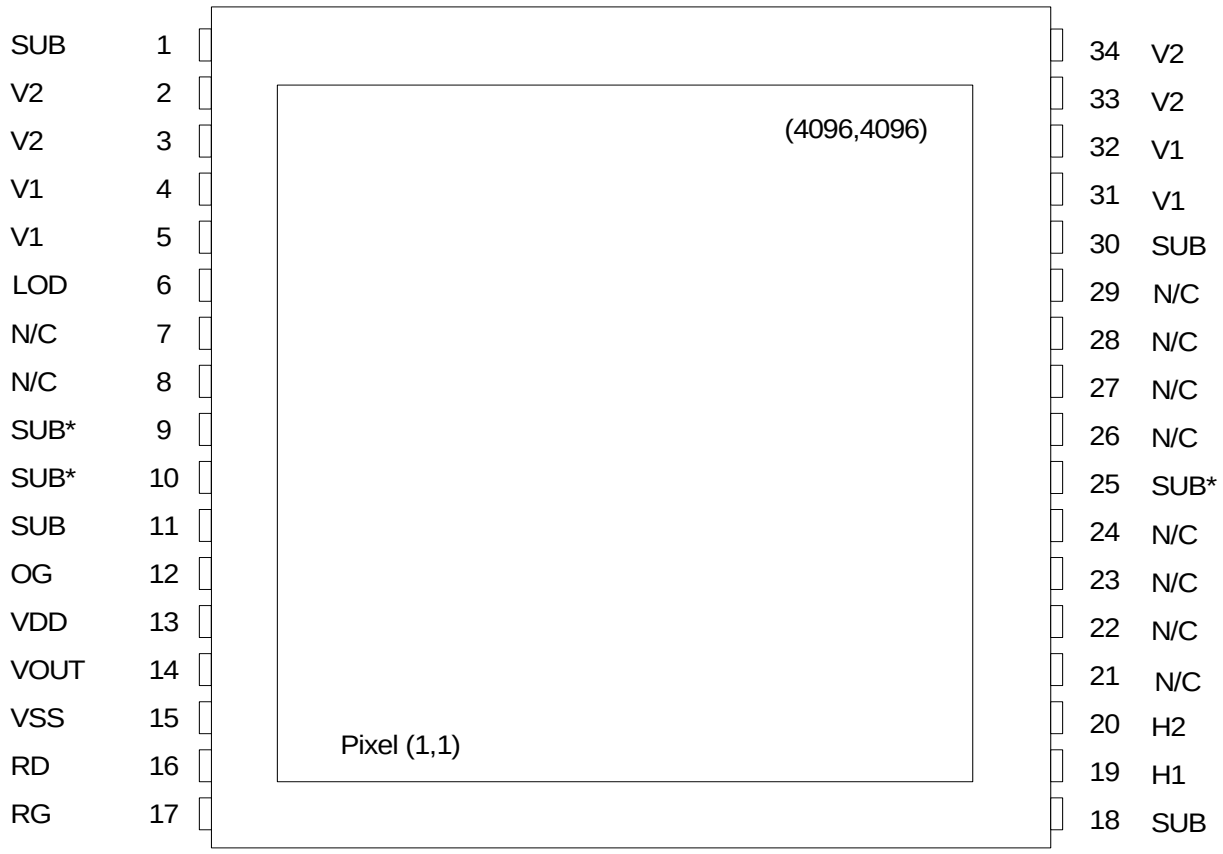

Figure 4: Device Orientation and Pinout

Notes:
1. Pins with the same name are to be tied together on the circuit board and have the same timing.
2. Unlike the KAF-16801, pins 9, 10, and, 25 are internally connected to SUB. They may be connected to SUB on the printed circuit board or otherwise must be left floating.

Pin	Name	Description
1	SUB	Substrate
2	V2	Vertical CCD Clock-Phase 2
3	V2	Vertical CCD Clock-Phase 2
4	V1	Vertical CCD Clock-Phase 1
5	V1	Vertical CCD Clock-Phase 1
6	LOD	Anti Blooming Drain
7	N/C	No Connection
8	N/C	No Connection
9	SUB*	Substrate or No Connection
10	SUB*	Substrate or No Connection
11	SUB	Substrate
12	OG	Output Gate
13	VDD	Output Amplifier Supply
14	VOUT	Video Output:
15	VSS	Output Amplifier Return
16	RD	Reset Drain
17	RG	Reset Gate
18	SUB	Substrate
19	H1	Horizontal Phase 1
20	H2	Horizontal Phase 2
21	N/C	No Connection
22	N/C	No Connection
23	N/C	No Connection
24	N/C	No Connection
25	SUB*	Substrate or No Connection
26	N/C	No Connection
27	N/C	No Connection
28	N/C	No Connection
29	N/C	No Connection
30	SUB	Substrate
31	V1	Vertical CCD Clock-Phase 1
32	V1	Vertical CCD Clock-Phase 1
33	V2	Vertical CCD Clock-Phase 2
34	V2	Vertical CCD Clock-Phase 2

Notes:

1. Unlike the KAF-16801, pins 9, 10, and, 25 are internally connected to SUB. They may be connected to SUB on the printed circuit board or must be left floating

Imaging Performance

Typical Operational Conditions

Description	Condition - Unless otherwise noted	Notes
Integration time (tint)	variable	
Horizontal clock frequency	4 MHz	
Temperature	25 °C	Room temperature
Mode	integrate – readout cycle	
Operation	Nominal operating voltages and timing with min. vertical pulse width tVw = 20 µs	

Specifications

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Saturation Signal	Vsat Ne^-_{sat}	1900 85k	2200 100k		mV e^-	1	die[11]
Quantum Efficiency (550 nm)	QE ($_{max}$)		60		%	1	design[12]
Responsivity (550)	R ($_{max}$)		28.7		$V/\mu J/cm^2$		design[12]
Photoresponse Non-Linearity	PRNL		1		%	2	design[12]
Photoresponse Non-Uniformity	PRNU		1		%	3	design[12]
Integration Dark Signal	Vdark, int		3 0.6	15 3	e/pix/sec pA/cm^2	4	die[11]
Readout Dark Current	Vdark, read		45	225	electrons	10	die[11]
Dark Signal Non-Uniformity	DSNU		3	15	e/pix/sec	5	die[11]
Dark Signal Doubling Temperature	ΔT		6.3		°C		design[12]
Read Noise	N_R		9	15	e^- rms	6	design[12]
Linear Dynamic Range	DR		80		dB	7	design[12]
Blooming Protection	Xab	100			Vsat	8	design[12]
Output Amplifier Sensitivity	$Vout/Ne^-$	20	22		$\mu V/e^-$		design[12]
DC Offset, output amplifier	Vodc		Vrd – 3.0	Vrd – 2.0	V	9	die[11]
Output Amplifier Bandwidth	f_{-3dB}		100		MHz		design[12]
Output Impedance, Amplifier	ROUT		160	200	Ohms		die[11]

Notes:

1. Increasing output load currents to improve bandwidth will decrease these values.
2. Worst case deviation from straight line fit, between 1% and 90% of $Vsat_{min}$.
3. One sigma deviation of a 128 x 128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25 °C.
5. Average dark signal of any of 32 x 32 blocks within the sensor. (Each block is 128 x 128 pixels.)
6. Output amplifier noise at 25 ˚C, operating at pixel frequency up to 4 MHz, bandwidth <10 MHz, tint = 0, and no dark current shot noise.
7. 20log ($Vsat/V_N$) - see Note 6 and Note 1.
   $V_N = N_R * Q/V$.
8. Xab is the number of times above the Vsat illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. Xab is measured at 4 ms.
9. Video level offset with respect to ground.
10. Readout dark current per pixel measured at 25 °C and vertical CCD clock width = 20 microseconds.
11. A parameter that is measured on every sensor during production testing.
12. A parameter that is quantified during the design verification activity.

Typical Performance Curves

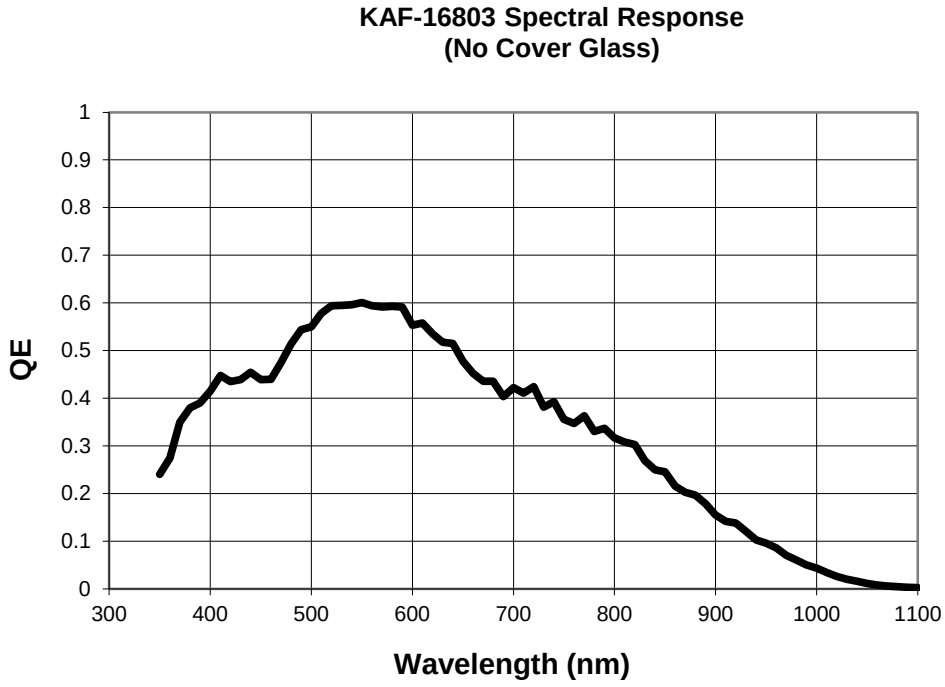

Figure 5: Typical Spectral Response

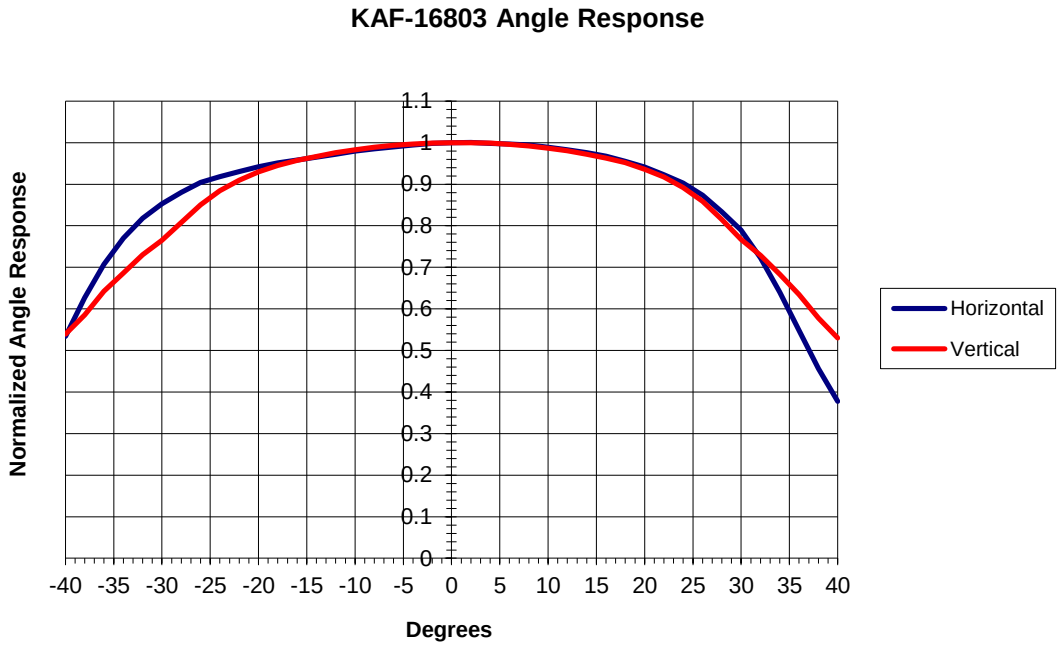

Figure 6: Typical Angle Response

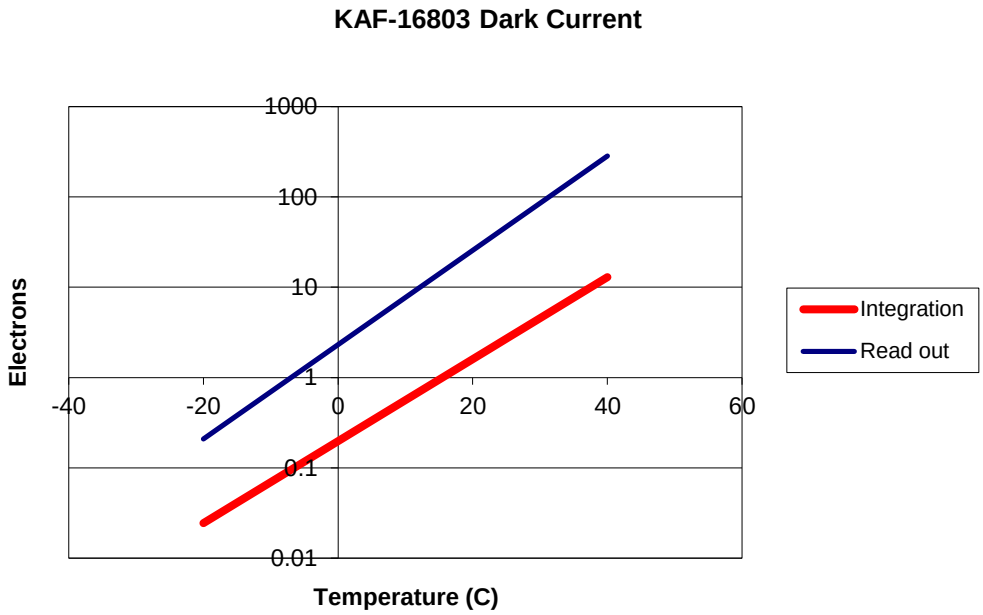

Figure 7: Dark Current

Noise Floor

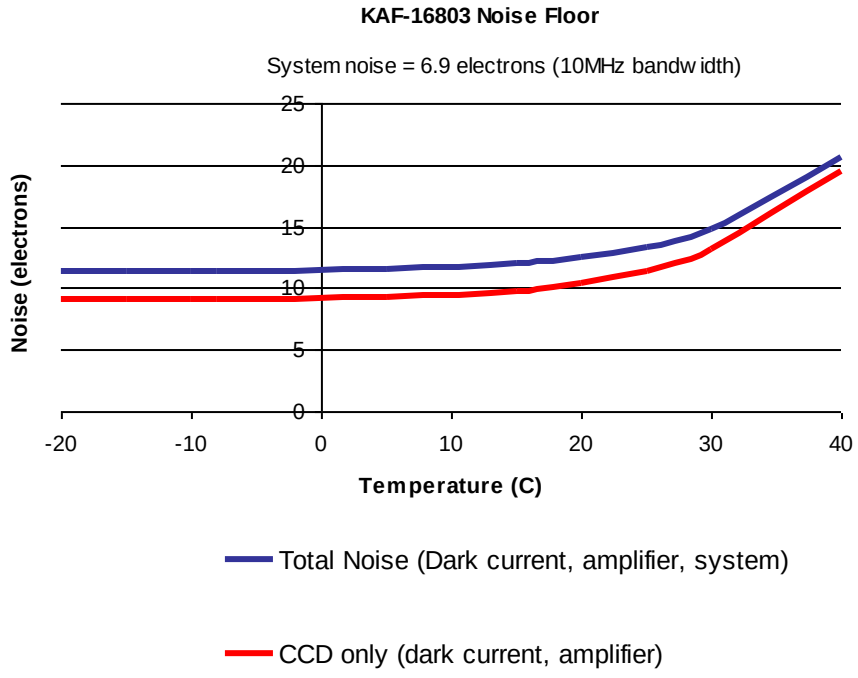

Figure 8: Noise Floor

Defect Definitions

Operationing Conditions

All defect tests performed at T ~25 °C

Specifications

Classification	Points	Clusters	Columns
Standard Grade	<200	<20	<10

Point Defects

Dark: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation

-- OR --

Bright: A Pixel with dark current >3,000 e/pixel/sec at 25 °C

Cluster Defect

A grouping of not more than 10 adjacent point defects

Cluster defects are separated by no less than 4 good pixels in any direction

Column Defect

A grouping of more than 10 point defects along a single column

-- OR --

A column containing a pixel with dark current > 15,000 e/pixel/sec (bright column)

-- OR --

A column that does not meet the CTE specification for all exposures less than the specified maximum saturation signal level and greater than 2 ke^-

-- OR --

A column that contains a pixel which loses more than 250 e under 2 ke^- illumination (trap defect)

Column defects are separated by no less than 4 good columns. No multiple column defects (double or more) will be permitted.

Column and cluster defects are separated by at least 4 good columns in the x direction.

Operation

Absolute Maximum Ratings

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{diode}	-0.5	+20	V	1,2
Gate Pin Voltages	V_{gate1}	-16	+16	V	1,3
Adjacent Gate Voltages	V_{1-2}	-16	+16	V	4
Output Bias Current	I_{out}		-30	mA	5
LOD Diode Voltage	V_{LOD}	-0.5	+13.0	V	1
Operating Temperature	T_{OP}	-60	60	°C	7

Notes:
1. Referenced to pin SUB
2. Includes pins: RD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H2, RG, VOG.
4. Voltage difference between adjacent gates. Includes: V1 to V2; H1 to H2; H1 to VOG; and V2 to H1.
5. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity).
6. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.
7. Noise performance will degrade at higher temperatures.

Power-up Sequence

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (SUB).
2. Supply the appropriate biases and clocks to the remaining pins.

DC Bias Operating Conditions

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	V_{RD}	12.75	13	13.625	V	I_{RD} = 0.01	
Output Amplifier Return	V_{SS}	1.75	2.0	2.25	V	I_{SS} = 3.0	
Output Amplifier Supply	V_{DD}	14.75	15.0	17.0	V	I_{OUT} + I_{SS}	
Substrate	V_{SUB}	0	0	0	V	0.01	
Output Gate	V_{OG}	1.0	2.0	2.5	V	0.01	
Lateral Overflow Drain	V_{LOD}	7.75	8.0	8.25	V	0.01	
Video Output Current	I_{OUT}	-3	-5	-7	mA		1

Note:
1. An output load sink must be applied to VOUT to activate output amplifier – see Figure 3.

AC Operating Conditions

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Notes
V1 Low Level	V1L	Low	-9.2	-9.0	-8.8	V	1
V1 High Level	V1H	High	2.3	2.5	2.7	V	1
V2 Low Level	V2L	Low	-9.2	-9.0	-8.8	V	1
V2 High Level	V2H	High	2.3	2.5	2.7	V	1
H1 Low Level	H1L	Low	-3.2	-3.0	-2.8	V	1
H1 High Level	H1H	High	6.8	7.0	7.2	V	1
H2 Low Level	H2L	Low	-3.2	-3.0	-2.8	V	1
H2 High Level	H2H	High	6.8	7.0	7.2	V	1
RG Low Level	RGL	Low	5.8	6.0	6.2	V	1
RG High Level	RGH	High	10.8	11.0	11.2	V	1

Note:
1. All pins draw less than 10 µA DC current. Capacitance values relative to SUB (substrate).

CAPACITANCE EQUIVALENT CIRCUIT

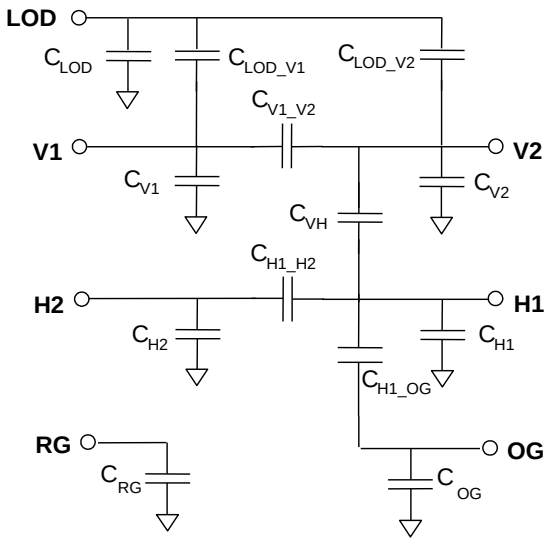

Figure 9: Equivalent Circuit Model

Description	Label	Value	Unit
LOD-Sub Capacitance	C_{LOD}	6.5	nF
LOD-V1 Capacitance	C_{LOD_Vq}	36	nF
LOD-V2 Capacitance	C_{LOD_V2}	36	nF
V1-V2 Capacitance	C_{V1_V2}	80	nF
V1-Sub Capacitance	C_{V1_SUB}	250	nF
V2-Sub Capacitance	C_{V2_SUB}	250	nF
V2-H1 Capacitance	C_{VH}	36	pF
H1-H2 Capacitance	C_{H1_H2}	75	pF
H1-Sub Capacitance	$C_{H1\ Sub}$	500	pF
H2-Sub Capacitance	C_{H2_Sub}	300	pF
OG-Sub Capacitance	$C_{OG\ Sub}$	5	pF
RG-Sub Capacitance	C_{RG_Sub}	13	pF

Timing

REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H		4	10	MHz	1
H1, H2 Rise, Fall Times	t_{H1r}, t_{H1f}	5			%	3
V1, V2 Rise, Fall Times	t_{V1r} , t_{V1f}	5			%	3
V1 - V2 Cross-over	V_{VCR}	-1	0	1	V	
H1 - H2 Cross-over	V_{HCR}	1	2	5	V	
H1, H2 Setup Time	t_{HS}	5	10		µs	
RG Clock Pulse Width	t_{RGw}	5	10		ns	4
V1, V2 Clock Pulse Width	t_{Vw}	20	20		µs	
Pixel Period (1 Count)	t_e	100	250		ns	2
Integration Time	t_{int}		-			5
Line Time	t_{line}	0.460	1.08		ms	6
Readout Time	$t_{readout}$	1,897	4,450		ms	7

Notes:

1. 50% duty cycle values.
2. CTE will degrade above the maximum frequency.
3. Relative to the pulse width (based on 50% of high/low levels).
4. RG should be clocked continuously.
5. Integration time is user specified.
6. $(4145 * t_e) + t_{HS} + (2 * t_{Vw}) = 1.08$ msec
7. $t_{readout} = t_{line} * 4128$ lines.

EDGE ALIGNMENT

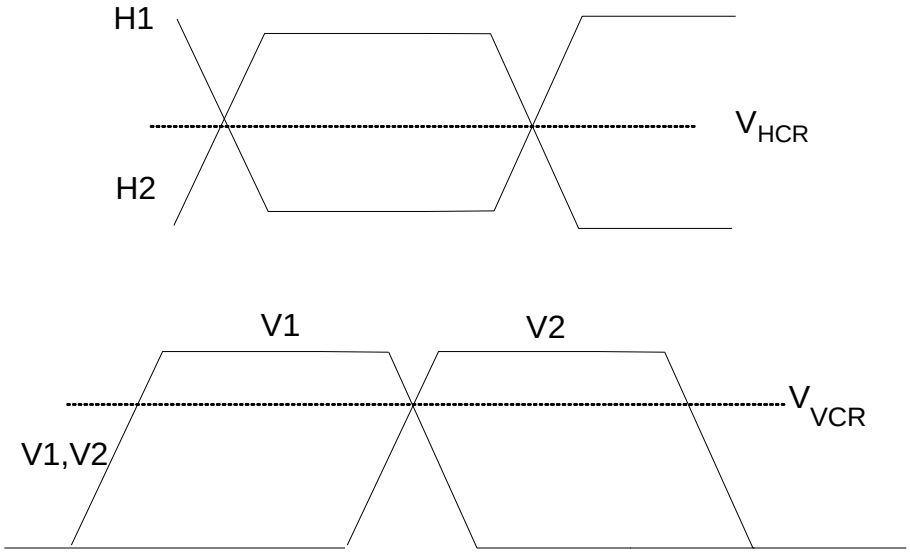

Figure 10: Edge Alignment

FRAME TIMING

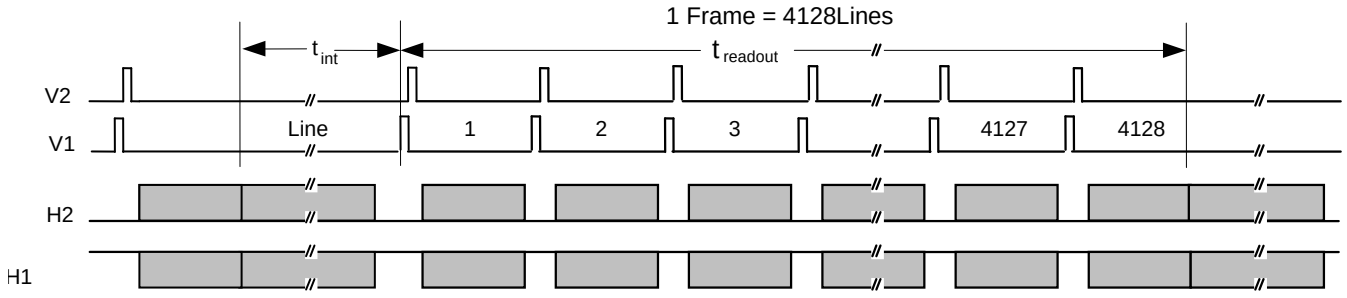

Figure 11: Frame Timing

Frame Timing Detail

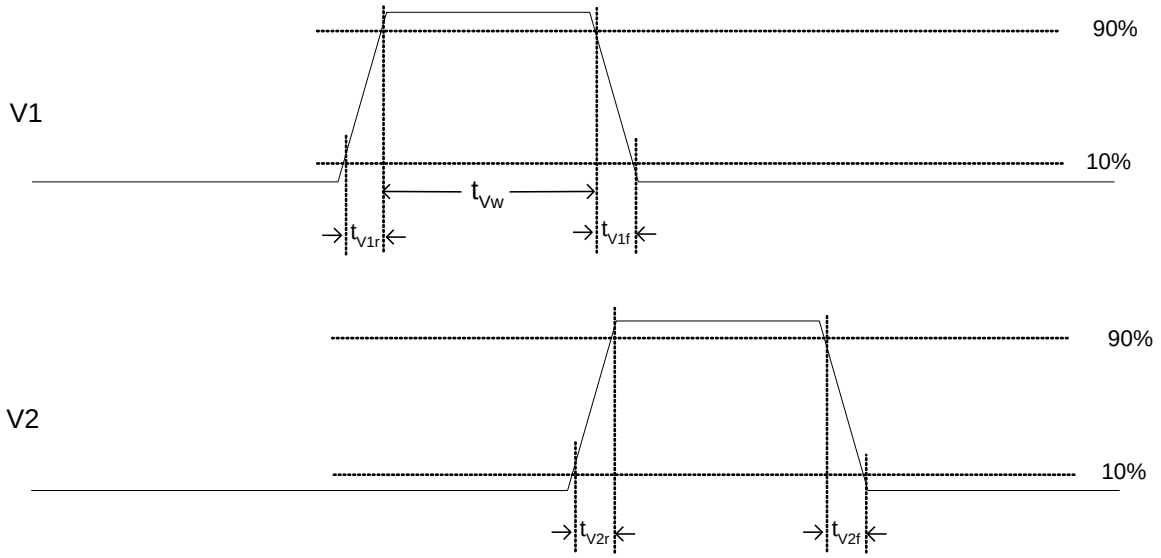

Figure 12: Frame Timing Detail

Line Timing (each output)

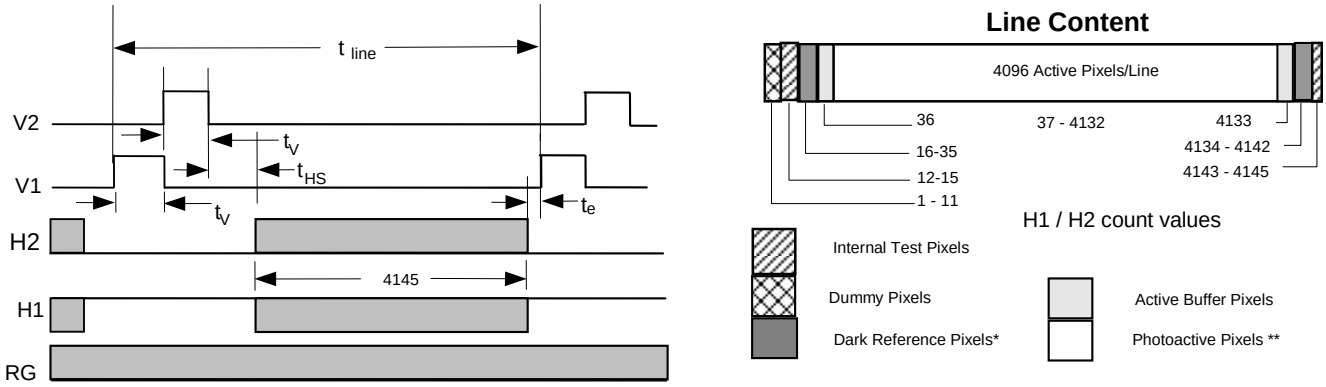

Figure 13: Line Timing

Pixel Timing

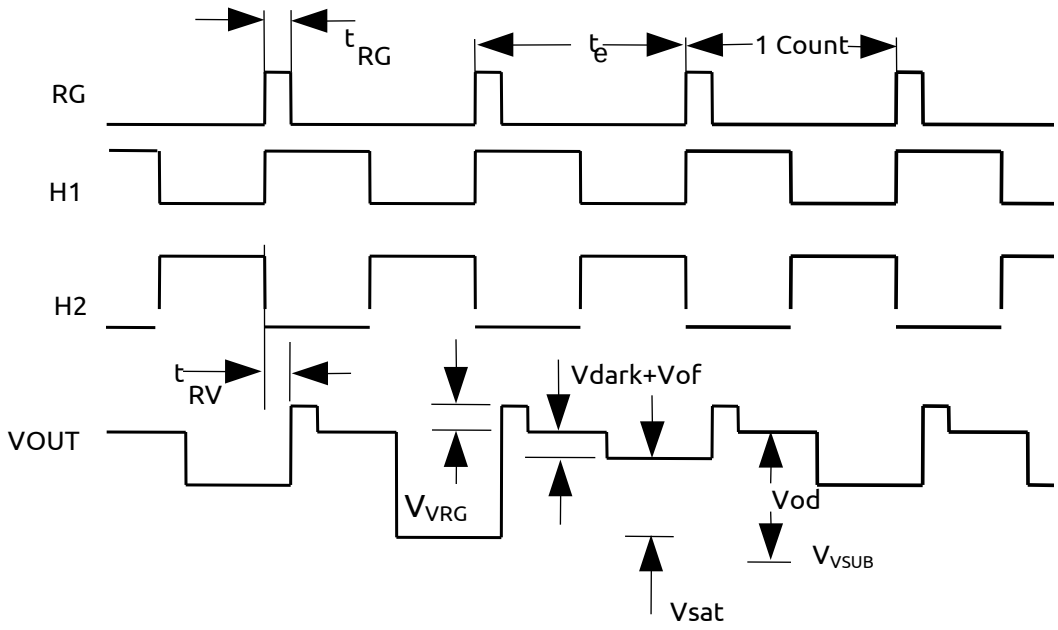

Figure 14: Pixel Timing

Pixel Timing Detail

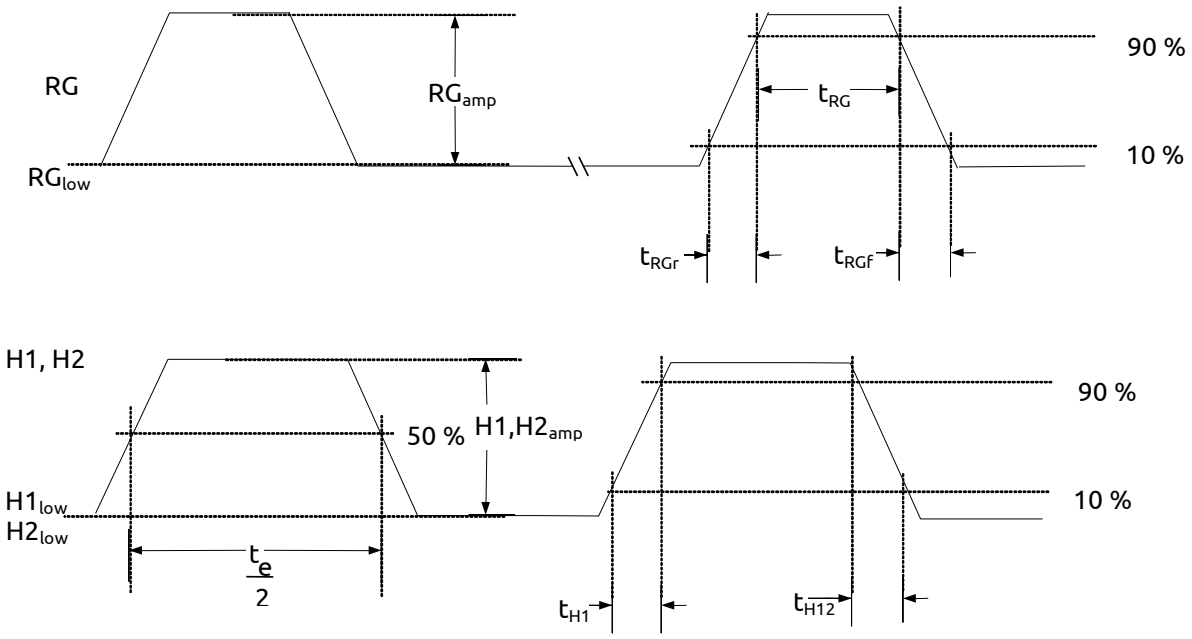

Figure 15: Pixel Timing Detail

EXAMPLE WAVEFORMS

Video Waveform Horizontal CCD Clocks

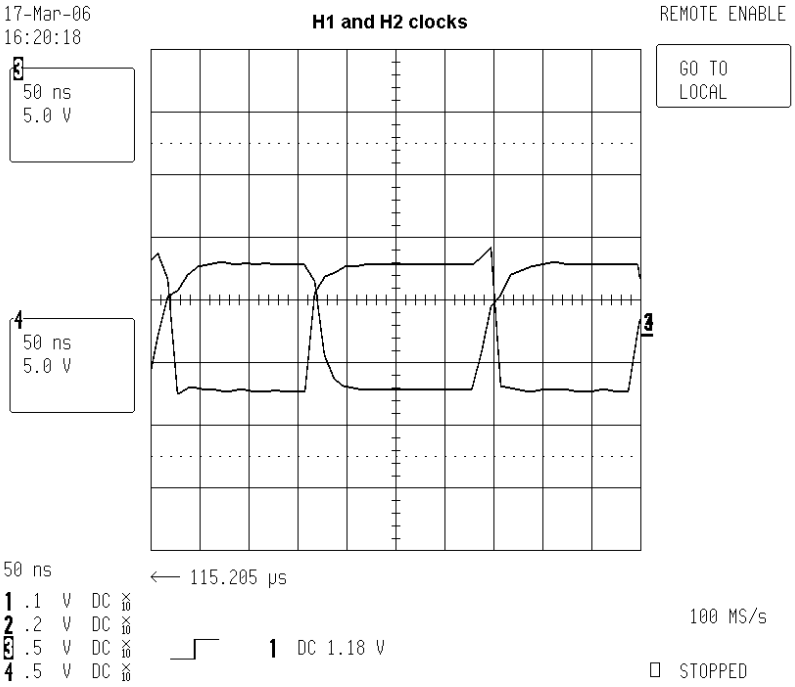

Figure 16: Horizontal Clock Waveform

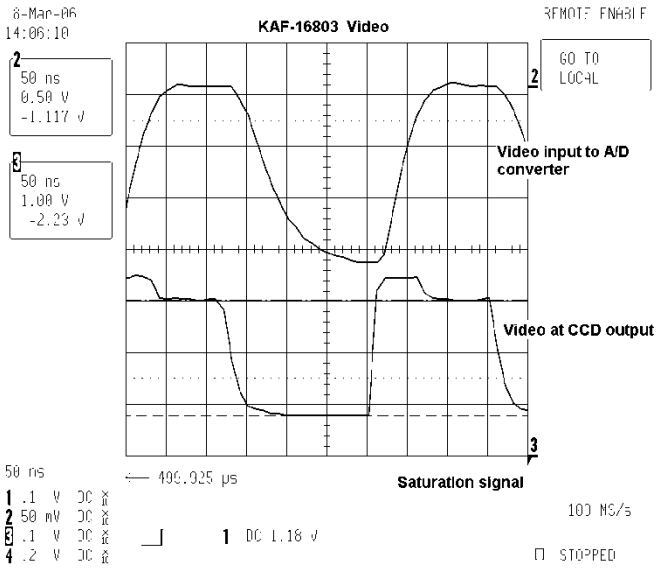

Figure 17: Video Waveform

Note:

Video Waveform – The bottom curve was taken at the CCD output. The top curve is bandwidth limited and was measured at the analog to digital converter.

Video Waveform and Clamp Clock

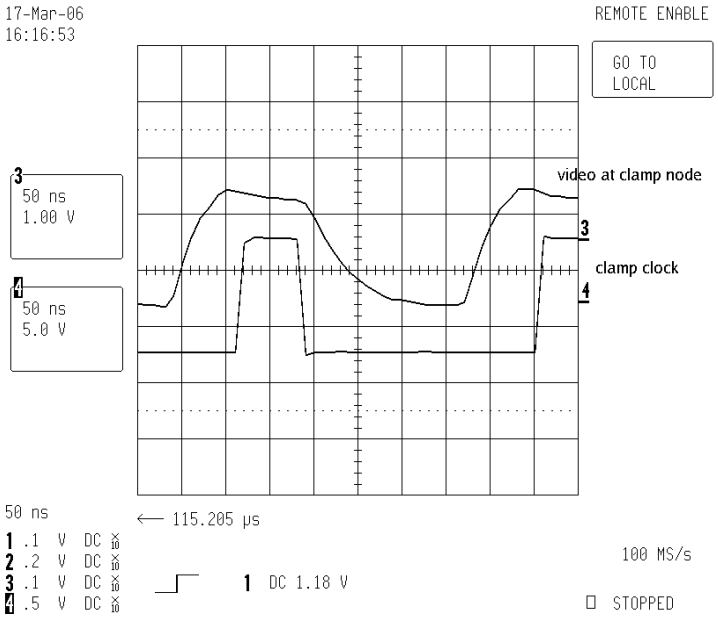

Figure 18: Video and Clamp

Video Waveform and Sample Clock

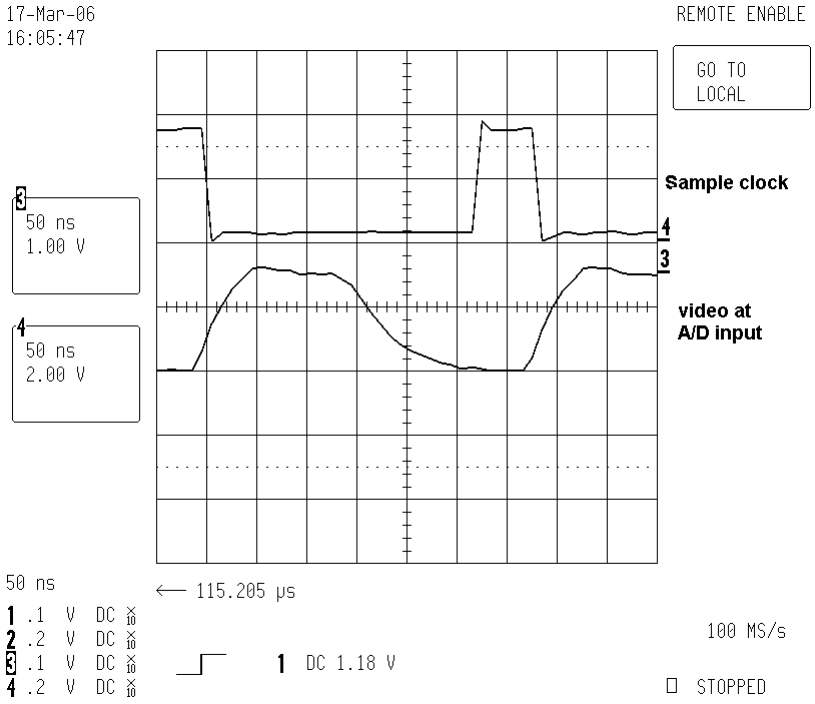

Figure 19: Video and Sample Clock

Storage and Handling

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-20	70	°C	1

Notes:
1. Long-term storage toward the maximum temperature will accelerate color filter degradation. (This condition applies to color parts only.)
2. T = 25 °C. Excessive humidity will degrade MTTF.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250 V per JESD22 Human Body Model test), or Class A (<200 V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.

Mechanical Information

COMPLETED ASSEMBLY

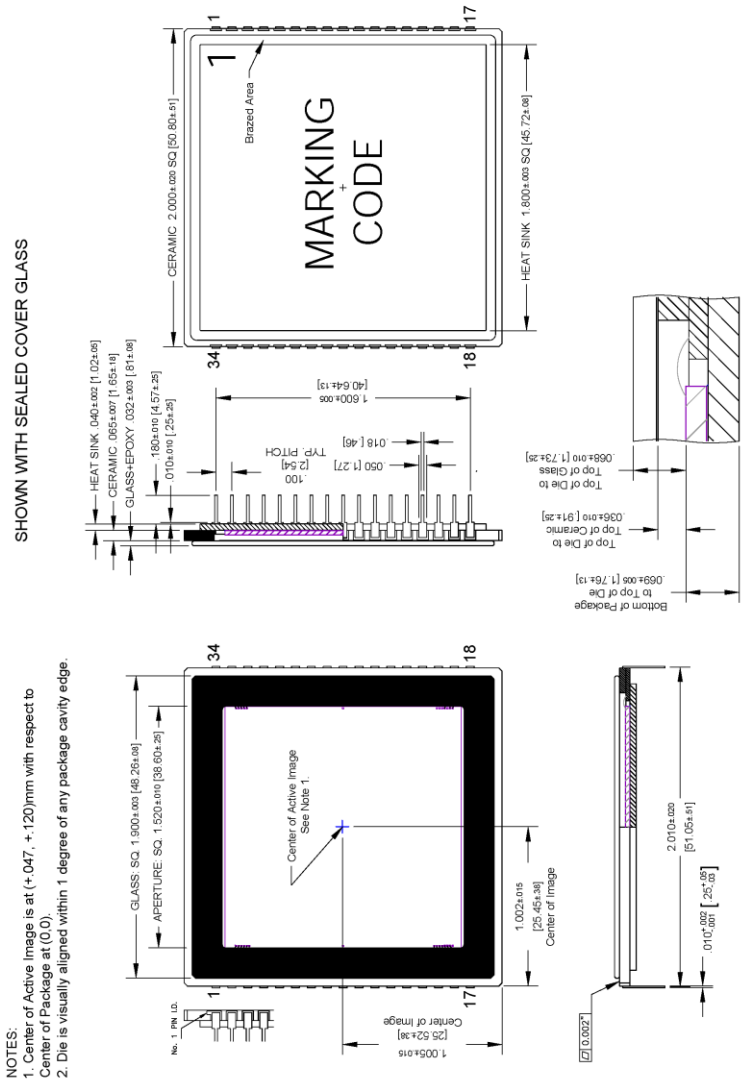

Figure 20: Completed Assembly Drawing (1 of 1)

COVER GLASS SPECIFICATION

1. Scratch and dig: 10 micron max
2. Substrate material Schott D263T eco or equivalent
3. Multilayer anti-reflective coating

Wavelength	Total Reflectance
420-450	≤ 2%
450-630	≤ 1%
630-680	≤ 2%

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

Revision Changes

MTD/PS-0994

Revision Number	Description of Changes
1.0	• Initial Release.
2.0	• P. 18 Changed Reset Drain Maximum to 13.625V
2.1	• P. 15 Updated Noise Floor Chart
3.0	• P. 5 Removed obsolete part numbers 4H0862 and 4H0864 and added new parts numbers 4H2053 and 4H2054
3.1	• P. 29 Changed cover glass material to D263T eco or equivalent

PS-0040

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections
1.1	• Updated branding

PUBLICATION ORDERING INFORMATION

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