

Vishay Siliconix

0.25 Ω Low-Voltage Dual SPDT Analog Switch

DESCRIPTION

The DG3535, DG3536 is a sub 1 Ω (0.25 Ω at 2.7 V) dual SPDT analog switches designed for low voltage applications.

The DG3535, DG3536 has on-resistance matching (less than 0.05 Ω at 2.7 V) and flatness (less than 0.2 Ω at 2.7 V) that are guaranteed over the entire voltage range. Additionally, low logic thresholds makes the DG3535, DG3536 an ideal interface to low voltage DSP control signals.

The DG3535, DG3536 has fast switching speed with break-before-make guaranteed. In the On condition, all switching elements conduct equally in both directions. Off-isolation and crosstalk is - 69 dB at 100 kHz.

The DG3535, DG3536 is built on Vishay Siliconix's high- density low voltage CMOS process. An eptiaxial layer is built in to prevent latchup. The DG3535, DG3536 contains the additional benefit of 2000 V ESD protection.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For MICRO FOOT analog switching products manufactured with tin/silver/copper (SnAgCu) device terminations, (Pb)-free "-E1" suffix is being used as a designator.

FEATURES

- Low voltage operation
- Low on-resistance R_{ON} : 0.25 Ω at 2.7 V
- 69 dB OIRR at 2.7 V, 100 kHz
- MICRO FOOT® package
- ESD protection > 2000 V
- Compliant to RoHS Directive 2002/95/EC

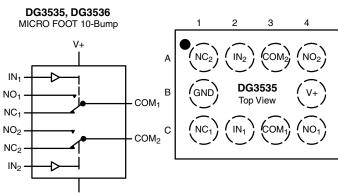
BENEFITS

- Reduced power consumption
- High accuracy
- Reduce board space
- 1.6 V logic compatible
- High bandwidth

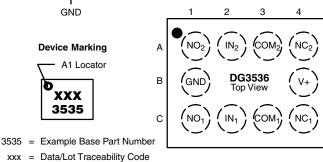
APPLICATIONS

- · Cellular phones
- Speaker headset switching
- Audio and video signal routing
- PCMCIA cards
- Battery operated systems
- Relay replacement

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE					
Logic	NC1 and NC2	NO1 and NO2			
0	ON	OFF			
1	OFF	ON			



ORDERING INFORMATION					
Temp. Range Package Part Number					
	MICRO FOOT: 10 Bump	DG3535DB-T5-E1			
- 40 °C to 85 °C	, ,	DG3535DB-T1-E1			
	238 μm Bump Height)	DG3536DB-T5-E1			

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ABSOLUTE MAXIMUM RATINGS						
Parameter	Limit	Unit				
Reference V+ to GND	- 0.3 to + 6					
IN, COM, NC, NO ^a		- 0.3 to (V+ + 0.3 V)	V			
Continuous Current (NO, NC, COM)	± 300	mA				
Peak Current (Pulsed at 1 ms, 10 % duty	± 500	IIIA				
Storage Temperature	(D Suffix)	- 65 to 150	90			
Package Solder Reflow Conditions ^b	IR/Convection	250 °C				
ESD per Method 3015.7	·	> 2	kV			
Power Dissipation (Packages) ^c	MICRO FOOT: 10 Bump (4 x 3 mm) ^d	457	mW			

Notes:

- a Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b Refer to IPC/JEDEC (J-STD-020B)
- c All bumps welded or soldered to PC board.
- d Derate 5.7 mW/°C above 70 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 3 V)							
		Test Conditions Otherwise Unless Specified		Limits - 40 °C to 85 °C			
Parameter	Symbol	$V+ = 3 V, \pm 10 \%, V_{IN} = 0.5 V \text{ or } 1.4 V^{e}$	Temp.a	Min.b	Typ.c	Max.b	Unit
Analog Switch							
Analog Signal Range ^d	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	٧
On-Resistance ^d	R _{ON}		Room Full		0.25	0.4 0.5	
R _{ON} Flatness ^d	R _{ON} Flatness	$V+ = 2.7 \text{ V}, V_{COM} = 0.6/1.5 \text{ V}$ $I_{NO}, I_{NC} = 100 \text{ mA}$				0.15	Ω
On-Resistance Match Between Channels ^d	$\Delta R_{DS(on)}$		Room			0.05	
Switch Off Leakage Current	I _{NO(off)}	V+ = 3.3 V,	Room Full	- 2 - 20		2 20	
	I _{COM(off)}	V_{NO} , $V_{NC} = 0.3 \text{ V/3 V}$, $V_{COM} = 3 \text{ V/0.3 V}$	Room Full	- 2 - 20		2 20	nA
Channel-On Leakage Current	I _{COM(on)}	$V+ = 3.3 \text{ V}, V_{NO}, V_{NC} = V_{COM} = 0.3 \text{ V/3 V}$	Room Full	- 2 - 20		2 20	
Digital Control							
Input High Voltage ^d	V _{INH}		Full	1.4			V
Input Low Voltage	V _{INL}		Full			0.5	v
Input Capacitance	C _{in}		Full		10		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	1		1	μΑ



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SPECIFICATIONS (V+ = 3 V)							
		Test Conditions Otherwise Unless Specified		Limits - 40 °C to 85 °C			
Parameter	Symbol	$V+ = 3 V$, $\pm 10 \%$, $V_{IN} = 0.5 V$ or 1.4 V^e	Temp.a	Min. ^b	Typ.c	Max.b	Unit
Dynamic Characteristics							
Turn-On Time	t _{ON}	V_{NO} or V_{NC} = 2 V, R_L = 50 Ω , C_L = 35 pF	Room Full		52	82 90	
Turn-Off Time	t _{OFF}		Room Full		43	73 78	ns
Break-Before-Make Time	t _d		Room	1	6		
Charge Injection ^d	Q _{INJ}	$C_L = 1 \text{ nF, } V_{GEN} = 1.5 \text{ V, } R_{GEN} = 0 \Omega$	Full		21		рC
Off-Isolation ^d	OIRR	D 5000 5 55 100 MI	Room		- 69		dB
Crosstalk ^d	X _{TALK}	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 100 kHz$	Room		- 69		uБ
N _O , N _C Off Capacitance ^d	C _{NO(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		145		
N _O , N _C On Capacitance	C _{NC(off)}		Room		145		nE
O. 100 d	C _{NO(on)}		Room		406		pF
Channel-On Capacitance ^d	C _{NC(on)}		Room		406		
Power Supply							
Power Supply Current	I+	V _{IN} = 0 or V+	Room Full		0.001	1 1	μΑ

Notes:

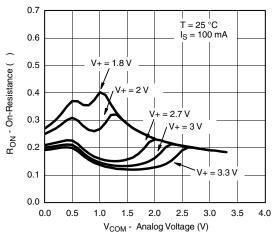
- a. Room = 25 $^{\circ}$ C, full = as determined by the operating suffix.
- b. Typical values are for design aid only, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Guarantee by design, nor subjected to production test.
- e. V_{IN} = input voltage to perform proper function.

0.8

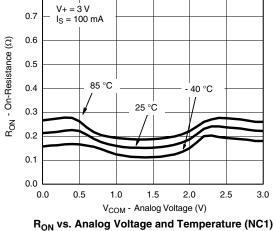
DG3535, DG3536

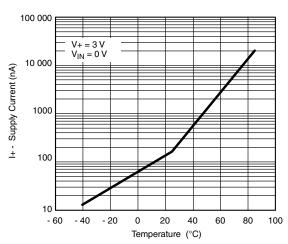
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

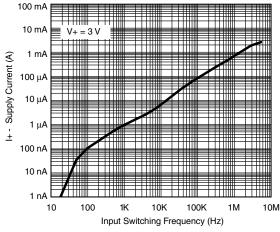


 R_{ON} vs. V_{COM} and Supply Voltage

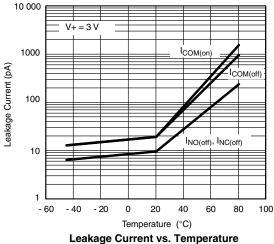


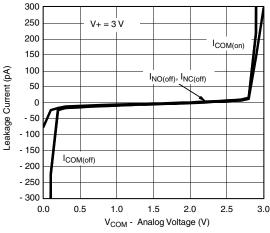


Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency



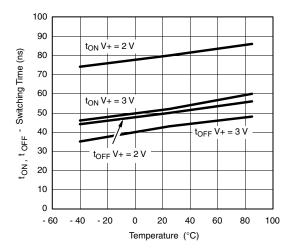


Leakage vs. Analog Voltage

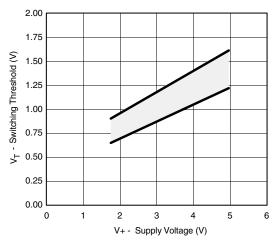


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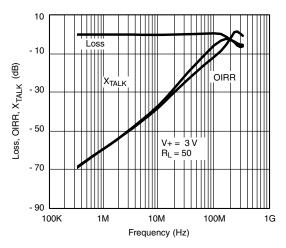
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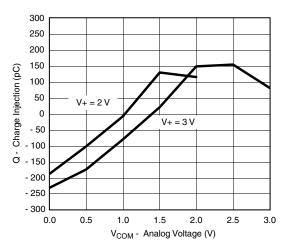
Switching Time vs. Temperature



Switching Threshold vs. Supply Voltage



Insertion Loss, Off-Isolation Crosstalk vs. Frequency

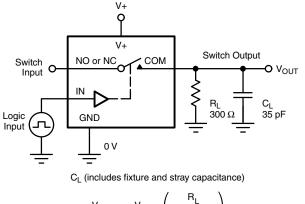


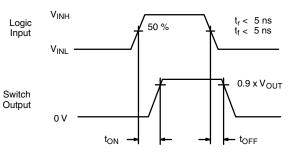
Charge Injection vs. Analog Voltage

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TEST CIRCUITS







Logic "1" = Switch On Logic input waveforms inverted for switches that have the opposite logic sense.

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$

Figure 1. Switching Time

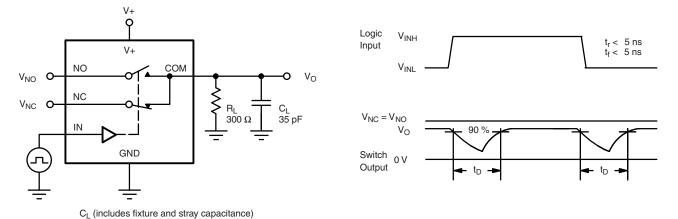
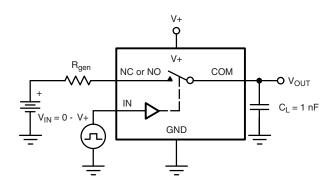
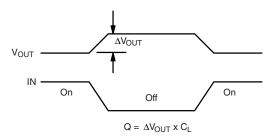


Figure 2. Break-Before-Make Interval





IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

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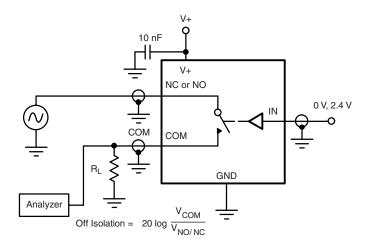


Figure 4. Off-Isolation

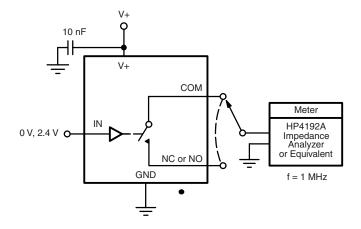


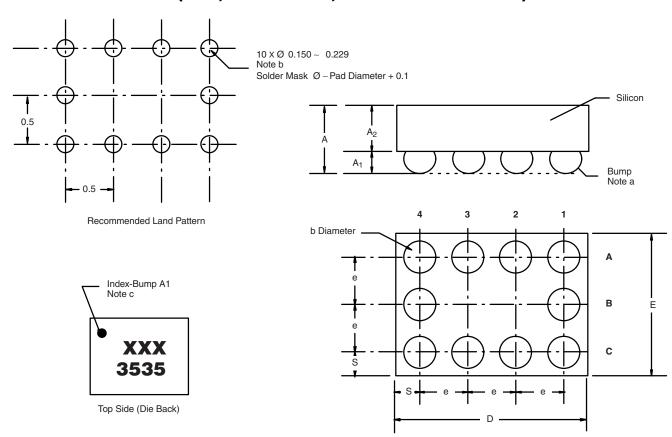
Figure 5. Channel Off/On Capacitance

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PACKAGE OUTLINE



MICRO FOOT: 10 BUMP (4 x 3, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)



Notes (Unless Otherwise Specified):

- a. Bump is Lead Free Sn/Ag/Cu.
- b. Non-solder mask defined copper landing pad.
- c. Laser Mark on silicon die back; back-lapped, no coating. Shown is not actual marking; sample only.

	Millimeters ^a		Inc	hes
Dim.	Min.	Max.	Min.	Max.
Α	0.688	0.753	0.0271	0.0296
A ₁	0.218	0.258	0.0086	0.0102
A ₂	0.470	0.495	0.0185	0.0195
b	0.306	0.346	0.0120	0.0136
D	1.980	2.020	0.0780	0.0795
E	1.480	1.520	0.0583	0.0598
е	0.5 BASIC 0.0197 BASIC		BASIC	
S	0.230	0.270	0.0091	0.0106

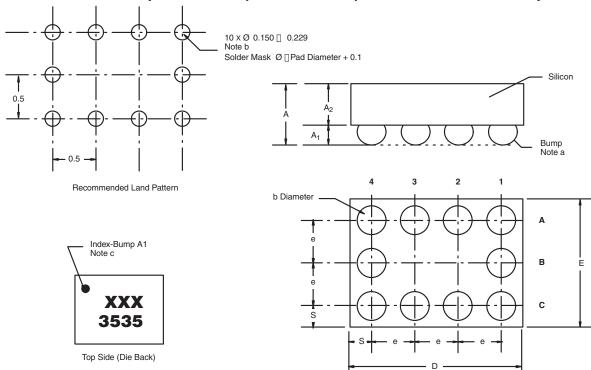
Notes:

a. Use millimeters as the primary measurement.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72961.



MICRO FOOT: 10-BUMP (4 mm x 3 mm, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)



Notes

(unless otherwise specified)

- a. Bump is lead (Pb)-free Sn/Ag/Cu.
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