FAIRCHILD
SEMICONDUCTOR®

November 2013

FCP9N60N / FCPF9N60NT

N-Channel SupreMOS® MOSFET

600 V, 9 A, 385 mΩ

Features

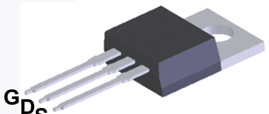
- $R_{DS(on)}$ = 330 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 4.5 A
- Ultra Low Gate Charge (Typ. Q_g = 22 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 106 pF)
- 100% Avalanche Tested
- RoHS Compliant

Application

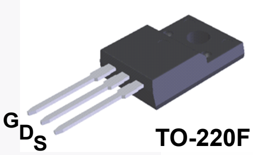
- LCD/LED/PDP TV
- Lighting
- Solar Inverter
- AC-DC Power Supply

Description

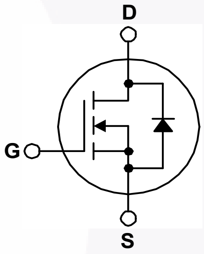
The SupreMOS® MOSFET is Fairchild Semiconductor's next generation of high voltage super-junction (SJ) technology employing a deep trench filling process that differentiates it from the conventional SJ MOSFETs. This advanced technology and precise process control provides lowest Rsp on-resistance, superior switching performance and ruggedness. SupreMOS MOSFET is suitable for high frequency switching power converter applications such as PFC, server/telecom power, FPD TV power, ATX power, and industrial power applications.



TO-220



TO-220F



Absolute Maximum Ratings $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter		FCP9N60N	FCPF9N60NT	Unit
V_{DSS}	Drain to Source Voltage		600		V
V_{GSS}	Gate to Source Voltage		±30		V
I_D	Drain Current	- Continuous ($T_C = 25^oC$)	9.0	9.0*	A
		- Continuous ($T_C = 100^oC$)	5.7	5.7*	
I_{DM}	Drain Current	- Pulsed (Note 1)	27	27*	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	135		mJ
I_{AR}	Avalanche Current	(Note 1)	3		A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	0.83		mJ
dv/dt	MOSFET dv/dt		100		V/ns
	Peak Diode Recovery dv/dt	(Note 3)	20		V/ns
P_D	Power Dissipation	($T_C = 25^oC$)	83.3	29.8	W
		- Derate Above 25°C	0.67	0.24	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300		°C

*Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FCP9N60N	FCPF9N60NT	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.5	4.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP9N60N	FCP9N60N	TO-220	Tube	N/A	N/A	50 units
FCPF9N60NT	FCPF9N60NT	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

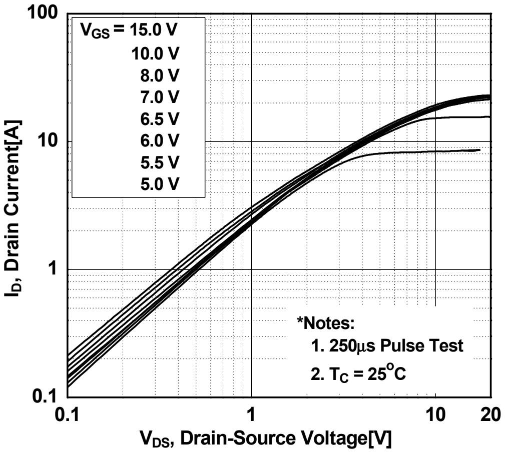
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V, T_C = 25^{o}C	600	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25^{o}C	-	0.72	-	V/^{o}C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 480 V, V_{GS} = 0 V	-	-	10	µA
		V_{DS} = 480 V, V_{GS} = 0 V, T_C = 125^{o}C	-	-	100	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 4.5 A	-	0.33	0.385	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 4.5 A	-	7.5	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	-	930	1240	pF
C_{oss}	Output Capacitance		-	35	50	pF
C_{rss}	Reverse Transfer Capacitance		-	2	4	pF
C_{oss}	Output Capacitance	V_{DS} = 380 V, V_{GS} = 0 V, f = 1 MHz	-	20	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	106	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 380 V, I_D = 4.5 A, V_{GS} = 10 V (Note 4)	-	22.0	29	nC
Q_{gs}	Gate to Source Gate Charge		-	4.1	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	7.1	-	nC
ESR	Equivalent Series Resistance (G-S)	f = 1 MHz		2.9		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 380 V, I_D = 4.5 A, V_{GS} = 10 V, R_G = 4.7 Ω (Note 4)	-	12.7	35.4	ns
t_r	Turn-On Rise Time		-	8.7	27.4	ns
$t_{d(off)}$	Turn-Off Delay Time		-	36.9	83.8	ns
t_f	Turn-Off Fall Time		-	10.2	30.4	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	9.0	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	27	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 4.5 A	-	-	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 4.5 A, dI_F/dt = 100 A/µs	-	213	-	ns
Q_{rr}	Reverse Recovery Charge		-	2.2	-	µC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 3 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 9 A, di/dt ≤ 200 A/µs, V_{DD} = 380 V, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

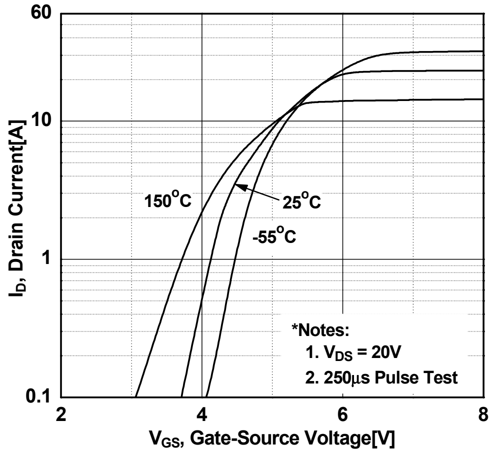
Typical Performance Characteristics

Figure 1. On-Region Characteristics



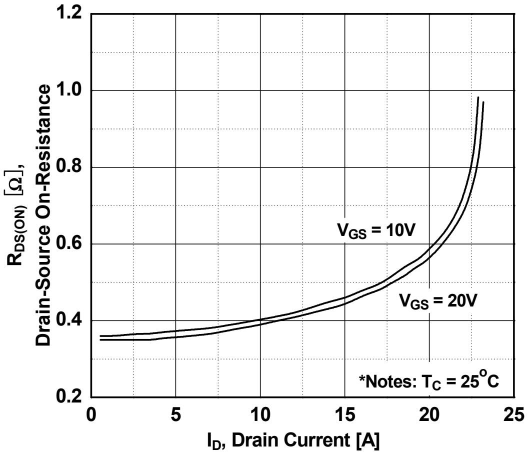
*Notes:
1. 250μs Pulse Test
2. T_C = 25°C

Figure 2. Transfer Characteristics



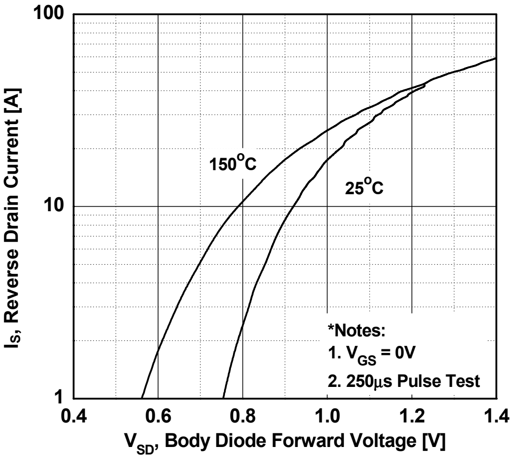
*Notes:
1. V_{DS} = 20V
2. 250μs Pulse Test

Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage



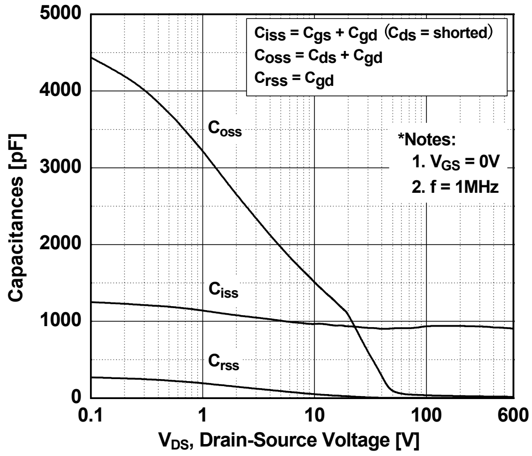
*Notes: T_C = 25°C

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



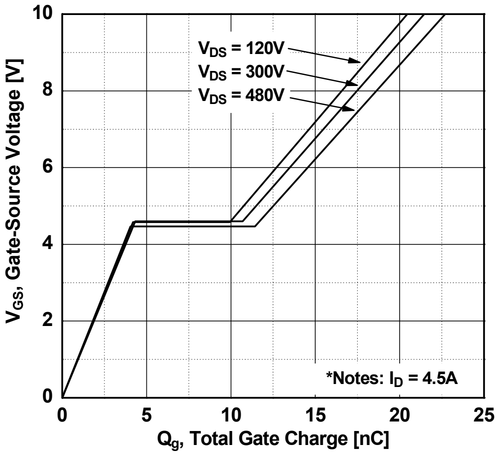
*Notes:
1. V_{GS} = 0V
2. 250μs Pulse Test

Figure 5. Capacitance Characteristics



*Notes:
1. V_{GS} = 0V
2. f = 1MHz

Figure 6. Gate Charge Characteristics



*Notes: I_D = 4.5A

Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

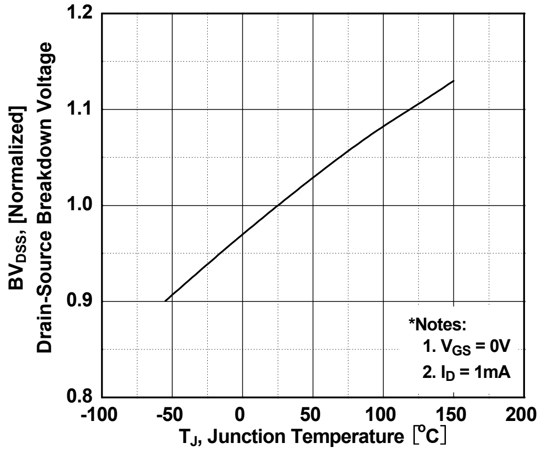


Figure 8. On-Resistance Variation vs. Temperature

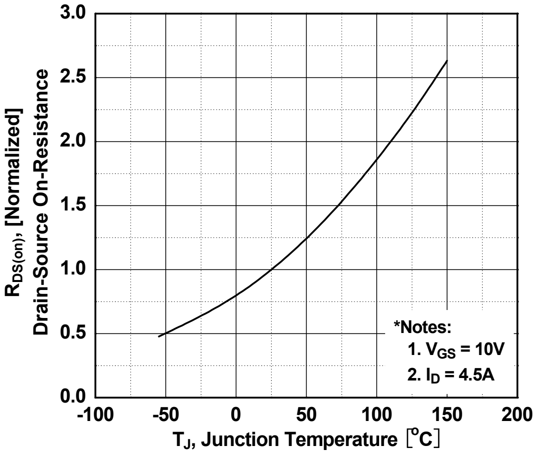


Figure 9. Maximum Safe Operating Area for FCPF9N60N

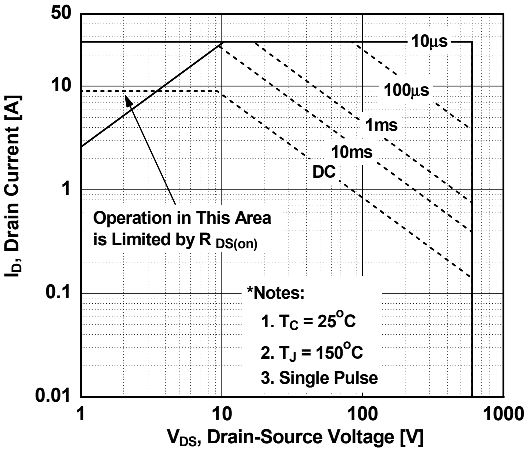


Figure 10. Maximum Safe Operating Area for FCPF9N60NT

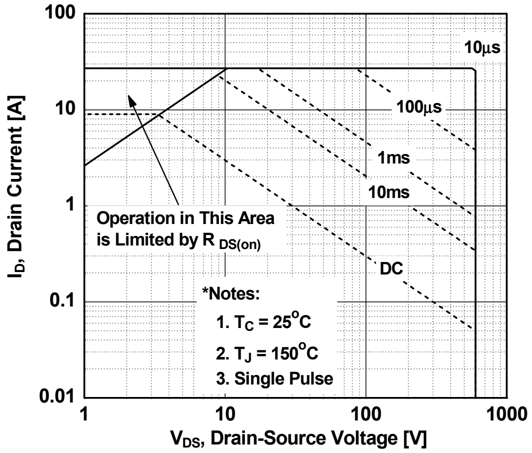
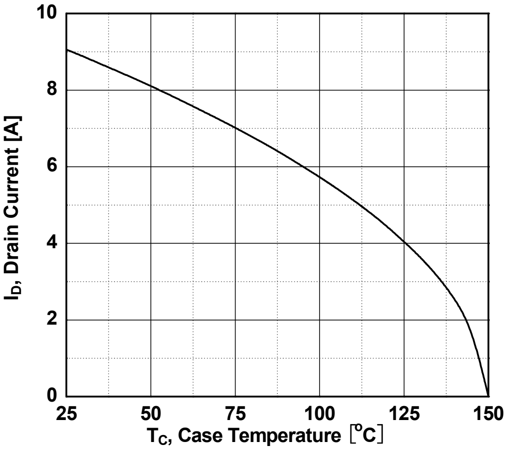
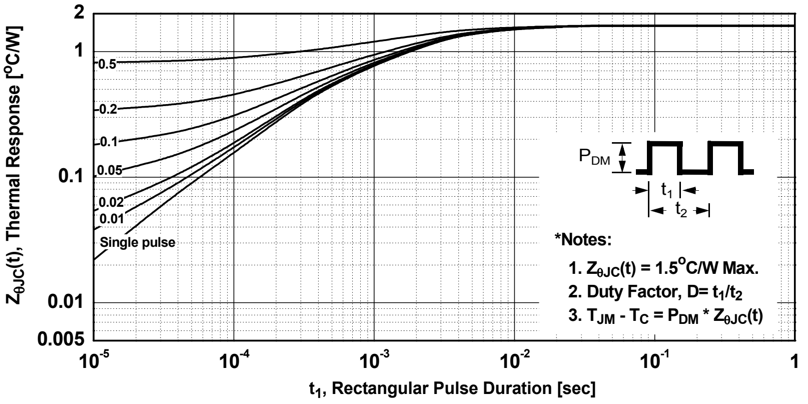


Figure 11. Maximum Drain Current vs. Case Temperature



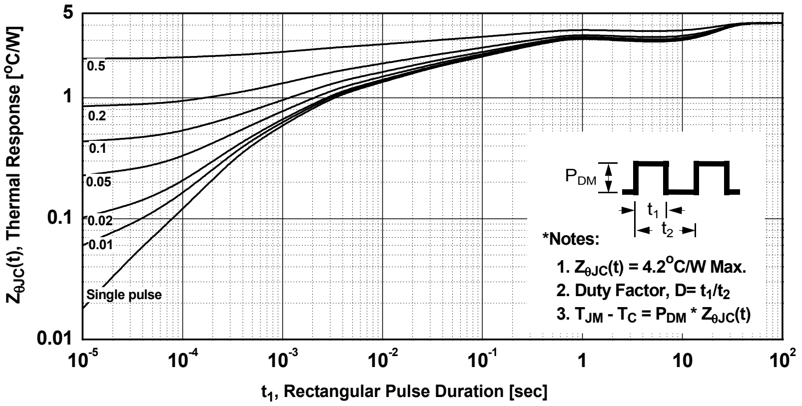
Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve for FCP9N60N



*Notes:
1. $Z_{\theta JC}(t) = 1.5°C/W$ Max.
2. Duty Factor, $D = t_1/t_2$
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$

Figure 13. Transient Thermal Response Curve for FCPF9N60NT



*Notes:
1. $Z_{\theta JC}(t) = 4.2°C/W$ Max.
2. Duty Factor, $D = t_1/t_2$
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$

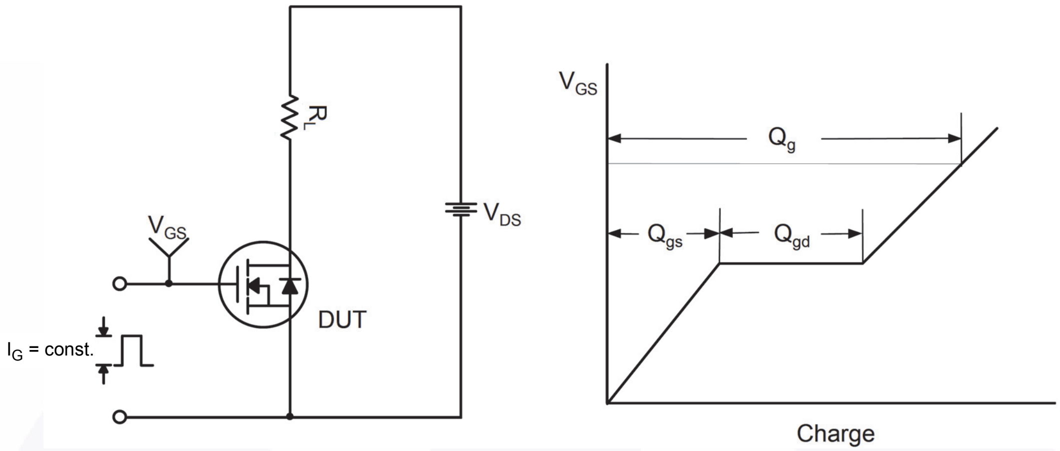


Figure 14. Gate Charge Test Circuit & Waveform

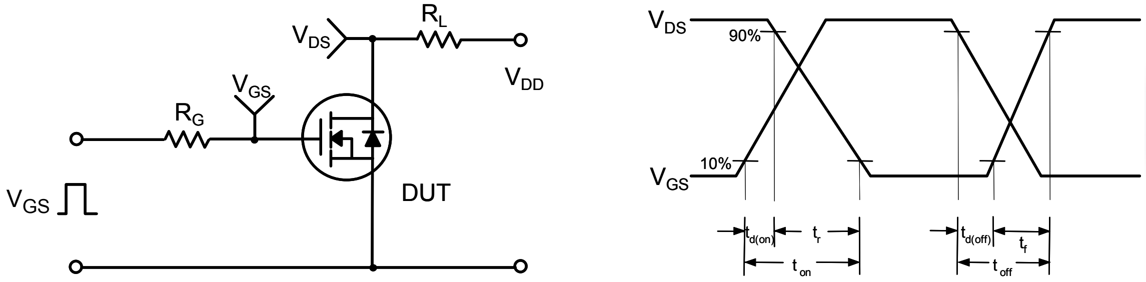


Figure 15. Resistive Switching Test Circuit & Waveforms

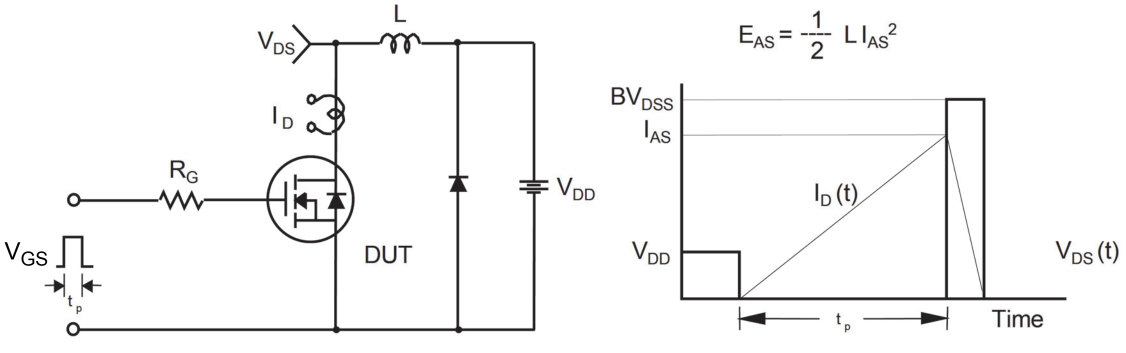


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

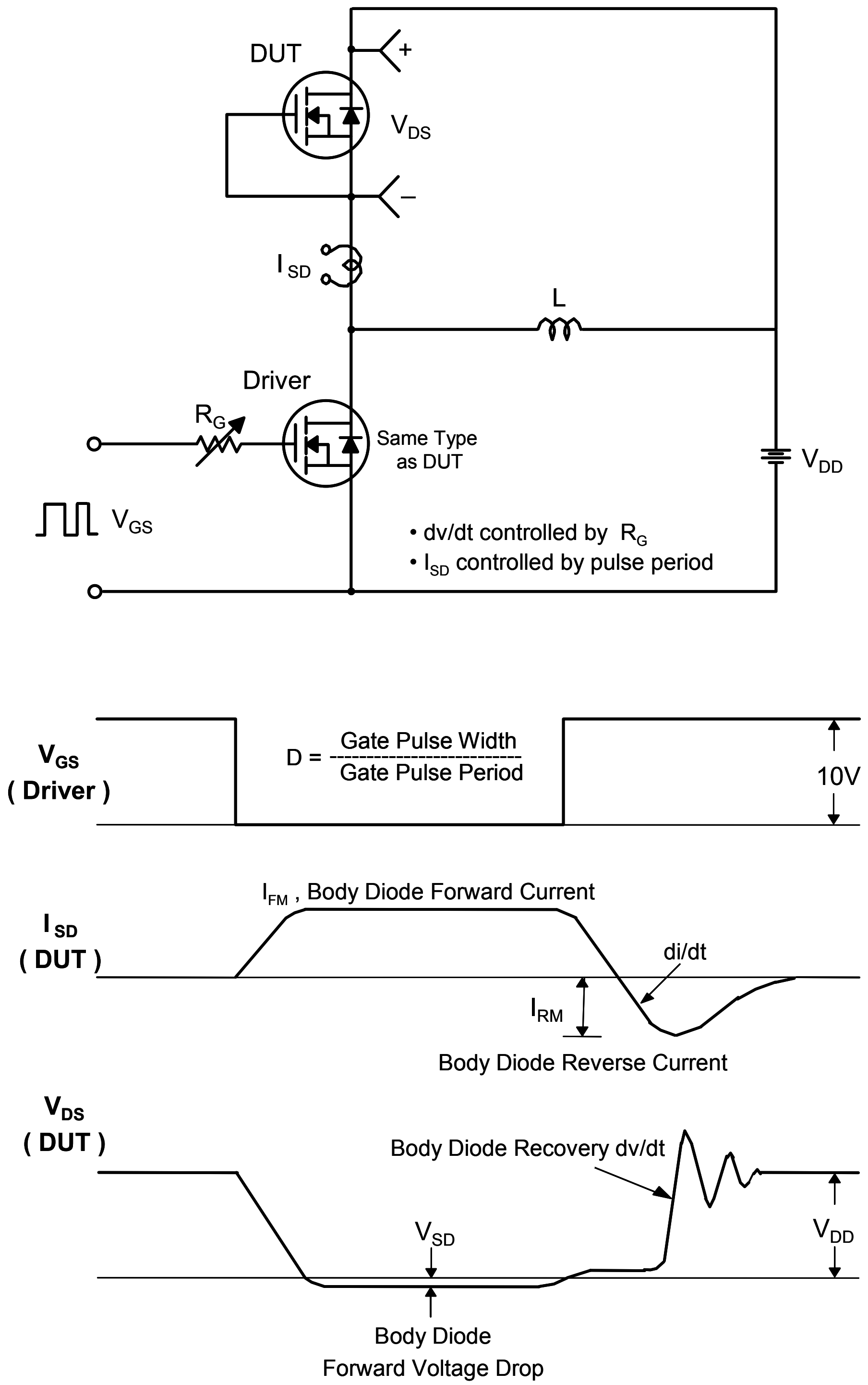
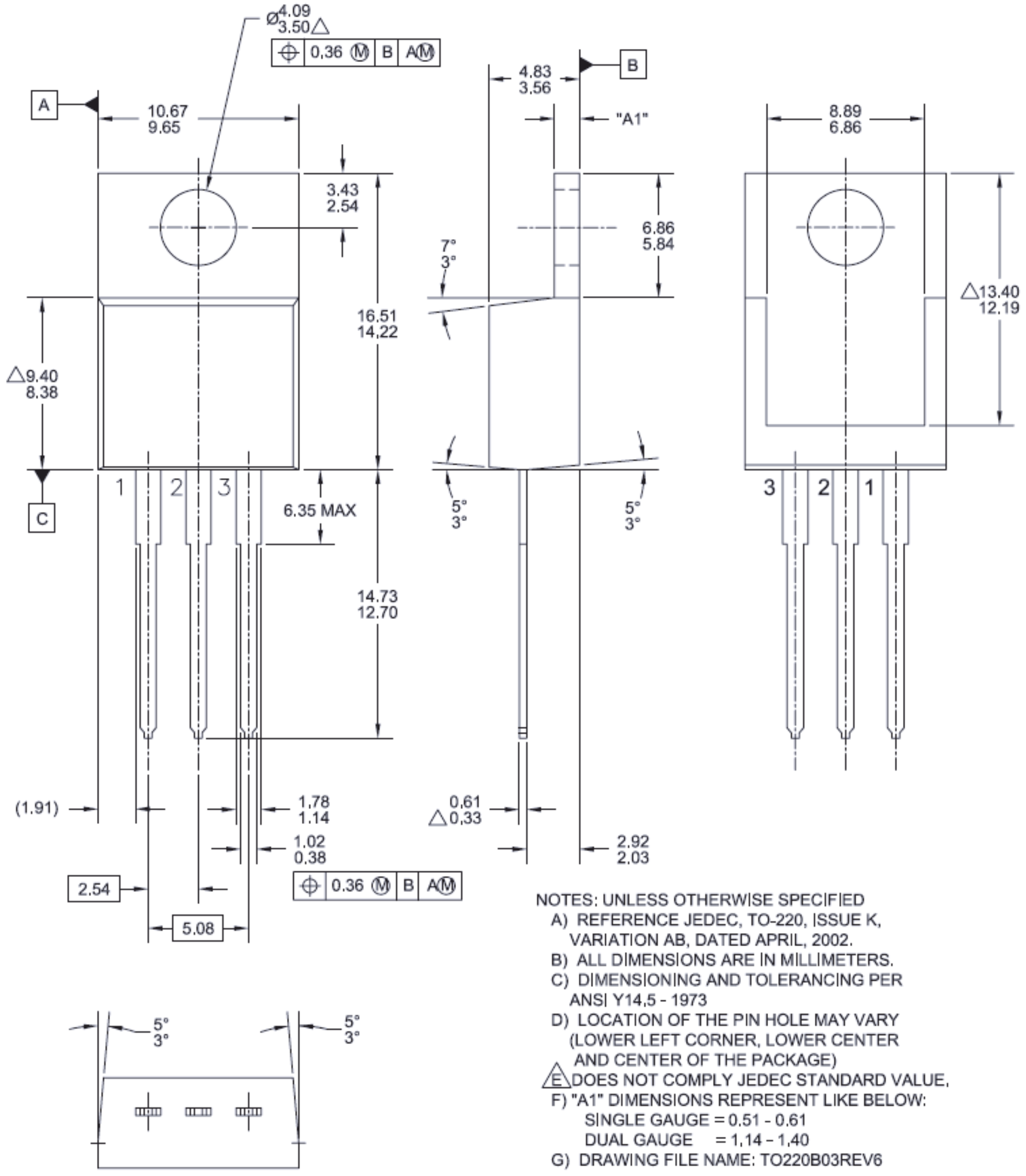


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1973

D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)

E) DOES NOT COMPLY JEDEC STANDARD VALUE.

F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.14 - 1.40

G) DRAWING FILE NAME: TO220B03REV6

Figure 18. TO-220, Molded, 3-Lead, Jedec Variation AB

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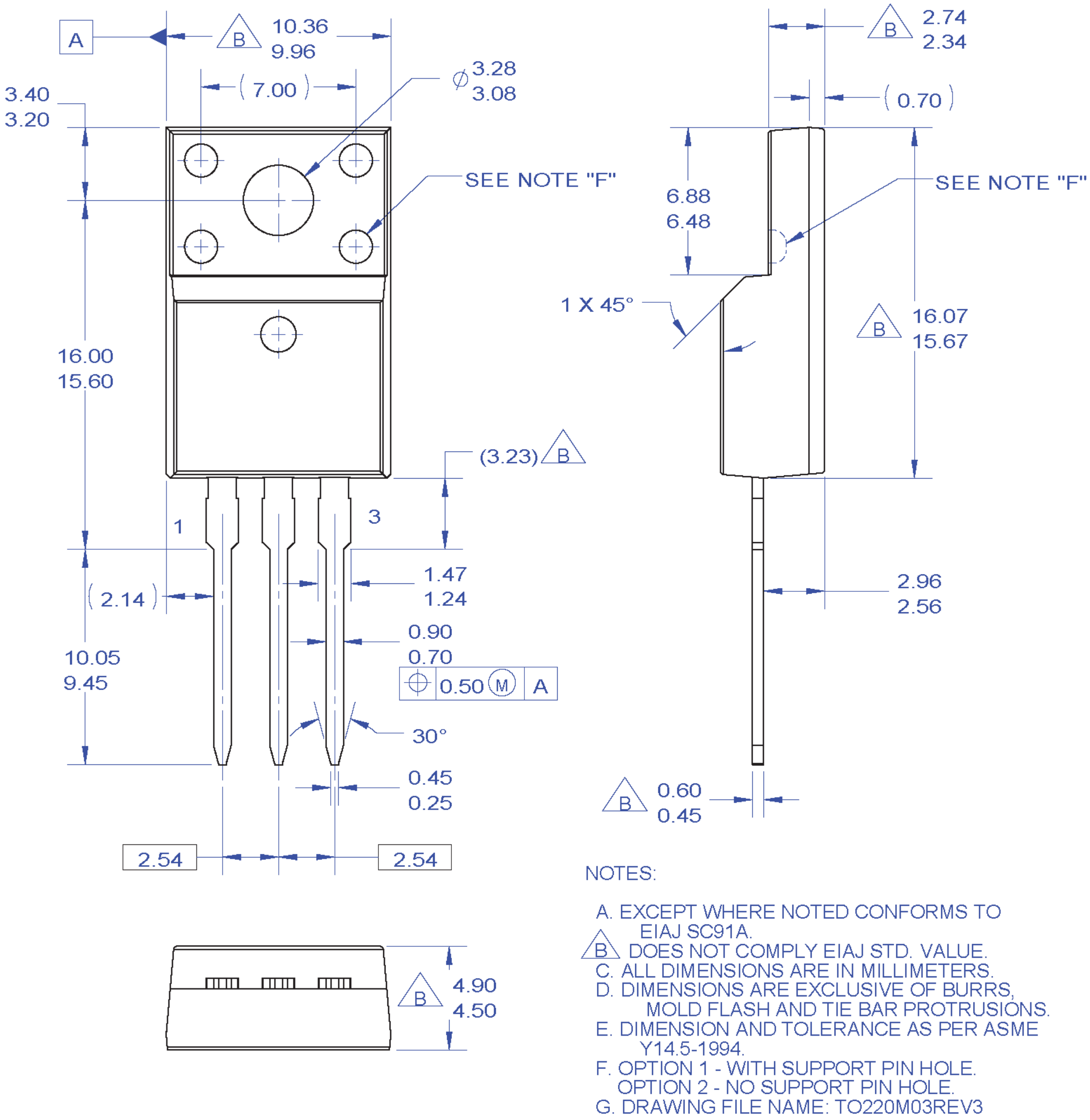
Mechanical Dimensions



NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.

B DOES NOT COMPLY EIAJ STD. VALUE.

C. ALL DIMENSIONS ARE IN MILLIMETERS.

D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.

F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.

G. DRAWING FILE NAME: TO220M03REV3

Figure 19. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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