SHARC Processor

ADSP-21161N

SUMMARY

High performance 32-Bit DSP—applications in audio, medical, military, wireless communications, graphics, imaging, motor-control, and telephony

Super Harvard Architecture—four independent buses for dual data fetch, instruction fetch, and nonintrusive zero-overhead I/O

Code compatible with all other sharc family DSPs

Single-instruction multiple-data (SIMD) computational architecture—two 32-bit IEEE floating-point computation units, each with a multiplier, ALU, shifter, and register file

Serial ports offer I^2S support via 8 programmable and simultaneous receive or transmit pins, which support up to 16 transmit or 16 receive channels of audio

Integrated peripherals—integrated I/O processor, 1M bit on-chip dual-ported SRAM, SDRAM controller, glueless multiprocessing features, and I/O ports (serial, link, external bus, SPI, and JTAG)

ADSP-21161N supports 32-bit fixed, 32-bit float, and 40-bit floating-point formats

100 MHz/110 MHz core instruction rate

Single-cycle instruction execution, including SIMD operations in both computational units

Up to 660 MFLOPs peak and 440 MFLOPs sustained performance

225-ball 17 mm × 17 mm CSP_BGA package

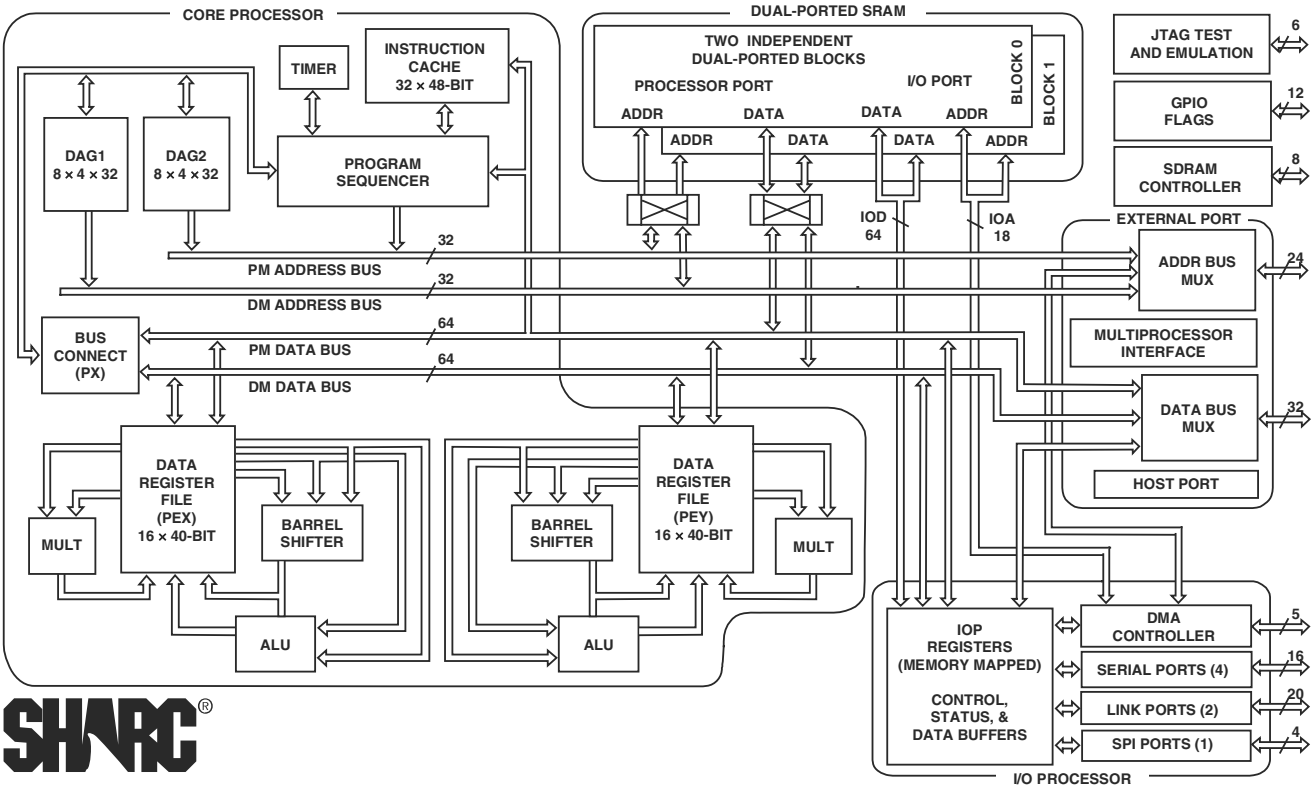

Figure 1. ADSP-21161N Functional Block Diagram

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Rev. C **Document Feedback**

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REVISION HISTORY

1/13—Rev. B to Rev. C

Updated Development Tools 9

Added section, Related Signal Chains 10

Added footnote 3 to Table 16 in
Memory Read — Bus Master 27

GENERAL DESCRIPTION

The ADSP-21161N SHARC® DSP is a low cost derivative of the ADSP-21160 featuring Analog Devices Super Harvard Architecture. Easing portability, the ADSP-21161N is source code compatible with the ADSP-21160 and with first generation ADSP-2106x SHARC processors in SISD (Single-Instruction, Single-Data) mode. Like other SHARC DSPs, the ADSP-21161N is a 32-bit processor that is optimized for high performance DSP applications. The ADSP-21161N includes a 100 MHz or 110 MHz core, a dual-ported on-chip SRAM, an integrated I/O processor with multiprocessing support, and multiple internal buses to eliminate I/O bottlenecks.

As was first offered in the ADSP-21160, the ADSP-21161N offers a single-instruction multiple-data (SIMD) architecture. Using two computational units (ADSP-2106x SHARC processors have one), the ADSP-21161N can double cycle performance versus the ADSP-2106x on a range of DSP algorithms.

Fabricated in a state of the art, high speed, low power CMOS process, the ADSP-21161N has a 10 ns or 9 ns instruction cycle time. With its SIMD computational hardware running at 110 MHz, the ADSP-21161N can perform 660 million floating-point operations per second. Table 1 shows performance benchmarks for the ADSP-21161N.

These benchmarks provide single-channel extrapolations of measured dual-channel processing performance. For more information on benchmarking and optimizing DSP code, for both single and dual-channel processing, see the Analog Devices Inc. website.

Table 1. Benchmarks

Benchmark Algorithm	100 MHz Instruction Rate	110 MHz Instruction Rate
1024 Point Complex FFT (Radix 4, with Reversal)	92 µs	83.6 µs
FIR Filter (Per Tap)	5 ns	4.5 ns
IIR Filter (Per Biquad)	20 ns	18.18 ns
Matrix Multiply (Pipelined)		
[3 × 3] × [3 × 1]	45 ns	40.9 ns
[4 × 4] × [4 × 1]	80 ns	72.72 ns
Divide (y/x)	60 ns	54.54 ns
Inverse Square Root	40 ns	36.36 ns
DMA Transfers	800M bytes/s	880M bytes/s

The ADSP-21161N continues SHARC's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features. These features include a 1M bit dual ported SRAM memory, host processor interface, I/O processor that supports 14 DMA channels, four serial ports, two link ports, SDRAM controller, SPI interface, external parallel bus, and glueless multiprocessing.

The block diagram of the ADSP-21161N on Page 1 illustrates the following architectural features:

- Two processing elements, each made up of an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core every core processor cycle
- Interval timer
- On-Chip SRAM (1M bit)
- SDRAM controller for glueless interface to SDRAMs
- External port that supports:
  - Interfacing to off-chip memory peripherals
  - Glueless multiprocessing support for six ADSP-21161N SHARCs
  - Host port read/write of IOP registers
- DMA controller
- Four serial ports
- Two link ports
- SPI compatible interface
- JTAG test access port
- 12 general-purpose I/O pins

Figure 2 shows a typical single-processor system. A multiprocessing system appears in Figure 5 on Page 8.

ADSP-21161N FAMILY CORE ARCHITECTURE

The ADSP-21161N includes the following architectural features of the ADSP-2116x family core. The ADSP-21161N is code compatible at the assembly level with the ADSP-21160, ADSP-21060, ADSP-21061, ADSP-21062, and ADSP-21065L.

SIMD Computational Engine

The ADSP-21161N contains two computational processing elements that operate as a single-instruction multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY, and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements.

When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

SIMD is supported only for internal memory accesses and is not supported for off-chip accesses.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform single-cycle instructions. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the SHARC enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-21161N features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 2). With the ADSP-21161N's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and an instruction (from the cache), all in a single cycle.

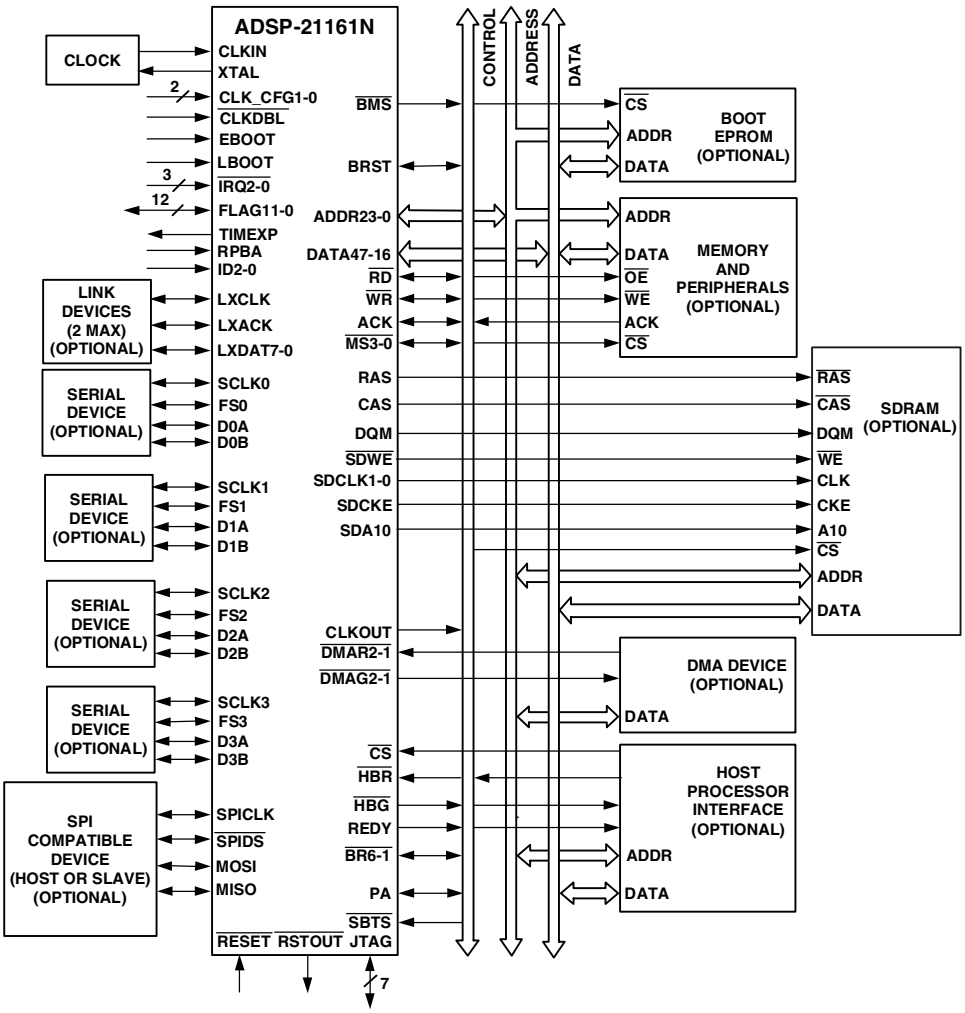


Figure 2. System Diagram

Instruction Cache

The ADSP-21161N includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache enables full-speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators With Hardware Circular Buffers

The ADSP-21161N's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-21161N contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wrap-around, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21161N can conditionally execute a multiply, an add, and a subtract in both processing elements, while branching, all in a single instruction.

ADSP-21161N MEMORY AND I/O INTERFACE FEATURES

The ADSP-21161N adds the following architectural features to the ADSP-2116x family core.

Dual-Ported On-Chip Memory

The ADSP-21161N contains one megabit of on-chip SRAM, organized as two blocks of 0.5M bits (Figure 3). Each block can be configured for different combinations of code and data storage. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor. The dual-ported memory in combination with three separate on-chip buses allow two data transfers from the core and one from the I/O processor, in a single cycle. On the ADSP-21161N, the memory can be configured as a maximum of 32K words of 32-bit data, 64K words of 16-bit data, 21K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to one megabit. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers. Using the DM bus and PM bus, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

Off-Chip Memory and Peripherals Interface

The ADSP-21161N's external port provides the processor's interface to off-chip memory and peripherals. The 62.7-M word off-chip address space (254.7-M word if all SDRAM) is included in the ADSP-21161N's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 24-bit address bus and a single 32-bit data bus. Every access to external memory is based on an address that fetches a 32-bit word. When fetching an instruction from external memory, two 32-bit data locations are being accessed for packed instructions. Unused link port lines can also be used as additional data lines DATA15–DATA0, allowing single-cycle execution of instructions from external memory, at up to 110 MHz. Figure 4 shows the alignment of various accesses to external memory.

The external port supports asynchronous, synchronous, and synchronous burst accesses. Synchronous burst SRAM can be interfaced gluelessly. The ADSP-21161N also can interface gluelessly to SDRAM. Addressing of external memory devices is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. The ADSP-21161N provides programmable memory wait states and external memory acknowledge controls to allow interfacing to memory and peripherals with variable access, hold, and disable time requirements.

SDRAM Interface

The SDRAM interface enables the ADSP-21161N to transfer data to and from synchronous DRAM (SDRAM) at the core clock frequency or at one-half the core clock frequency. The synchronous approach, coupled with the core clock frequency, supports data transfer at a high throughput—up to 440M bytes/s for 32-bit transfers and up to 660M bytes/s for 48-bit transfers.

The SDRAM interface provides a glueless interface with standard SDRAMs—16Mb, 64Mb, 128Mb, and 256Mb— and includes options to support additional buffers between the ADSP-21161N and SDRAM. The SDRAM interface is extremely flexible and provides capability for connecting SDRAMs to any one of the ADSP-21161N's four external memory banks, with up to all four banks mapped to SDRAM.

Systems with several SDRAM devices connected in parallel may require buffering to meet overall system timing requirements. The ADSP-21161N supports pipelining of the address and control signals to enable such buffering between itself and multiple SDRAM devices.

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-21161N processor to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of

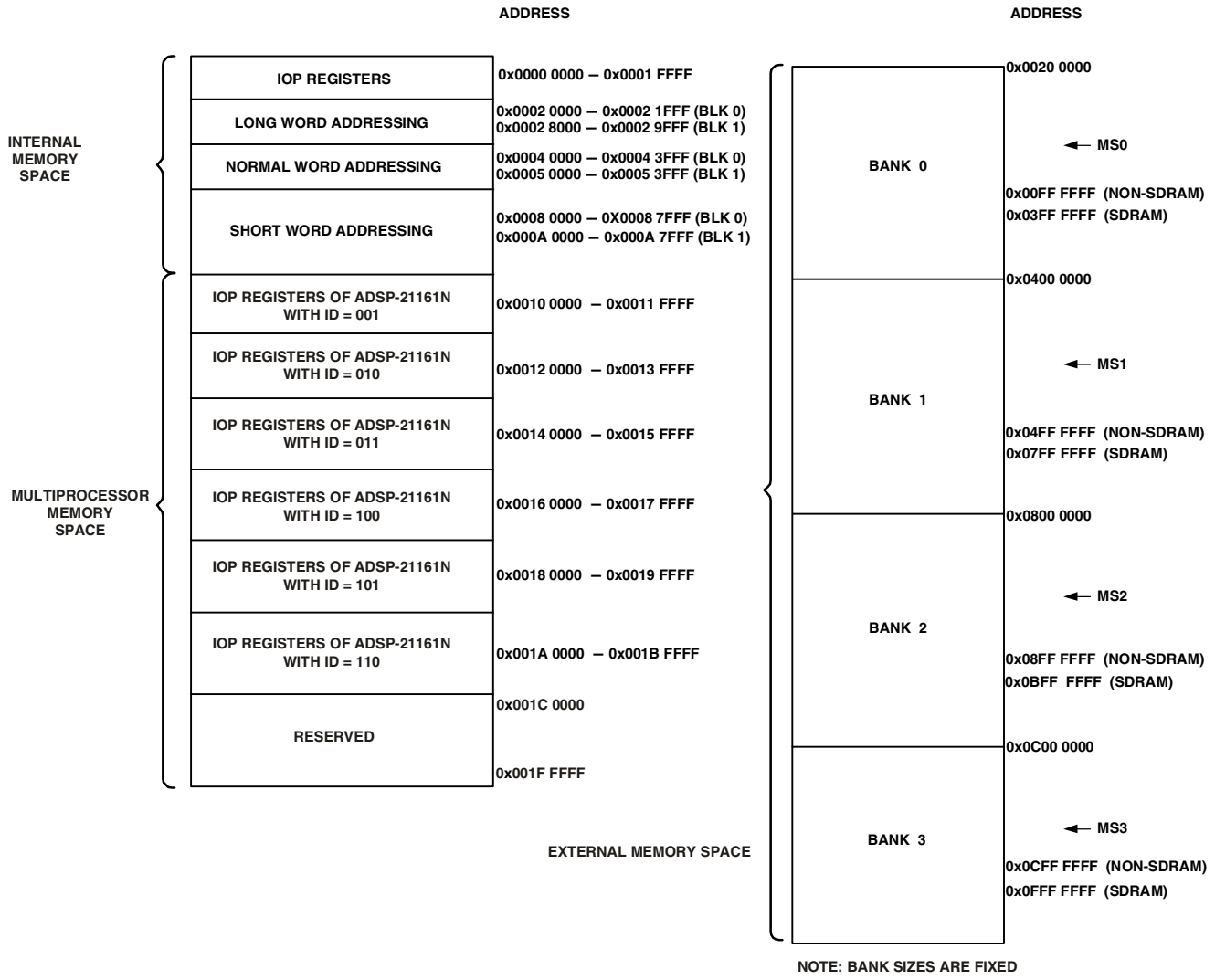


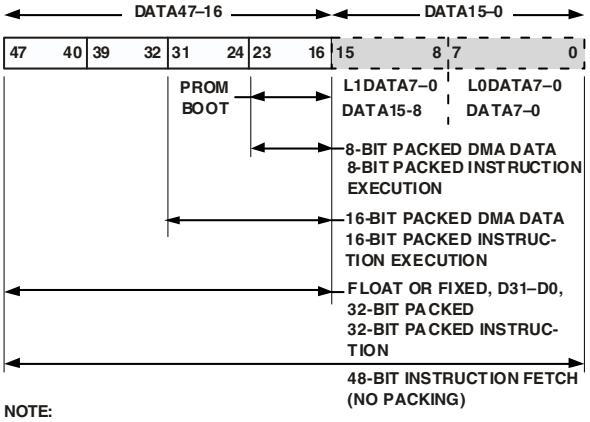
Figure 3. Memory Map

JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on SHARC Analog Devices DSP Tools product line of JTAG emulator operation, see the appropriate Emulator Hardware User's Guide. For detailed information on the interfacing of Analog Devices JTAG emulators with Analog Devices DSP products with JTAG emulation ports, please refer to Engineer to Engineer Note *EE-68: Analog Devices JTAG Emulation Technical Reference*. Both of these documents can be found on the Analog Devices website.

DMA Controller

The ADSP-21161N's on-chip DMA controller enables zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-21161N's internal memory and external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21161N's internal memory and its serial ports, link ports, or the SPI-compatible (Serial Peripheral Interface) port. External bus packing and unpacking of 32-, 48-, or 64-bit words in internal memory is performed during DMA transfers from either 8-, 16-, or 32-bit wide external memory. Fourteen channels of DMA are available on the ADSP-21161N—two are shared between the SPI interface and the link ports, eight via the serial ports, and four via the processor's external port (for host processor, other ADSP-21161Ns, memory, or I/O transfers). Programs can be downloaded to the ADSP-21161N using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{\text{DMAR2–1}}$, $\overline{\text{DMAG2–1}}$). Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.



NOTE:
EXTRA DATA LINES DATA15–0 ARE ONLY ACCESSIBLE IF LINK PORTS ARE DISABLED. ENABLE THESE ADDITIONAL DATA LINKS BY SELECTING IPACK1–0 = 01 IN SYSCON.

Figure 4. External Data Alignment Options

Multiprocessing

The ADSP-21161N offers powerful features tailored to multiprocessing DSP systems. The external port and link ports provide integrated glueless multiprocessing support.

The external port supports a unified address space (see Figure 3) that enables direct interprocessor accesses of each ADSP-21161N's internal memory-mapped (I/O processor) registers. All other internal memory can be indirectly accessed via DMA transfers initiated via the programming of the IOP DMA parameter and control registers. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-21161Ns and a host processor (Figure 5). Master processor change over incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock enables indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Using an instruction rate of 110 MHz, maximum throughput for interprocessor data transfer is 440M bytes/s over the external port.

Two link ports provide a second method of multiprocessing communications. Each link port can support communications to another ADSP-21161N. The ADSP-21161N, running at 110 MHz, has a maximum throughput for interprocessor communications over the links of 220M bytes/s. The link ports and cluster multiprocessing can be used concurrently or independently.

Link Ports

The ADSP-21161N features two 8-bit link ports that provide additional I/O capabilities. With the capability of running at 110 MHz, each link port can support 110M bytes/s. Link port I/O is especially useful for point-to-point interprocessor communication in multiprocessing systems. The link ports can operate independently and simultaneously, with a maximum data throughput of 220M bytes/s. Link port data is packed into 48- or 32-bit words and can be directly read by the core processor or DMA-transferred to on-chip memory. Each link port has its own double-buffered input and output registers. Clock/acknowledge handshaking controls link port transfers. Transfers are programmable as either transmit or receive.

Serial Ports

The ADSP-21161N features four synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. Each serial port is made up of two data lines, a clock and frame sync. The data lines can be programmed to either transmit or receive.

The serial ports operate at up to half the clock rate of the core, providing each with a maximum data rate of 55M bit/s. The serial data pins are programmable as either a transmitter or receiver, providing greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via a dedicated DMA. Each of the serial ports features a Time Division Multiplex (TDM) multichannel mode, where two serial ports are TDM transmitters and two serial ports are TDM receivers (SPORT0 Rx paired with SPORT2 Tx, SPORT1 Rx paired with SPORT3 Tx). Each of the serial ports also support the I^2S protocol (an industry standard interface commonly used by audio codecs, ADCs and DACs), with two data pins, allowing four I^2S channels (using two I^2S stereo devices) per serial port, with a maximum of up to 16 I^2S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For I^2S mode, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated.

Serial Peripheral (Compatible) Interface

Serial Peripheral Interface (SPI) is an industry standard synchronous serial link, enabling the ADSP-21161N SPI-compatible port to communicate with other SPI-compatible devices. SPI is a 4-wire interface consisting of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-21161N SPI-compatible peripheral implementation also features programmable baud rate and clock phase/polarities. The ADSP-21161N SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

Host Processor Interface

The ADSP-21161N host interface enables easy connection to standard 8-bit, 16-bit, or 32-bit microprocessor buses with little additional hardware required. The host interface is accessed through the ADSP-21161N's external port. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead. The host processor requests the ADSP-21161N's external bus with the host bus request ($\overline{HBR}$), host bus grant ($\overline{HBG}$), and chip select (CS) signals. The host can directly read and write the internal IOP registers of the ADSP-21161N, and can access the DMA channel

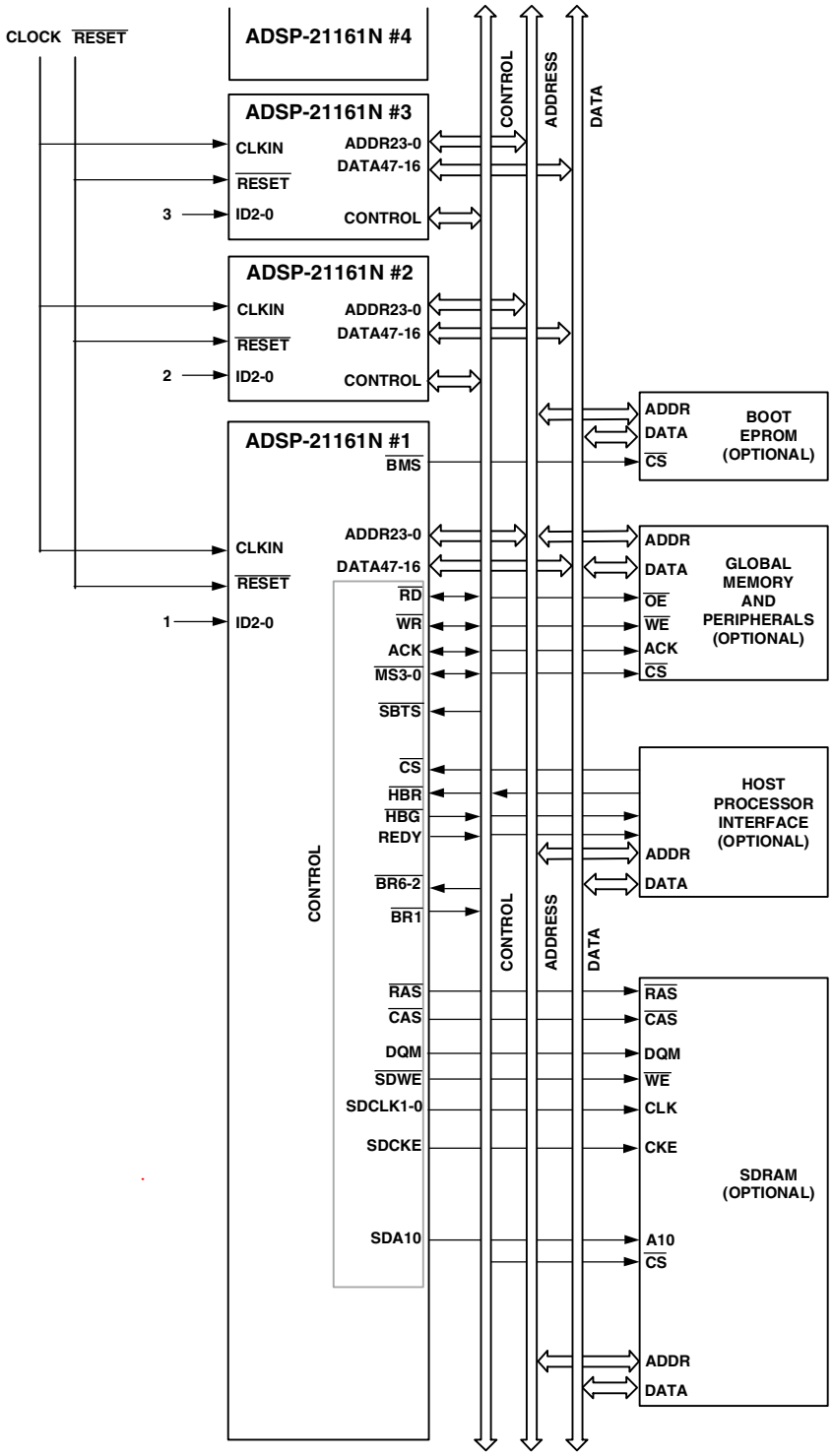


Figure 5. Shared Memory Multiprocessing System

setup and message registers. DMA setup via a host would allow it to access any internal memory address via DMA transfers. Vector interrupt support provides efficient execution of host commands.

The host processor interface can be used in either multiprocessor or single processor SHARC systems. For multiprocessor systems, host access to the SHARC requires address pins ADDR17, ADDR18, ADDR19, and ADDR20 to be driven low. It is not enough to tie these pins to ground through a resistor

(for example 10k ohm). These pins must be driven low with a strong enough drive strength (10–50 ohms) to overcome the SHARC keeper latches present on these pins. If the drive strength provided is not strong enough, data access failures can occur.

For single processor SHARC systems using this host access feature, address pins ADDR17, ADDR18, ADDR19, and ADDR20 may be tied low (for example through a 10k ohm resistor), driven low by a buffer/driver, or left floating. Any of these options is sufficient.

General-Purpose I/O Ports

The ADSP-21161N also contains 12 programmable, general purpose I/O pins that can function as either input or output. As output, these pins can signal peripheral devices; as input, these pins can provide the test for conditional branching.

Program Booting

The internal memory of the ADSP-21161N can be booted at system power-up from either an 8-bit EPROM, a host processor, the SPI interface, or through one of the link ports. Selection of the boot source is controlled by the Boot Memory Select ($\overline{BMS}$), EBOOT (EPROM Boot), and Link/Host Boot (LBOOT) pins. 8-, 16-, or 32-bit host processors can also be used for booting.

Phase-Locked Loop and Crystal Double Enable

The ADSP-21161N uses an on-chip phase-locked loop (PLL) to generate the internal clock for the core. The CLK_CFG1–0 pins are used to select ratios of 2:1, 3:1, and 4:1. In addition to the PLL ratios, the $\overline{CLKDBL}$ pin can be used for more clock ratio options. The (1×/2× CLKIN) rate set by the $\overline{CLKDBL}$ pin determines the rate of the PLL input clock and the rate at which the external port operates. With the combination of CLK_CFG1–0 and $\overline{CLKDBL}$, ratios of 2:1, 3:1, 4:1, 6:1, and 8:1 between the core and CLKIN are supported. See also Figure 8 on Page 20.

Power Supplies

The ADSP-21161N has separate power supply connections for the analog (AV_{DD}/AGND), internal (V_{DDINT}), and external (V_{DDEXT}) power supplies. The internal and analog supplies must meet the 1.8 V requirement. The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same supply.

Note that the analog supply (AV_{DD}) powers the ADSP-21161N's clock generator PLL. To produce a stable clock, provide an external circuit to filter the power input to the AV_{DD} pin. Place the filter as close as possible to the pin. The AV_{DD} filter circuit shown in Figure 6 must be added for each ADSP-21161N in the multiprocessor system. To prevent noise coupling, use a wide trace for the analog ground (AGND) signal and install a decoupling capacitor as close as possible to the pin.

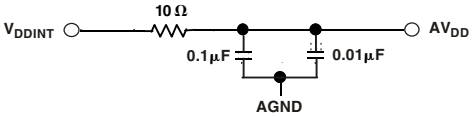


Figure 6. Analog Power (AV_{DD}) Filter Circuit

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of Cross-

Core Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21161N architecture and functionality. For detailed information on the ADSP-2116x Family core architecture and instruction set, refer to the *ADSP-21161 SHARC DSP Hardware Reference* and the *ADSP-21160 SHARC DSP Instruction Set Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/signal chains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

ADSP-21161N pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$). Tie or pull unused inputs to V_{DDEXT} or GND, except for the following:

- ADDR23–0, DATA47–0, BRST, CLKOUT (Note: These pins have a logic-level hold circuit enabled on the ADSP-21161N DSP with ID2–0 = 00x.)
- $\overline{\text{PA}}$, ACK, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{DMARx}}$, $\overline{\text{DMAGx}}$, (ID2–0 = 00x) (Note: These pins have a pull-up enabled on the ADSP-21161N DSP with ID2–0 = 00x.)
- LxCLK, LxACK, LxDAT7–0 (LxPDRDE = 0) (Note: See Link Port Buffer Control Register Bit definitions in the ADSP-21161N *SHARC DSP Hardware Reference*.)
- DxA, DxB, SCLKx, SPICLK, MISO, MOSI, $\overline{\text{EMU}}$, TMS,$\overline{\text{TRST}}$, TDI (Note: These pins have a pull-up.)

The following symbols appear in the Type column of Table 2: A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, and T = Three-State (when $\overline{\text{SBTS}}$ is asserted or when the ADSP-21161N is a bus slave).

Unlike previous SHARC processors, the ADSP-21161N contains internal series resistance equivalent to 50 Ω on all input/output drivers except the CLKIN and XTAL pins. Therefore, for traces longer than six inches, external series resistors on control, data, clock, or frame sync pins are not required to dampen reflections from transmission line effects for point-to-point connections. However, for more complex networks such as a star configuration, series termination is still recommended.

Table 2. Pin Function Descriptions

Pin	Type	Function
ADDR23–0	I/O/T	**External Bus Address.** The ADSP-21161N outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/writes of the IOP registers of other ADSP-21161Ns while all other internal memory resources can be accessed indirectly via DMA control (that is, accessing IOP DMA parameter registers). The ADSP-21161N inputs addresses when a host processor or multiprocessing bus master is reading or writing its IOP registers. A keeper latch on the DSP's ADDR23-0 pins maintains the input at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x.
DATA47–16	I/O/T	**External Bus Data.** The ADSP-21161N inputs and outputs data and instructions on these pins. Pull-up resistors on unused data pins are not necessary. A keeper latch on the DSP's DATA47–16 pins maintains the input at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x. **Note:** *DATA15–8 pins (multiplexed with L1DAT7–0) can also be used to extend the data bus if the link ports are disabled and will not be used. In addition, DATA7–0 pins (multiplexed with L0DAT7–0) can also be used to extend the data bus if the link ports are not used. This enables execution of 48-bit instructions from external SBSRAM (system clock speed-external port), SRAM (system clock speed-external port) and SDRAM (core clock or one-half the core clock speed). The IPACKx Instruction Packing Mode Bits in SYSCON should be set correctly (IPACK1–0=0x1) to enable this full instruction Width/No-packing Mode of operation.*
$\overline{\text{MS3–0}}$	I/O/T	**Memory Select Lines.** These outputs are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank sizes are fixed to 16 M words for non-SDRAM and 64M words for SDRAM. The $\overline{\text{MS3–0}}$ outputs are decoded memory address lines. In asynchronous access mode, the $\overline{\text{MS3–0}}$ outputs transition with the other address outputs. In synchronous access modes, the $\overline{\text{MS3–0}}$ outputs assert with the other address lines; however, they deassert after the first CLKIN cycle in which ACK is sampled asserted. In a multiprocessor system, the $\overline{\text{MSx}}$ signals are tracked by slave SHARCs.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe.** $\overline{\text{RD}}$ is asserted whenever ADSP-21161N reads a word from external memory or from the IOP registers of other ADSP-21161Ns. External devices, including other ADSP-21161Ns, must assert $\overline{\text{RD}}$ for reading from a word of the ADSP-21161N IOP register memory. In a multiprocessing system, $\overline{\text{RD}}$ is driven by the bus master. $\overline{\text{RD}}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.
$\overline{\text{WR}}$	I/O/T	**Memory Write Low Strobe.** $\overline{\text{WR}}$ is asserted when ADSP-21161N writes a word to external memory or IOP registers of other ADSP-21161Ns. External devices must assert $\overline{\text{WR}}$ for writing to ADSP-21161N IOP registers. In a multiprocessing system, the bus master drives WR. $\overline{\text{WR}}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.

Table 2. Pin Function Descriptions (Continued)

Pin	Type	Function
BRST	I/O/T	**Sequential Burst Access.** BRST is asserted by ADSP-21161N to indicate that data associated with consecutive addresses is being read or written. A slave device samples the initial address and increments an internal address counter after each transfer. The incremented address is not pipelined on the bus. A master ADSP-21161N in a multiprocessor environment can read slave external port buffers (EPBx) using the burst protocol. BRST is asserted after the initial access of a burst transfer. It is asserted for every cycle after that, except for the last data request cycle (denoted by $\overline{RD}$ or $\overline{WR}$ asserted and BRST negated). A keeper latch on the DSP's BRST pin maintains the input at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x.
ACK	I/O/S	**Memory Acknowledge.** External devices can de-assert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21161N deasserts ACK as an output to add wait states to a synchronous access of its IOP registers. ACK has a 20 kΩ internal pull-up resistor that is enabled during reset or on DSPs with ID2–0=00x.
$\overline{SBTS}$	I/S	**Suspend Bus and Three-State.** External devices can assert $\overline{SBTS}$ (low) to place the external bus address, data, selects, and strobes in a high impedance state for the following cycle. If the ADSP-21161N attempts to access external memory while $\overline{SBTS}$ is asserted, the processor will halt and the memory access will not be completed until $\overline{SBTS}$ is deasserted. $\overline{SBTS}$ should only be used to recover from host processor/ADSP-21161N deadlock.
$\overline{CAS}$	I/O/T	**SDRAM Column Access Strobe.** In conjunction with $\overline{RAS}$, $\overline{MSx}$, $\overline{SDWE}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{RAS}$	I/O/T	**SDRAM Row Access Strobe.** In conjunction with $\overline{CAS}$, $\overline{MSx}$, $\overline{SDWE}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{SDWE}$	I/O/T	**SDRAM Write Enable.** In conjunction with $\overline{CAS}$, $\overline{RAS}$, $\overline{MSx}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
DQM	O/T	**SDRAM Data Mask.** In write mode, DQM has a latency of zero and is used during a precharge command and during SDRAM power-up initialization.
SDCLK0	I/O/S/T	**SDRAM Clock Output 0.** Clock for SDRAM devices.
SDCLK1	O/S/T	**SDRAM Clock Output 1.** Additional clock for SDRAM devices. For systems with multiple SDRAM devices, handles the increased clock load requirements, eliminating need of off-chip clock buffers. Either SDCLK1 or both SDCLKx pins can be three-stated.
SDCKE	I/O/T	**SDRAM Clock Enable.** Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	O/T	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with a non-SDRAM accesses or host accesses. This pin replaces the DSP's A10 pin only during SDRAM accesses.
$\overline{IRQ2–0}$	I/A	**Interrupt Request Lines.** These are sampled on the rising edge of CLKIN and may be either edge-triggered or level-sensitive.
FLAG11–0	I/O/A	**Flag Pins.** Each is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
TIMEXP	O	**Timer Expired.** Asserted for four core clock cycles when the timer is enabled and TCOUNT decrements to zero.
$\overline{HBR}$	I/A	**Host Bus Request.** Must be asserted by a host processor to request control of the ADSP-21161N's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the ADSP-21161N that is bus master will relinquish the bus and assert $\overline{HBG}$. To relinquish the bus, the ADSP-21161N places the address, data, select, and strobe lines in a high impedance state. $\overline{HBR}$ has priority over all ADSP-21161N bus requests ($\overline{BR6–1}$) in a multiprocessing system.
$\overline{HBG}$	I/O	**Host Bus Grant.** Acknowledges an $\overline{HBR}$ bus request, indicating that the host processor may take control of the external bus. $\overline{HBG}$ is asserted (held low) by the ADSP-21161N until $\overline{HBR}$ is released. In a multiprocessing system, $\overline{HBG}$ is output by the ADSP-21161N bus master and is monitored by all others. After $\overline{HBR}$ is asserted, and before $\overline{HBG}$ is given, $\overline{HBG}$ will float for 1 t_{CK} (1 CLKIN cycle). To avoid erroneous grants, $\overline{HBG}$ should be pulled up with a 20 kΩ to 50 kΩ external resistor.
$\overline{CS}$	I/A	**Chip Select.** Asserted by host processor to select the ADSP-21161N.

Table 2. Pin Function Descriptions (Continued)

Pin	Type	Function
REDY	O (O/D)	**Host Bus Acknowledge**. The ADSP-21161N deasserts REDY (low) to add wait states to a host access of its IOP registers when $\overline{CS}$ and $\overline{HBR}$ inputs are asserted.
$\overline{DMAR1}$	I/A	**DMA Request 1** (DMA Channel 11). Asserted by external port devices to request DMA services. $\overline{DMAR1}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.
$\overline{DMAR2}$	I/A	**DMA Request 2** (DMA Channel 12). Asserted by external port devices to request DMA services. $\overline{DMAR2}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.
$\overline{DMAG1}$	O/T	**DMA Grant 1** (DMA Channel 11). Asserted by ADSP-21161N to indicate that the requested DMA starts on the next cycle. Driven by bus master only. $\overline{DMAG1}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.
$\overline{DMAG2}$	O/T	**DMA Grant 2** (DMA Channel 12). Asserted by ADSP-21161N to indicate that the requested DMA starts on the next cycle. Driven by bus master only. $\overline{DMAG2}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.
$\overline{BR6–1}$	I/O/S	**Multiprocessing Bus Requests**. Used by multiprocessing ADSP-21161Ns to arbitrate for bus mastership. An ADSP-21161N only drives its own $\overline{BRx}$ line (corresponding to the value of its ID2–0 inputs) and monitors all others. In a multiprocessor system with less than six ADSP-21161Ns, the unused $\overline{BRx}$ pins should be pulled high; the processor's own $\overline{BRx}$ line must not be pulled high or low because it is an output.
BMSTR	O	**Bus Master Output**. In a multiprocessor system, indicates whether the ADSP-21161N is current bus master of the shared external bus. The ADSP-21161N drives BMSTR high only while it is the bus master. In a single-processor system (ID=000), the processor drives this pin high. This pin is used for debugging purposes.
ID2–0	I	**Multiprocessing ID**. Determines which multiprocessing bus request ($\overline{BR6}$–$\overline{BR1}$) is used by ADSP-21161N. ID=001 corresponds to $\overline{BR1}$, ID=010 corresponds to $\overline{BR2}$, and so on. Use ID=000 or ID=001 in single-processor systems. These lines are a system configuration selection that should be hardwired or only changed at reset.
RPBA	I/S	**Rotating Priority Bus Arbitration Select**. When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection that must be set to the same value on every ADSP-21161N. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every ADSP-21161N.
$\overline{PA}$	I/O/T	**Priority Access**. Asserting its $\overline{PA}$ pin enables an ADSP-21161N bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{PA}$ is connected to all ADSP-21161Ns in the system. If access priority is not required in a system, the $\overline{PA}$ pin should be left unconnected. $\overline{PA}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.
DxA	I/O	**Data Transmit or Receive Channel A** (Serial Ports 0, 1, 2, 3). Each DxA pin has an internal pull-up resistor. Bidirectional data pin. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
DxB	I/O	**Data Transmit or Receive Channel B** (Serial Ports 0, 1, 2, 3). Each DxB pin has an internal pull-up resistor. Bidirectional data pin. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SCLKx	I/O	**Transmit/Receive Serial Clock** (Serial Ports 0, 1, 2, 3). Each SCLK pin has an internal pull-up resistor. This signal can be either internally or externally generated.
FSx	I/O	**Transmit or Receive Frame Sync** (Serial Ports 0, 1, 2, 3). The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally. It can be active high or low or an early or a late frame sync, in reference to the shifting of serial data.
SPICLK	I/O	**Serial Peripheral Interface Clock Signal**. Driven by the master, this signal controls the rate at which data is transferred. The master may transmit data at a variety of baud rates. SPICLK cycles once for each bit transmitted. SPICLK is a gated clock that is active during data transfers, only for the length of the transferred word. Slave devices ignore the serial clock if the slave select input is driven inactive (HIGH). SPICLK is used to shift out and shift in the data driven on the MISO and MOSI lines. The data is always shifted out on one clock edge of the clock and sampled on the opposite edge of the clock. Clock polarity and clock phase relative to data are programmable into the SPICTL control register and define the transfer format. SPICLK has a 50 kΩ internal pull-up resistor.

Table 2. Pin Function Descriptions (Continued)

Pin	Type	Function
$\overline{\text{SPIDS}}$	I	**Serial Peripheral Interface Slave Device Select**. An active low signal used to enable slave devices. This input signal behaves like a chip select, and is provided by the master device for the slave devices. In multimaster mode $\overline{\text{SPIDS}}$ signal can be asserted to a master device to signal that an error has occurred, as some other device is also trying to be the master device. If asserted low when the device is in master mode, it is considered a multimaster error. For a single-master, multiple-slave configuration where FLAG3–0 are used, this pin must be tied or pulled high to V_{DDEXT} on the master device. For ADSP-21161N to ADSP-21161N SPI interaction, any of the master ADSP-21161N's FLAG3–0 pins can be used to drive the $\overline{\text{SPIDS}}$ signal on the ADSP-21161N SPI slave device.
MOSI	I/O (o/d)	**SPI Master Out Slave**. If the ADSP-21161N is configured as a master, the MOSI pin becomes a data transmit (output) pin, transmitting output data. If the ADSP-21161N is configured as a slave, the MOSI pin becomes a data receive (input) pin, receiving input data. In an ADSP-21161N SPI interconnection, the data is shifted out from the MOSI output pin of the master and shifted into the MOSI input(s) of the slave(s). MOSI has an internal pull-up resistor.
MISO	I/O (o/d)	**SPI Master In Slave Out**. If the ADSP-21161N is configured as a master, the MISO pin becomes a data receive (input) pin, receiving input data. If the ADSP-21161N is configured as a slave, the MISO pin becomes a data transmit (output) pin, transmitting output data. In an ADSP-21161N SPI interconnection, the data is shifted out from the MISO output pin of the slave and shifted into the MISO input pin of the master. MISO has an internal pull-up resistor. MISO can be configured as o/d by setting the OPD bit in the SPICTL register. **Note:** *Only one slave is allowed to transmit data at any given time.*
LxDAT7–0 [DATA15–0]	I/O [I/O/T]	Link Port Data (Link Ports 0–1). For silicon revisions 1.2 and higher, each LxDAT pin has a keeper latch that is enabled when used as a data pin; or a 20 kΩ internal pull-down resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register. For silicon revisions 0.3, 1.0, and 1.1 each LxDAT pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register. **Note:** *L1DAT7–0 are multiplexed with the DATA15–8 pins L0DAT7–0 are multiplexed with the DATA7–0 pins. If link ports are disabled and are not used, these pins can be used as additional data lines for executing instructions at up to the full clock rate from external memory. See DATA47–16 for more information.*
LxCLK	I/O	**Link Port Clock** (Link Ports 0–1). Each LxCLK pin has an internal pull-down 50 kΩ resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register.
LxACK	I/O	**Link Port Acknowledge** (Link Ports 0–1). Each LxACK pin has an internal pull-down 50 kΩ resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register.
EBOOT	I	**EPROM Boot Select**. For a description of how this pin operates, see the table in the $\overline{\text{BMS}}$ pin description. This signal is a system configuration selection that should be hardwired.
LBOOT	I	**Link Boot**. For a description of how this pin operates, see the table in the $\overline{\text{BMS}}$ pin description. This signal is a system configuration selection that should be hardwired.
$\overline{\text{BMS}}$	I/O/T	**Boot Memory Select**. Serves as an output or input as selected with the EBOOT and LBOOT pins (see Table 4). This input is a system configuration selection that should be hardwired. For Host and PROM boot, DMA channel 10 (EPB0) is used. For Link boot and SPI boot, DMA channel 8 is used. Three-state only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output).
CLKIN	I	**Local Clock In**. Used in conjunction with XTAL. CLKIN is the ADSP-21161N clock input. It configures the ADSP-21161N to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the ADSP-21161N to use the external clock source such as an external clock oscillator.The ADSP-21161N external port cycles at the frequency of CLKIN. The instruction cycle rate is a multiple of the CLKIN frequency; it is programmable at power-up via the CLK_CFG1–0 pins. CLKIN may not be halted, changed, or operated below the specified frequency.
XTAL	O	**Crystal Oscillator Terminal 2**. Used in conjunction with CLKIN to enable the ADSP-21161N's internal clock oscillator or to disable it to use an external clock source. See CLKIN.
CLK_CFG1-0	I	**Core/CLKIN Ratio Control**. ADSP-21161N core clock (instruction cycle) rate is equal to n × PLLICLK where n is user selectable to 2, 3, or 4, using the CLK_CFG1–0 inputs. These pins can also be used in combination with the $\overline{\text{CLKDBL}}$ pin to generate additional core clock rates of 6 × CLKIN and 8 × CLKIN (see the Clock Rate Ratios table in the $\overline{\text{CLKDBL}}$ description).

Table 2. Pin Function Descriptions (Continued)

Pin	Type	Function
$\overline{\text{CLKDBL}}$	I	**Crystal Double Mode Enable**. This pin is used to enable the 2× clock double circuitry, where CLKOUT can be configured as either 1× or 2× the rate of CLKIN. This CLKIN double circuit is primarily intended to be used for an external crystal in conjunction with the internal clock generator and the XTAL pin. The internal clock generator when used in conjunction with the XTAL pin and an external crystal is designed to support up to a maximum of 27.5 MHz external crystal frequency. $\overline{\text{CLKDBL}}$ can be used in XTAL mode to generate a 55 MHz input into the PLL. The 2× clock mode is enabled (during $\overline{\text{RESET}}$ low) by tying $\overline{\text{CLKDBL}}$ to GND, otherwise it is connected to V_{DDEXT} for 1× clock mode. For example, this enables the use of a 27.5 MHz crystal to enable 110 MHz core clock rates and a 55 MHz CLKOUT operation when CLK_CFG0=0, CLK_CFG1=0 and $\overline{\text{CLKDBL}}$=0. This pin can also be used to generate different clock rate ratios for external clock oscillators as well. The possible clock rate ratio options (up to 110 MHz) for either CLKIN (external clock oscillator) or XTAL (crystal input) are shown in Table 3 on Page 16. An 8:1 ratio enables the use of a 12.5 MHz crystal to generate a 100 MHz core (instruction clock) rate and a 25 MHz CLKOUT (external port) clock rate. See also Figure 8 on Page 20. **Note:** *When using an external crystal, the maximum crystal frequency cannot exceed 27.5 MHz. For all other external clock sources, the maximum CLKIN frequency is 55 MHz.*
CLKOUT	O/T	**Local Clock Out**. CLKOUT is 1× or 2× and is driven at either 1× or 2× the frequency of CLKIN frequency by the current bus master. The frequency is determined by the $\overline{\text{CLKDBL}}$ pin. This output is three-stated when the ADSP-21161N is not the bus master or when the host controls the bus ($\overline{\text{HBG}}$ asserted). A keeper latch on the DSP's CLKOUT pin maintains the output at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x. If $\overline{\text{CLKDBL}}$ enabled, CLKOUT=2 × CLKIN If $\overline{\text{CLKDBL}}$ disabled, CLKOUT=1 × CLKIN **Note:** *CLKOUT is only controlled by the* $\overline{\text{CLKDBL}}$ *pin and operates at either 1 × CLKIN or 2 × CLKIN.* Do not use CLKOUT in multiprocessing systems. Use CLKIN instead.
$\overline{\text{RESET}}$	I/A	**Processor Reset**. Resets the ADSP-21161N to a known state and begins execution at the program memory location specified by the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
$\overline{\text{RSTOUT}}$[1]	O	**Reset Out**. When $\overline{\text{RSTOUT}}$ is asserted (low), this pin indicates that the core blocks are in reset. It is deasserted 4080 cycles after $\overline{\text{RESET}}$ is deasserted indicating that the PLL is stable and locked.
TCK	I	**Test Clock (JTAG)**. Provides a clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG)**. Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG)**. Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG)**. Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG)**. Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21161N. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D)	**Emulation Status**. Must be connected to the ADSP-21161N Analog Devices DSP Tools product line of JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 50 kΩ internal pull-up resistor.
V_{DDINT}	P	**Core Power Supply**. Nominally +1.8 V dc and supplies the DSP's core processor (14 pins).
V_{DDEXT}	P	**I/O Power Supply**. Nominally +3.3 V dc. (13 pins).
AVDD	P	**Analog Power Supply**. Nominally +1.8 V dc and supplies the DSP's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on Page 9.
AGND	G	**Analog Power Supply Return**.
GND	G	**Power Supply Return**. (26 pins).
NC		**Do Not Connect**. Reserved pins that must be left open and unconnected. (4 pins)

[1] $\overline{\text{RSTOUT}}$ exists only for silicon revisions 1.2 and greater.

Table 3. Clock Rate Ratios

$\overline{\text{CLKDBL}}$	CLK_CFG1	CLK_CFG0	Core:CLKIN	CLKIN:CLKOUT
1	0	0	2:1	1:1
1	0	1	3:1	1:1
1	1	0	4:1	1:1
0	0	0	4:1	1:2
0	0	1	6:1	1:2
0	1	0	8:1	1:2

BOOT MODES

Table 4. Boot Mode Selection

EBOOT	LBOOT	$\overline{\text{BMS}}$	Booting Mode
1	0	Output	EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.)
0	0	1 (Input)	Host Processor
0	1	0 (Input)	Serial Boot via SPI
0	1	1 (Input)	Link Port
0	0	0 (Input)	No Booting. Processor executes from external memory.
1	1	x (Input)	Reserved

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	Test Conditions	100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage		1.71	1.89	1.71	1.89	V
AV_{DD}	Analog (PLL) Supply Voltage		1.71	1.89	1.71	1.89	V
V_{DDEXT}	External (I/O) Supply Voltage		3.13	3.47	3.13	3.47	V
V_{IH}	High Level Input Voltage[2]	@ V_{DDEXT} = Max	2.0	V_{DDEXT}+0.5	2.0	V_{DDEXT}+0.5	V
V_{IL}	Low Level Input Voltage[2]	@ V_{DDEXT} = Min	–0.5	+0.8	–0.5	+0.8	V
T_{CASE}	Case Operating Temperature[3]		–40	+105	–40	+125	°C

[1] Specifications subject to change without notice.

[2] Applies to input and bidirectional pins: DATA47–16, ADDR23–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG11–0, $\overline{HBG}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{PA}$, $\overline{BRST}$, FSx, DxA, DxB, SCLKx, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDCLK0, LxDAT7–0, LxCLK, LxACK, SPICLK, MOSI, MISO, $\overline{SPIDS}$, EBOOT, LBOOT, $\overline{BMS}$, SDCKE, CLK_CFGx, $\overline{CLKDBL}$, CLKIN, $\overline{RESET}$, TRST, TCK, TMS, TDI.

[3] See Thermal Characteristics on Page 55 for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OH} = –2.0 mA[2]	2.4		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OL} = 4.0 mA[2]		0.4	V
I_{IH}	High Level Input Current[3, 4]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{IL}	Low Level Input Current[3]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{IHC}	CLKIN High Level Input Current[5]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		35	µA
I_{ILC}	CLKIN Low Level Input Current[5]	@ V_{DDEXT} = Max, V_{IN} = 0 V		35	µA
I_{IKH}	Keeper High Load Current[6]	@ V_{DDEXT} = Max, V_{IN} = 2.0 V	–250	–100	µA
I_{IKL}	Keeper Low Load Current[6]	@ V_{DDEXT} = Max, V_{IN} = 0.8 V	50	200	µA
I_{IKH-OD}	Keeper High Overdrive Current[6, 7, 8]	@ V_{DDEXT} = Max	–300		µA
I_{IKL-OD}	Keeper Low Overdrive Current[6, 7, 8]	@ V_{DDEXT} = Max	300		µA
I_{ILPU}	Low Level Input Current Pull-Up[4]	@ V_{DDEXT} = Max, V_{IN} = 0 V		350	µA
I_{OZH}	Three-State Leakage Current[9, 10, 11]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{OZL}	Three-State Leakage Current[9, 12, 13]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{OZLPU1}	Three-State Leakage Current Pull-Up1[10]	@ V_{DDEXT} = Max, V_{IN} = 0 V		500	µA
I_{OZLPU2}	Three-State Leakage Current Pull-Up2[11]	@ V_{DDEXT} = Max, V_{IN} = 0 V		350	µA
I_{OZHPD1}	Three-State Leakage Current Pull-Down1[12]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		350	µA
I_{OZHPD2}	Three-State Leakage Current Pull-Down2[13]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		500	µA
$I_{DD-INPEAK}$	Supply Current (Internal)[14, 15]	t_{CCLK} = 9.0 ns, V_{DDINT} = Max		965	mA
		t_{CCLK} = 10.0 ns, V_{DDINT} = Max		900	
$I_{DD-INHIGH}$	Supply Current (Internal)[15, 16]	t_{CCLK} = 9.0 ns, V_{DDINT} = Max		700	mA
		t_{CCLK} = 10.0 ns, V_{DDINT} = Max		650	
$I_{DD-INLOW}$	Supply Current (Internal)[15, 17]	t_{CCLK} = 9.0 ns, V_{DDINT} = Max		535	mA
		t_{CCLK} = 10.0 ns, V_{DDINT} = Max		500	
$I_{DD-IDLE}$	Supply Current (Idle)[15, 18]	t_{CCLK} = 9.0 ns, V_{DDINT} = Max		425	mA
		t_{CCLK} = 10.0 ns, V_{DDINT} = Max		400	
AI_{DD}	Supply Current (Analog)[19]	@ AV_{DD} = Max		10	mA
C_{IN}	Input Capacitance[20, 21]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.8 V		4.7	pF

[1] Applies to output and bidirectional pins: DATA47–16, ADDR23–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, ACK, DQM, FLAG11–0, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, BMSTR, $\overline{PA}$, BRST, FSx, DxA, DxB, SCLKx, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDA10, LxDAT7–0, LxCLK, LxACK, SPICLK, MOSI, MISO, $\overline{BMS}$, SDCLKx, SDCKE, $\overline{EMU}$, XTAL, TDO, CLKOUT, TIMEXP, $\overline{RSTOUT}$.

[2] See Output Drive Currents on Page 54 for typical drive current capabilities.

[3] Applies to input pins: DATA47–16, ADDR23–0, $\overline{MS3–0}$, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG11–0, $\overline{HBG}$, $\overline{HBR}$, $\overline{CS}$, $\overline{BR6–1}$, ID2–0, RPBA, BRST, FSx, DxA, DxB, SCLKx, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDCLK0, LxDAT7–0, LxCLK, LxACK, SPICLK, MOSI, MISO, $\overline{SPIDS}$, EBOOT, LBOOT, $\overline{BMS}$, SDCKE, CLK_CFGx, $\overline{CLKDBL}$, TCK, $\overline{RESET}$, CLKIN.

[4] Applies to input pins with 20 kΩ internal pull-ups: $\overline{RD}$, $\overline{WR}$, ACK, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{PA}$, $\overline{TRST}$, TMS, TDI.

[5] Applies to CLKIN only.

[6] Applies to all pins with keeper latches: ADDR23–0, DATA47–0, $\overline{MS3–0}$, BRST, CLKOUT.

[7] Current required to switch from kept high to low or from kept low to high.

[8] Characterized, but not tested.

[9] Applies to three-statable pins: DATA47–16, ADDR23–0, $\overline{MS3–0}$, CLKOUT, FLAG11–0, REDY, $\overline{HBG}$, $\overline{BMS}$, $\overline{BR6–1}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, DQM, SDCLKx, SDCKE, SDA10, BRST.

[10] Applies to three-statable pins with 20 kΩ pull-ups: $\overline{RD}$, $\overline{WR}$, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{PA}$.

[11] Applies to three-statable pins with 50 kΩ internal pull-ups: DxA, DxB, SCLKx, SPICLK., $\overline{EMU}$, MISO, MOSI.

[12] Applies to three-statable pins with 50 kΩ internal pull-downs: LxDAT7–0 (below Revision1.2), LxCLK, LxACK. Use I_{OZHPD2} for Rev. 1.2 and higher.

[13] Applies to three-statable pins with 20 kΩ internal pull-downs: LxDAT7-0 (Revision 1.2 and higher).

[14] The test program used to measure $I_{DDINPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified. For more information, see Power Dissipation on Page 20.

[15] Current numbers are for V_{DDINT} and AVDD supplies combined.

[16] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. For more information, see Power Dissipation on Page 20.

[17] $I_{DDINLOW}$ is a composite average based on a range of low activity code. For more information, see Power Dissipation on Page 20.

[18] Idle denotes ADSP-21161N state during execution of IDLE instruction. For more information, see Power Dissipation on Page 20.

[19] Characterized, but not tested.

[20] Applies to all signal pins.

[21] Guaranteed, but not tested.

PACKAGE INFORMATION

The information presented in Figure 7 provides details about how to read the package brand and relate it to specific product features.

Figure 7. Typical Package Brand

Table 5. Package Brand Information

Brand Key	Field Description
ADSP-21161N	Model Number
t	Temperature Range
pp	Package Type
z	RoHS Compliance Option
vvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliance Designation
yyww	Date Code

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 6 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +2.2 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +2.2 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DDEXT} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

The ADSP-21161N's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the DSP uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the DSP's internal clock (the clock source for the external port logic and I/O pads).

The ADSP-21161N's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, link ports, serial ports, and external port (as required for read/write strobes in asynchronous access mode). During reset, program the ratio between the DSP's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 and $\overline{\text{CLKDBL}}$ pins. Even though the internal clock is the clock source for the external port, it behaves as described in the Clock Rate Ratio chart in Table 3 on Page 16. To determine switching frequencies for the serial and link ports, divide down the internal clock, using the programmable divider control of each port (DIVx for the serial ports and LxCLKD for the link ports).

Note the following definitions of various clock periods that are a function of CLKIN and the appropriate ratio control (Table 7).

Figure 8 enables Core-to-CLKIN ratios of 2:1, 3:1, 4:1, 6:1, and 8:1 with external oscillator or crystal. It also shows support for CLKOUT-to-CLKIN ratios of 1:1 and 2:1.

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times.

See Figure 37 on Page 54 under Test Conditions for voltage reference levels.

Switching characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

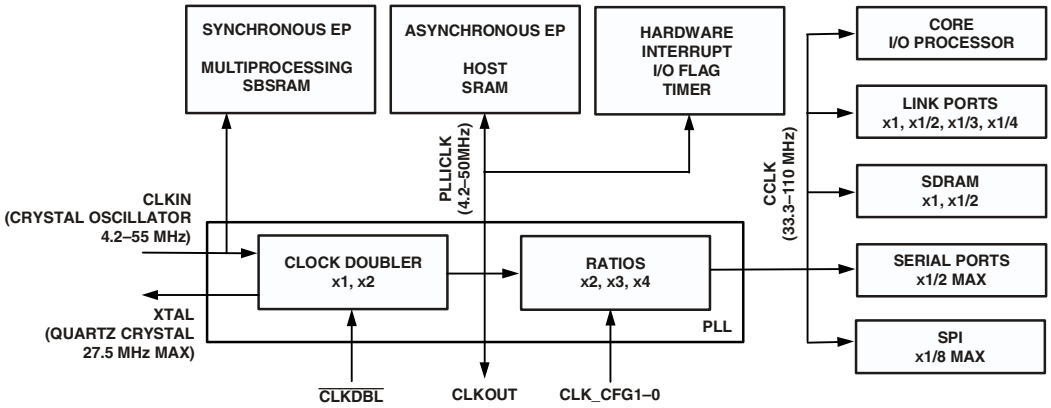


Figure 8. Core Clock and System Clock Relationship to CLKIN

Table 7. CLKOUT and CCLK Clock Generation Operation

Timing Requirements	Description[1]	Calculation
CLKIN	Input Clock	$1/t_{CK}$
CLKOUT	External Port System Clock	$1/t_{CKOP}$
PLLICLK	PLL Input Clock	$1/t_{PLLIN}$
CCLK	Core Clock	$1/t_{CCLK}$
t_{CK}	CLKIN Clock Period	1/CLKIN
t_{CCLK}	(Processor) Core Clock Period	1/CCLK
t_{LCLK}	Link Port Clock Period	$(t_{CCLK}) \times LR$
t_{SCLK}	Serial Port Clock Period	$(t_{CCLK}) \times SR$
t_{SDK}	SDRAM Clock Period	$(t_{CCLK}) \times SDCKR$
t_{SPICLK}	SPI Clock Period	$(t_{CCLK}) \times SPIR$

[1] where:
LR = link port-to-core clock ratio (1, 2, 3, or 1:4, determined by LxCLKD)
SR = serial port-to-core clock ratio (wide range, determined by CLKDIV)
SDCKR = SDRAM-to-Core Clock Ratio (1:1 or 1:2, determined by SDCTL register)
SPIR = SPI-to-Core Clock Ratio (wide range, determined by SPICTL register)
LCLK = Link Port Clock
SCLK = Serial Port Clock
SDK = SDRAM Clock
SPICLK = SPI Clock

POWER DISSIPATION

Total power dissipation has two components: one due to internal circuitry and one due to the switching of external output drivers.

Internal power dissipation depends on the instruction execution sequence and the data operands involved. Using the current specifications ($I_{DDINPEAK}$, $I_{DDINHIGH}$, $I_{DDINLOW}$, I_{DDIDLE}) from the Electrical Characteristics on Page 18 and the current-versus-operation information in Table 8, the programmer can estimate the ADSP-21161N's internal power supply (V_{DDINT}) input current for a specific application, according to the following formula:

$$\begin{aligned} &\%\ Peak \times I_{DD\text{-}INPEAK} \\ &\%\ High \times I_{DD\text{-}INHIGH} \\ &\%\ Low \times I_{DD\text{-}INLOW} \\ +\ &\%\ Peak \times I_{DD\text{-}IDLE} \\ &= I_{DDINT} \end{aligned}$$

Table 8. Operation Types Versus Input Current

Operation	Peak Activity[1] ($I_{DDINPEAK}$)	High Activity[1] ($I_{DDINHIGH}$)	Low Activity[1] ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access[2]	2 per t_{CK} cycle (DM×64 and PM×64)	1 per t_{CK} cycle (DM×64)	None
Internal Memory DMA	1 per 2 t_{CCLK} cycles	1 per 2 t_{CCLK} cycles	N/A
External Memory DMA	1 per external port cycle (×32)	1 per external port cycle (×32)	N/A
Data bit pattern for core memory access and DMA	Worst case	Random	N/A

[1] The state of the PEYEN bit (SIMD versus SISD mode) does not influence these calculations.
[2] These assume a 2:1 core clock ratio. For more information on ratios and clocks (t_{CK} and t_{CCLK}), see the timing ratio definitions on Page 19.

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- The number of output pins that switch during each cycle (O)
- The maximum frequency at which they can switch (f)
- Their load capacitance (C)
- Their voltage swing (V_{DD})

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^{2} \times f$$

The load capacitance should include the processor package capacitance (C_{IN}). The switching frequency includes driving the load high and then back low. At a maximum rate of $1/t_{CK}$, address and data pins can drive high and low, while writing to a SDRAM memory.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external memory (32 bit)
- Two 1M × 16 SDRAM chips are used, each with a load of 10 pF (ignoring trace capacitance)
- External Data Memory writes can occur every cycle at a rate of $1/t_{CK}$ with 50% of the pins switching
- The bus cycle time is 55 MHz
- The external SDRAM clock rate is 110 MHz
- Ignoring SDRAM refresh cycles
- Addresses are incremental and on the same page

The P_{EXT} equation is calculated for each class of pins that can drive, as shown in Table 9.

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + P_{INT} + P_{PLL}$$

Where:

P_{EXT} is from Table 9.

P_{INT} is $I_{DDINT} \times 1.8$ V, using the calculation I_{DDINT} listed in Power Dissipation on Page 20.

P_{PLL} is $AI_{DD} \times 1.8$ V, using the value for AI_{DD} listed in the Electrical Characteristics on Page 18.

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Table 9. External Power Calculations—110 MHz Instruction Rate

Pin Type	Number of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	11	20	24.7 pF	55 MHz	10.9 V	= 0.033 W
$\overline{MSx}$	4	0	24.7 pF	N/A	10.9 V	= 0.000 W
$\overline{SDWE}$	1	0	24.7 pF	N/A	10.9 V	= 0.000 W
Data	32	50	14.7 pF	55 MHz	10.9 V	= 0.141 W
SDCLK0	1	100	24.7 pF	110 MHz	10.9 V	= 0.030 W

P_{EXT} = 0.204 W

Power-Up Sequencing — Silicon Revision 1.2 and Greater

The timing requirements for DSP startup are given in Table 10.

During the power-up sequence of the DSP, differences in the ramp-up rates and activation time between the two supplies can cause current to flow in the I/O ESD protection circuitry. To prevent damage to the ESD diode protection circuitry, Analog Devices recommends including a bootstrap Schottky diode.

The bootstrap Schottky diode is connected between the 1.8 V and 3.3 V power supplies as shown in Figure 9. It protects the ADSP-21161N from partially powering the 3.3 V supply. Including a Schottky diode will shorten the delay between the supply ramps and thus prevent damage to the ESD diode protection circuitry. With this technique, if the 1.8 V rail rises ahead of the 3.3 V rail, the Schottky diode pulls the 3.3 V rail along with the 1.8 V rail.

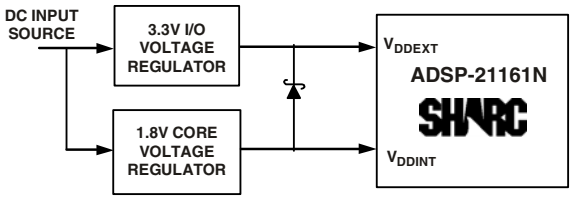


Figure 9. Dual Voltage Schottky Diode

Table 10. Power-Up Sequencing Silicon Revision 1.2 and Greater (DSP Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{RESET}$ Low Before V_{DDINT}/V_{DDEXT} on	0		ns
$t_{IVDDEVDD}$	V_{DDINT} on Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD}	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid[1]	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{RESET}$ Deasserted[2]	10		µs
t_{PLLRST}	PLL Control Setup Before $\overline{RESET}$ Deasserted[3]	20		µs
t_{WRST}	Subsequent $\overline{RESET}$ Low Pulsewidth[4]	$4t_{CK}$		ns
Switching Requirements				
$t_{CORERST}$	DSP core reset deasserted after $\overline{RESET}$ deasserted	$4080t_{CK}$[3, 5]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.8 and 3.3 volt rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case start-up timing of crystal oscillators. Refer to the crystal oscillator manufacturer's data sheet for start-up time. Assume a 25 ms maximum oscillator start-up time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of 4 CLKIN cycles for $\overline{RESET}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4080 cycle count depends on t_{SRST} specification in Table 12. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4081 cycles maximum.

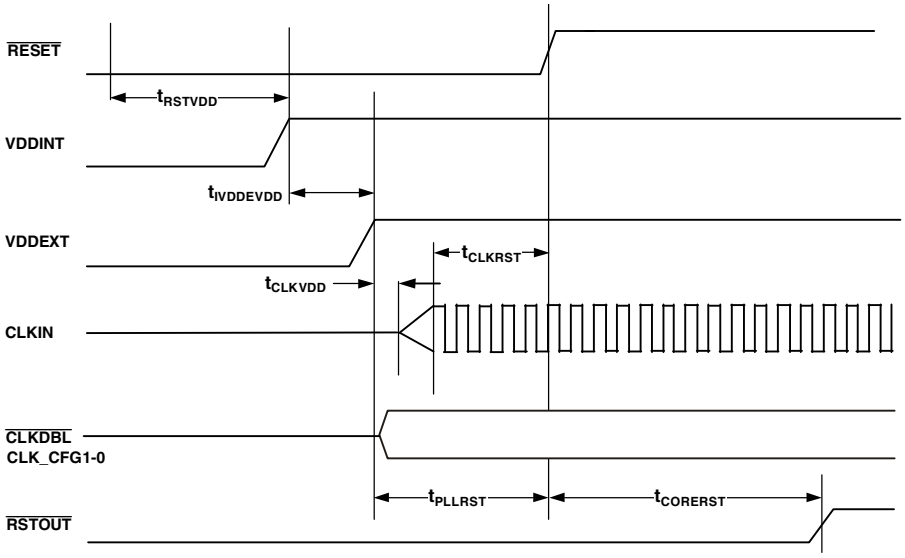


Figure 10. Power-Up Sequencing for Silicon Revision 1.2 and Greater (DSP Startup)

Clock Input

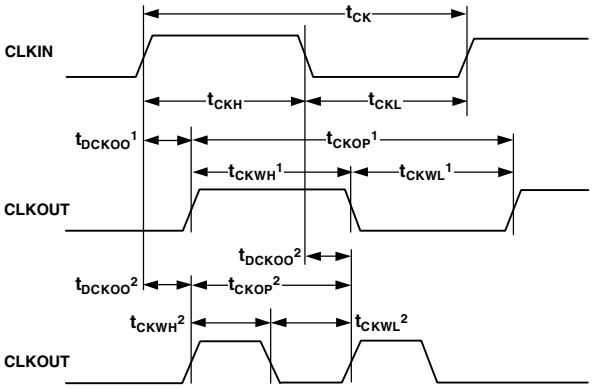
In systems that use multiprocessing or SBSRAM, $\overline{\text{CLKDBL}}$ cannot be enabled nor can the systems use an external crystal as the CLKIN source.

Do not use CLKOUT as the clock source for the SBSRAM device. Using an external crystal in conjunction with $\overline{\text{CLKDBL}}$ to generate a CLKOUT frequency is not supported. Negative hold times can result from the potential skew between CLKIN and CLKOUT.

Table 11. Clock Input

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
t_{CK}	CLKIN Period[1]	20	238	18	238	ns
t_{CKL}	CLKIN Width Low[1]	7.5	119	7	119	ns
t_{CKH}	CLKIN Width High[1]	7.5	119	7	119	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3		3	ns
t_{CCLK}	CCLK Period	10	30	9	30	ns
Switching Characteristics						
t_{DCKOO}	CLKOUT Delay After CLKIN	0	2	0	2	ns
t_{CKOP}	CLKOUT Period	$t_{CK}-1$	$t_{CK}+1$	$t_{CK}-1$	$t_{CK}+1$	ns
t_{CKWH}	CLKOUT Width High	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	ns
t_{CKWL}	CLKOUT Width Low	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	ns

[1] CLKIN is dependent on the configuration of the CLKCFGx and $\overline{\text{CLKDBL}}$ pins to achieve desired t_{CCLK}.

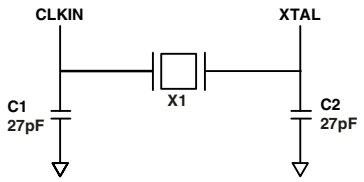


NOTES:
1. WHEN CLKDBL IS DISABLED, ANY SPECIFICATION TO CLKIN APPLIES TO THE RISING EDGE, ONLY.
2. WHEN CLKDBL IS ENABLED, ANY SPECIFICATION TO CLKIN APPLIES TO THE RISING OR FALLING EDGE.

Figure 11. Clock Input

Clock Signals

The ADSP-21161N can use an external clock or a crystal. See CLKIN pin description. The programmer can configure the ADSP-21161N to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 12 shows the component connections used for a crystal operating in fundamental mode.



SUGGESTED COMPONENTS FOR 100MHz OPERATION:
ECLIPTEK EC2SM-25.000M (SURFACE MOUNT PACKAGE)
ECLIPTEK EC-25.000M (THROUGH-HOLE PACKAGE)
C1 = 27pF
C2 = 27pF

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. THIS 25MHz CRYSTAL GENERATES A 100MHz CCLK AND A 50MHz EP CLOCK WITH $\overline{\text{CLKDBL}}$ ENABLED AND A 2:1 PLL MULTIPLY RATIO.

Figure 12. 100 MHz Operation (Fundamental Mode Crystal)

Reset

Table 12. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulsewidth Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	8.5		ns

[1] Applies after the power-up sequence is complete.
[2] Only required if multiple ADSP-21161Ns must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-21161Ns communicating over the shared bus (through the external port), because the bus arbitration logic synchronizes itself automatically after reset.

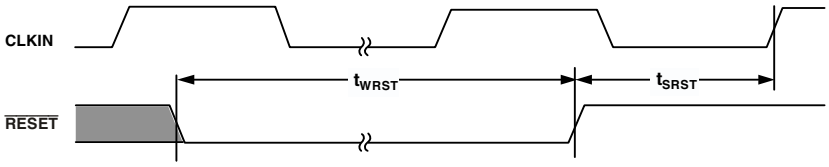


Figure 13. Reset

Interrupts

Table 13. Interrupts

Parameter		Min	Max	Unit
Timing Requirements				
t_{SIR}	$\overline{IRQ2–0}$ Setup Before CLKIN[1]	6		ns
t_{HIR}	$\overline{IRQ2–0}$ Hold After CLKIN[1]	0		ns
t_{IPW}	$\overline{IRQ2–0}$ Pulsewidth[2]	t_{CKOP} + 2		ns

[1] Only required for $\overline{IRQx}$ recognition in the following cycle.
[2] Applies only if t_{SIR} and t_{HIR} requirements are not met.

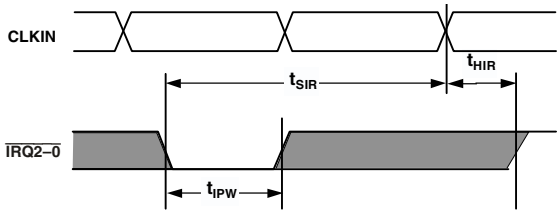


Figure 14. Interrupts

Timer

Table 14. Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{DTEX}	CCLK to TIMEXP	1	7	ns

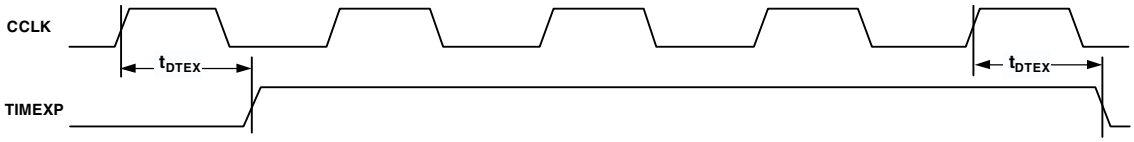


Figure 15. Timer

Flags

Table 15. Flags

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirement						
t_{SFI}	FLAG11–0_{IN} Setup Before CLKIN[1]	4		4		ns
t_{HFI}	FLAG11–0_{IN} Hold After CLKIN[1]	1		1		ns
t_{DWRFI}	FLAG11–0_{IN} Delay After $\overline{RD}/\overline{WR}$ Low[1]		12		9	ns
t_{HFIWR}	FLAG11–0_{IN} Hold After $\overline{RD}/\overline{WR}$ Deasserted[1]	0		0		ns
Switching Characteristics						
t_{DFO}	FLAG11–0_{OUT} Delay After CLKIN		9		9	ns
t_{HFO}	FLAG11–0_{OUT} Hold After CLKIN	1		1		ns
t_{DFOE}	CLKIN to FLAG11–0_{OUT} Enable	1		1		ns
t_{DFOD}	CLKIN to FLAG11–0_{OUT} Disable		5		5	ns

[1] Flag inputs meeting these setup and hold times for instruction cycle N will affect conditional instructions in instruction cycle N+2.

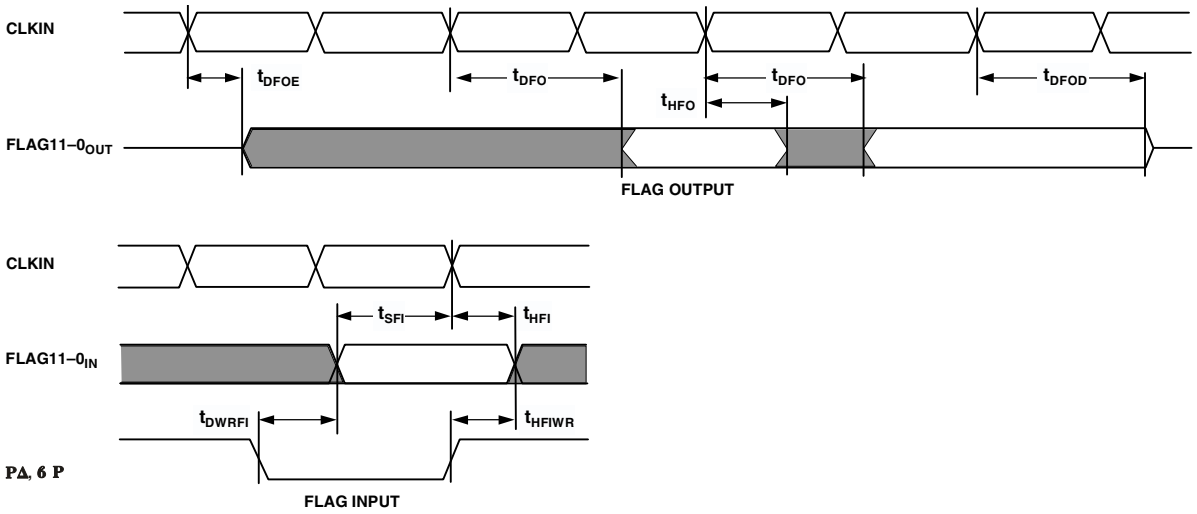


Figure 16. Flags

Memory Read — Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN except for ACK pin requirements listed in footnote 4 of Table 16. These specifications apply when the ADSP-21161N is the bus master accessing external memory space in asynchronous access mode.

Table 16. Memory Read — Bus Master

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
t_{DAD}	Address, Selects Delay to Data Valid[1, 2, 3]		$t_{CKOP}-0.25t_{CCLK}-8.5+W$		$t_{CKOP}-0.25t_{CCLK}-6.75+W$	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1,3]		$0.75t_{CKOP}-11+W$		$0.75t_{CKOP}-11+W$	ns
t_{HDA}	Data Hold from Address, Selects[4]	0		0		ns
t_{SDS}	Data Setup to $\overline{RD}$ High	8		8		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[4]	1		1		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 5]		$t_{CKOP}-0.5t_{CCLK}-12+W$		$t_{CKOP}-0.5t_{CCLK}-12+W$	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[5]		$t_{CKOP}-0.75t_{CCLK}-11+W$		$t_{CKOP}-0.75t_{CCLK}-11+W$	ns
t_{SAKC}	ACK Setup to CLKIN[5]	$0.5t_{CCLK}+3$		$0.5t_{CCLK}+3$		ns
t_{HAKC}	ACK Hold After CLKIN	1		1		ns
Switching Characteristics						
t_{DRHA}	Address Selects Hold After $\overline{RD}$ High	$0.25t_{CCLK}-1+H$		$0.25t_{CCLK}-1+H$		ns
t_{DARL}	Address Selects to $\overline{RD}$ Low[2]	$0.25t_{CCLK}-3$		$0.25t_{CCLK}-3$		ns
t_{RW}	$\overline{RD}$ Pulsewidth	$t_{CKOP}-0.5t_{CCLK}-1+W$		$t_{CKOP}-0.5t_{CCLK}-1+W$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	$0.5t_{CCLK}-1+HI$		$0.5t_{CCLK}-1+HI$		ns

W = (number of wait states specified in WAIT register) × t_{CKOP}.
HI = t_{CKOP} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CKOP} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

[1] Data Delay/Setup: User must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{MSx}$, $\overline{BMS}$ is referenced.
[3] The maximum limits of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where ACK is always high.
[4] Data Hold: User must meet t_{HDA} or t_{HDRH} in asynchronous access mode. See Example System Hold Time Calculation on Page 54 for the calculation of hold times given capacitive and dc loads.
[5] For asynchronous access, ACK is sampled only after the programmed wait states for the access have been counted. For the first CLKIN cycle of a new external memory access, ACK must be driven low (deasserted) by t_{DAAK}, t_{DSAK}, or t_{SAKC}. For the second and subsequent cycles of an asynchronous external memory access, the t_{SAKC} and t_{HAKC} must be met for both assertion and deassertion of ACK signal.

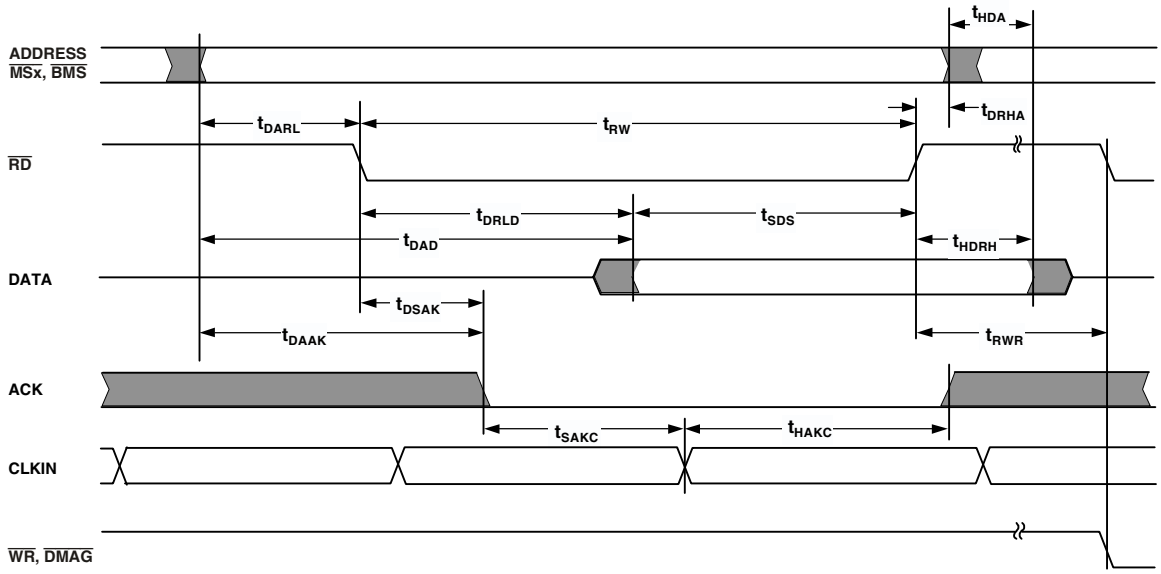


Figure 17. Memory Read — Bus Master

Memory Write — Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN except for ACK pin requirements listed in footnote 1 of Table 17. These specifications apply when the ADSP-21161N is the bus master accessing external memory space in asynchronous access mode.

Table 17. Memory Write — Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		t_{CKOP}–0.5t_{CCLK}–12+W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		t_{CKOP}–0.75t_{CCLK}–11+W	ns
t_{SAKC}	ACK Setup to CLKIN[1]	0.5t_{CCLK}+3		ns
t_{HAKC}	ACK Hold After CLKIN[1]	1		ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	t_{CKOP} – 0.25t_{CCLK} – 3 + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	0.25t_{CCLK} – 3		ns
t_{WW}	$\overline{WR}$ Pulsewidth	t_{CKOP} – 0.5t_{CCLK} – 1 + W		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	t_{CKOP} – 0.25t_{CCLK} – 13.5 + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	0.25t_{CCLK} – 1 + H		ns
t_{DWHD}	Data Hold After $\overline{WR}$ Deasserted	0.25t_{CCLK} – 1 + H		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[3]	0.25t_{CCLK} – 2 + H	0.25t_{CCLK}+2.5+H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	0.5t_{CCLK} – 1.25 + HI		ns
t_{DDWR}	Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	0.25t_{CCLK} – 3 + I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	–0.25t_{CCLK} – 1		ns

W = (number of wait states specified in WAIT register) × t_{CKOP}.
H = t_{CKOP} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
HI = t_{CKOP} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
I = t_{CKOP} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

[1] For asynchronous access, ACK is sampled only after the programmed wait states for the access have been counted. For the first CLKIN cycle of a new external memory access, ACK must be driven low (deasserted) by t_{DAAK}, t_{DSAK}, or t_{SAKC}. For the second and subsequent cycles of an asynchronous external memory access, the t_{SAKC} and t_{HAKC} must be met for both assertion and deassertion of ACK signal.
[2] The falling edge of $\overline{MSx}$, $\overline{BMS}$ is referenced.
[3] See Example System Hold Time Calculation on Page 54 for calculation of hold times given capacitive and dc loads.

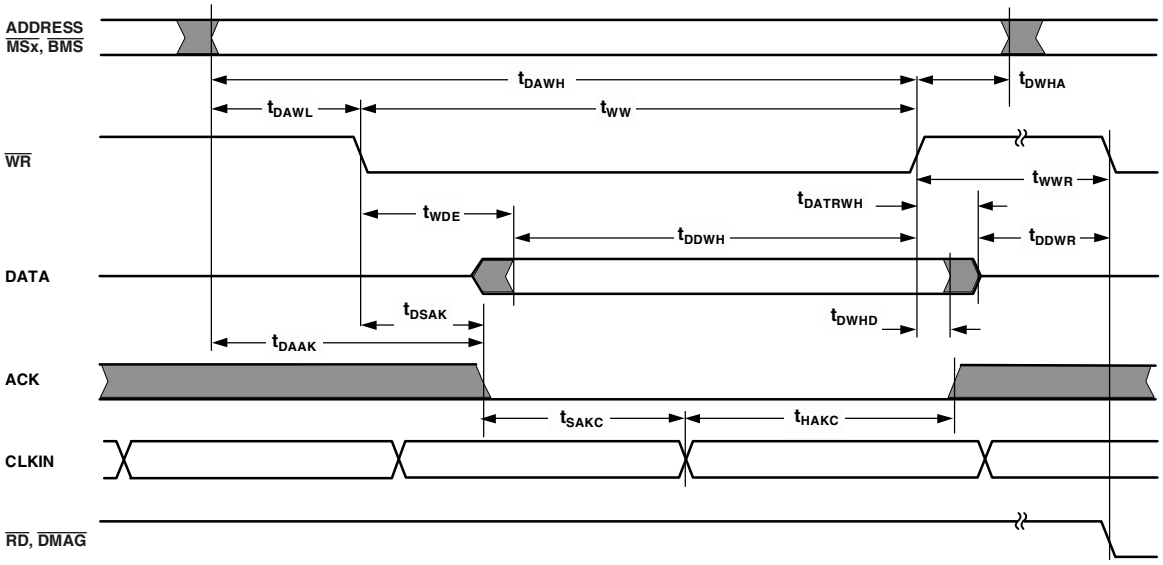


Figure 18. Memory Write — Bus Master

Synchronous Read/Write — Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN, relative to timing or for accessing a slave ADSP-21161N (in multiprocessor memory space). When accessing a slave ADSP-21161N, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write — Bus Slave on Page 32). The slave ADSP-21161N must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Table 18. Synchronous Read/Write — Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDATI}	Data Setup Before CLKIN	5.5		ns
t_{HSDATI}	Data Hold After CLKIN	1		ns
t_{SACKC}	ACK Setup Before CLKIN	$0.5t_{CCLK}+3$		ns
t_{HACKC}	ACK Hold After CLKIN	1		ns
Switching Characteristics				
t_{DADDO}	Address, $\overline{MSx}$, $\overline{BMS}$, BRST, Delay After CLKIN		10	ns
t_{HADDO}	Address, $\overline{MSx}$, $\overline{BMS}$, BRST, Hold After CLKIN	1.5		ns
t_{DRDO}	$\overline{RD}$ High Delay After CLKIN	$0.25t_{CCLK}-1$	$0.25t_{CCLK}+9$	ns
t_{DWRO}	$\overline{WR}$ High Delay After CLKIN	$0.25t_{CCLK}-1$	$0.25t_{CCLK}+9$	ns
t_{DRWL}	$\overline{RD}/\overline{WR}$ Low Delay After CLKIN	$0.25t_{CCLK}-1$	$0.25t_{CCLK}+9$	ns
t_{DDATO}	Data Delay After CLKIN		12.5	ns
t_{HDATO}	Data Hold After CLKIN	1.5		ns

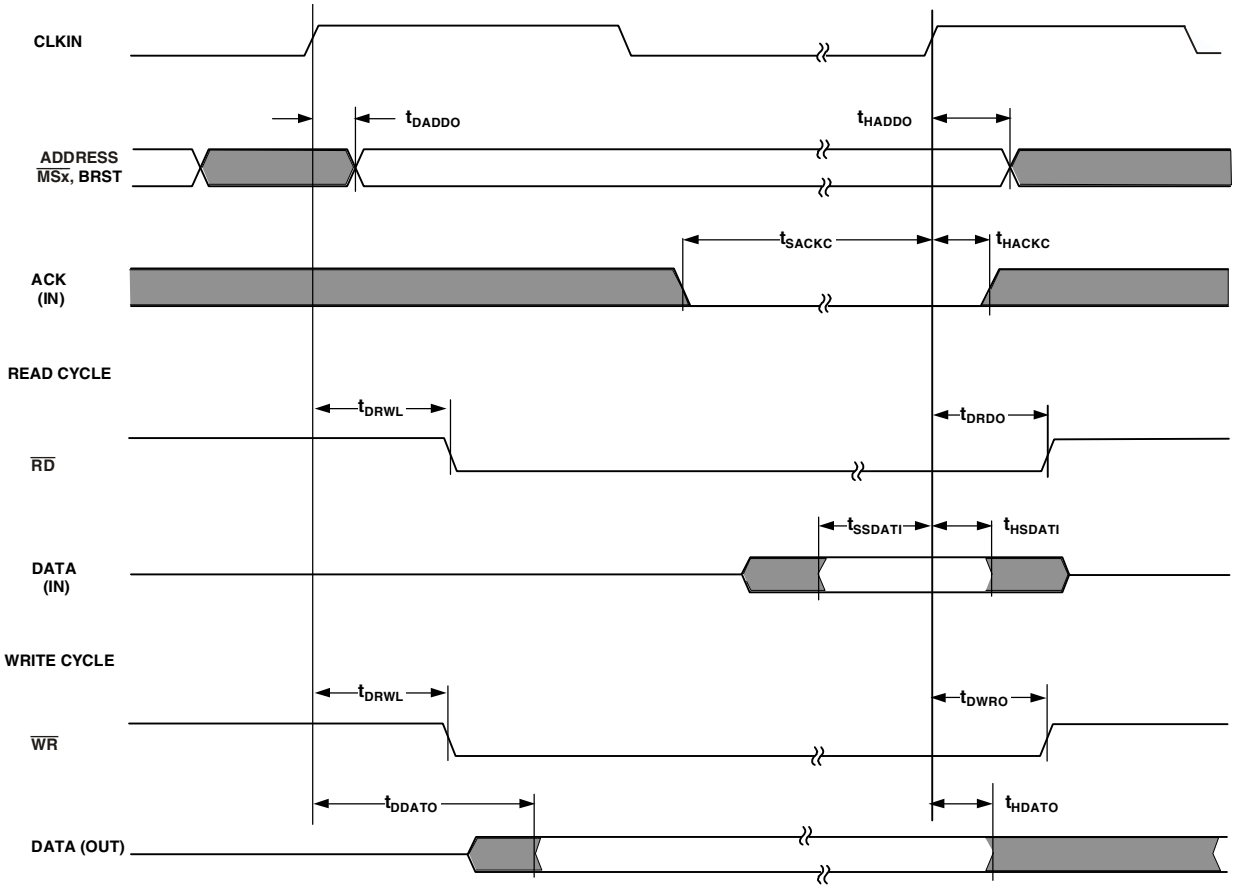


Figure 19. Synchronous Read/Write — Bus Master

Synchronous Read/Write — Bus Slave

Use these specifications for ADSP-21161N bus master accesses of a slave's IOP registers in multiprocessor memory space. The bus master must meet these (bus slave) timing requirements.

Table 19. Synchronous Read/Write — Bus Slave

Parameter		Min	Max	Unit
Timing Requirements				
t_{SADDI}	Address, BRST Setup Before CLKIN	5		ns
t_{HADDI}	Address, BRST Hold After CLKIN	1		ns
t_{SRWI}	$\overline{RD}/\overline{WR}$ Setup Before CLKIN	5		ns
t_{HRWI}	$\overline{RD}/\overline{WR}$ Hold After CLKIN	1		ns
t_{SSDATI}	Data Setup Before CLKIN	5.5		ns
t_{HSDATI}	Data Hold After CLKIN	1		ns
Switching Characteristics				
t_{DDATO}	Data Delay After CLKIN		12.5	ns
t_{HDATO}	Data Hold After CLKIN	1.5		ns
t_{DACKC}	ACK Delay After CLKIN		10	ns
t_{HACKO}	ACK Hold After CLKIN	1.5		ns

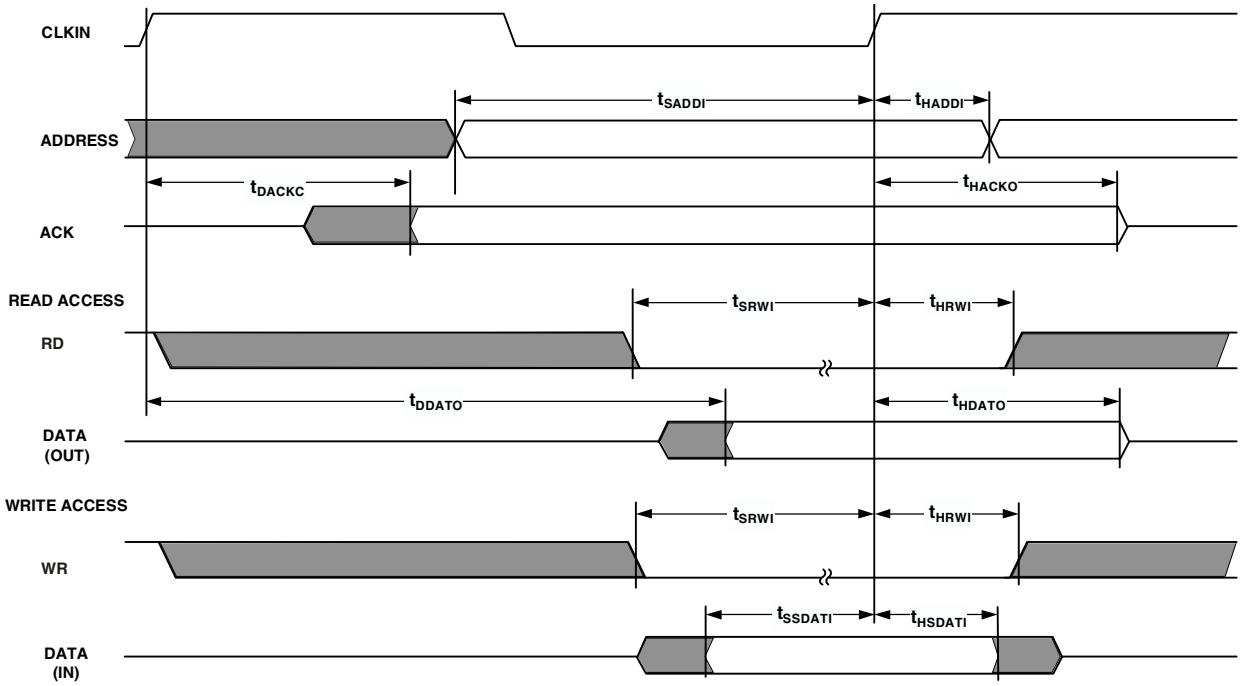


Figure 20. Synchronous Read/Write — Bus Slave

Host Bus Request

Use these specifications for asynchronous host bus requests of an ADSP-21161N ($\overline{HBR}$, $\overline{HBG}$).

Table 20. Host Bus Request

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$ Valid		19		19	ns
t_{SHBRI}	$\overline{HBR}$ Setup Before CLKIN[1]	6		6		ns
t_{HHBRI}	$\overline{HBR}$ Hold After CLKIN[1]	1		1		ns
t_{SHBGI}	$\overline{HBG}$ Setup Before CLKIN	6		6		ns
t_{HHBGI}	$\overline{HBG}$ Hold After CLKIN	1		1		ns
Switching Characteristics						
t_{DHBGO}	$\overline{HBG}$ Delay After CLKIN		7		7	ns
t_{HHBGO}	$\overline{HBG}$ Hold After CLKIN	1.5		1.5		ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{CS}$ and $\overline{HBR}$ Low[2]		10		10	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{HBG}$[2]	t_{CKOP} + 14		t_{CKOP} + 12		ns
t_{ARDYTR}	REDY (A/D) Disable from $\overline{CS}$ or $\overline{HBR}$ High[2]		11		11	ns

[1] Only required for recognition in the current cycle.
[2] (O/D) = open drain, (A/D) = active drive.

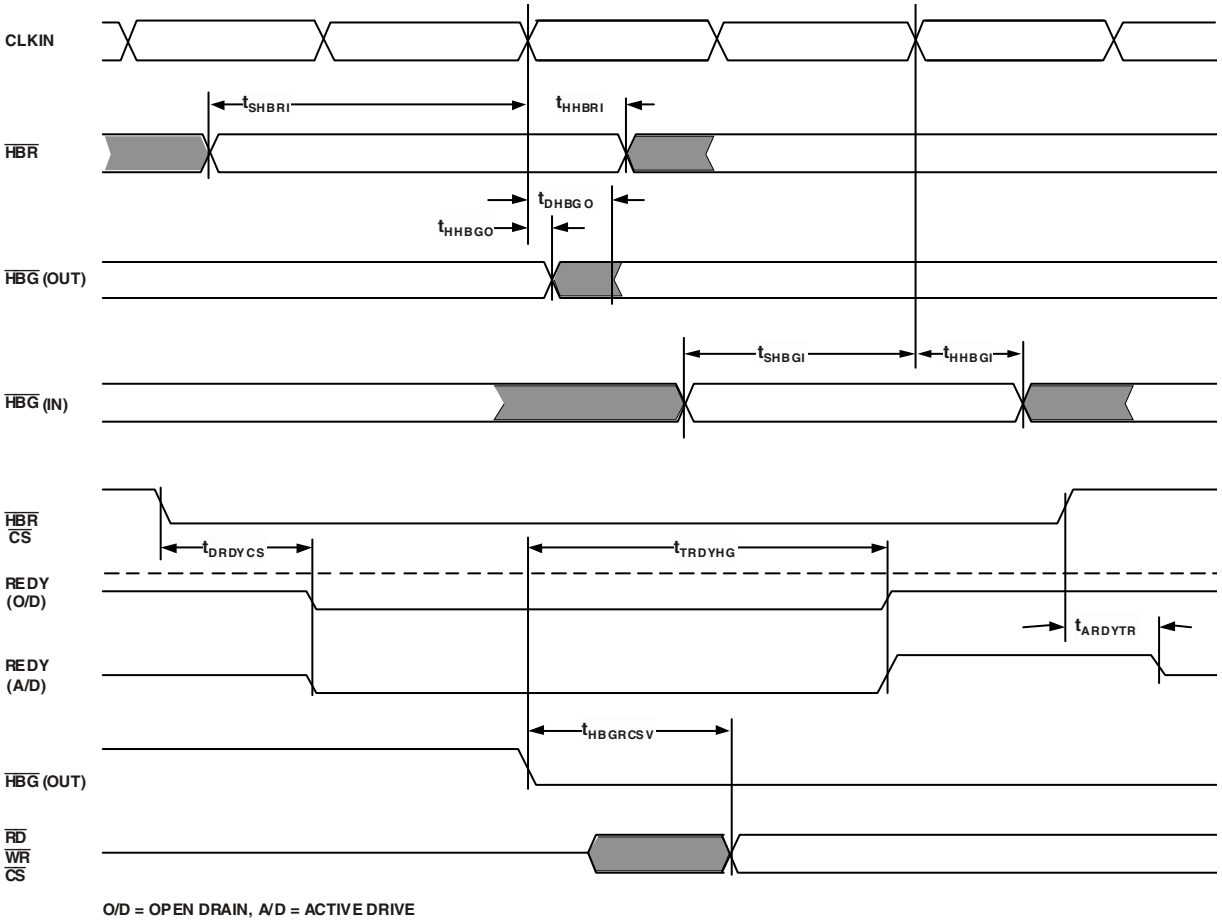


Figure 21. Host Bus Request

Multiprocessor Bus Request

Use these specifications for passing of bus mastership between multiprocessing ADSP-21161Ns ($\overline{BRx}$).

Table 21. Multiprocessor Bus Request

Parameter		Min	Max	Unit
Timing Requirements				
t_{SBRI}	$\overline{BRx}$ Setup Before CLKIN High	9		ns
t_{HBRI}	$\overline{BRx}$ Hold After CLKIN High	0.5		ns
t_{SPAI}	$\overline{PA}$ Setup Before CLKIN High	9		ns
t_{HPAI}	$\overline{PA}$ Hold After CLKIN High	1		ns
t_{SRPBAI}	RPBA Setup Before CLKIN High	6		ns
t_{HRPBAI}	RPBA Hold After CLKIN High	2		ns
Switching Characteristics				
t_{DBRO}	$\overline{BRx}$ Delay After CLKIN High		8	ns
t_{HBRO}	$\overline{BRx}$ Hold After CLKIN High	1.0		ns
t_{DPASO}	$\overline{PA}$ Delay After CLKIN High, Slave		8	ns
t_{TRPAS}	$\overline{PA}$ Disable After CLKIN High, Slave	1.5		ns
t_{DPAMO}	$\overline{PA}$ Delay After CLKIN High, Master		$0.25t_{CCLK}+9$	ns
t_{PATR}	$\overline{PA}$ Disable Before CLKIN High, Master	$0.25t_{CCLK}-5$		ns

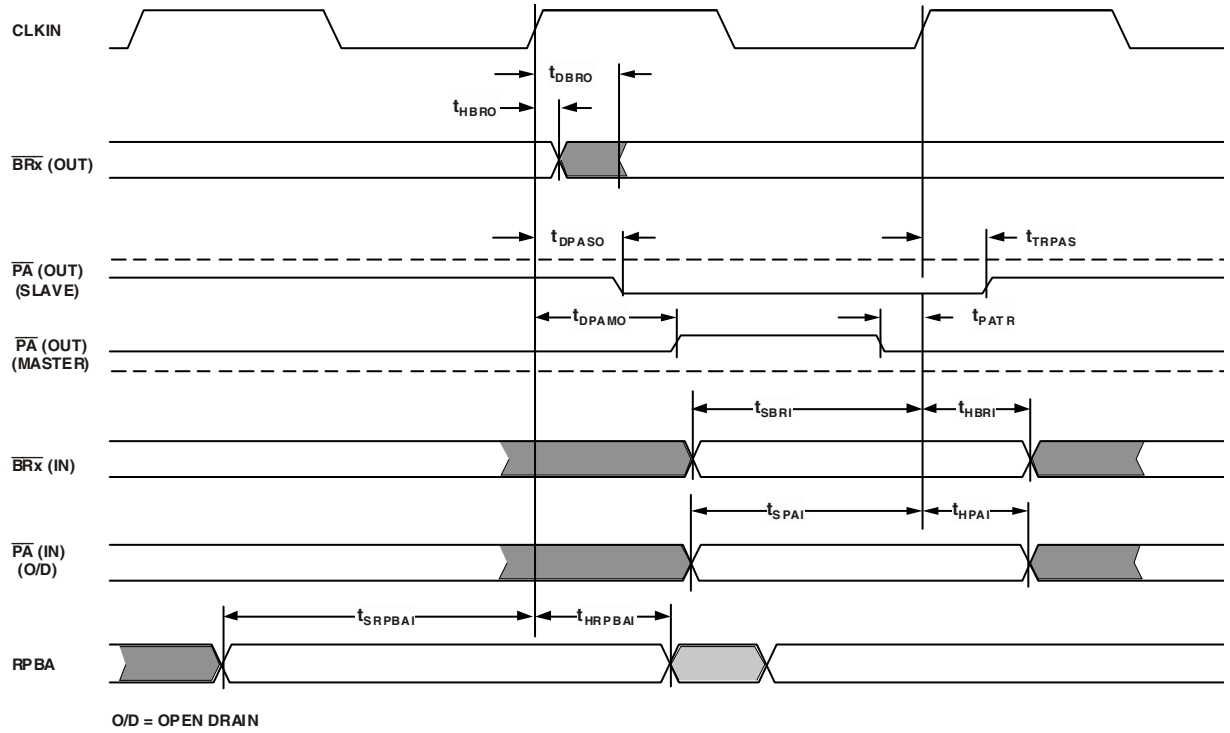


Figure 22. Multiprocessor Bus Request

Asynchronous Read/Write — Host to ADSP-21161N

Use these specifications for asynchronous host processor accesses of an ADSP-21161N, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the ADSP-21161N, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the ADSP-21161N's IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing. Although the DSP will recognize $\overline{HBR}$ asserted before reset, a $\overline{HBG}$ will not be returned by the DSP until after reset is deasserted and the DSP completes bus synchronization. **Note**: *Host internal memory access is not supported.*

Table 22. Read Cycle

Parameter		Min	Max	Unit
Timing Requirements				
t_{SADRDL}	Address Setup and $\overline{CS}$ Low Before $\overline{RD}$ Low	0		ns
t_{HADRDH}	Address Hold and $\overline{CS}$ Hold Low After $\overline{RD}$	2		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	3.5		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (O/D) Disable	0		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (A/D) Disable	0		ns
Switching Characteristics				
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	2		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{RD}$ Low		10	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulsewidth for Read	$1.5t_{CCLK}$		ns
t_{HDARWH}	Data Disable After $\overline{RD}$ High	2	6	ns

Table 23. Write Cycle

Parameter		Min	Max	Unit
Timing Requirements				
t_{SCSWRL}	$\overline{CS}$ Low Setup Before $\overline{WR}$ Low	0		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold After $\overline{WR}$ High	0		ns
t_{SADWRH}	Address Setup Before $\overline{WR}$ High	6		ns
t_{HADWRH}	Address Hold After $\overline{WR}$ High	2		ns
t_{WWRL}	$\overline{WR}$ Low Width	$t_{CCLK}+1$		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	3.5		ns
$t_{DWRHRDY}$	$\overline{WR}$ High Delay After REDY (O/D) or (A/D) Disable	0		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	5		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	4		ns
Switching Characteristics				
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{WR}$/$\overline{CS}$ Low[1]		11	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulsewidth for Write[1]	12		ns

[1] Only when slave write FIFO is full.

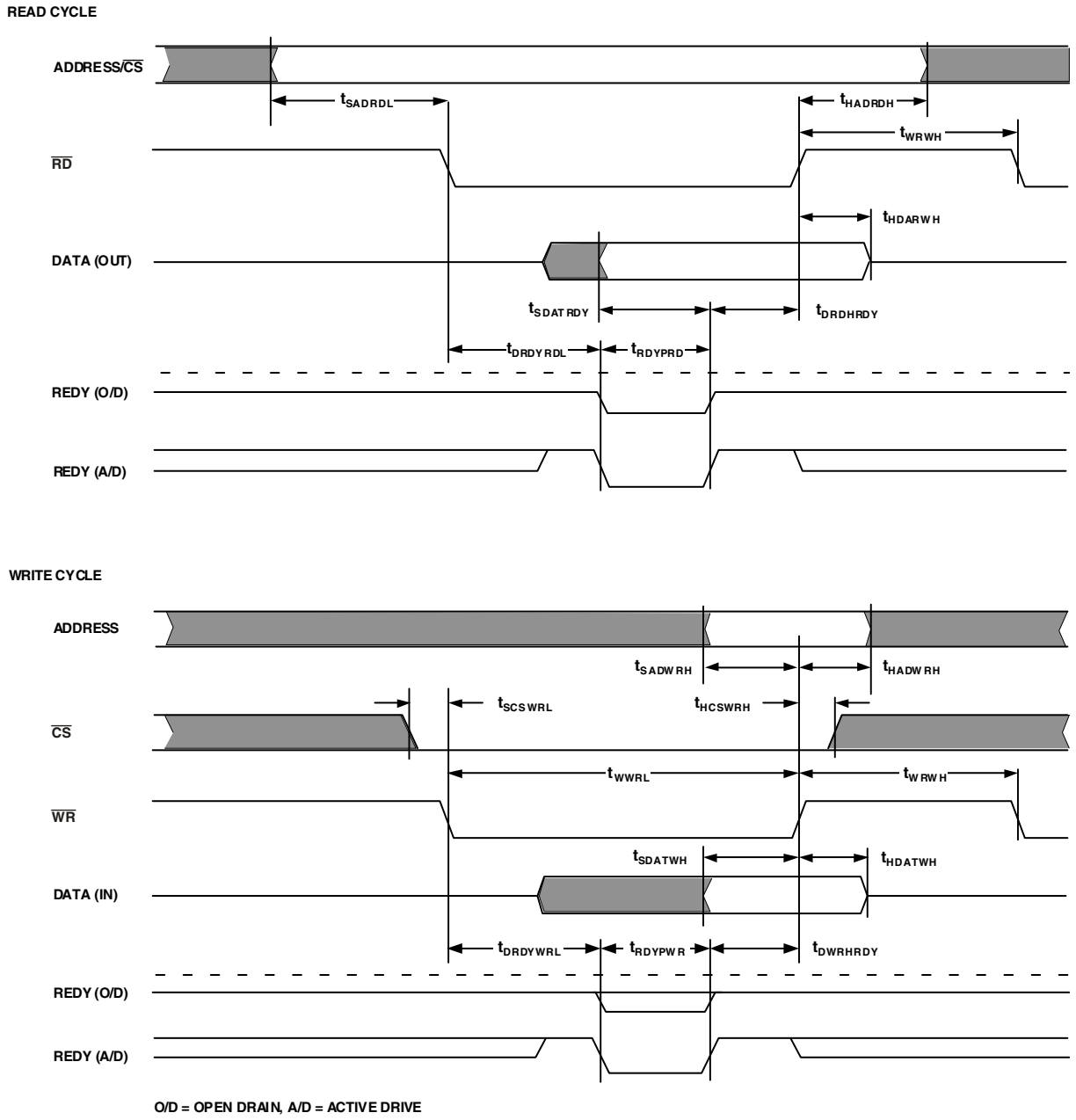


Figure 23. Asynchronous Read/Write — Host to ADSP-21161N

Three-State Timing — Bus Master, Bus Slave

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{SBTS}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{SBTS}$ pin.

During reset, the DSP will not respond to $\overline{SBTS}$, $\overline{HBR}$, and MMS accesses. Although the DSP will recognize $\overline{HBR}$ asserted before reset, a $\overline{HBG}$ will not be returned by the DSP until after reset is deasserted and the DSP completes bus synchronization.

Table 24. Three-State Timing — Bus Master, Bus Slave

Parameter		Min	Max	Unit
Timing Requirements				
t_{STSCK}	$\overline{SBTS}$ Setup Before CLKIN	6		ns
t_{HTSCK}	$\overline{SBTS}$ Hold After CLKIN	2		ns
Switching Characteristics				
t_{MIENA}	Address/Select Enable After CLKIN High	1.5	9	ns
t_{MIENS}	Strobes Enable After CLKIN High[1]	–1.5	+9	ns
t_{MIENHG}	$\overline{HBG}$ Enable After CLKIN	1.5	9	ns
t_{MITRA}	Address/Select Disable After CLKIN High	$0.5t_{CKOP}–20$	$0.5t_{CKOP}–15$	ns
t_{MITRS}	Strobes Disable After CLKIN High	$t_{CKOP}– 0.25t_{CCLK}–17$	$t_{CKOP}– 0.25t_{CCLK}–12.5$	ns
t_{MITRHG}	$\overline{HBG}$ Disable After CLKIN[2]	$0.5t_{CKOP}+N\times t_{CCLK}–20$	$0.5t_{CKOP}+N\times t_{CCLK}–15$	ns
t_{DATEN}	Data Enable After CLKIN[3]	1.5	10	ns
t_{DATTR}	Data Disable After CLKIN[3]	1.5	6	ns
t_{ACKEN}	ACK Enable After CLKIN High	1.5	9	ns
t_{ACKTR}	ACK Disable After CLKIN High	0.2	5	ns
t_{CDCEN}	CLKOUT Enable After CLKIN[2]	$0.5t_{CKOP}+N\times t_{CCLK}$	$0.5t_{CKOP}+N\times t_{CCLK}+5$	ns
t_{CDCTR}	CLKOUT Disable After CLKIN	$t_{CKOP}–5$	t_{CKOP}	ns
t_{ATRHBG}	Address/Select Disable Before $\overline{HBG}$ Low[4]	$1.5t_{CKOP}–6$	$1.5t_{CKOP}+2$	ns
t_{STRHBG}	$\overline{RD}/\overline{WR}/\overline{DMAGx}$ Disable Before $\overline{HBG}$ Low[4]	$t_{CKOP}+ 0.25t_{CCLK}–4$	$t_{CKOP}+ 0.25t_{CCLK}+3$	ns
t_{BTRHBG}	$\overline{BMS}$ Disable Before $\overline{HBG}$ Low[4]	$0.5t_{CKOP}–4$	$0.5t_{CKOP}+2$	ns
t_{MENHBG}	Memory Interface Enable After $\overline{HBG}$ High[4]	$t_{CKOP}–5$	$t_{CKOP}+5$	ns

[1] Strobes = $\overline{RD}$, $\overline{WR}$, $\overline{DMAGx}$.
[2] Where N = 0.5, 1.0, 1.5 for 1:2, 1:3, and 1:4, respectively.
[3] In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.
[4] Memory Interface = Address, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{DMAGx}$, and $\overline{BMS}$ (in EPROM boot mode). $\overline{BMS}$ is only an output in EPROM boot mode.

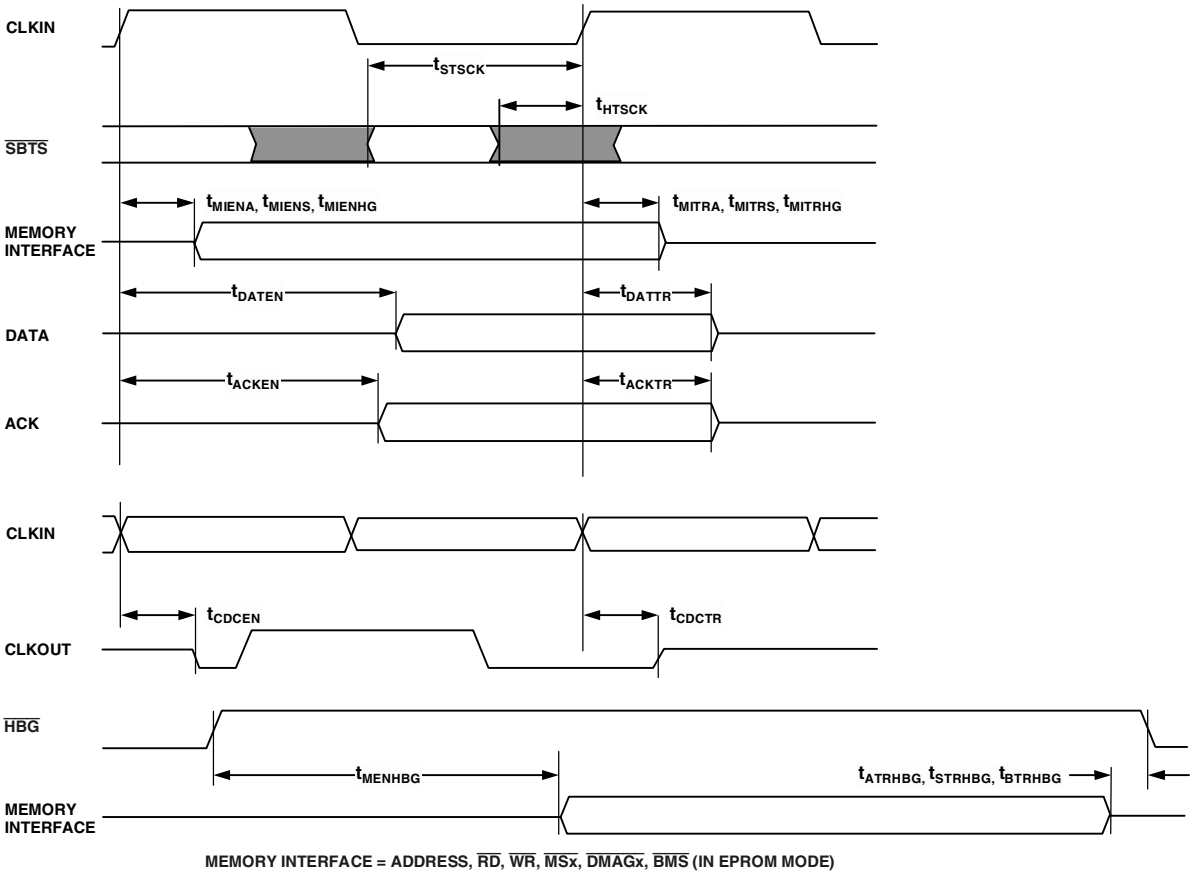


Figure 24. Three-State Timing — Bus Master, Bus Slave

DMA Handshake

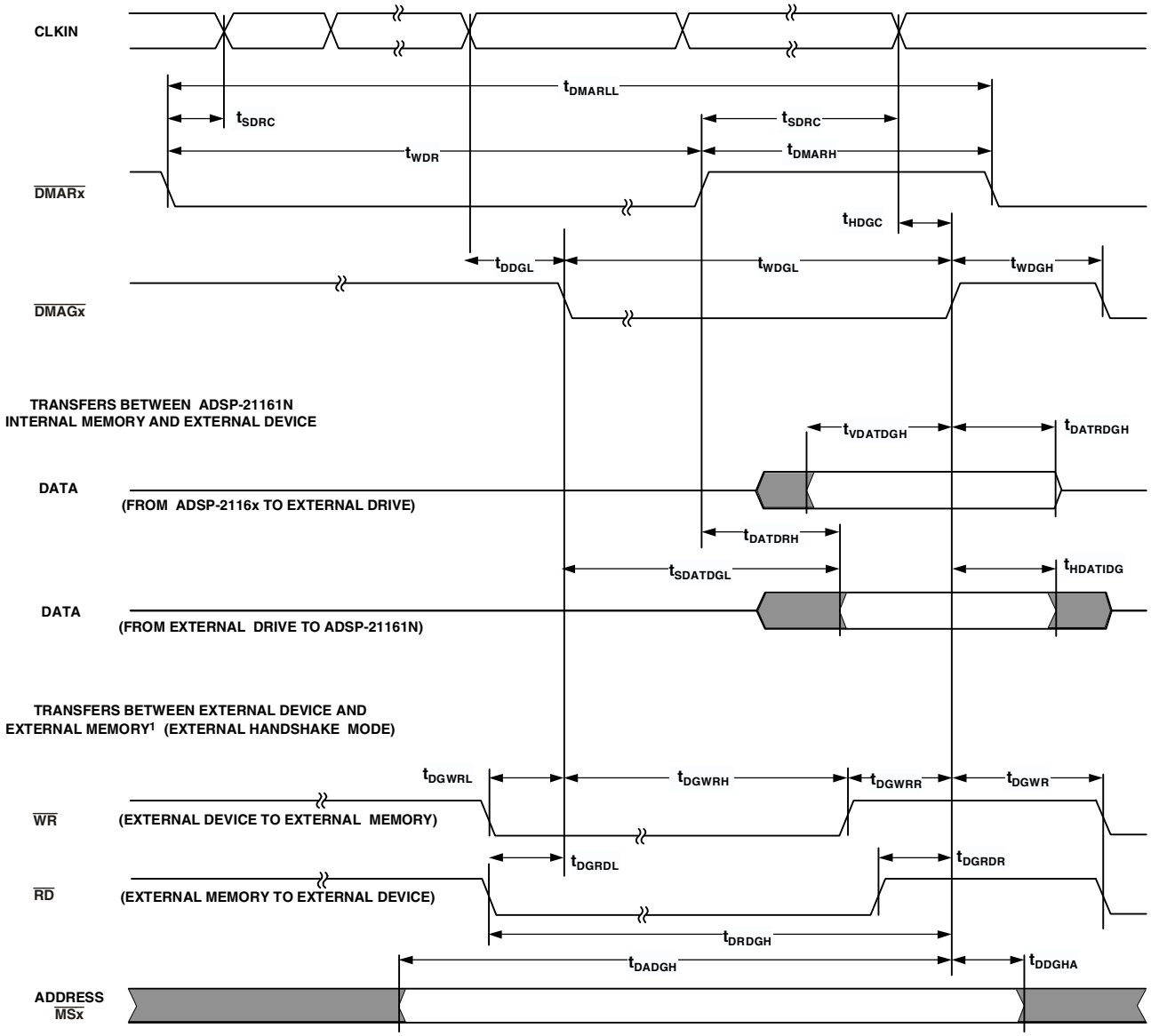
These specifications describe the three DMA handshake modes. In all three modes $\overline{DMAR}$ is used to initiate transfers. For handshake mode, $\overline{DMAG}$ controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the ADDR23–0, $\overline{RD}$, $\overline{WR}$, $\overline{MS3–0}$, ACK, and $\overline{DMAG}$ signals. For Paced Master mode, the data transfer is controlled by ADDR23–0, $\overline{RD}$, $\overline{WR}$, $\overline{MS3–0}$, and ACK (not $\overline{DMAG}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for ADDR23–0, $\overline{RD}$, $\overline{WR}$, $\overline{MS3–0}$, DATA47–16, and ACK also apply.

Table 25. DMA Handshake

		100 MHz		110 MHz		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements						
t_{SDRC}	$\overline{DMARx}$ Setup Before CLKIN[1]	3.5		3.5		ns
t_{WDR}	$\overline{DMARx}$ Width Low (Nonsynchronous)[2]	$t_{CCLK}+4.5$		$t_{CCLK}+4.5$		ns
$t_{SDATDGL}$	Data Setup After $\overline{DMAGx}$ Low[3]		$t_{CKOP}-0.5t_{CCLK}-7$		$t_{CKOP}-0.5t_{CCLK}-7$	ns
$t_{HDATIDG}$	Data Hold After $\overline{DMAGx}$ High	2		2		ns
t_{DATDRH}	Data Valid After $\overline{DMARx}$ High[3]		$t_{CKOP}+3$		$t_{CKOP}+3$	ns
t_{DMARLL}	$\overline{DMARx}$ Low Edge to Low Edge[4]	t_{CKOP}		t_{CKOP}		ns
t_{DMARH}	$\overline{DMARx}$ Width High[2]	$t_{CCLK}+4.5$		$t_{CCLK}+4.5$		ns
Switching Characteristics						
t_{DDGL}	$\overline{DMAGx}$ Low Delay After CLKIN	$0.25t_{CCLK}+1$	$0.25t_{CCLK}+9$	$0.25t_{CCLK}+1$	$0.25t_{CCLK}+9$	ns
t_{WDGH}	$\overline{DMAGx}$ High Width	$0.5t_{CCLK}-1+HI$		$0.5t_{CCLK}-1+HI$		ns
t_{WDGL}	$\overline{DMAGx}$ Low Width	$t_{CKOP}-0.5t_{CCLK}-1$		$t_{CKOP}-0.5t_{CCLK}-1$		ns
t_{HDGC}	$\overline{DMAGx}$ High Delay After CLKIN	$t_{CKOP}-0.25t_{CCLK}+1.0$	$t_{CKOP}-0.25t_{CCLK}+9$	$t_{CKOP}-0.25t_{CCLK}+1.0$	$t_{CKOP}-0.25t_{CCLK}+9$	ns
$t_{VDATDGH}$	Data Valid Before $\overline{DMAGx}$ High[5]	$t_{CKOP}-0.25t_{CCLK}-8$	$t_{CKOP}-0.25t_{CCLK}+5$	$t_{CKOP}-0.25t_{CCLK}-8$	$t_{CKOP}-0.25t_{CCLK}+5$	ns
$t_{DATRDGH}$	Data Disable After $\overline{DMAGx}$ High[6]	$0.25t_{CCLK}-3$	$0.25t_{CCLK}+4$	$0.25t_{CCLK}-3$	$0.25t_{CCLK}+4$	ns
t_{DGWRL}	$\overline{WRx}$ Low Before $\overline{DMAGx}$ Low	–1.5	+2	–1.5	+2	ns
t_{DGWRH}	$\overline{DMAGx}$ Low Before $\overline{WRx}$ High	$t_{CKOP}-0.5t_{CCLK}-2+W$		$t_{CKOP}-0.5t_{CCLK}-2+W$		ns
t_{DGWRR}	$\overline{WRx}$ High Before $\overline{DMAGx}$ High[7]	–1.5	+2	–1.5	+2	ns
t_{DGRDL}	$\overline{RDx}$ Low Before $\overline{DMAGx}$ Low	–1.5	+2	–1.5	+2	ns
t_{DRDGH}	$\overline{RDx}$ Low Before $\overline{DMAGx}$ High	$t_{CKOP}-0.5t_{CCLK}-2+W$		$t_{CKOP}-0.5t_{CCLK}-2+W$		ns
t_{DGRDR}	$\overline{RDx}$ High Before $\overline{DMAGx}$ High[7]	–1.5	+2	–1.5	+2	ns
t_{DGWR}	$\overline{DMAGx}$ High to $\overline{WRx}$, $\overline{RDx}$ Low	$0.5t_{CCLK}-2+HI$		$0.5t_{CCLK}-2+HI$		ns
t_{DADGH}	Address/Select Valid to $\overline{DMAGx}$ High	15		13		ns
t_{DDGHA}	Address/Select Hold After $\overline{DMAGx}$ High	1		1		ns

W = (number of wait states specified in WAIT register) × t_{CKOP}.
HI = t_{CKOP} (if data bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

[1] Only required for recognition in the current cycle.
[2] Maximum throughput (@ 110 MHz) using $\overline{DMARx}$/$\overline{DMAGx}$ handshaking equals $t_{WDR} + t_{DMARH} = (t_{CCLK}+4.5) + (t_{CCLK}+4.5) = 27$ ns (37 MHz). This throughput limit applies to non-synchronous access mode only.
[3] $t_{SDATDGL}$ is the data setup requirement if $\overline{DMARx}$ is not being used to hold off completion of a write. Otherwise, if $\overline{DMARx}$ low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{DMARx}$ is brought high.
[4] Use t_{DMARLL} if $\overline{DMARx}$ transitions synchronous with CLKIN. Otherwise, use t_{WDR} and t_{DMARH}.
[5] $t_{VDATDGH}$ is valid if $\overline{DMARx}$ is not being used to hold off completion of a read. If $\overline{DMARx}$ is used to prolong the read, then $t_{VDATDGH} = t_{CKOP} - 0.25t_{CCLK} - 8 + (n \times t_{CKOP})$ where n equals the number of extra cycles that the access is prolonged.
[6] See Example System Hold Time Calculation on Page 54 for calculation of hold times given capacitive and dc loads.
[7] This parameter applies for synchronous access mode only.



[1]MEMORY READ BUS MASTER, MEMORY WRITE BUS MASTER, OR SYNCHRONOUS READ/WRITE BUS MASTER TIMING SPECIFICATIONS FOR ADDR23–0, $\overline{RD}$, $\overline{WR}$, $\overline{MS3\text{-}0}$ AND ACK ALSO APPLY HERE.

Figure 25. DMA Handshake

SDRAM Interface — Bus Master

Use these specifications for ADSP-21161N bus master accesses of SDRAM:

Table 26. SDRAM Interface — Bus Master

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
t_{SDSDK}	Data Setup Before SDCLK	2.0		2.0		ns
t_{HDSDK}	Data Hold After SDCLK	2.3		2.3		ns
Switching Characteristics						
t_{DSDK1}	First SDCLK Rise Delay After CLKIN[1, 2]	$0.75t_{CCLK} + 1.5$	$0.75t_{CCLK} + 8.0$	$0.75t_{CCLK} + 1.5$	$0.75t_{CCLK} + 8.0$	ns
t_{SDK}	SDCLK Period	t_{CCLK}	$2 \times t_{CCLK}$	t_{CCLK}	$2 \times t_{CCLK}$	ns
t_{SDKH}	SDCLK Width High	4		3		ns
t_{SDKL}	SDCLK Width Low	4		3		ns
$t_{DCADSDK}$	Command, Address, Data, Delay After SDCLK[3]		$0.25t_{CCLK} +2.5$		$0.25t_{CCLK} +2.5$	ns
$t_{HCADSDK}$	Command, Address, Data, Hold After SDCLK[3]	2.0		2.0		ns
$t_{SDTRSDK}$	Data Three-State After SDCLK[4]		$0.5t_{CCLK} + 2.0$		$0.5t_{CCLK} + 2.0$	ns
$t_{SDENSDK}$	Data Enable After SDCLK[5]	$0.75t_{CCLK}$		$0.75t_{CCLK}$		ns
t_{SDCTR}	Command Three-State After CLKIN	$0.5t_{CCLK} - 1.5$	$0.5t_{CCLK} + 6.0$	$0.5t_{CCLK} - 1.5$	$0.5t_{CCLK} + 6.0$	ns
t_{SDCEN}	Command Enable After CLKIN	2	5	2	5	ns
$t_{SDSDKTR}$	SDCLK Three-State After CLKIN	0	3	0	3	ns
$t_{SDSDKEN}$	SDCLK Enable After CLKIN	1	4	1	4	ns
t_{SDATR}	Address Three-State After CLKIN	$-0.25\ t_{CCLK} - 5$	$-0.25t_{CCLK}$	$-0.25\ t_{CCLK} - 5$	$-0.25t_{CCLK}$	ns
t_{SDAEN}	Address Enable After CLKIN	−0.4	+7.2	−0.4	+7.2	ns

[1] For the second, third, and fourth rising edges of SDCLK delay from CLKIN, add appropriate number of SDCLK period to the t_{DSDK1} and t_{SSDKC1} values, depending upon the SDCKR value and the core clock to CLKIN ratio.
[2] Subtract t_{CCLK} from result if value is greater than or equal to t_{CCLK}.
[3] Command = SDCKE, $\overline{MSx}$, DQM, $\overline{RAS}$, $\overline{CAS}$, SDA10, and $\overline{SDWE}$.
[4] SDRAM Controller adds one SDRAM CLK three-stated cycle delay on a read, followed by a write.
[5] Valid when DSP transitions to SDRAM master from SDRAM slave.

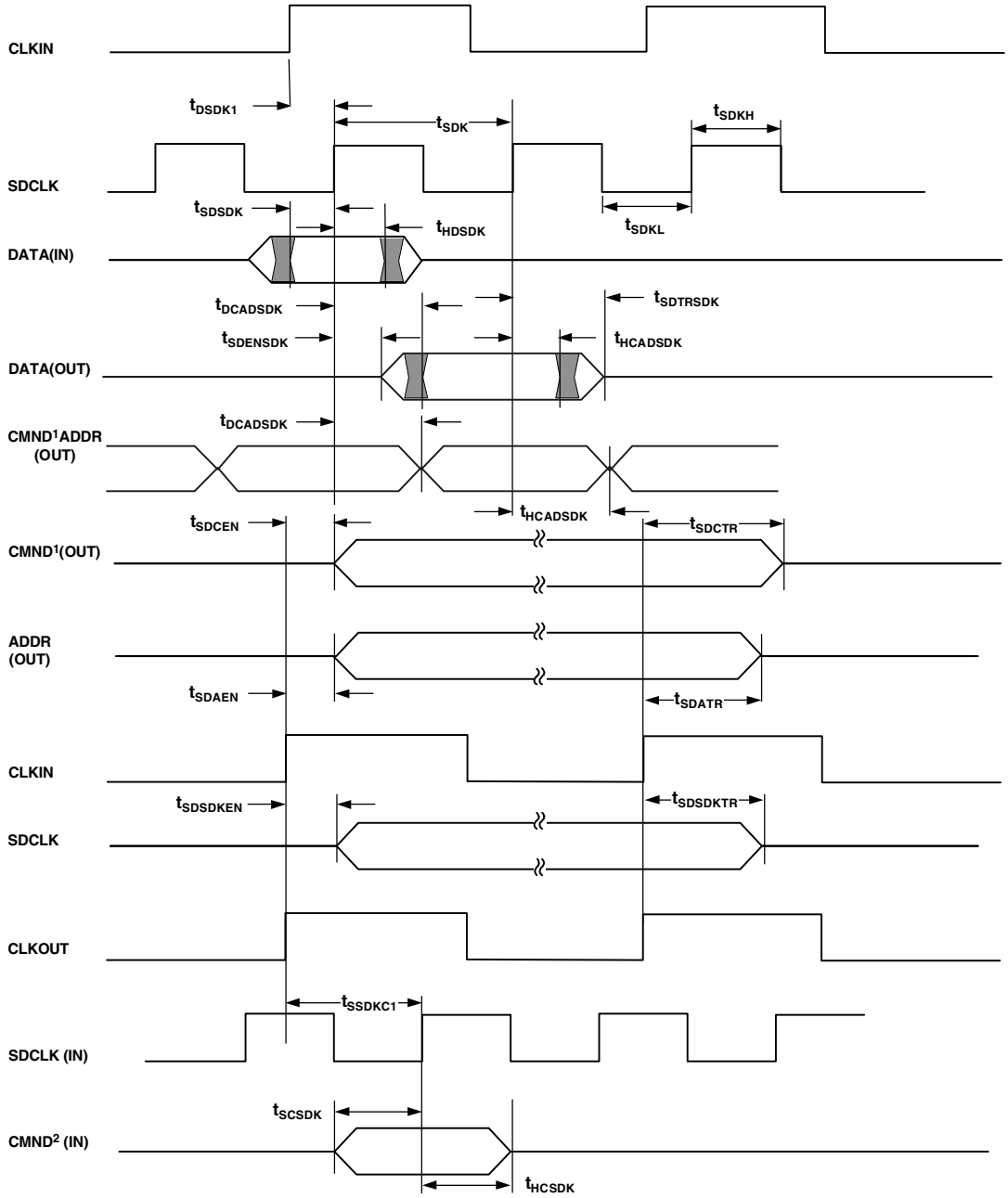
SDRAM Interface — Bus Slave

These timing requirements allow a bus slave to sample the bus master's SDRAM command and detect when a refresh occurs:

Table 27. SDRAM Interface — Bus Slave

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDKC1}	First SDCLK Rise after CLKOUT[1, 2, 3]	$SDCK \times t_{CCLK} - 0.5t_{CCLK} - 0.5$	$SDCKR \times t_{CCLK} - 0.25t_{CCLK} + 2.0$	ns
t_{SCSDK}	Command Setup before SDCLK[4]	2		ns
t_{HCSDK}	Command Hold after SDCLK[4]	1		ns

[1] For the second, third, and fourth rising edges of SDCLK delay from CLKOUT, add appropriate number of SDCLK period to the t_{DSDK1} and t_{SSDKC1} values, depending upon the SDCKR value and the Core clock to CLKOUT ratio.
[2] SDCKR = 1 for SDCLK equal to core clock frequency and SDCKR = 2 for SDCLK equal to half core clock frequency.
[3] Subtract t_{CCLK} from result if value is greater than or equal to t_{CCLK}.
[4] Command = SDCKE, $\overline{RAS}$, $\overline{CAS}$, and $\overline{SDWE}$.



[1]COMMAND = SDCKE, $\overline{\text{MSx}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{SDWE}}$, DQM, AND SDA10.
[2]COMMAND = SDCKE, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, AND $\overline{\text{SDWE}}$.

Figure 26. SDRAM Interface

Link Ports

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA relative to LCLK, (setup skew = $t_{LCLKTWH}$ min − t_{DLDCH} − t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LCLK relative to LDATA, (hold skew = $t_{LCLKTWL}$ min − t_{HLDCH} − t_{HLDCL}). Calculations made directly from speed specifications will result in unrealistically small skew times because they include multiple tester guardbands. The setup and hold skew times shown below are calculated to include only one tester guardband.

ADSP-21161N Setup Skew = 1.5 ns max

ADSP-21161N Hold Skew = 1.5 ns max

Note that there is a two-cycle effect latency between the link port enable instruction and the DSP enabling the link port.

Table 28. Link Ports — Receive

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLDCL}	Data Setup Before LCLK Low	1		ns
t_{HLDCL}	Data Hold After LCLK Low	3.5		ns
t_{LCLKIW}	LCLK Period	t_{LCLK}		ns
$t_{LCLKRWL}$	LCLK Width Low	4.0		ns
$t_{LCLKRWH}$	LCLK Width High	4.0		ns
Switching Characteristics				
t_{DLALC}	LACK Low Delay After LCLK High[1]	8	12	ns

[1] LACK goes low with t_{DLALC} relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.

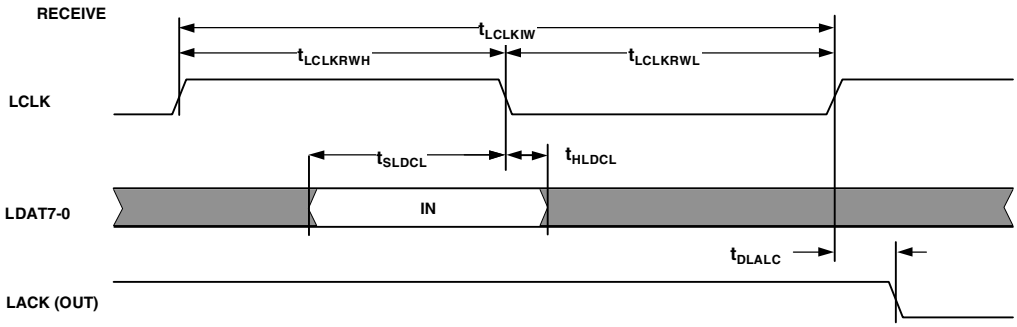


Figure 27. Link Ports—Receive

Table 29. Link Ports — Transmit

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLACH}	LACK Setup Before LCLK High	8		ns
t_{HLACH}	LACK Hold After LCLK High	−2		ns
Switching Characteristics				
t_{DLDCH}	Data Delay After LCLK High		3	ns
t_{HLDCH}	Data Hold After LCLK High	0		ns
$t_{LCLKTWL}$	LCLK Width Low	$0.5t_{LCLK}-1.0$	$0.5t_{LCLK}+1.0$	ns
$t_{LCLKTWH}$	LCLK Width High	$0.5t_{LCLK}-1.0$	$0.5t_{LCLK}+1.0$	ns
t_{DLACLK}	LCLK Low Delay After LACK High	$0.5t_{LCLK}+3$	$3t_{LCLK}+11$	ns

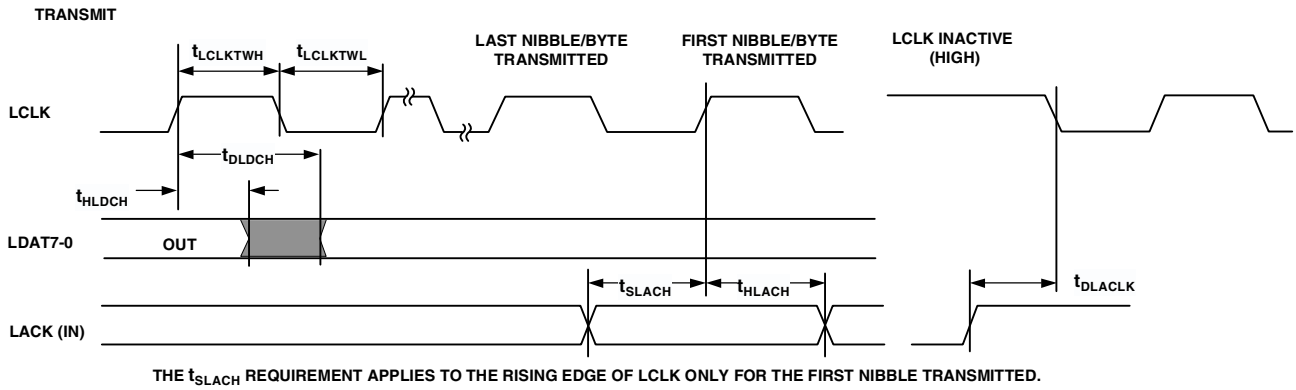


Figure 28. Link Ports—Transmit

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Table 30. Serial Ports — External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}	Transmit/Receive FS Setup Before Transmit/Receive SCLK[1]	3.5		ns
t_{HFSE}	Transmit/Receive FS Hold After Transmit/Receive SCLK[1]	2		ns
t_{SDRE}	Receive Data Setup Before Receive SCLK[1]	1.5		ns
t_{HDRE}	Receive Data Hold After Receive SCLK[1]	4		ns
t_{SCLKW}	SCLKx Width	7		ns
t_{SCLK}	SCLKx Period	$2t_{CCLK}$		ns

[1] Referenced to sample edge.

Table 31. Serial Ports — Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}	FS Setup Time Before SCLK (Transmit/Receive Mode)[1]	8		ns
t_{HFSI}	FS Hold After SCLK (Transmit/Receive Mode)[1]	$0.5t_{CCLK}+1$		ns
t_{SDRI}	Receive Data Setup Before SCLK[1]	4		ns
t_{HDRI}	Receive Data Hold After SCLK[1]	3		ns

[1] Referenced to sample edge.

Table 32. Serial Ports — External Clock

		100 MHz		110 MHz		
Parameter		Min	Max	Min	Max	Unit
Switching Characteristics						
t_{DFSE}	FS Delay After SCLK (Internally Generated FS) [1, 2, 3]		13		13	ns
t_{HOFSE}	FS Hold After SCLK (Internally Generated FS)[1, 2, 3]	3		2.75		ns
t_{DDTE}	Transmit Data Delay After SCLK [1, 2]		16		16	ns
t_{HDTE}	Transmit Data Hold After SCLK [1, 2]	0		0		ns

[1] Referenced to drive edge.
[2] SCLK/FS Configured as a transmit clock/frame sync with the DDIR bit = 1 in SPCTLx register.
[3] SCLK/FS Configured as a receive clock/frame sync with the DDIR bit = 0 in SPCTLx register.

Table 33. Serial Ports — Internal Clock

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	FS Delay After SCLK (Internally Generated FS)[1, 2, 3]		4.5	ns
t_{HOFSI}	FS Hold After SCLK (Internally Generated FS)[1, 2, 3]	–1.5		ns
t_{DDTI}	Transmit Data Delay After SCLK[1, 2]		7.5	ns
t_{HDTI}	Transmit Data Hold After SCLK[1, 2]	0		ns
t_{SCLKIW}	SCLK Width[2]	$0.5t_{SCLK}–2.5$	$0.5t_{SCLK}+2$	ns

[1] Referenced to drive edge.
[2] SCLK/FS Configured as a transmit clock/frame sync with the DDIR bit = 1 in SPCTLx register.
[3] SCLK/FS Configured as a receive clock/frame sync with the DDIR bit = 0 in SPCTLx register.

Table 34. Serial Ports —– Enable and Three-State

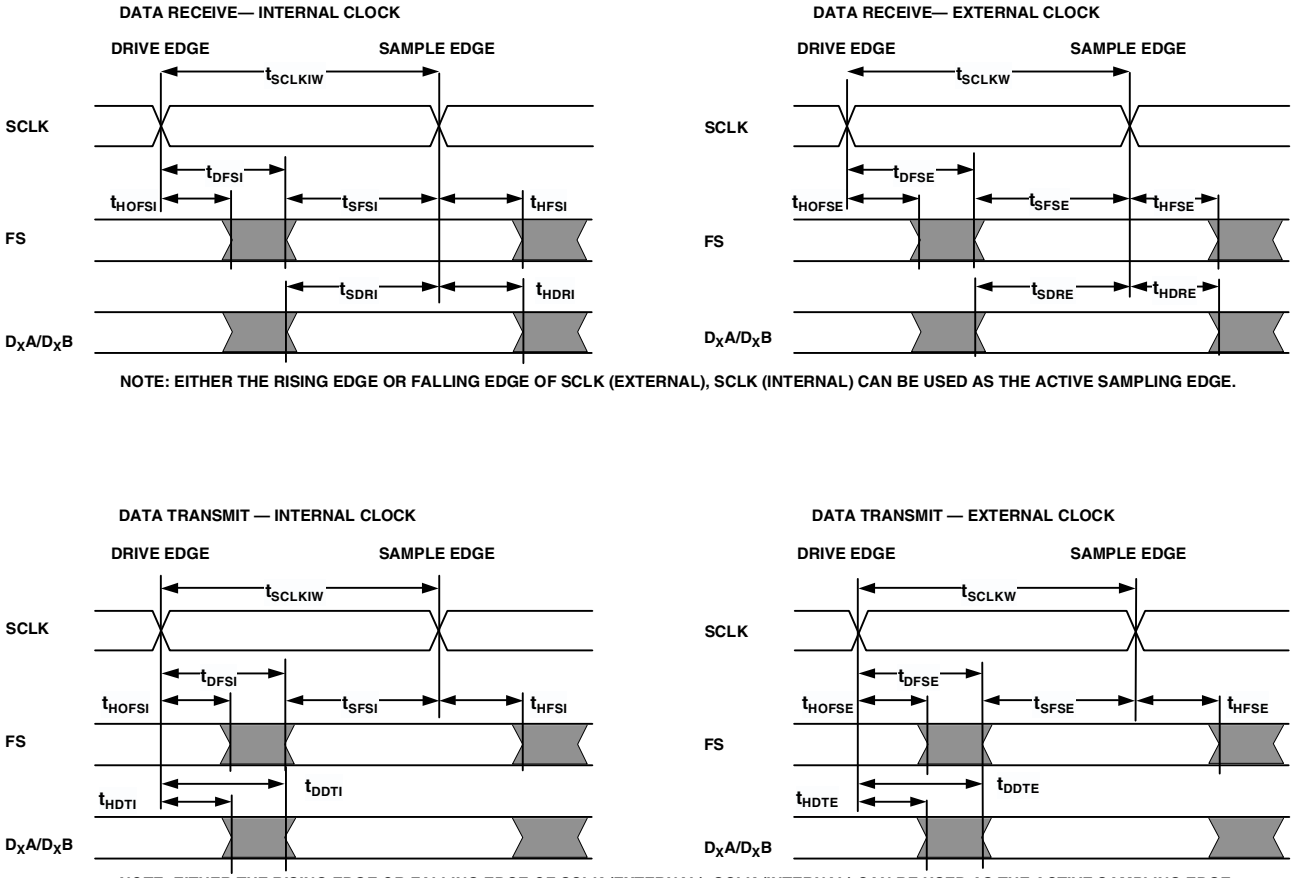
Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External Transmit SCLK[1, 2]	4		ns
t_{DDTTE}	Data Disable from External Transmit SCLK[1]		10	ns
t_{DDTIN}	Data Enable from Internal Transmit SCLK[1]	0		ns
t_{DDTTI}	Data Disable from Internal Transmit SCLK[1]		3	ns

[1] Referenced to drive edge.
[2] SCLK/FS Configured as a transmit clock/frame sync with the DDIR bit = 1 in SPCTLx register.

Table 35. Serial Ports — External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0[1]		13	ns
$t_{DDTENFS}$	Data Enable from Late FS or MCE = 1, MFD = 0[1]	0.5		ns

[1] MCE = 1, Transmit FS enable and Transmit FS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.



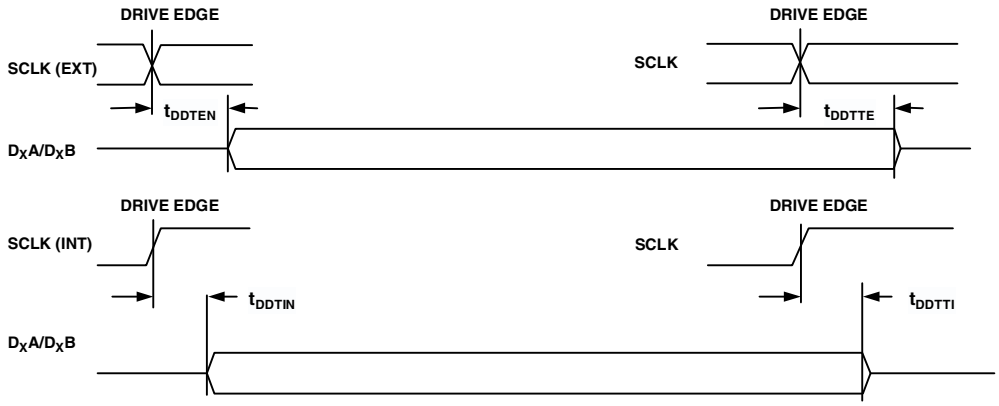


Figure 29. Serial Ports

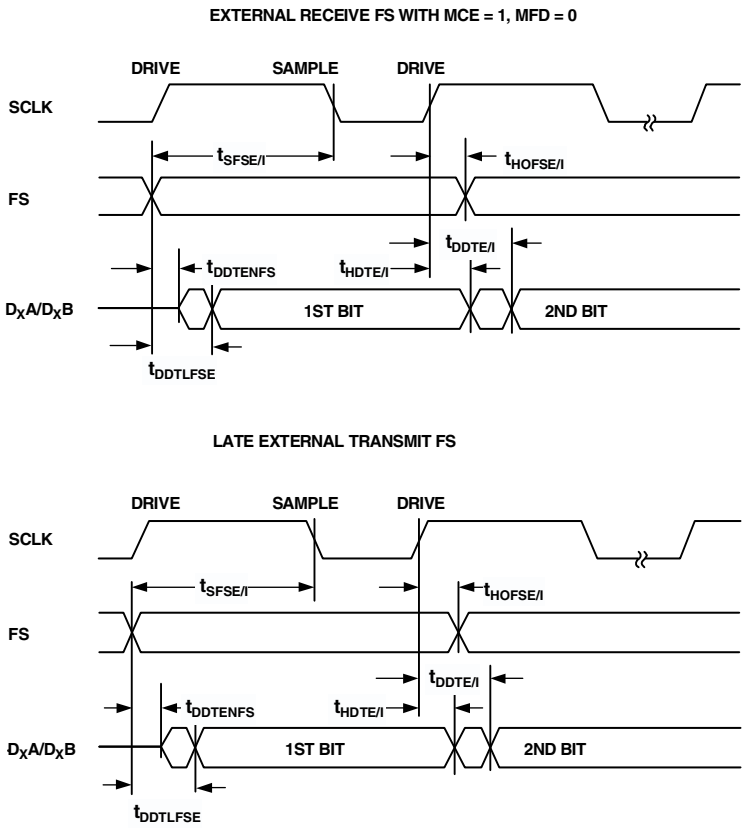


Figure 30. Serial Ports — External Late Frame Sync

SPI Interface Specifications

Table 36. SPI Interface Protocol — Master Switching and Timing

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Set-up Time)	$0.5t_{CCLK}+10$		$0.5t_{CCLK}+10$		ns
t_{HSPIDM}	SPICLK Last Sampling Edge to Data Input Not Valid	$0.5t_{CCLK}+1$		$0.5t_{CCLK}+1$		ns
Switching Characteristics						
$t_{SPICLKM}$	Serial Clock Cycle	$8t_{CCLK}$		$8t_{CCLK}-4$		ns
t_{SPICHM}	Serial Clock High Period	$4t_{CCLK}-4$		$4t_{CCLK}-4$		ns
t_{SPICLM}	Serial Clock Low Period	$4t_{CCLK}-4$		$4t_{CCLK}-4$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		3		3	ns
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	0		0		ns
t_{SDSCIM_0}	FLAG3–0 (SPI Device Select) Low to First SPICLK Edge for CPHASE = 0	$5t_{CCLK}$		$5t_{CCLK}$		ns
t_{SDSCIM_1}	FLAG3–0 (SPI Device Select) Low to First SPICLK Edge for CPHASE = 1	$3t_{CCLK}$		$3t_{CCLK}$		ns
t_{HDSM}	Last SPICLK Edge to FLAG3–0 High	$t_{CCLK}-3$		$t_{CCLK}-3$		ns
t_{SPITDM}	Sequential Transfer Delay	$2t_{CCLK}$		$2t_{CCLK}$		ns

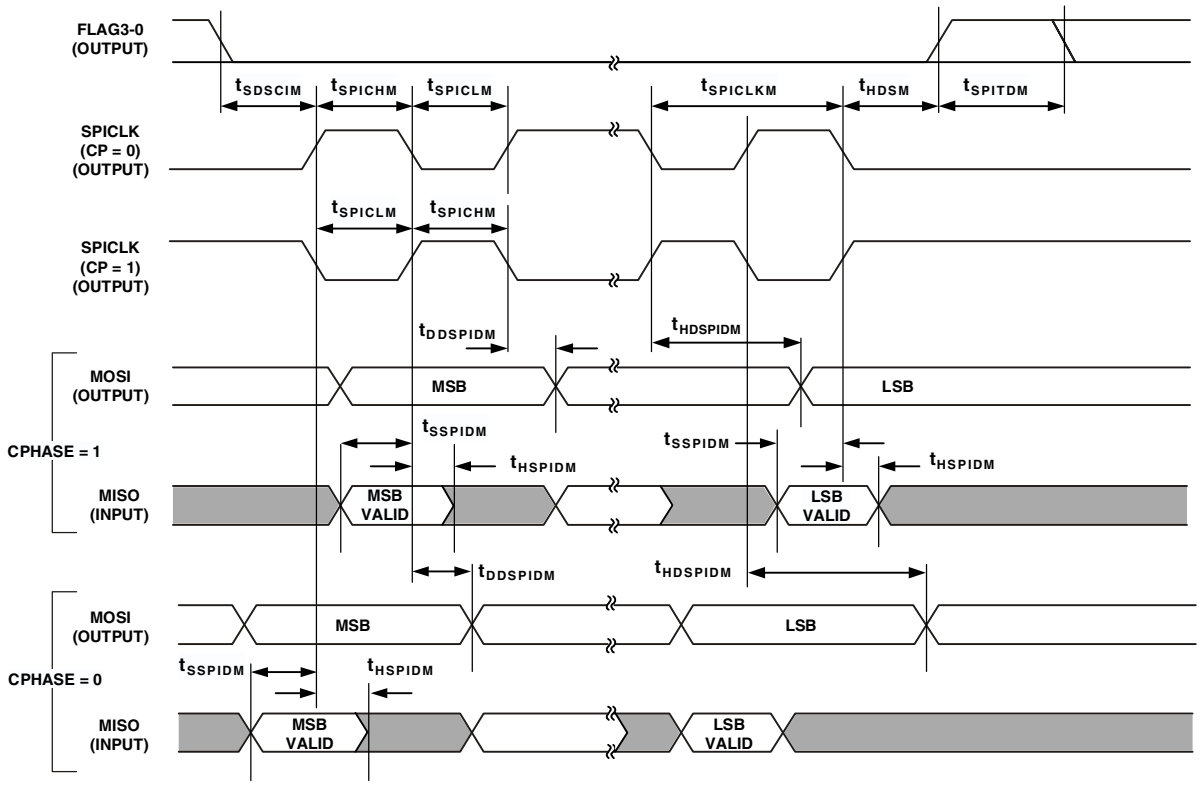


Figure 31. SPI Interface Protocol — Master Switching and Timing

Table 37. SPI Interface Protocol — Slave Switching and Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPICLKS}$	Serial Clock Cycle	$8t_{CCLK}$		ns
t_{SPICHS}	Serial Clock High Period	$4t_{CCLK}–4$		ns
t_{SPICLS}	Serial Clock Low Period	$4t_{CCLK}–4$		ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge			
	CPHASE = 0	$3.5t_{CCLK}+8$		ns
	CPHASE = 1	$1.5t_{CCLK}+8$		ns
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted CPHASE = 0	0		ns
t_{SSPIDS}	Data Input Valid to SPICLK Edge (Data Input Set-up Time)	0		ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	$t_{CCLK}+1$		ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulsewidth (CPHASE = 0)	t_{CCLK}		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	2	$0.5t_{CCLK}+5.5$	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	1.5	$0.5t_{CCLK}+5.5$	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		$0.75t_{CCLK}+3$	ns
$t_{HDSPIDS}$[1]	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$0.25t_{CCLK}+3$		ns
t_{HDLSBS}[1]	SPICLK Edge to Last Bit Out Not Valid (Data Out Hold Time) for LSB	$0.5t_{SPICLK}+4.5t_{CCLK}$		ns
t_{DSOV}[2]	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$1.5t_{CCLK}+7$	ns

[1] When CPHASE = 0 and baud rate is greater than 1, t_{HDLSBS} affects the length of the last bit transmitted.
[2] Applies to the first deassertion of $\overline{SPIDS}$ only.

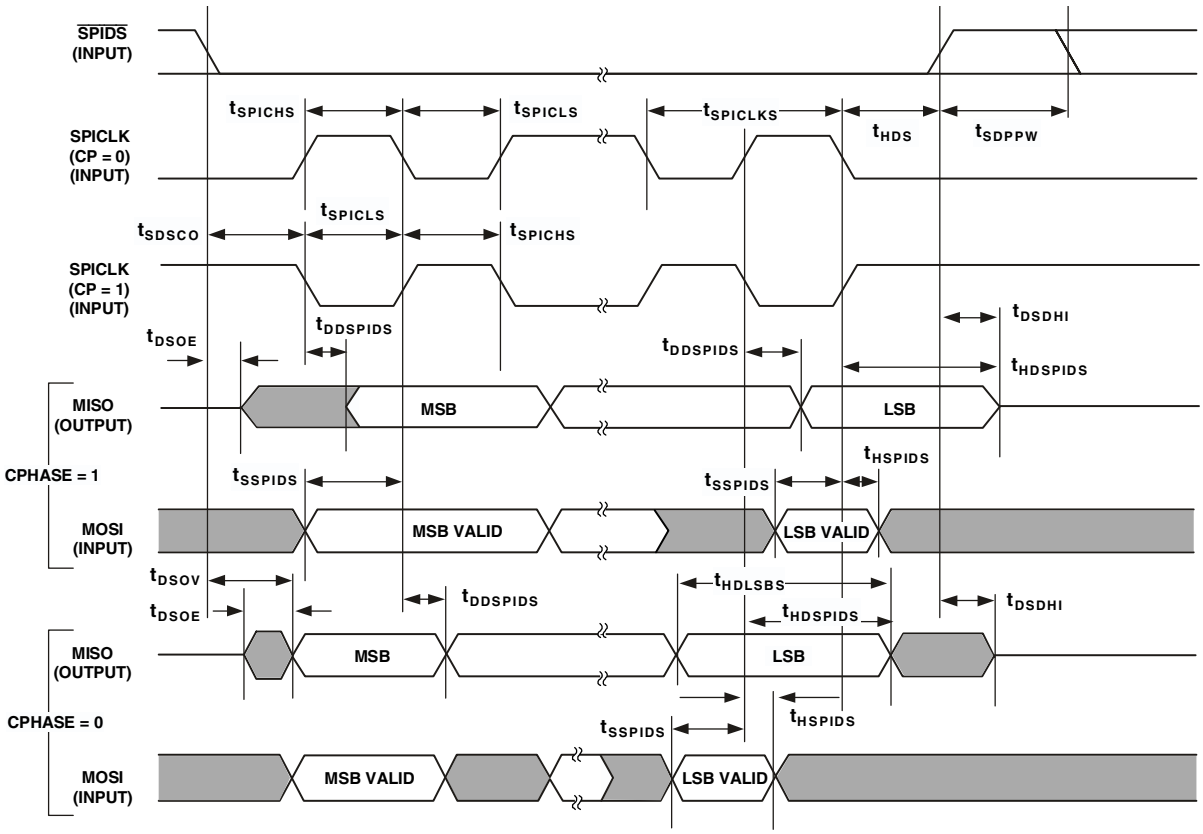


Figure 32. SPI Interface Protocol — Slave Switching and Timing

JTAG Test Access Port and Emulation

Table 38. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	2		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	15		ns
t_{TRSTW}	$\overline{TRST}$ Pulsewidth	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		13	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		30	ns

[1] System Inputs = DATA47–16, ADDR23–0, $\overline{RD}$, $\overline{WR}$, ACK, RPBA, $\overline{SPIDS}$, EBOOT, LBOOT, $\overline{DMAR2–1}$, CLK_CFG1–0, $\overline{CLKDBL}$, $\overline{CS}$, $\overline{HBR}$, $\overline{SBTS}$, ID2–0, $\overline{IRQ2–0}$, $\overline{RESET}$, $\overline{BMS}$, MISO, MOSI, SPICLK, DxA, DxB, SCLKx, FSx, LxDAT7–0, LxCLK, LxACK, $\overline{SDWE}$, $\overline{HBG}$, $\overline{RAS}$, $\overline{CAS}$, SDCLK0, SDCKE, BRST, $\overline{BR6–1}$, $\overline{PA}$, $\overline{MS3–0}$, FLAG11–0.

[2] System Outputs = $\overline{BMS}$, MISO, MOSI, SPICLK, DxA, DxB, SCLKx, FSx, LxDAT7–0, LxCLK, LxACK, DATA47–16, $\overline{SDWE}$, ACK, $\overline{HBG}$, $\overline{RAS}$, $\overline{CAS}$, SDCLK1–0, SDCKE, BRST, $\overline{RD}$, $\overline{WR}$, $\overline{BR6–1}$, $\overline{PA}$, $\overline{MS3–0}$, ADDR23–0, FLAG11–0, $\overline{DMAG2–1}$, DQM, REDY, CLKOUT, SDA10, TIMEXP, $\overline{EMU}$, BMSTR, $\overline{RSTOUT}$.

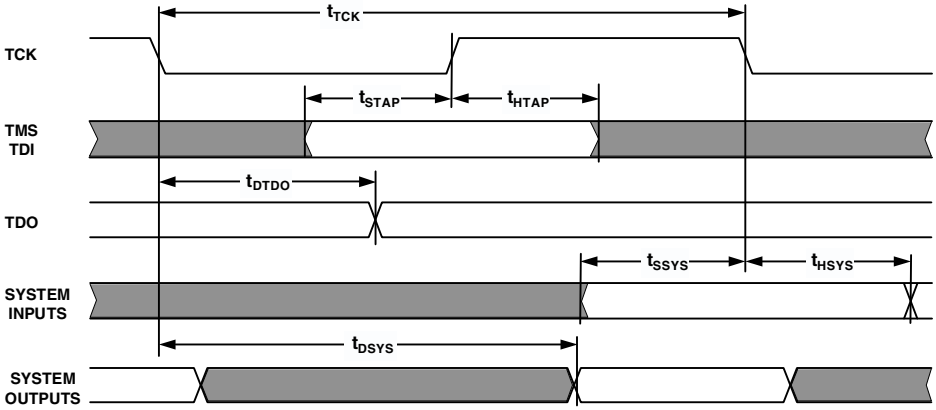


Figure 33. JTAG Test Access Port and Emulation

OUTPUT DRIVE CURRENTS

Figure 34 shows typical I-V characteristics for the output drivers of the ADSP-21161N. The curves represent the current drive capability of the output drivers as a function of output voltage.

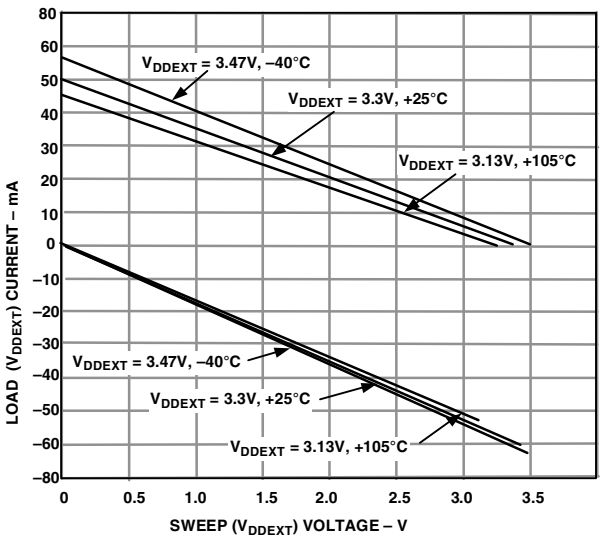


Figure 34. Typical Drive Currents

TEST CONDITIONS

The DSP is tested for output enable, disable, and hold time.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving. The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram (Figure 35). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high-impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 35. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

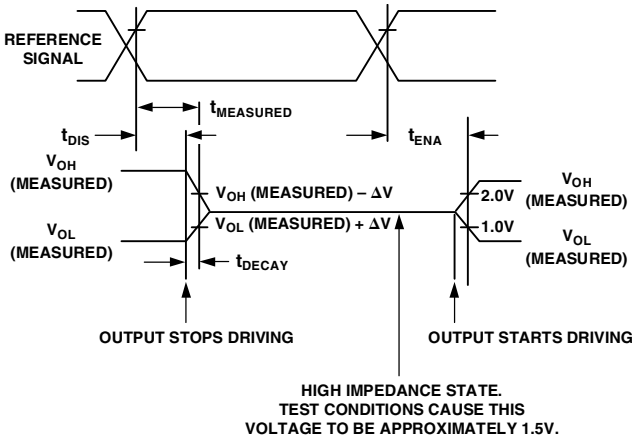


Figure 35. Output Enable/Disable

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21161N's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

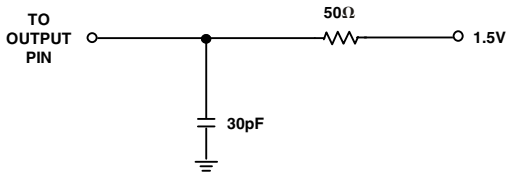


Figure 36. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

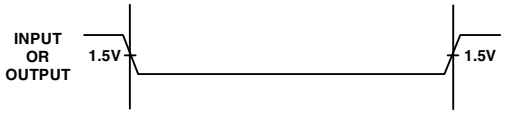


Figure 37. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

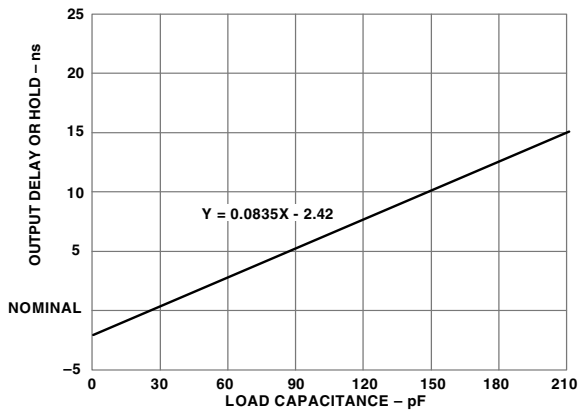


Figure 38. Typical Output Delay or Hold vs. Load Capacitance (at Max Case Temperature)

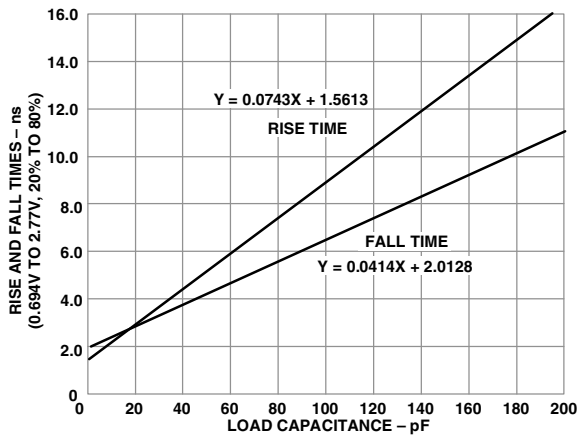


Figure 39. Typical Output Rise/Fall Time (20% – 80%, V_{DDEXT} = Max)

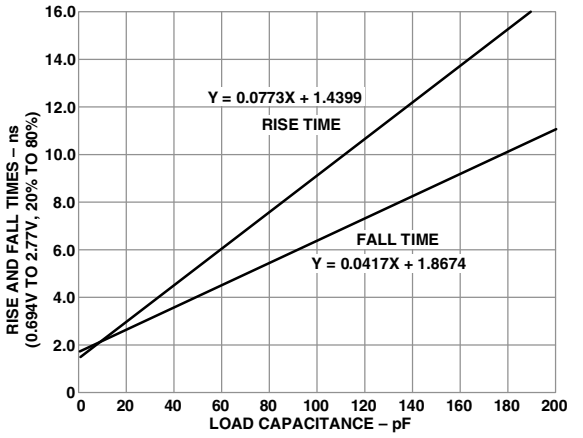


Figure 40. Typical Output Rise/Fall Time (20% – 80%, V_{DDEXT} = Min)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 36 on Page 54). Figure 38 shows graphically how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see Output Disable Time on Page 54.) The graphs of Figure 38, Figure 39, and Figure 40 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% – 80%, V = Min) vs. Load Capacitance.

ENVIRONMENTAL CONDITIONS

The thermal characteristics in which the DSP is operating influence performance.

Thermal Characteristics

The ADSP-21161N is packaged in a 225-ball chip scale package ball grid array (CSP_BGA). The ADSP-21161N is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} data sheet specification is not exceeded, a heatsink and/or an air flow source may be used. Use the center block of ground pins (CSP_BGA balls: F6-10, G6-10, H6-10, J6-10, K6-10) to provide thermal pathways to the printed circuit board's ground plane. A heatsink should be attached to the ground plane (as close as possible to the thermal pathways) with a thermal adhesive.

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

where:

- T_{CASE} = Case temperature (measured on top surface of package)
- T_{AMB} = Ambient temperature °C
- PD = Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).
- θ_{CA} = Value from Table 39.

Table 39. Airflow Over Package Versus θ_{CA}

Airflow (Linear Ft./Min.)	0	200	400
θ_{CA} (°C/W)θ_{JC}[1]	17.9	15.2	13.7

[1] = 6.8°C/W.

225-BALL CSP_BGA BALL CONFIGURATIONS

Table 40. 225-Ball CSP_BGA Ball Assignments

Ball Name	Ball Number	Ball Name	Ball Number	Ball Name	Ball Number	Ball Name	Ball Number
NC	A01	$\overline{\text{TRST}}$	B01	TMS	C01	TDO	D01
BMSTR	A02	TDI	B02	$\overline{\text{EMU}}$	C02	TCK	D02
$\overline{\text{BMS}}$	A03	RPBA	B03	GND	C03	FLAG11	D03
$\overline{\text{SPIDS}}$	A04	MOSI	B04	SPICLK	C04	MISO	D04
EBOOT	A05	FS0	B05	D0B	C05	SCLK0	D05
LBOOT	A06	SCLK1	B06	D1A	C06	D1B	D06
SCLK2	A07	D2B	B07	D2A	C07	FS1	D07
D3B	A08	D3A	B08	FS2	C08	V_{DDINT}	D08
L0DAT4	A09	L0DAT7	B09	FS3	C09	SCLK3	D09
L0ACK	A10	L0CLK	B10	L0DAT6	C10	L0DAT5	D10
L0DAT2	A11	L0DAT1	B11	L1DAT7	C11	L0DAT3	D11
L1DAT6	A12	L1DAT4	B12	L1DAT3	C12	L1DAT5	D12
L1CLK	A13	L1ACK	B13	L1DAT1	C13	DATA42	D13
L1DAT2	A14	L1DAT0	B14	DATA45	C14	DATA46	D14
NC	A15	$\overline{\text{RSTOUT}}$[1]	B15	DATA47	C15	DATA44	D15
FLAG10	E01	FLAG5	F01	FLAG1	G01	FLAG0	H01
$\overline{\text{RESET}}$	E02	FLAG7	F02	FLAG2	G02	$\overline{\text{IRQ0}}$	H02
FLAG8	E03	FLAG9	F03	FLAG4	G03	V_{DDINT}	H03
D0A	E04	FLAG6	F04	FLAG3	G04	$\overline{\text{IRQ1}}$	H04
V_{DDEXT}	E05	V_{DDINT}	F05	V_{DDEXT}	G05	V_{DDINT}	H05
V_{DDINT}	E06	GND	F06	GND	G06	GND	H06
V_{DDEXT}	E07	GND	F07	GND	G07	GND	H07
V_{DDINT}	E08	GND	F08	GND	G08	GND	H08
V_{DDEXT}	E09	GND	F09	GND	G09	GND	H09
V_{DDINT}	E10	GND	F10	GND	G10	GND	H10
V_{DDEXT}	E11	V_{DDINT}	F11	V_{DDEXT}	G11	V_{DDINT}	H11
L0DAT0	E12	DATA37	F12	DATA34	G12	DATA29	H12
DATA39	E13	DATA40	F13	DATA35	G13	DATA28	H13
DATA43	E14	DATA38	F14	DATA33	G14	DATA30	H14
DATA41	E15	DATA36	F15	DATA32	G15	DATA31	H15
$\overline{\text{IRQ2}}$	J01	TIMEXP	K01	ADDR19	L01	ADDR16	M01
ID1	J02	ADDR22	K02	ADDR17	L02	ADDR12	M02
ID2	J03	ADDR20	K03	ADDR21	L03	ADDR18	M03
ID0	J04	ADDR23	K04	ADDR2	L04	ADDR6	M04
V_{DDEXT}	J05	V_{DDINT}	K05	V_{DDEXT}	L05	ADDR0	M05
GND	J06	GND	K06	V_{DDINT}	L06	$\overline{\text{MS1}}$	M06
GND	J07	GND	K07	V_{DDEXT}	L07	$\overline{\text{BR6}}$	M07
GND	J08	GND	K08	V_{DDINT}	L08	V_{DDEXT}	M08
GND	J09	GND	K09	V_{DDEXT}	L09	$\overline{\text{WR}}$	M09
GND	J10	GND	K10	V_{DDINT}	L10	SDA10	M10
V_{DDEXT}	J11	V_{DDINT}	K11	V_{DDEXT}	L11	$\overline{\text{RAS}}$	M11
DATA26	J12	DATA22	K12	$\overline{\text{CAS}}$	L12	ACK	M12
DATA24	J13	DATA19	K13	DATA20	L13	DATA17	M13
DATA25	J14	DATA21	K14	DATA16	L14	$\overline{\text{DMAG2}}$	M14
DATA27	J15	DATA23	K15	DATA18	L15	$\overline{\text{DMAG1}}$	M15

Table 40. 225-Ball CSP_BGA Ball Assignments (Continued)

Ball Name	Ball Number	Ball Name	Ball Number	Ball Name	Ball Number	Ball Name	Ball Number
ADDR14	N01	ADDR13	P01	NC	R01		
ADDR15	N02	ADDR9	P02	ADDR11	R02		
ADDR10	N03	ADDR8	P03	ADDR7	R03		
ADDR5	N04	ADDR4	P04	ADDR3	R04		
ADDR1	N05	$\overline{MS2}$	P05	$\overline{MS3}$	R05		
$\overline{MS0}$	N06	$\overline{SBTS}$	P06	$\overline{PA}$	R06		
$\overline{BR5}$	N07	$\overline{BR4}$	P07	$\overline{BR3}$	R07		
$\overline{BR2}$	N08	$\overline{BR1}$	P08	$\overline{RD}$	R08		
BRST	N09	SDCLK1	P09	CLKOUT	R09		
SDCKE	N10	SDCLK0	P10	$\overline{HBR}$	R10		
$\overline{CS}$	N11	REDY	P11	$\overline{HBG}$	R11		
CLK_CFG1	N12	CLKIN	P12	$\overline{CLKDBL}$	R12		
CLK_CFG0	N13	DQM	P13	XTAL	R13		
AVDD	N14	AGND	P14	$\overline{SDWE}$	R14		
$\overline{DMAR1}$	N15	$\overline{DMAR2}$	P15	NC	R15		

[1] $\overline{RSTOUT}$ exists only for silicon revisions 1.2 and greater. Leave this ball unconnected for silicon revisions 0.3, 1.0, and 1.1.

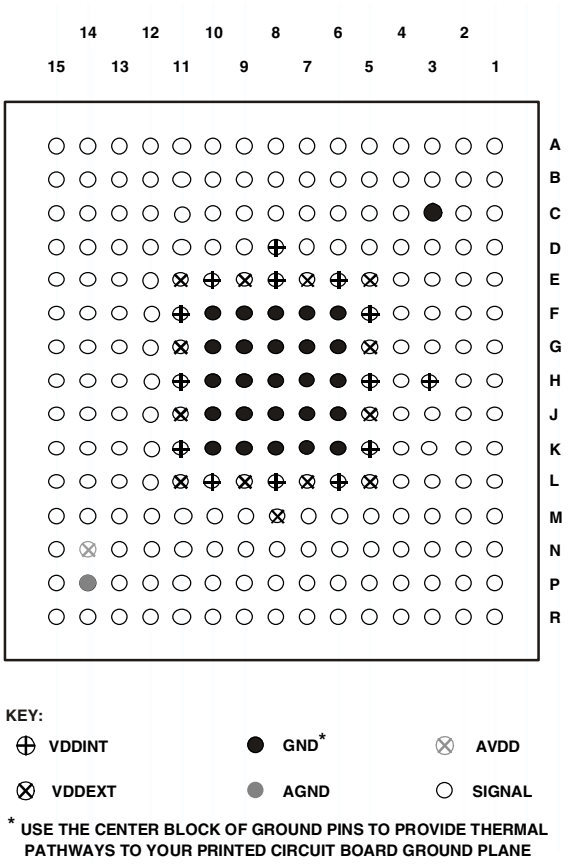
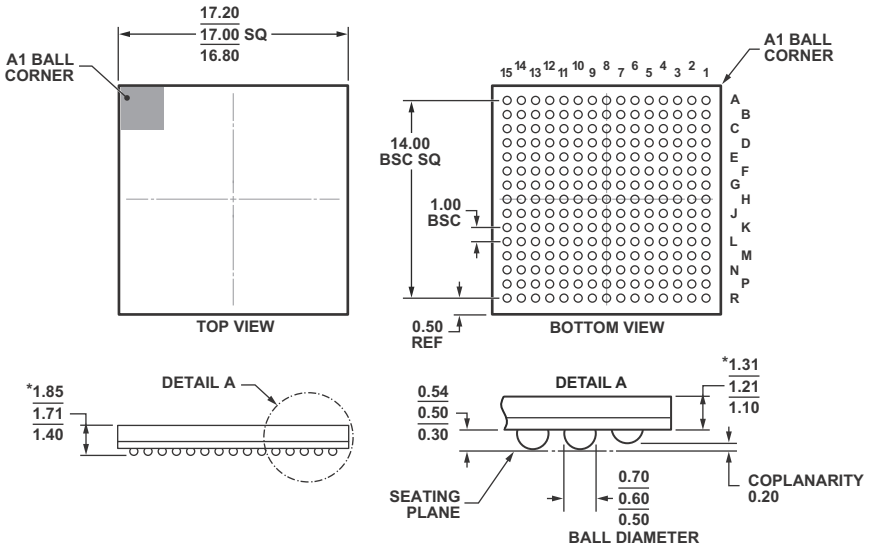


Figure 41. 225-Ball CSP_BGA Ball Assignments (Bottom View, Summary)

OUTLINE DIMENSIONS

The ADSP-21161N comes in a 17 mm × 17 mm, 225-ball CSP_BGA package with 15 rows of balls.



*COMPLIANT TO JEDEC STANDARDS MO-192-AAF-2 WITH THE EXCEPTION TO PACKAGE HEIGHT AND THICKNESS.

Figure 42. 225-Ball CSP_BGA (BC-225-1)

SURFACE-MOUNT DESIGN

Table 41 is provided as an aid to PCB design. For industry standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 41. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
225-Ball CSP_BGA (BC-225-1)	Solder Mask Defined	0.40 mm diameter	0.53 mm diameter

ORDERING GUIDE

Model[1]	Temperature Range[2]	Instruction Rate	On-Chip SRAM	Package Description	Package Option
ADSP-21161NKCA-100	0°C to 85°C	100 MHz	1M bit	225-Ball CSP_BGA	BC-225-1
ADSP-21161NCCA-100	−40°C to +105°C	100 MHz	1M bit	225-Ball CSP_BGA	BC-225-1
ADSP-21161NKCAZ100	0°C to 85°C	100 MHz	1M bit	225-Ball CSP_BGA	BC-225-1
ADSP-21161NCCAZ100	−40°C to +105°C	100 MHz	1M bit	225-Ball CSP_BGA	BC-225-1
ADSP-21161NYCAZ110	−40°C to +125°C	110 MHz	1M bit	225-Ball CSP_BGA	BC-225-1

[1] Z = RoHS Compliant Part.
[2] Referenced temperature is case temperature.

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