BURR - BROWN®

DAC7631

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Serial Input, 16-Bit, Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW POWER: 2.5mW
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 10μs to 0.003%
- 15-BIT LINEARITY AND MONOTONICITY: –40°C to +85°C
- USER SELECTABLE RESET TO MID-SCALE OR ZERO-SCALE
- SMALL SSOP-20 PACKAGE

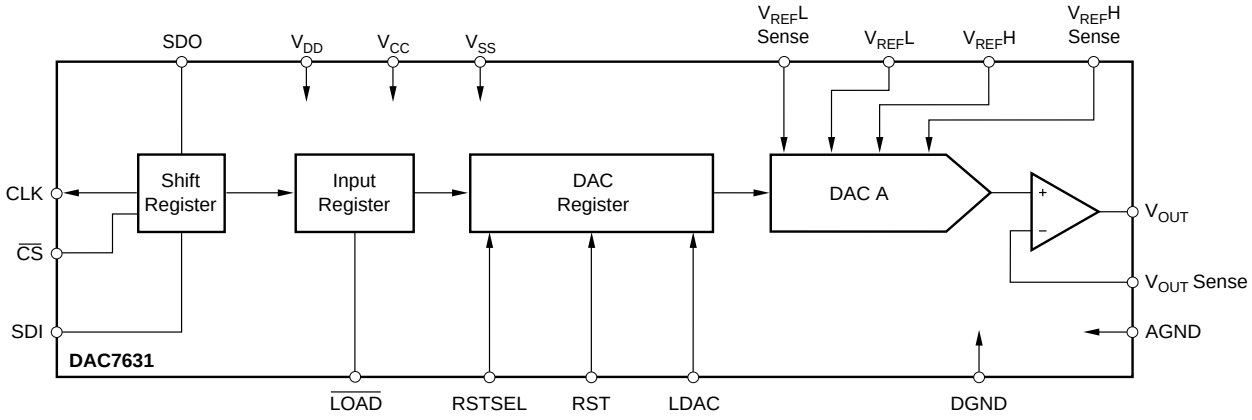
APPLICATIONS

- ATE PIN ELECTRONICS
- PROCESS CONTROL
- CLOSED-LOOP SERVO-CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS

DESCRIPTION

The DAC7631 is a serial input, 16-bit, voltage output Digital-to-Analog Converter (D/A) with guaranteed 15-bit monotonic performance over the –40°C to +85°C temperature range. An asynchronous reset clears all registers to either mid-scale (8000_H) or zero-scale (0000_H), selectable via the RESETSEL pin. The device can be powered from a single +5V supply or from dual +5V and –5V supplies.

Low power and small size makes the DAC7631 ideal for process control, data acquisition systems, and closed-loop servo-control. The device is available in a SSOP-20 package, and is guaranteed over the –40°C to +85°C temperature range.



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SPECIFICATIONS (Dual Supply)

At $T_A = T_{MIN}$ to T_{MAX}, $V_{DD} = V_{CC} = +5V$, $V_{SS} = -5V$, $V_{REF}H = +2.5V$, and $V_{REF}L = -2.5V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7631E			DAC7631EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error			±3	±4		±2	±3	LSB
Differential Linearity Error			±2	±3		±1	±2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			Bits
Bipolar Zero Error			±1	±2		*	*	mV
Bipolar Zero Error Drift			5	10		*	*	ppm/°C
Full-Scale Error			±1	±2		*	*	mV
Full-Scale Error Drift			5	10		*	*	ppm/°C
Power Supply Rejection Ratio (PSRR)	At Full Scale		10	100		*	*	ppm/V
ANALOG OUTPUT								
Voltage Output	$V_{REF} = -2.5V$, $R_L = 10k\Omega$, $V_{SS} = -5V$	$V_{REF}L$		$V_{REF}H$	*		*	V
Output Current		–1.25		+1.25	*		*	mA
Maximum Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			–10, +30			*		mA
Short-Circuit Duration	GND or V_{CC} or V_{SS}		Indefinite			*		
REFERENCE INPUT								
Ref High Input Voltage Range		$V_{REF}L + 1.25$		+2.5	*		*	V
Ref Low Input Voltage Range		–2.5		$V_{REF}H - 1.25$	*		*	V
Ref High Input Current			500			*		µA
Ref Low Input Current			–500			*		µA
DYNAMIC PERFORMANCE								
Settling Time	To ±0.003%, 5V Output Step		8	10		*	*	µs
Digital Feedthrough			2			*		nV-s
Output Noise Voltage	f = 10kHz		60			*		$nV/\sqrt{Hz}$
DAC Glitch	$7FFF_H$ to 8000_H or 8000_H to $7FFF_H$		40			*		nV-s
DIGITAL INPUT								
V_{IH}		$0.7 \cdot V_{DD}$			*			V
V_{IL}				$0.3 \cdot V_{DD}$			*	V
I_{IH}				±10			*	µA
I_{IL}				±10			*	µA
DIGITAL OUTPUT								
V_{OH}	$I_{OH} = -0.8mA$	3.6	4.5		*	*		V
V_{OL}	$I_{OL} = 1.6mA$		0.3	0.4		*	*	V
POWER SUPPLY								
V_{DD}		+4.75	+5.0	+5.25	*	*	*	V
V_{CC}		+4.75	+5.0	+5.25	*	*	*	V
V_{SS}		–5.25	–5.0	–4.75	*	*	*	V
I_{CC}			0.4	0.5		*	*	mA
I_{DD}			50			*		µA
I_{SS}		–0.6	–0.5		*	*		mA
Power			4	5.5		*	*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Specifications same as DAC7631E.

SPECIFICATIONS (Single Supply)

At $T_A = T_{MIN}$ to T_{MAX}, $V_{DD} = V_{CC} = +5V$, $V_{SS} = 0V$, $V_{REF}H = +2.5V$, and $V_{REF}L = 0V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7631E			DAC7631EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error(1)			±3	±4		±2	±3	LSB
Differential Linearity Error			±2	±3		±1	±2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			Bits
Zero Scale Error			±1	±2		*	*	mV
Zero Scale Error Drift			5	10		*	*	ppm/°C
Full-Scale Error			±1	±2		*	*	mV
Full-Scale Error Drift			5	10		*	*	ppm/°C
Power Supply Rejection Ratio (PSRR)	At Full Scale		10	100		*	*	ppm/V
ANALOG OUTPUT								
Voltage Output	$V_{REF}L = 0V$, $V_{SS} = 0V$, $R_L = 10k\Omega$	0		$V_{REF}H$	*		*	V
Output Current		–1.25		+1.25	*		*	mA
Maximum Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			±30			*		mA
Short-Circuit Duration	GND or V_{CC}		Indefinite			*		
REFERENCE INPUT								
Ref High Input Voltage Range		$V_{REF}L + 1.25$		+2.5	*		*	V
Ref Low Input Voltage Range		0		$V_{REF}H - 1.25$	*		*	V
Ref High Input Current			250			*		µA
Ref Low Input Current			–250			*		µA
DYNAMIC PERFORMANCE								
Settling Time	To ±0.003%, 2.5V Output Step		8	10		*	*	µs
Digital Feedthrough			2			*		nV-s
Output Noise Voltage, f = 10kHz			60			*		$nV/\sqrt{Hz}$
DAC Glitch	$7FFF_H$ to 8000_H or 8000_H to $7FFF_H$		40			*		nV-s
DIGITAL INPUT								
V_{IH}		0.7 • V_{DD}			*			V
V_{IL}				0.3 • V_{DD}			*	V
I_{IH}				±10			*	µA
I_{IL}				±10			*	µA
DIGITAL OUTPUT								
V_{OH}	$I_{OH} = –0.8mA$	3.6	4.5		*	*		V
V_{OL}	$I_{OL} = 1.6mA$		0.3	0.4		*	*	V
POWER SUPPLY								
V_{DD}		+4.75	+5.0	+5.25	*	*	*	V
V_{CC}		+4.75	+5.0	+5.25	*	*	*	V
V_{SS}		0	0	0	*	*	*	V
I_{CC}			0.4	0.5		*	*	mA
I_{DD}			50			*		µA
Power			1.8	2.5		*	*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

NOTE: (1) If $V_{SS} = 0V$ specification applies at Code 0040_H and above due to possible negative zero-scale error.

* Specifications same as DAC7631E.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to V_{SS}	–0.3V to +11V
V_{DD} to GND	–0.3V to +5.5V
V_{REFL} to V_{SS}	–0.3V to (V_{DD} – V_{SS})
V_{DD} to V_{REFH}	–0.3V to (V_{DD} – V_{SS})
V_{REFH} to V_{REFL}	–0.3V to (V_{DD} – V_{SS})
Digital Input Voltage to GND	–0.3V to V_{DD} + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

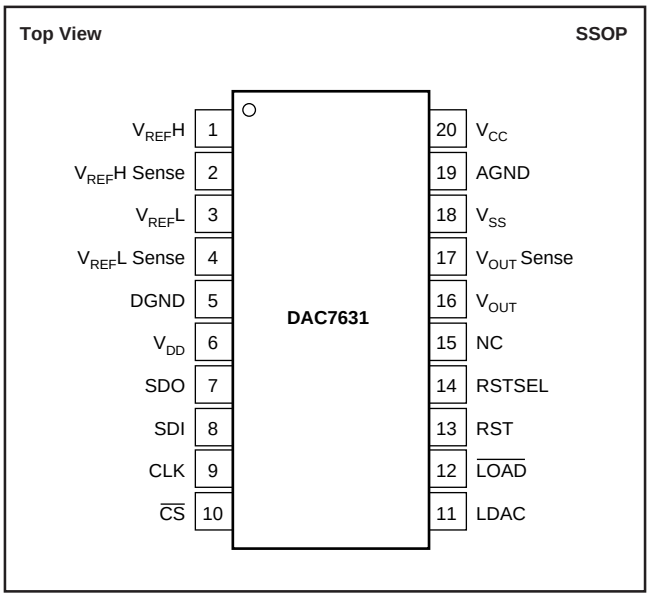
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER[1]	TRANSPORT MEDIA
DAC7631E	±4	±3	SSOP-20	334	–40°C to +85°C	DAC7631E	Rails
"	"	"	"	"	"	DAC7631E/1K	Tape and Reel
DAC7631EB	±3	±2	SSOP-20	334	–40°C to +85°C	DAC7631EB	Rails
"	"	"	"	"	"	DAC7631EB/1K	Tape and Reel

NOTE : (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "DAC7631E/1K" will get a single 1000-piece Tape and Reel.

PIN CONFIGURATION



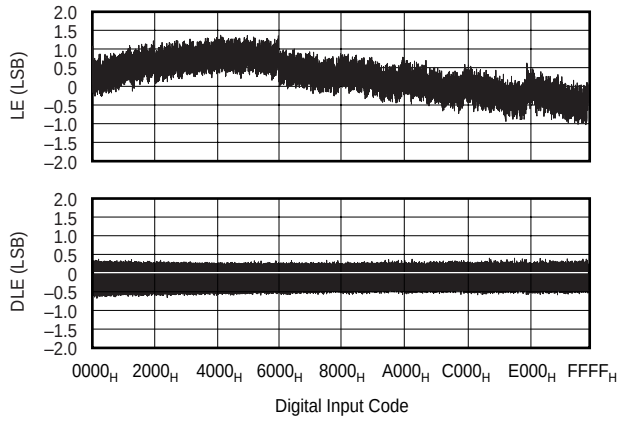
PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	$V_{REF}H$	DAC Reference High Input
2	$V_{REF}H$ Sense	DAC Reference Sense High Input
3	$V_{REF}L$	DAC Reference Low Input
4	$V_{REF}L$ Sense	DAC Reference Sense Low Input
5	DGND	Digital Ground
6	V_{DD}	Logic Power Supply
7	SDO	Serial Data Output
8	SDI	Serial Data Input
9	CLK	Data Clock
10	$\overline{CS}$	Chip Select, Active LOW.
11	LDAC	DAC Register Load Control, Rising Edge Triggered.
12	$\overline{LOAD}$	DAC Input Register Load Control, Active LOW.
13	RST	Reset, Rising Edge. Depending on the state of RSTSEL, the DAC Register is set to either midscale or zero.
14	RSTSEL	Reset Select. Determines the action of RST. If HIGH, a RST command will set the DAC register to midscale. If low, a RST command will set the DAC register to zero.
15	NC	No Connection
16	V_{OUT}	DAC Voltage Output
17	V_{OUT} Sense	DAC Output Amplifier Inverting Input, Used to Close the Feedback Loop at the Load.
18	V_{SS}	Negative Power Supply
19	AGND	Analog Ground
20	V_{CC}	Positive Power Supply

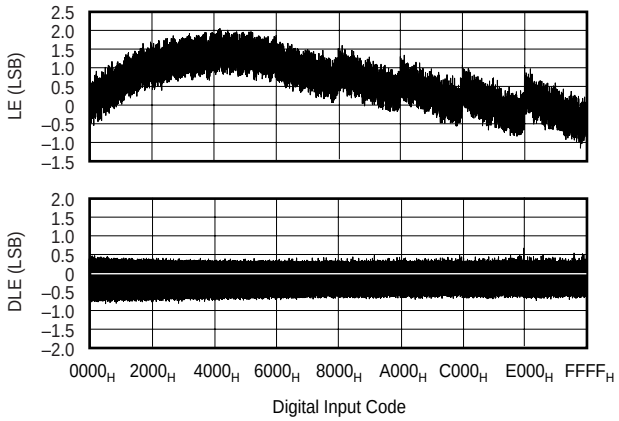
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V

At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, and V_{REFL} = 0V, representative unit, unless otherwise specified.

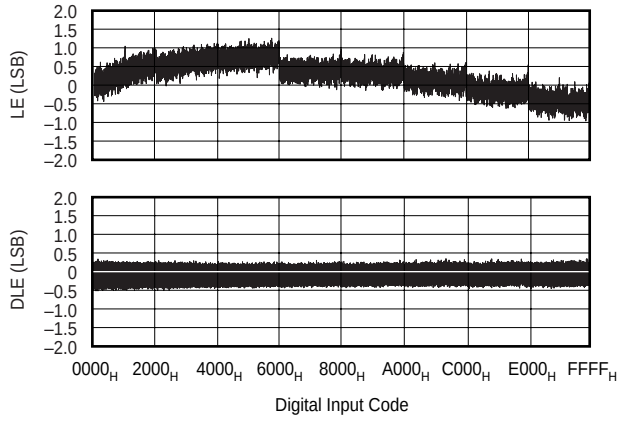
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(+25°C)



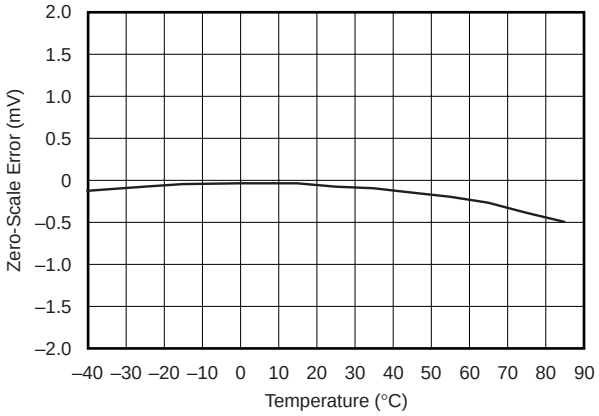
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(+85°C)



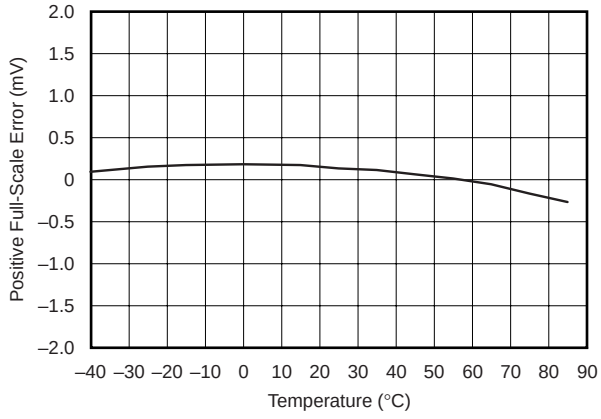
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(–40°C)



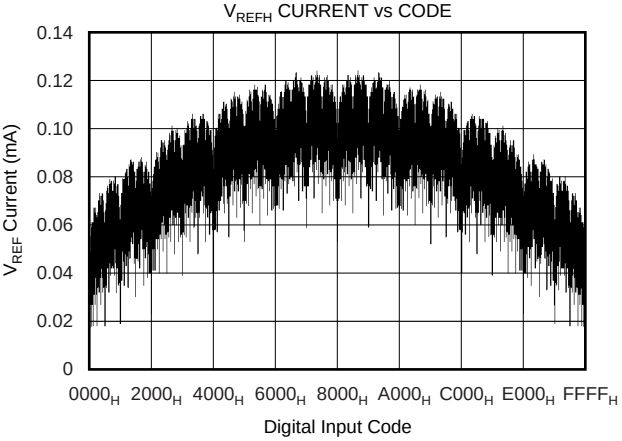
ZERO-SCALE ERROR vs TEMPERATURE
(Code 0040_H)



POSITIVE FULL-SCALE ERROR vs TEMPERATURE
(Code $FFFF_H$)



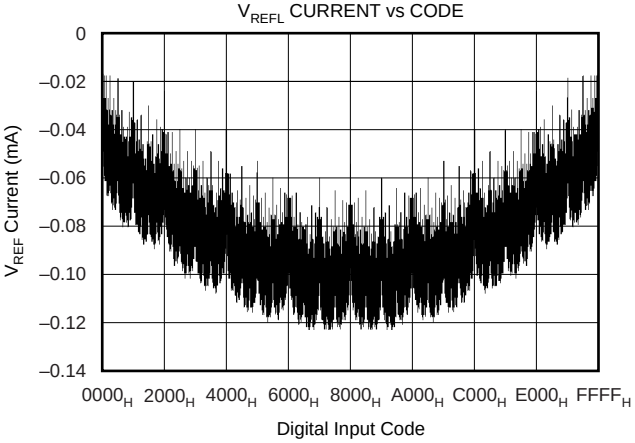
V_{REFH} CURRENT vs CODE



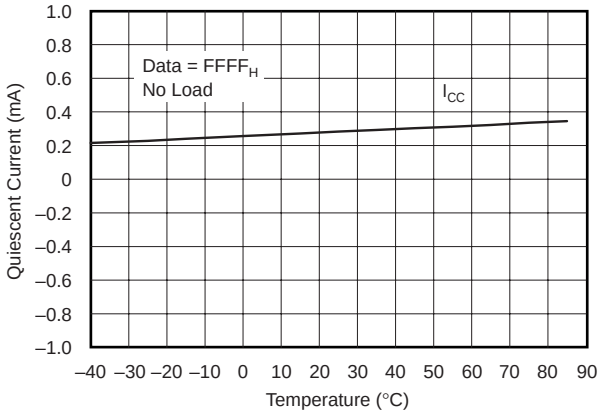
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, and V_{REFL} = 0V, representative unit, unless otherwise specified.

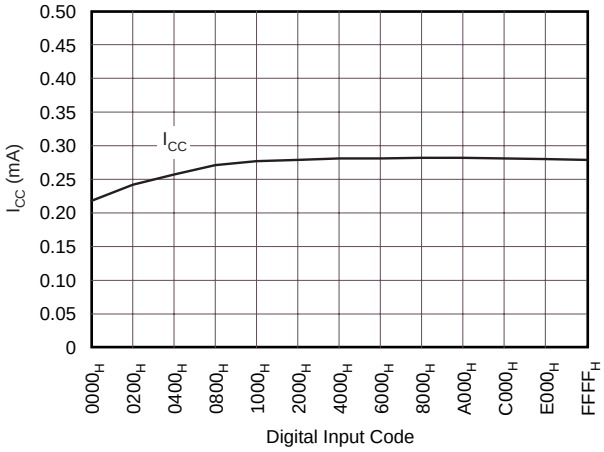
V_{REFL} CURRENT vs CODE



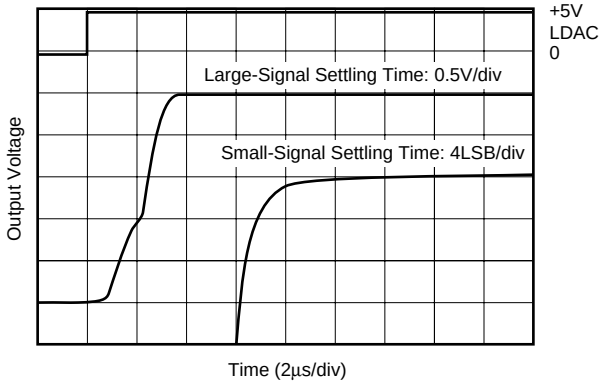
POWER SUPPLY CURRENT vs TEMPERATURE



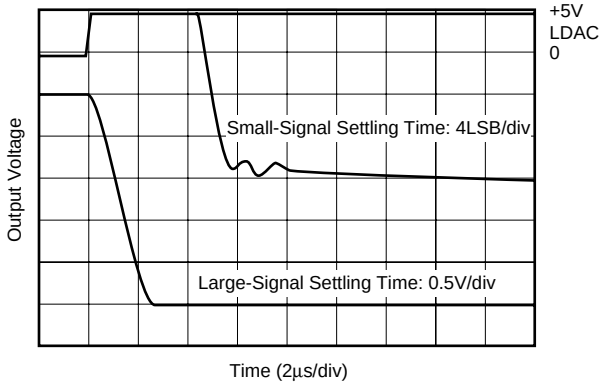
POSITIVE SUPPLY CURRENT vs DIGITAL INPUT CODE



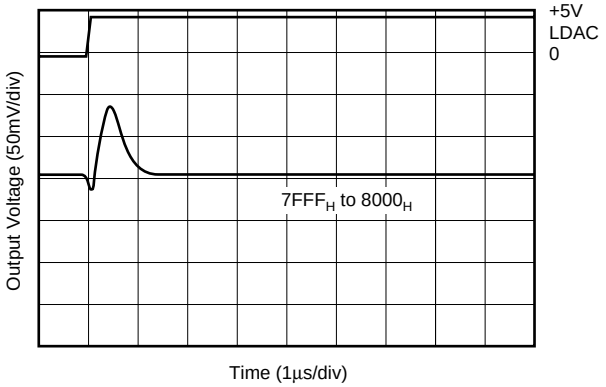
OUTPUT VOLTAGE vs SETTLING TIME (0V to +2.5V)



OUTPUT VOLTAGE vs SETTLING TIME (+2.5V to 2mV)



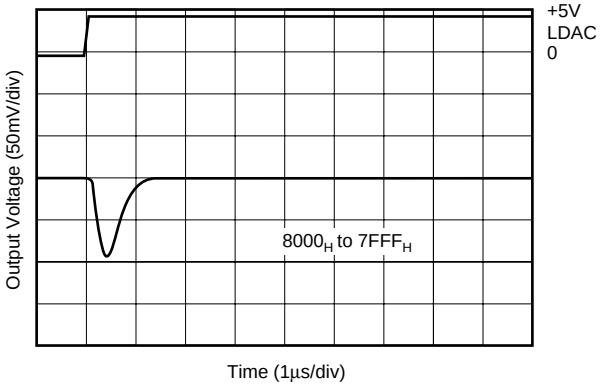
OUTPUT VOLTAGE vs MIDSCALE GLITCH PERFORMANCE



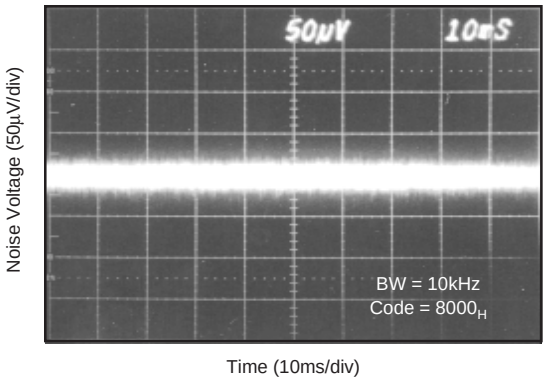
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, and V_{REFL} = 0V, representative unit, unless otherwise specified.

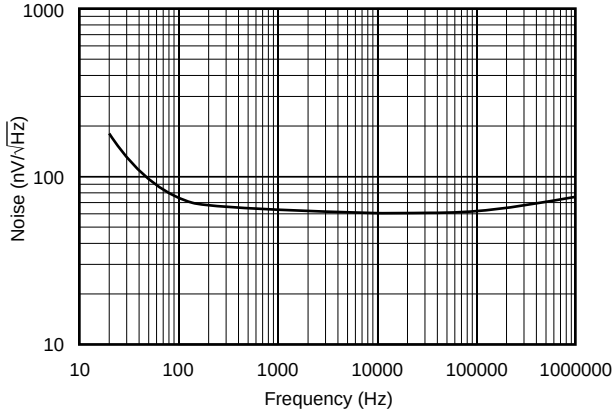
OUTPUT VOLTAGE
vs MIDSCALE GLITCH PERFORMANCE



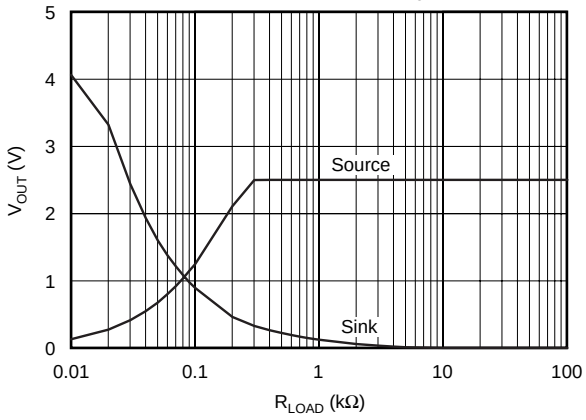
BROADBAND NOISE



OUTPUT NOISE VOLTAGE vs FREQUENCY



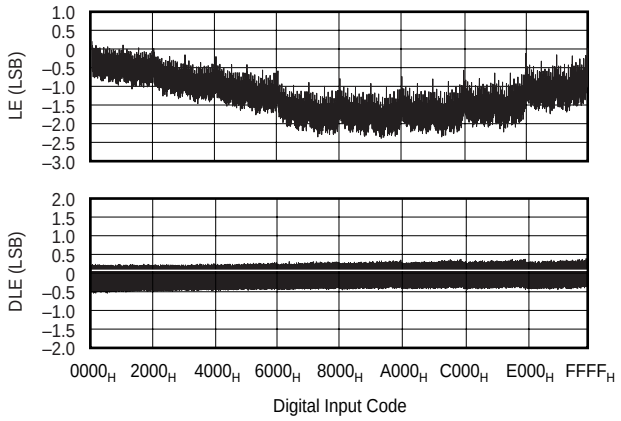
OUTPUT VOLTAGE vs R_{LOAD}



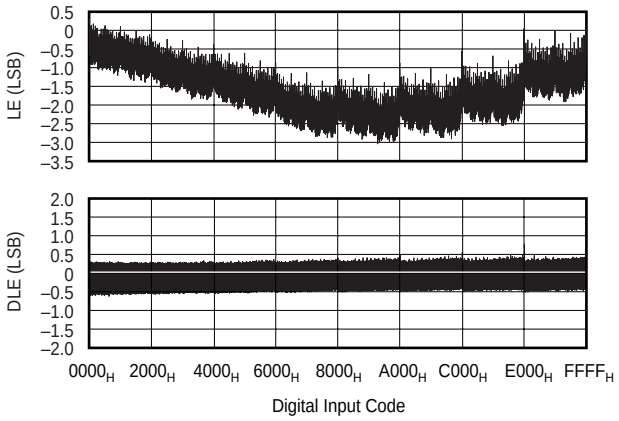
TYPICAL PERFORMANCE CURVES: V_{SS} = –5V

At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, and V_{REFL} = –2.5V, representative unit, unless otherwise specified.

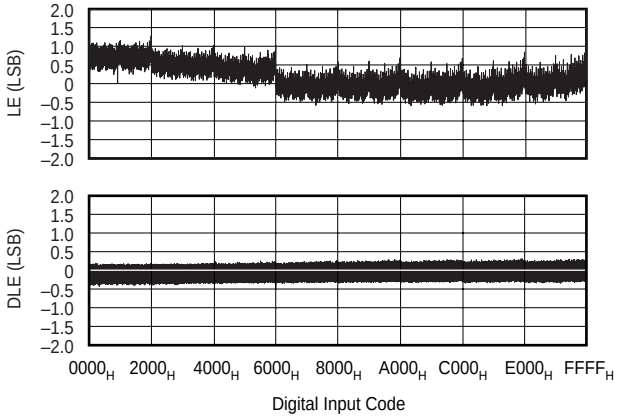
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE **(+25°C)**



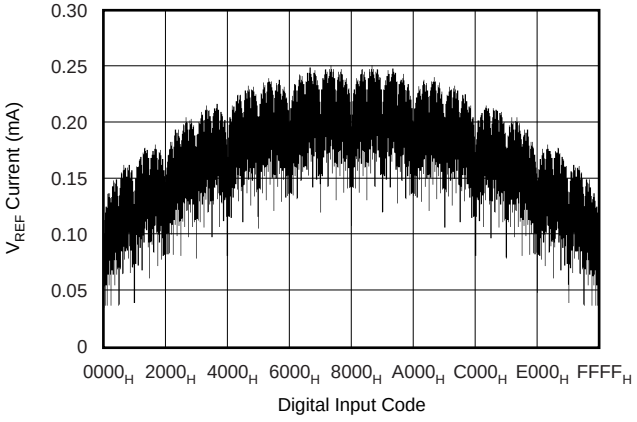
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE **(+85°C)**



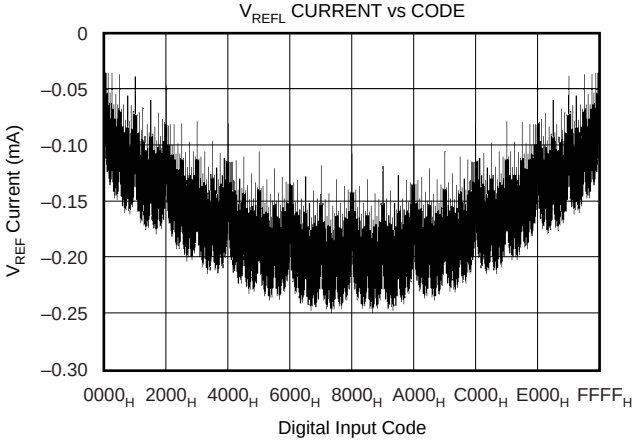
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE **(–40°C)**



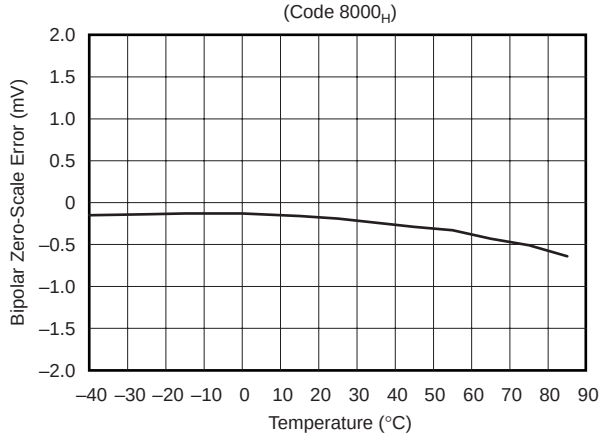
V_{REFH} CURRENT vs CODE



V_{REFL} CURRENT vs CODE



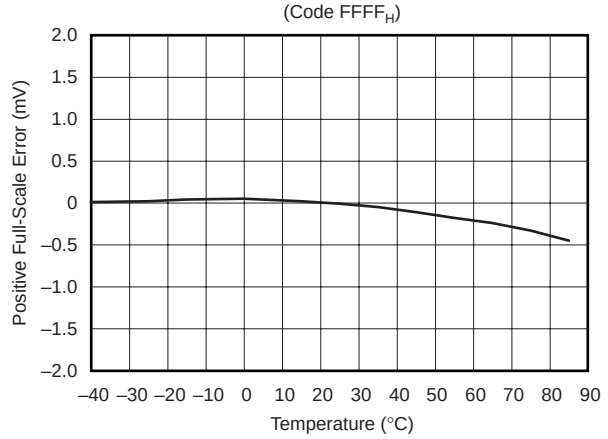
BIPOLAR ZERO-SCALE ERROR vs TEMPERATURE (Code 8000_H)



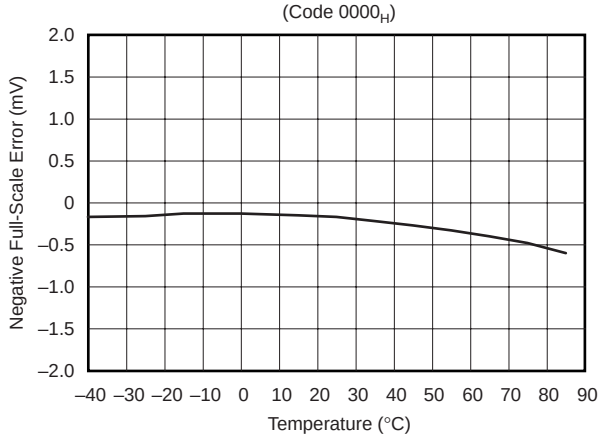
TYPICAL PERFORMANCE CURVES: V_{SS} = –5V (Cont.)

At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, and V_{REFL} = –2.5V, representative unit, unless otherwise specified.

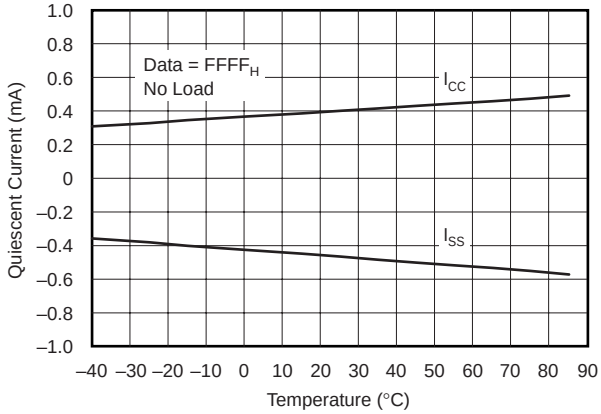
POSITIVE FULL-SCALE ERROR vs TEMPERATURE
(Code $FFFF_H$)



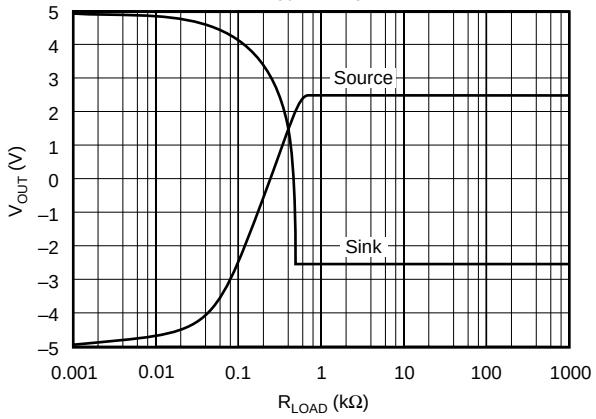
NEGATIVE FULL-SCALE ERROR vs TEMPERATURE
(Code 0000_H)



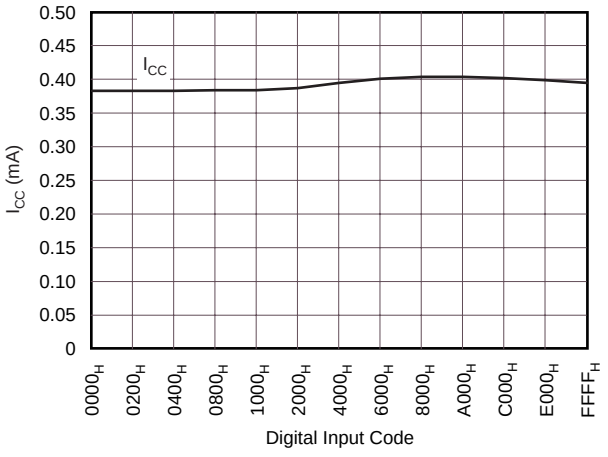
POWER SUPPLY CURRENT vs TEMPERATURE



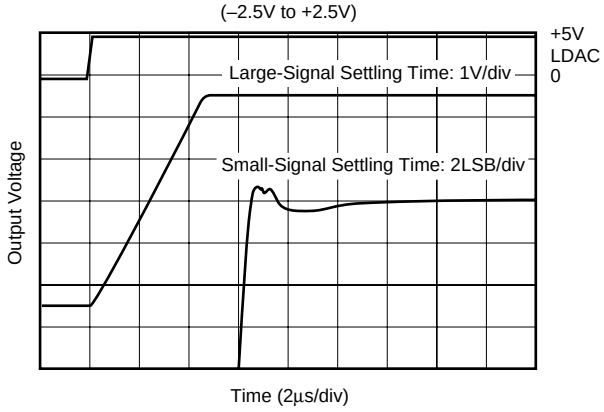
V_{OUT} vs R_{LOAD}



POSITIVE SUPPLY CURRENT
vs DIGITAL INPUT CODE

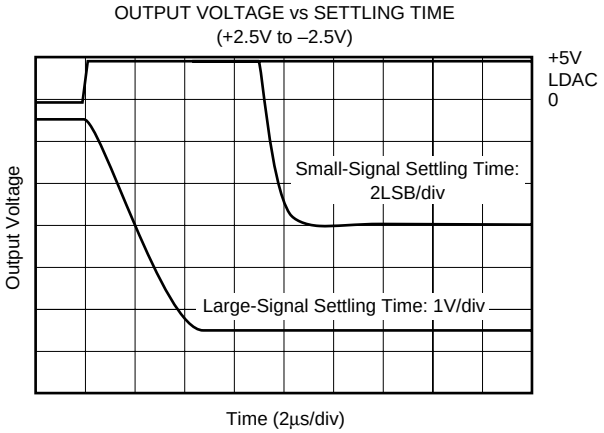


OUTPUT VOLTAGE vs SETTLING TIME
(–2.5V to +2.5V)



TYPICAL PERFORMANCE CURVES: V_{SS} = –5V (Cont.)

At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, and V_{REFL} = –2.5V, representative unit, unless otherwise specified.



THEORY OF OPERATION

The DAC7631 is a 16-bit voltage-output Digital-to-Analog Converter (DAC). The architecture is an R-2R ladder configuration with the three MSB's segmented, followed by an operational amplifier that serves as a buffer, as shown in Figure 1. The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set by external voltage references at $V_{REF}L$ and $V_{REF}H$, respectively.

The digital input is a 16-bit serial word representing the 16-bit DAC input code, sent MSB first. The DAC7631 can be powered from either a single +5V supply or a dual ±5V supply. The device offers a reset function which immediately sets the output voltage and DAC register to mid-scale code (8000H) or to zero-scale code (0000H). See Figures 2 and 3 for the basic operation of the DAC7631.

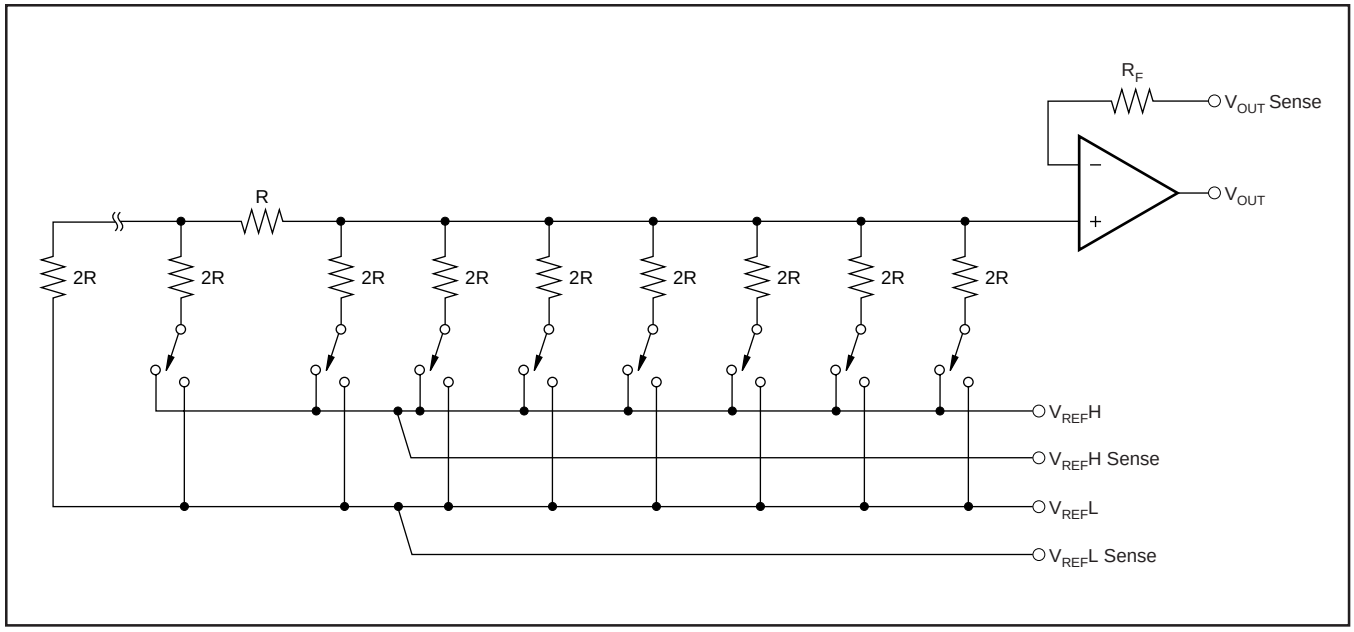


FIGURE 1. DAC7631 Architecture.

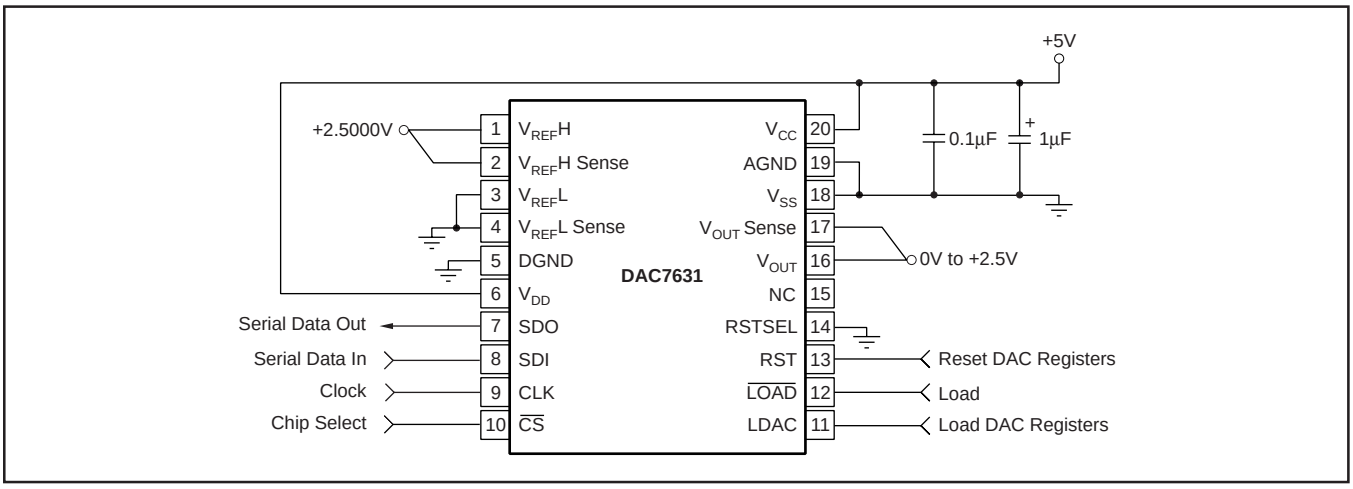


FIGURE 2. Basic Single-Supply Operation.

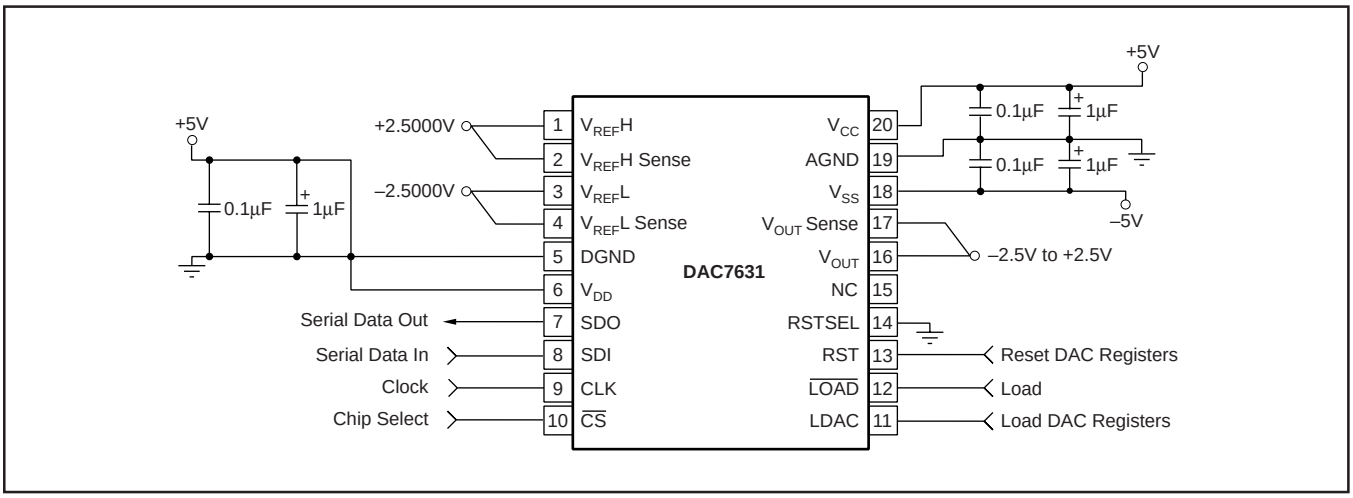


FIGURE 3. Basic Dual-Supply Operation.

ANALOG OUTPUTS

When V_{SS} = –5V (dual supply operation), the output amplifier can swing to within 2.25V of the supply rails, guaranteed over the –40°C to +85°C temperature range. When V_{SS} = 0V (single-supply operation), and with R_{LOAD} also connected to ground, the output can swing to ground. Care must also be taken when measuring the zero-scale error when V_{SS} = 0V. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (0000_H, 0001_H, 0002_H, etc.) if the output amplifier has a negative offset. At the negative limit of –2mV, the first specified output starts at code 0040_H.

Due to the high accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 2.5V full-scale range has a 1LSB value of 38µV. With a load current of 1mA, series wiring and connector resistance of only 40mΩ (R_{W2}) will cause a voltage drop of 40µV, as shown in Figure 4. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 1mA load, a 10 milli-inch wide printed circuit conductor 600 milli-inches long will result in a voltage drop of 30µV.

The DAC7631 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (as shown in Figure 4), thus ensuring an accurate output voltage.

REFERENCE INPUTS

The reference inputs, $V_{REF}L$ and $V_{REF}H$, can be any voltage between V_{SS} + 2.5V and V_{CC} – 2.5V, provided that $V_{REF}H$ is at least 1.25V greater than $V_{REF}L$. The minimum output of each DAC is equal to $V_{REF}L$ plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to $V_{REF}H$ plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of –4.75V to –5.25V. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the $V_{REF}H$ input and out of $V_{REF}L$ depends on the DAC output voltage, and can vary from a few microamps to approximately 0.3mA in dual supply or 0.15mA in single-supply operation. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. The DAC7631 features a reference drive and sense connection such that the internal errors caused by the changing reference current and the circuit impedances can be minimized. Figures 5 through 13 show different reference configurations, and the effect on the linearity and differential linearity.

DIGITAL INTERFACE

Table I shows the basic control logic for the DAC7631. The interface consists of a serial clock input (CLK), serial data input (SDI), DAC input register load control signal ($\overline{LOAD}$), and DAC load control signal (LDAC). In addition, a chip select input ($\overline{CS}$) is provided to simplify device selection in systems with multiple devices. An asynchronous reset input (RST), triggered by a rising edge, is provided to force start-up conditions, periodic resets, or emergency resets to a known state. The action of RST can be selected using the reset select (RSTSEL) pin.

SERIAL DATA INPUT

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

$\overline{CS}$	RST	RSTSEL	LDAC	$\overline{LOAD}$	INPUT REGISTER	DAC REGISTER	MODE
L	H	X	X	L	Write	Hold	Write Input
H	H	X	↑	H	Hold	Write	Update
H	H	X	H	H	Hold	Hold	Hold
X	↑	L	X	X	Reset to Zero	Reset to Zero	Reset to Zero
X	↑	H	X	X	Reset to Midscale	Reset to Midscale	Reset to Midscale

TABLE I. DAC7631 Logic Truth Table.

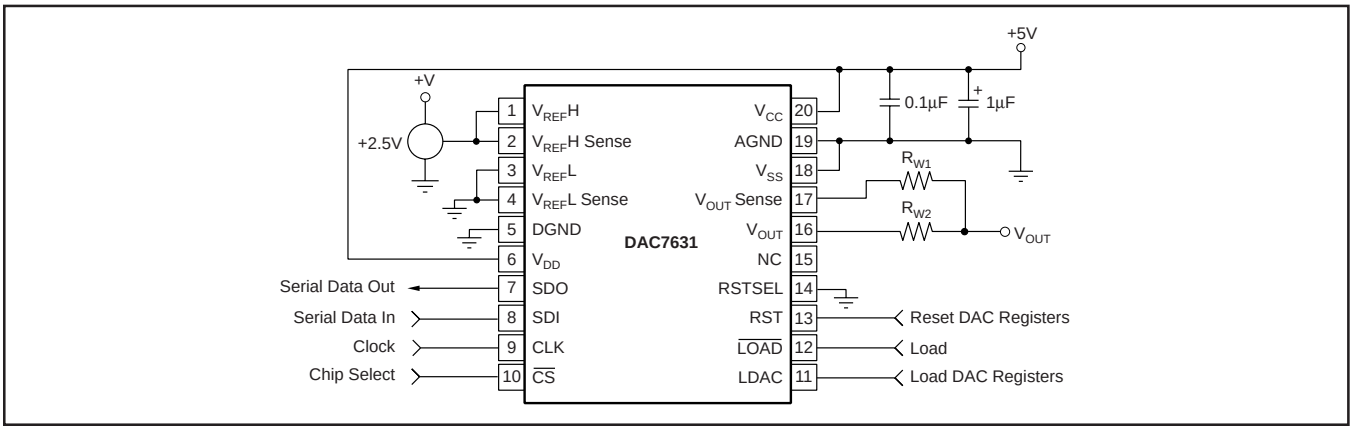


FIGURE 4. Analog Output Closed-loop Configuration. R_{W1} and R_{W2} represent wiring resistance.

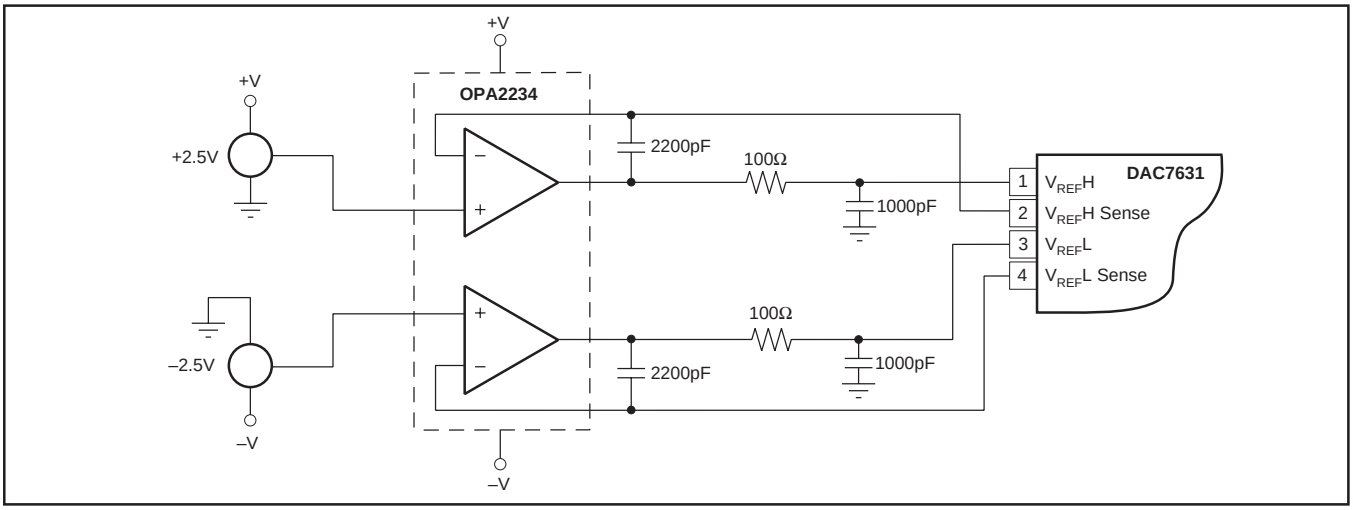


FIGURE 5. Dual-supply Buffered References.

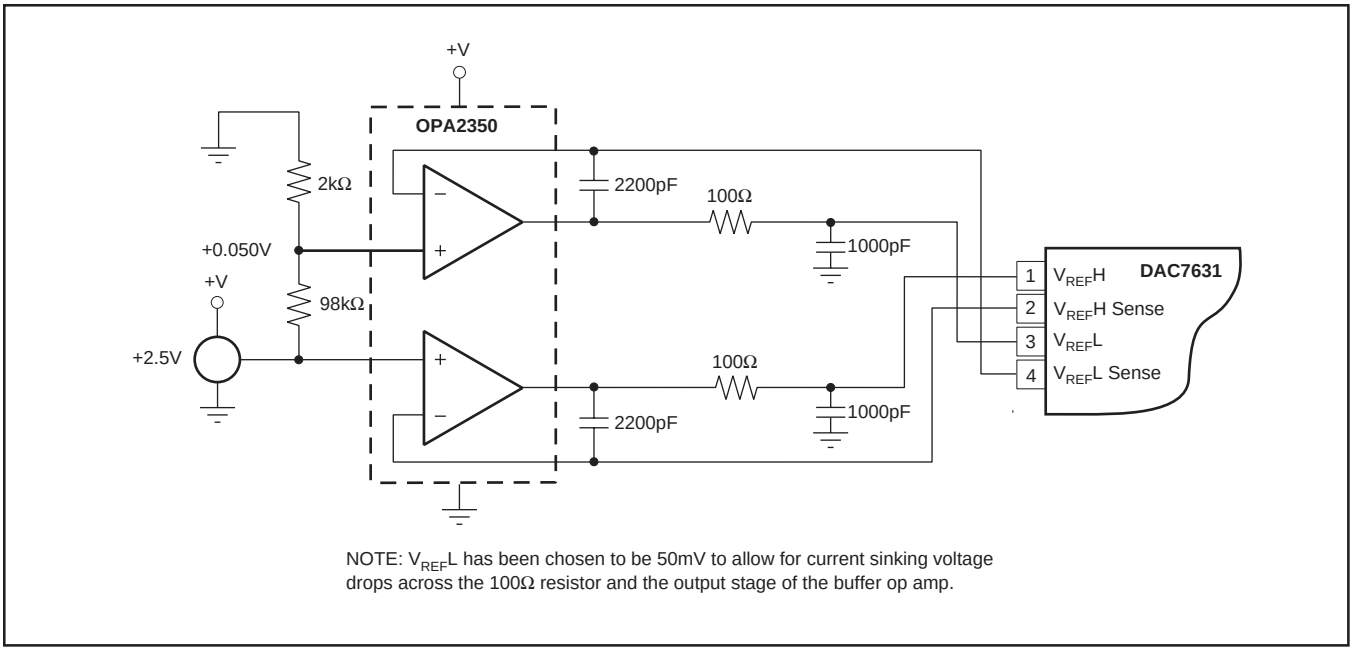


FIGURE 6. Single-supply Buffered Reference, $V_{REF}L$ = 50mV.

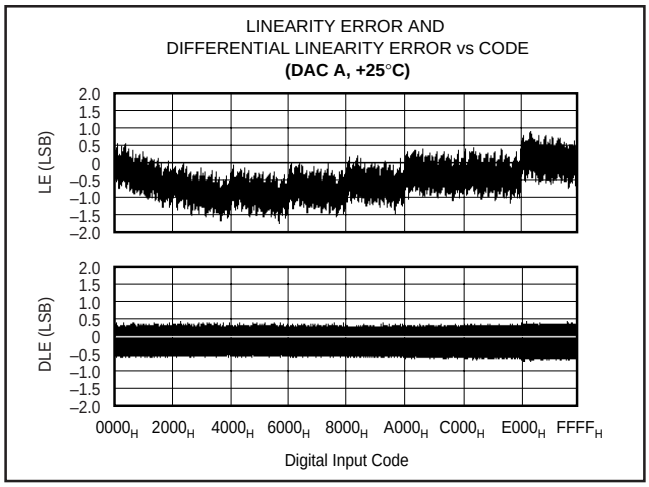


FIGURE 7. Integral Linearity and Differential Linearity Error Curves for Figure 6.

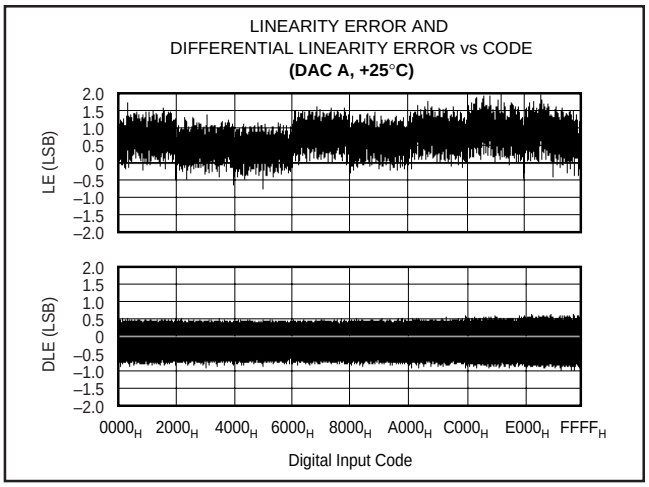


FIGURE 8. Integral Linearity and Differential Linearity Error Curves for Figure 9.

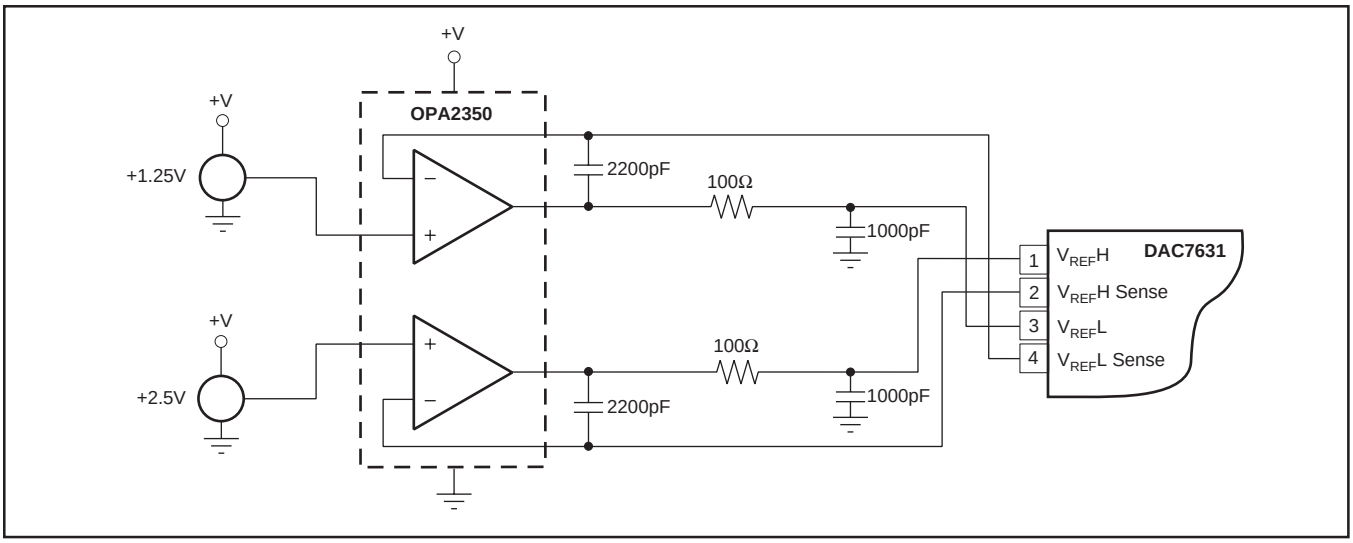


FIGURE 9. Single-supply Buffered Reference, $V_{REF}L$ = +1.25V, $V_{REF}H$ = –1.25V.

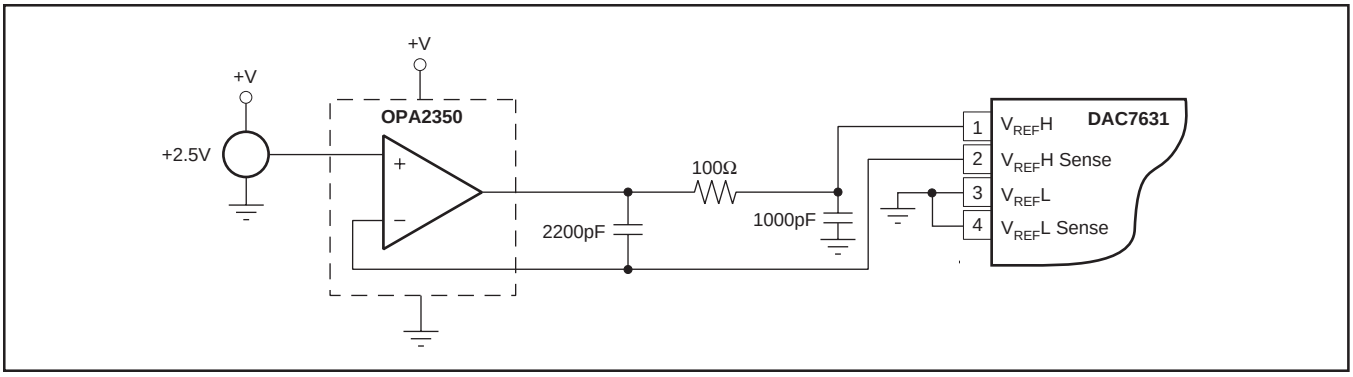


FIGURE 10. Single-supply Buffered $V_{REF}H$.

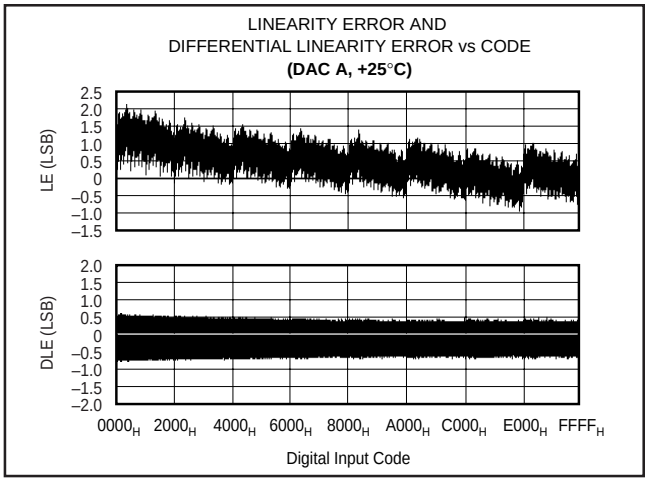


FIGURE 11. Linearity and Differential Error Curves for Figure 10.

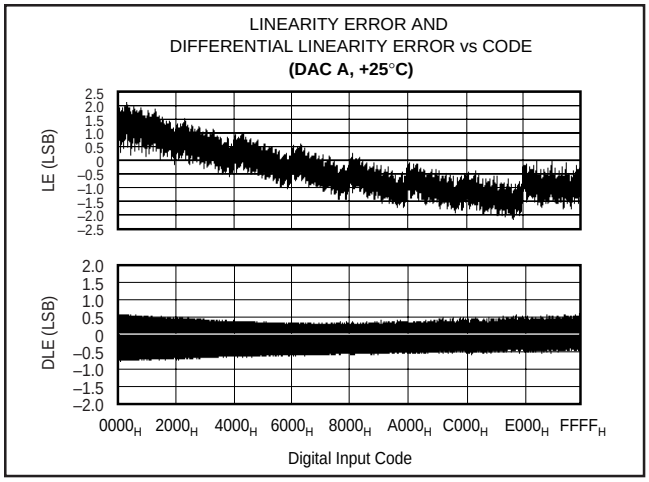


FIGURE 13. Linearity and Differential Error Curves for Figure 12.

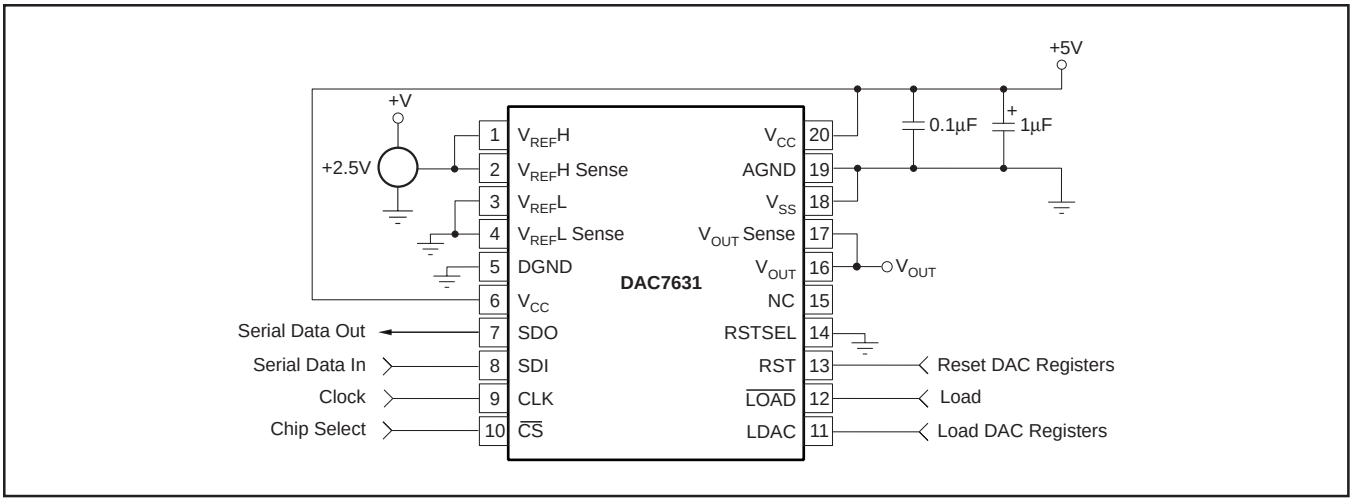


FIGURE 12. Low cost Single-supply Configuration.

Data is shifted into the device through the SDI and CLK pins and arrives in a shift register. Once all 16 bits have been transferred, the $\overline{\text{LOAD}}$ pin, which is level-sensitive, should be brought low to latch the data into a buffer register called the DAC input register. To latch the new data into the DAC itself, the LDAC pin, which is edge-sensitive, must be brought high. When this is done, the DAC will assume the new value and the output voltage will change (provided that the new value is different from the old one). Note that settling time is measured from the time that the LDAC pin is brought high, since the device's output does not begin to change until then.

The DAC7631's double-buffering scheme allows the device to be updated through the serial interface without disturbing the voltage on the output pin. It also allows the user to use separate logic for driving the serial input and triggering

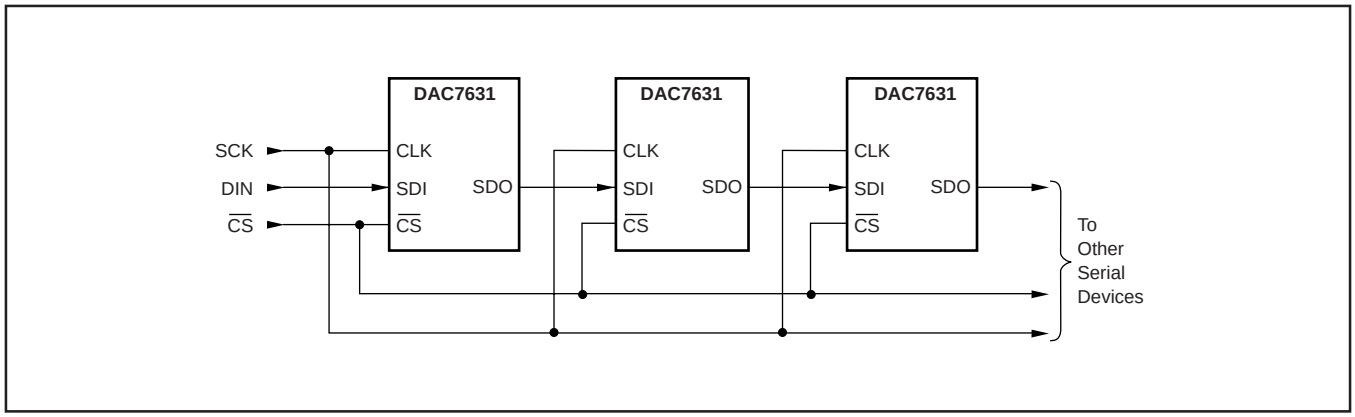


FIGURE 14. Daisy-chaining DAC7631.

DAC updates; i.e., the LDAC pin can be driven with a separate signal, such as a timing clock, which need not be directly related to the serial data timing. This makes it easy to synchronize DAC7631 updates with external events or with other DACs.

Note that $\overline{CS}$ and CLK are combined with an OR gate, which controls the serial-to-parallel shift register. These two inputs are completely interchangeable. In addition, care must be taken with the state of CLK when $\overline{CS}$ rises at the end of a serial transfer. If CLK is LOW when $\overline{CS}$ rises, the OR gate will provide a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong input register(s). If both $\overline{CS}$ and CLK are used, $\overline{CS}$ should rise only when CLK is HIGH. If not, then either $\overline{CS}$ or CLK can be used to operate the shift register. See Table II for more information.

$\overline{CS}$(1)	CLK(1)	$\overline{LOAD}$	RST	SERIAL SHIFT REGISTER
H(2)	X(3)	H	H	No Change
L(4)	L	H	H	No Change
L	↑(5)	H	H	Advanced One Bit
↑	L	H	H	Advanced One Bit
H(6)	X	L(7)	H	No Change
H(6)	X	H	↑(8)	No Change

NOTES: (1) $\overline{CS}$ and CLK are interchangeable. (2) H = Logic HIGH. (3) X = Don't Care. (4) L = Logic LOW (5) = Positive Logic Transition. (6) A HIGH value is suggested in order to avoid a "false clock" from advancing the shift register and changing the shift register. (7) If data is clocked into the serial register while $\overline{LOAD}$ is LOW, the DAC register will change. This will corrupt the data in each DAC register that has been erroneously selected. (8) Rising edge of RST causes no change in the contents of the serial shift register.

TABLE II. Serial Shift Register Truth Table.

SERIAL-DATA OUTPUT

The Serial-Data Output (SDO) is the internal shift register's output. For DAC7631, the SDO is a driven output and does not require an external pull-up. Any number of DAC7631's can be daisy chained by connecting the SDO pin of one device to the SDI pin of the following device in the chain, as shown in Figure 14.

DIGITAL TIMING

Figure 15 and Table III provide detailed timing for the digital interface of the DAC7631.

DIGITAL INPUT CODING

The DAC7631 input data is in Straight Binary format. The output voltage is given by Equation 1:

$$V_{OUT} = V_{REF}L + \frac{(V_{REF}H - V_{REF}L) \cdot N}{65,536} \qquad (1)$$

where N is the digital input code. This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

DIGITALLY-PROGRAMMABLE CURRENT SOURCE

The DAC7631 offers a unique set of features that allows a wide range of flexibility in designing applications circuits such as programmable current sources. The DAC7631 offers both a differential reference input, as well as an open-loop configuration around the output amplifier. The open-loop configuration around the output amplifier allows a transistor to be placed within the loop to implement a digitally-programmable, unidirectional current source. The availability of a differential reference allows programmability for both the full-scale and zero-scale currents. The output current is calculated as:

$$I_{OUT} = \left(\left(\frac{V_{REF}H - V_{REF}L}{R_{SENSE}}\right) \cdot \left(\frac{N}{65,536}\right)\right) + \left(V_{REF}L / R_{SENSE}\right) \qquad (2)$$

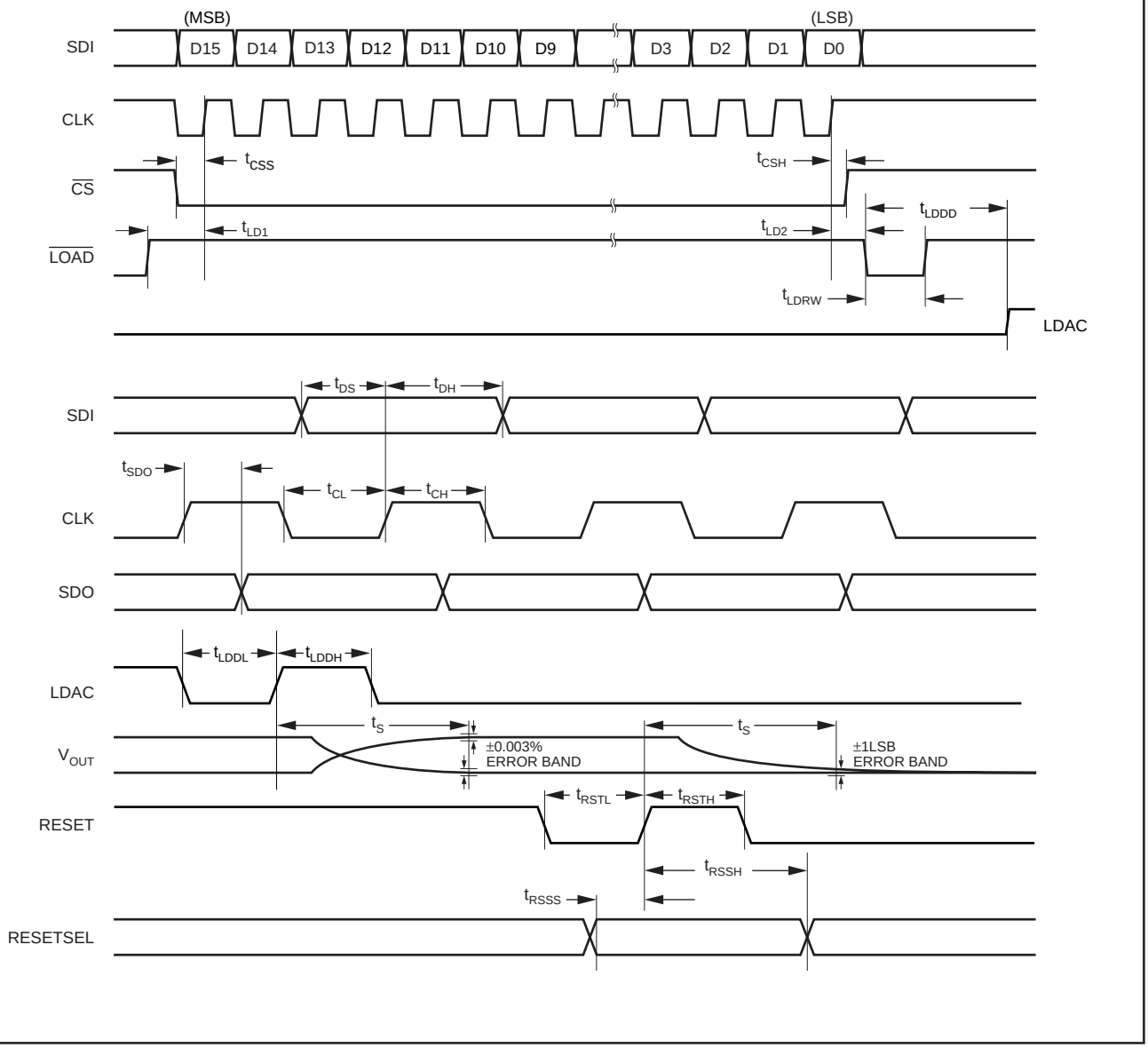


FIGURE 15. Digital Input and Output Timing.

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{DS}	Data Valid to CLK Rising	10		ns
t_{DH}	Data Held Valid after CLK Rises	20		ns
t_{CH}	CLK HIGH	25		ns
t_{CL}	CLK LOW	25		ns
t_{CSS}	$\overline{CS}$ LOW to CLK Rising	15		ns
t_{CSH}	CLK HIGH to $\overline{CS}$ Rising	0		ns
t_{LD1}	$\overline{LOAD}$ HIGH to CLK Rising	10		ns
t_{LD2}	CLK Rising to $\overline{LOAD}$ LOW	30		ns
t_{LDRW}	$\overline{LOAD}$ LOW Time	30		ns
t_{LDDL}	LDAC LOW Time	100		ns
t_{LDDH}	LDAC HIGH Time	150		ns
t_{SDO}	SDO Propagation Delay	10	45	ns
t_{RSSS}	RESETSEL Valid to RESET HIGH	0		ns
t_{RSSH}	RESET HIGH to RESETSEL Not Valid	100		ns
t_{RSTL}	RESET LOW Time	10		ns
t_{RSTH}	RESET HIGH Time	10		ns
t_{LDDD}	$\overline{LOAD}$ LOW to LDAC Rising Time	40		ns
t_S	Settling Time		10	µs

TABLE III. Timing Specifications (T_A = –40°C to +85°C).

Figure 16 shows a DAC7631 in a 4mA to 20mA current output configuration. The output current can be determined by Equation 3:

$$I_{OUT} = \left(\left(\frac{2.5V - 0.5V}{125\Omega}\right) \bullet \left(\frac{N}{65,536}\right)\right) + \left(\frac{0.5V}{125\Omega}\right) \quad (3)$$

At full-scale, the output current is 16mA, plus the 4mA, for the zero current. At zero scale the output current is the offset current of 4mA (0.5V/125Ω).

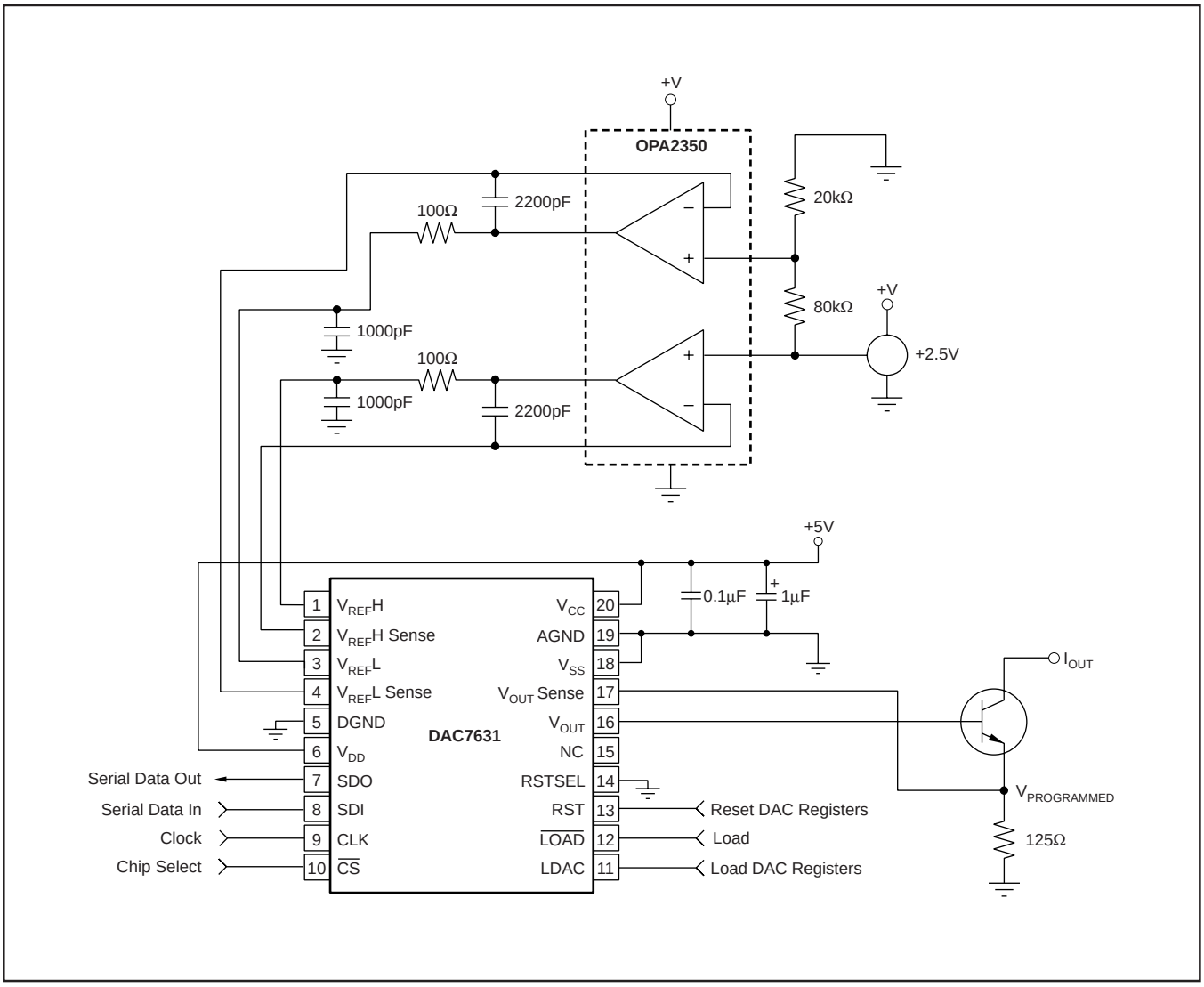


FIGURE 16. 4-to-20mA Digitally Controlled Current Source (1/2 DAC7631).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC7631E	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7631E/1K	ACTIVE	SSOP	DB	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7631E/1KG4	ACTIVE	SSOP	DB	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7631EB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7631EB/1K	ACTIVE	SSOP	DB	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7631EB/1KG4	ACTIVE	SSOP	DB	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7631EBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7631EG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

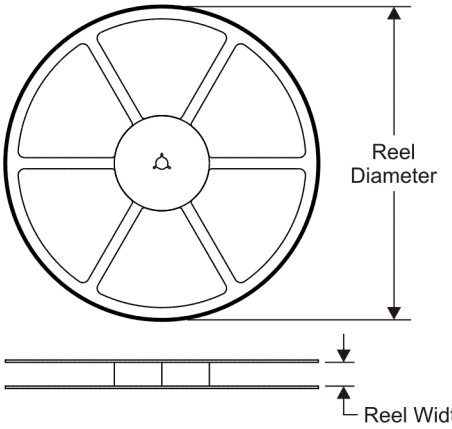
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

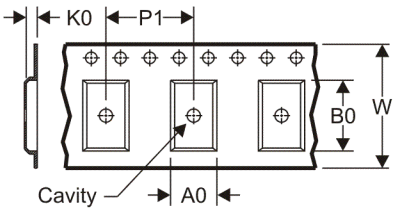
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

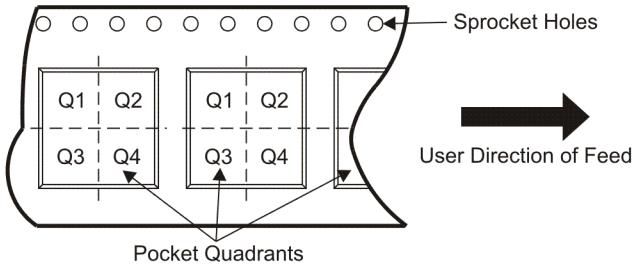


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

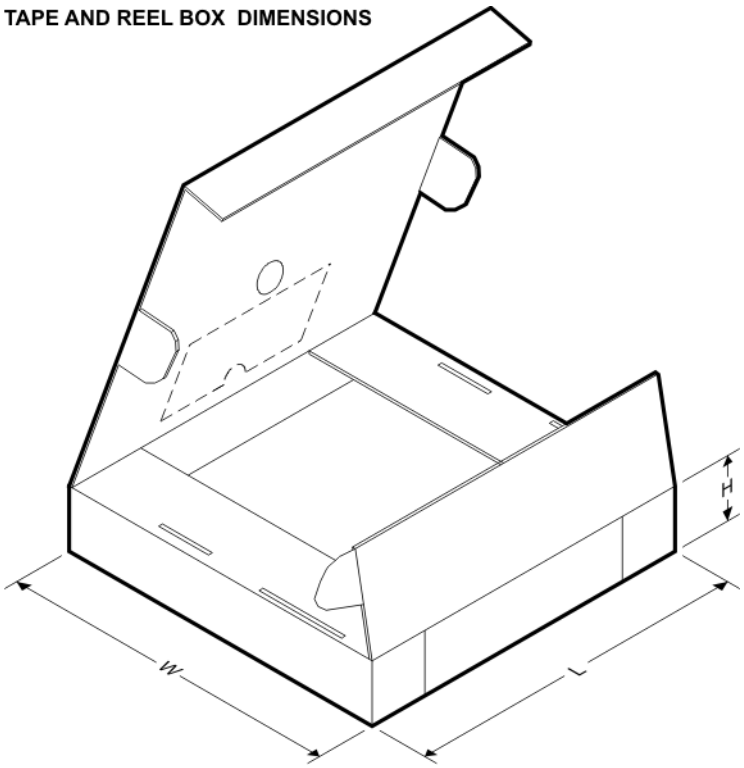
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7631E/1K	SSOP	DB	20	1000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
DAC7631EB/1K	SSOP	DB	20	1000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7631E/1K	SSOP	DB	20	1000	346.0	346.0	33.0
DAC7631EB/1K	SSOP	DB	20	1000	346.0	346.0	33.0

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