UCC27524A Dual 5-A, High-Speed, Low-Side Gate Driver With Negative Input Voltage Capability

1 Features

- Industry-Standard Pin Out
- Two Independent Gate-Drive Channels
- 5-A Peak Source and Sink-Drive Current
- Independent-Enable Function for Each Output
- TTL and CMOS Compatible Logic Threshold Independent of Supply Voltage
- Hysteretic-Logic Thresholds for High Noise Immunity
- Ability to Handle Negative Voltages (–5 V) at Inputs
- Inputs and Enable Pin-Voltage Levels Not Restricted by VDD Pin Bias Supply Voltage
- 4.5 to 18-V Single-Supply Range
- Outputs Held Low During VDD-UVLO (Ensures Glitch-Free Operation at Power Up and Power Down)
- Fast Propagation Delays (13-ns Typical)
- Fast Rise and Fall Times (7-ns and 6-ns Typical)
- 1-ns Typical Delay Matching Between 2-Channels
- Two Outputs are Paralleled for Higher Drive Current
- Outputs Held in Low When Inputs Floating
- SOIC-8, HVSSOP-8 PowerPAD™ Package Options
- Operating Temperature Range of –40 to 140°C

2 Applications

- Switch-Mode Power Supplies
- DC-to-DC Converters
- Motor Control, Solar Power
- Gate Drive for Emerging Wide Band-Gap Power Devices Such as GaN

3 Description

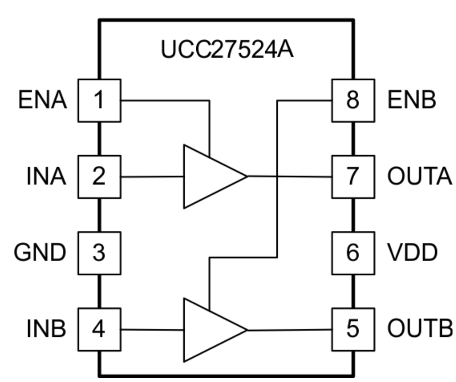
The UCC27524A device is a dual-channel, high-speed, low-side, gate-driver device capable of effectively driving MOSFET and IGBT power switches. The UCC27524A is a variant of the UCC2752x family. The UCC27524A adds the ability to handle –5 V directly at the input pins for increased robustness. The UCC27524A is a dual non-inverting driver. Using a design that inherently minimizes shoot-through current, the UCC27524A is capable of delivering high-peak current pulses of up to 5-A source and 5-A sink into capacitive loads along with rail-to-rail drive capability and extremely small propagation delay typically 13 ns. In addition, the drivers feature matched internal propagation delays between the two channels which are very well suited for applications requiring dual-gate drives with critical timing, such as synchronous rectifiers. This also enables connecting two channels in parallel to effectively increase current-drive capability or driving two switches in parallel with a single input signal. The input pin thresholds are based on TTL and CMOS compatible low-voltage logic, which is fixed and independent of the VDD supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC27524A	SOIC (8)	4.90 mm x 3.91 mm
	HVSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Dual Non-Inverting Inputs



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4 Revision History

Changes from Revision A (August 2013) to Revision B — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Original (August 2013) to Revision A — **Page**

- Changed marketing status from Product Preview to Production Data. 1
- Changed Enable voltage, ENA and ENB minimum from 0 to –2. 4

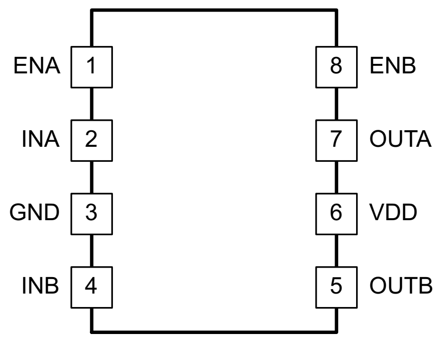
5 Description (Continued)

For safety purpose, internal pull-up and pull-down resistors on the input pins of the UCC27524A ensure that outputs are held LOW when input pins are in floating condition. UCC27524A features Enable pins (ENA and ENB) to have better control of the operation of the driver applications. The pins are internally pulled up to VDD for active-high logic and are left open for standard operation.

UCC27524A family of devices are available in SOIC-8 (D), VSSOP-8 with exposed pad (DGN) packages.

6 Pin Configuration and Functions

8-Pin
D, DGN Package
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ENA	1	I	Enable input for Channel A: ENA is biased LOW to disable the Channel A output regardless of the INA state. ENA is biased HIGH or left floating to enable the Channel A output. ENA is allowed to float; hence the pin-to-pin compatibility with the UCC2732X N/C pin.
ENB	8	I	Enable input for Channel B: ENB is biased LOW to disables the Channel B output regardless of the INB state. ENB is biased HIGH or left floating to enable Channel B output. ENB is allowed to float hence; the pin-to-pin compatibility with the UCC2752A N/C pin.
GND	3	-	Ground: All signals are referenced to this pin.
INA	2	I	Input to Channel A: INA is the non-inverting input in the UCC27524A device. OUTA is held LOW if INA is unbiased or floating.
INB	4	I	Input to Channel B: INB is the non-inverting input in the UCC27524A device. OUTB is held LOW if INB is unbiased or floating.
OUTA	7	O	Output of Channel A
OUTB	5	O	Output of Channel B
VDD	6	I	Bias supply input

7 Specifications

7.1 Absolute Maximum Ratings[(1)(2)]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range	VDD	–0.3	20	V
OUTA, OUTB voltage	DC	–0.3	VDD + 0.3	V
	Repetitive pulse < 200 ns[(3)]	–2	VDD + 0.3	V
Output continuous source/sink current	I_{OUT_DC}		0.3	A
Output pulsed source/sink current (0.5 µs)	I_{OUT_pulsed}		5	A
INA, INB, ENA, ENB voltage[(4)]		–5	20	V
Operating virtual junction temperature, T_J range		–40	150	°C
Lead temperature	Soldering, 10 seconds		300	°C
	Reflow		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) Values are verified by characterization on bench.
(4) The maximum voltage on the Input and Enable pins is not restricted by the voltage on the VDD pin.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	–4000	4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	–1000	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, VDD	4.5	12	18	V
Operating junction temperature range	–40		140	°C
Input voltage, INA, INB	–2		18	V
Enable voltage, ENA and ENB	–2		18	

7.4 Thermal Information

THERMAL METRIC		UCC27524A SOIC (D) 8 PINS	UCC27524A MSOP (DGN)(1) 8 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	130.9	71.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	80.0	65.6	
θ_{JB}	Junction-to-board thermal resistance(4)	71.4	7.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	21.9	7.4	
ψ_{JB}	Junction-to-board characterization parameter(6)	70.9	31.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	n/a	19.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics

V_{DD} = 12 V, T_A = T_J = –40 °C to 140 °C, 1-µF capacitor from V_{DD} to GND. Currents are positive into, negative out of the specified terminal (unless otherwise noted,)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
BIAS CURRENTS						
$I_{DD(off)}$	Startup current, (based on UCC27524 Input configuration)	VDD = 3.4 V, INA = VDD, INB = VDD	55	110	175	µA
		VDD = 3.4 V, INA = GND, INB = GND	25	75	145	
UNDER VOLTAGE LOCKOUT (UVLO)						
V_{ON}	Supply start threshold	T_J = 25 °C	3.91	4.2	4.5	V
		T_J = –40 °C to 140 °C	3.7	4.2	4.65	
V_{OFF}	Minimum operating voltage after supply start		3.4	3.9	4.4	
VDD_H	Supply voltage hysteresis		0.2	0.3	0.5	
INPUTS (INA, INB, INA+, INA–, INB+, INB–), UCC27524A (D, DGN)						
V_{IN_H}	Input signal high threshold	Output high for non-inverting input pins Output low for inverting input pins	1.9	2.1	2.3	V
V_{IN_L}	Input signal low threshold	Output low for non-inverting input pins Output high for inverting input pins	1	1.2	1.4	
V_{IN_HYS}	Input hysteresis		0.7	0.9	1.1	
OUTPUTS (OUTA, OUTB)						
$I_{SNK/SRC}$	Sink/source peak current(1)	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz		±5		A
V_{DD}-V_{OH}	High output voltage	I_{OUT} = –10 mA			0.075	V
V_{OL}	Low output voltage	I_{OUT} = 10 mA			0.01	
R_{OH}	Output pullup resistance(2)	I_{OUT} = –10 mA	2.5	5	7.5	Ω
R_{OL}	Output pulldown resistance	I_{OUT} = 10 mA	0.15	0.5	1	Ω

(1) Ensured by design.
(2) R_{OH} represents on-resistance of only the P-Channel MOSFET device in the pullup structure of the UCC27524A output stage.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time(1)	C_{LOAD} = 1.8 nF		7	18	ns
t_F	Fall time(1)	C_{LOAD} = 1.8 nF		6	10	
t_M	Delay matching between 2 channels	INA = INB, OUTA and OUTB at 50% transition point		1	4	
t_{PW}	Minimum input pulse width that changes the output state			15	25	
t_{D1}, t_{D2}	Input to output propagation delay(1)	C_{LOAD} = 1.8 nF, 5-V input pulse	6	13	23	
t_{D3}, t_{D4}	EN to output propagation delay(1)	C_{LOAD} = 1.8 nF, 5-V enable pulse	6	13	23	

(1) See the timing diagrams in Figure 1 and Figure 2

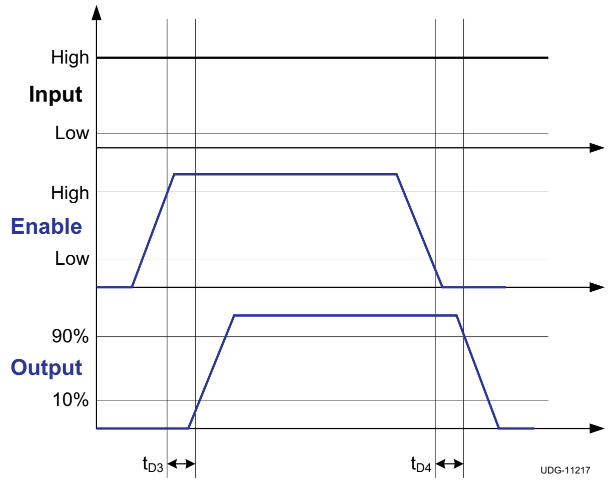


Figure 1. Enable Function (For Non-Inverting Input-Driver Operation)

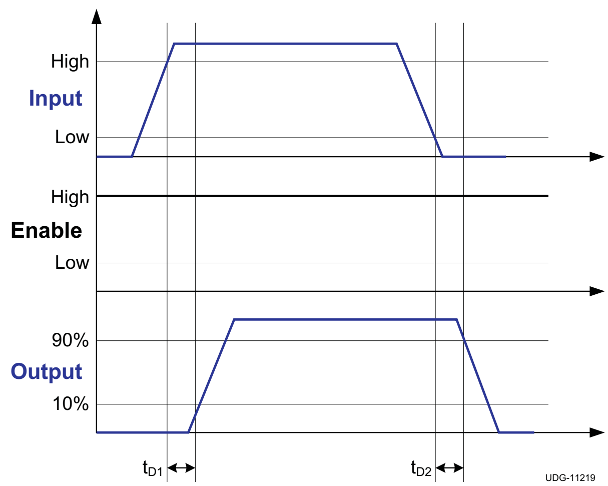


Figure 2. Non-Inverting Input-Driver Operation

7.7 Typical Characteristics

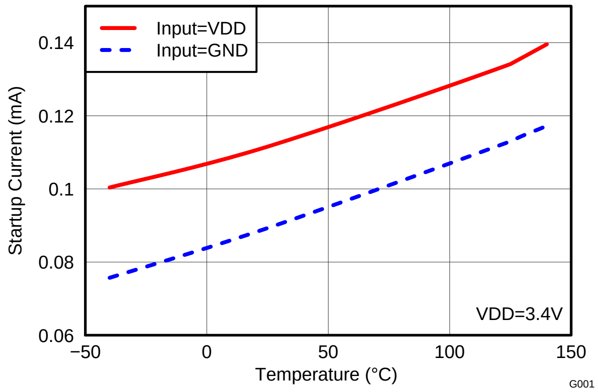


Figure 3. Start-Up Current vs Temperature

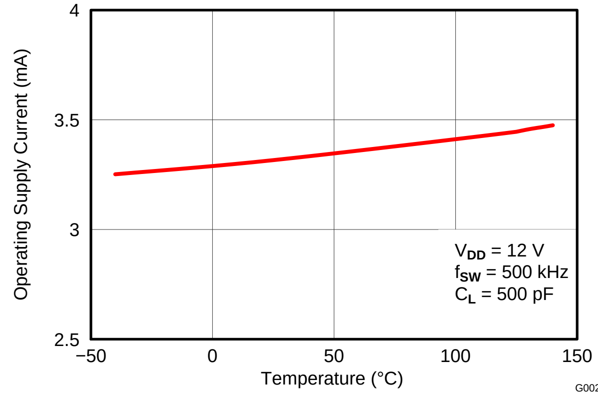


Figure 4. Operating Supply Current vs Temperature (Outputs Switching)

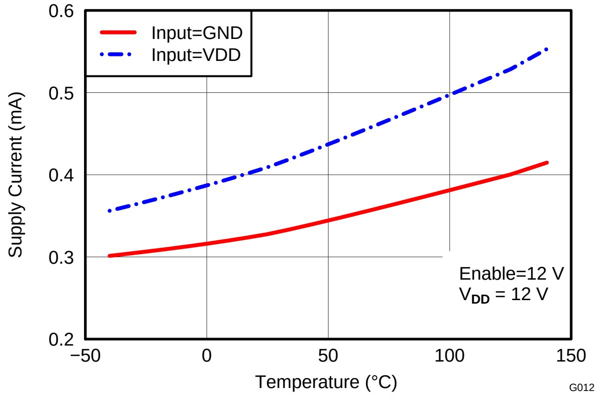


Figure 5. Supply Current vs Temperature (Outputs In DC On/Off Condition)

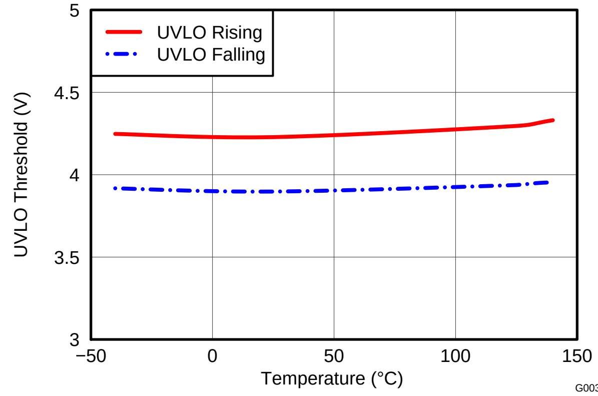


Figure 6. UVLO Threshold vs Temperature

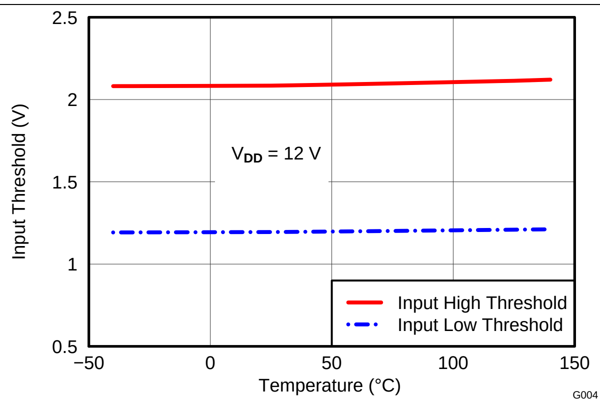


Figure 7. Input Threshold vs Temperature

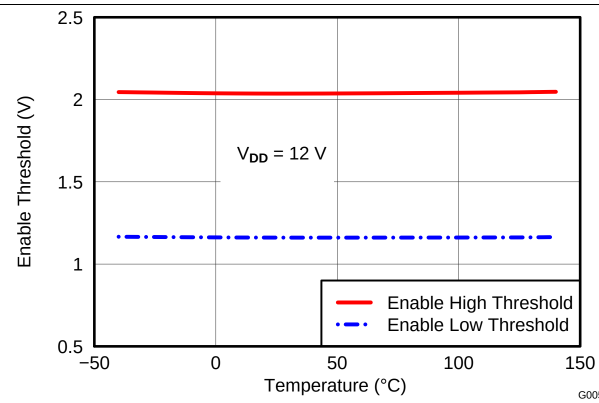


Figure 8. Enable Threshold vs Temperature

Typical Characteristics (continued)

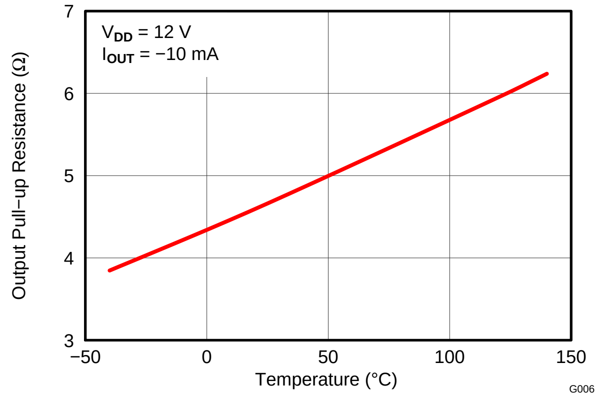


Figure 9. Output Pullup Resistance vs Temperature

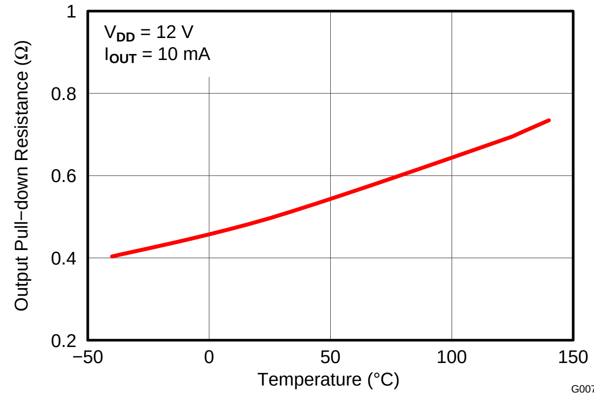


Figure 10. Output Pulldown Resistance vs Temperature

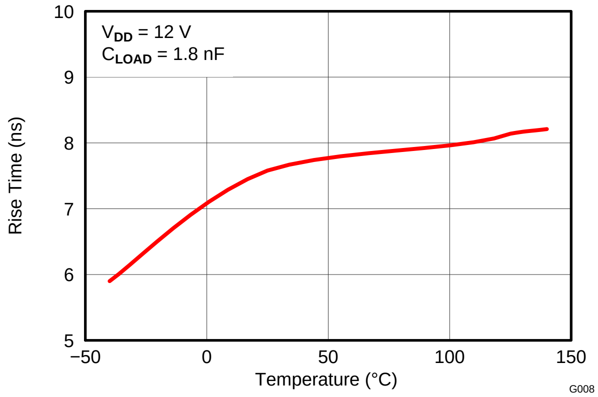


Figure 11. Rise Time vs Temperature

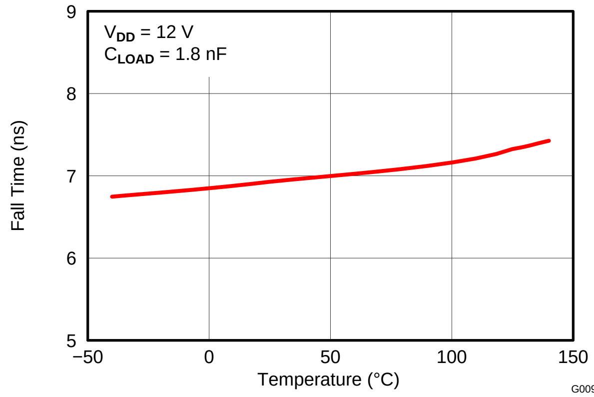


Figure 12. Fall Time vs Temperature

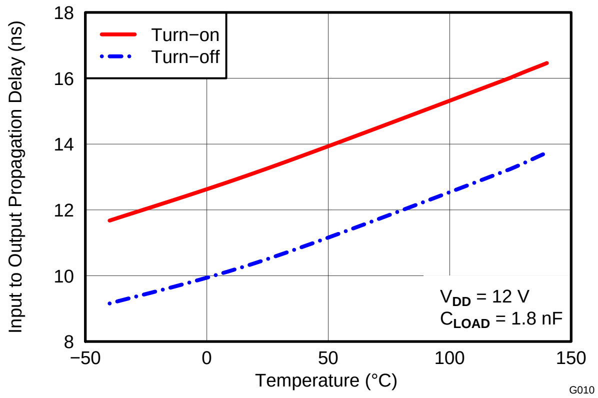


Figure 13. Input to Output Propagation Delay vs Temperature

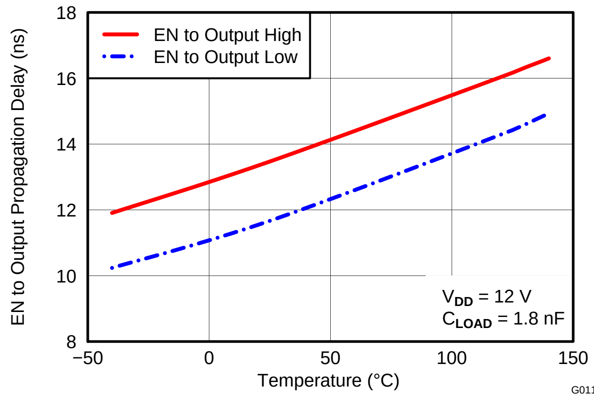


Figure 14. En to Output Propagation Delay vs Temperature

Typical Characteristics (continued)

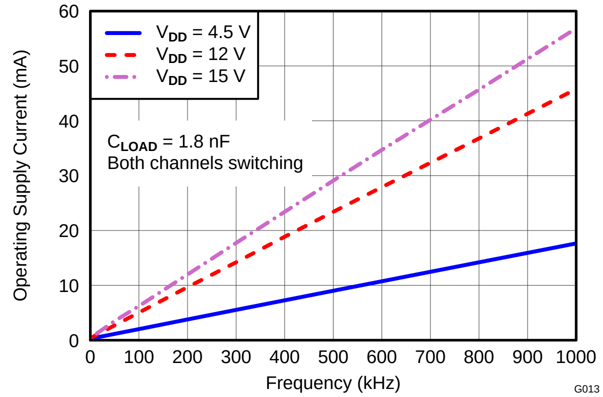


Figure 15. Operating Supply Current vs Frequency

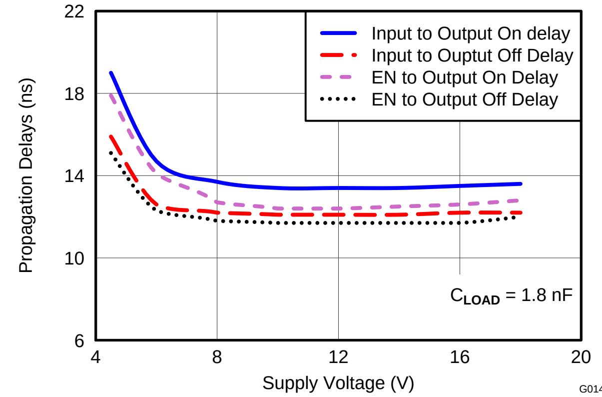


Figure 16. Propagation Delays vs Supply Voltage

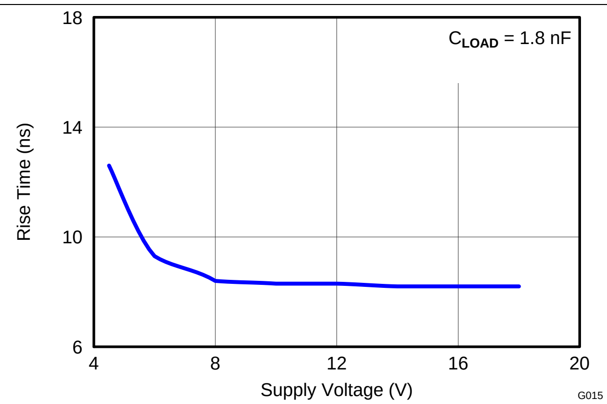


Figure 17. Rise Time vs Supply Voltage

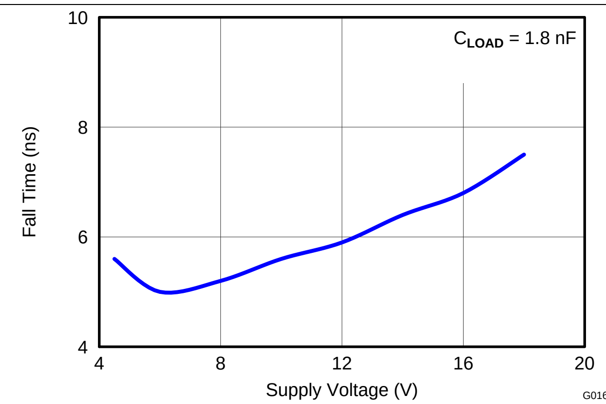


Figure 18. Fall Time vs Supply Voltage

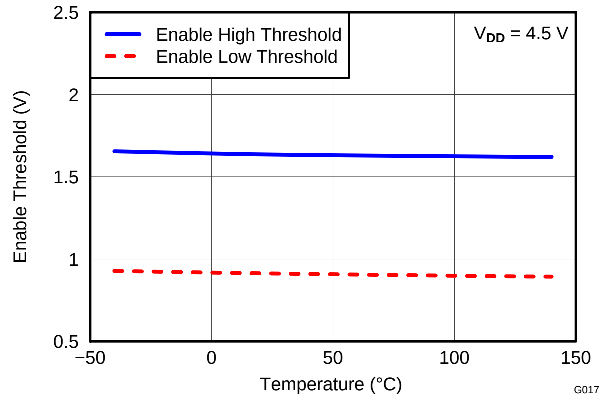


Figure 19. Enable Threshold vs Temperature

8 Detailed Description

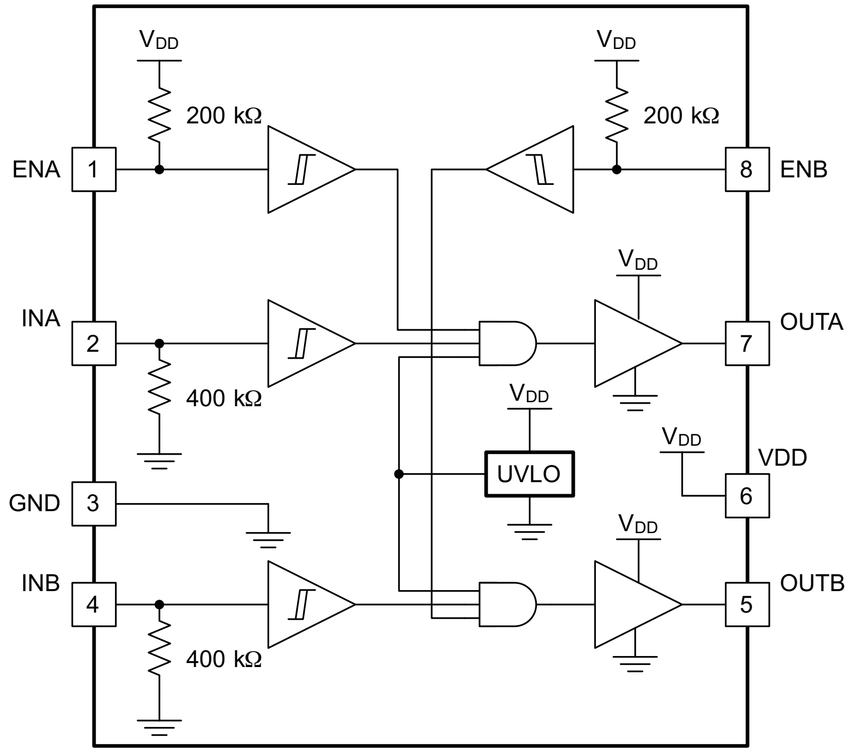
8.1 Overview

The UCC27524A device represents Texas Instruments' latest generation of dual-channel low-side high-speed gate-driver devices featuring a 5-A source and sink current capability, industry best-in-class switching characteristics, and a host of other features listed in Table 1 all of which combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

Table 1. UCC27524A Features and Benefits

FEATURE	BENEFIT
Best-in-class 13-ns (typ) propagation delay	Extremely low-pulse transmission distortion
1-ns (typ) delay matching between channels	Ease of paralleling outputs for higher (2 times) current capability, ease of driving parallel-power switches
Expanded VDD Operating range of 4.5 to 18 V	Flexibility in system design
Expanded operating temperature range of –40 °C to +140 °C (See *Electrical Characteristics* table)	
VDD UVLO Protection	Outputs are held Low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down
Outputs held Low when input pins (INx) in floating condition	Safety feature, especially useful in passing abnormal condition tests during safety certification
Outputs enable when enable pins (ENx) in floating condition	Pin-to-pin compatibility with the UCC27324 device from Texas Instruments, in designs where Pin 1 and Pin 8 are in floating condition
CMOS/TTL compatible input and enable threshold with wide hysteresis	Enhanced noise immunity, while retaining compatibility with microcontroller logic-level input signals (3.3 V, 5 V) optimized for digital power
Ability of input and enable pins to handle voltage levels not restricted by VDD pin bias voltage	System simplification, especially related to auxiliary bias supply architecture
Ability to handle –5 V_{DC} (max) at input pins	Increased robustness in noisy environments

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Supply Current

The UCC27524A products feature very low quiescent I_{DD} currents. The typical operating-supply current in UVLO state and fully-on state (under static and switching conditions) are summarized in Figure 3, Figure 4 and Figure 5. The I_{DD} current when the device is fully on and outputs are in a static state (DC high or DC low, see Figure 4) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current because of switching, and finally any current related to pullup resistors on the enable pins and inverting input pins. For example when the inverting input pins are pulled low additional current is drawn from the VDD supply through the pullup resistors (see though). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

A complete characterization of the I_{DD} current as a function of switching frequency at different V_{DD} bias voltages under 1.8-nF switching load in both channels is provided in Figure 15. The strikingly linear variation and close correlation with theoretical value of average I_{OUT} indicates negligible shoot-through inside the gate-driver device attesting to its high-speed characteristics.

8.3.2 Input Stage

The input pins of UCC27524A gate-driver devices are based on a TTL and CMOS compatible input-threshold logic that is independent of the VDD supply voltage. With typically high threshold = 2.1 V and typically low threshold = 1.2 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power-controller devices. Wider hysteresis (typ 0.9 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. UCC27524A devices also feature tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature (refer to Figure 7). The very low input capacitance on these pins reduces loading and increases switching speed.

Feature Description (continued)

The UCC27524A device features an important safety feature wherein, whenever any of the input pins is in a floating condition, the output of the respective channel is held in the low state. This is achieved using GND pulldown resistors on all the non-inverting input pins (INA, INB), as shown in the device block diagrams.

The input stage of each driver is driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns) with a slow changing input voltage, the output of the driver may switch repeatedly at a high frequency. While the wide hysteresis offered in UCC27524A definitely alleviates this concern over most other TTL input threshold devices, extra care is necessary in these implementations. If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device. This external resistor has the additional benefit of reducing part of the gate-charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

8.3.3 Enable Function

The enable function is an extremely beneficial feature in gate-driver devices especially for certain applications such as synchronous rectification where the driver outputs disable in light-load conditions to prevent negative current circulation and to improve light-load efficiency.

UCC27524A device is provided with independent enable pins ENx for exclusive control of each driver-channel operation. The enable pins are based on a non-inverting configuration (active-high operation). Thus when ENx pins are driven high the drivers are enabled and when ENx pins are driven low the drivers are disabled. Like the input pins, the enable pins are also based on a TTL and CMOS compatible input-threshold logic that is independent of the supply voltage and are effectively controlled using logic signals from 3.3-V and 5-V microcontrollers. The UCC27524A devices also feature tight control of the Enable-function threshold-voltage levels which eases system design considerations and ensures stable operation across temperature (refer to Figure 8). The ENx pins are internally pulled up to VDD using pullup resistors as a result of which the outputs of the device are enabled in the default state. Hence the ENx pins are left floating or Not Connected (N/C) for standard operation, where the enable feature is not needed. Essentially, this floating allows the UCC27524A device to be pin-to-pin compatible with TI’s previous generation of drivers (UCC27323, UCC27324, and UCC27325 respectively), where Pin 1 and Pin 8 are N/C pins. If the channel A and Channel B inputs and outputs are connected in parallel to increase the driver current capacity, ENA and ENB are connected and driven together.

8.3.4 Output Stage

The UCC27524A device output stage features a unique architecture on the pullup structure which delivers the highest peak-source current when it is most needed during the Miller plateau region of the power-switch turnon transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pullup structure features a P-Channel MOSFET and an additional N-Channel MOSFET in parallel. The function of the N-Channel MOSFET is to provide a brief boost in the peak sourcing current enabling fast turnon. This is accomplished by briefly turning-on the N-Channel MOSFET during a narrow instant when the output is changing state from Low to High.

Feature Description (continued)

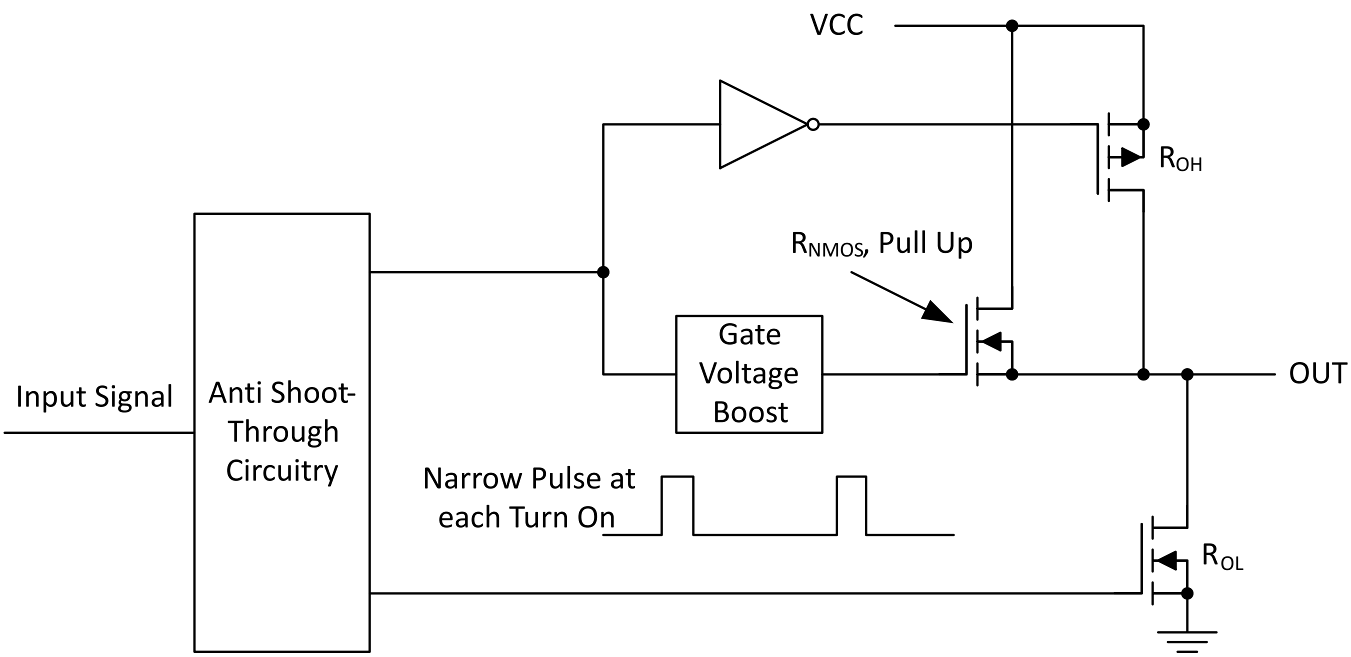


Figure 20. UCC27524A Gate Driver Output Structure

The R_{OH} parameter (see *Electrical Characteristics*) is a DC measurement and it is representative of the on-resistance of the P-Channel device only. This is because the N-Channel device is held in the off state in DC condition and is turned-on only for a narrow instant when output changes state from low to high. Note that effective resistance of the UCC27524A pullup stage during the turnon instant is much lower than what is represented by R_{OH} parameter.

The pulldown structure in the UCC27524A device is simply composed of a N-Channel MOSFET. The R_{OL} parameter (see *Electrical Characteristics*), which is also a DC measurement, is representative of the impedance of the pulldown stage in the device. In the UCC27524A device, the effective resistance of the hybrid pullup structure during turnon is estimated to be approximately 1.5 × R_{OL}, estimated based on design considerations.

Each output stage in the UCC27524A device is capable of supplying 5-A peak source and 5-A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS-output stage which delivers very low drop-out. The presence of the MOSFET-body diodes also offers low impedance to switching overshoots and undershoots which means that in many cases, external Schottky-diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

The UCC27524A device is particularly suited for dual-polarity, symmetrical drive-gate transformer applications where the primary winding of transformer driven by OUTA and OUTB, with inputs INA and INB being driven complementary to each other. This situation is because of the extremely low drop-out offered by the MOS output stage of these devices, both during high (V_{OH}) and low (V_{OL}) states along with the low impedance of the driver output stage, all of which allow alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure accurate reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turnon or turnoff interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

Feature Description (continued)

8.3.5 Low Propagation Delays And Tightly Matched Outputs

The UCC27524A driver device features a best in class, 13-ns (typical) propagation delay between input and output which goes to offer the lowest level of pulse-transmission distortion available in the industry for high frequency switching applications. For example in synchronous rectifier applications, the SR MOSFETs are driven with very low distortion when a single driver device is used to drive both the SR MOSFETs. Further, the driver devices also feature an extremely accurate, 1-ns (typical) matched internal-propagation delays between the two channels which is beneficial for applications requiring dual gate drives with critical timing. For example in a PFC application, a pair of paralleled MOSFETs can be driven independently using each output channel, which the inputs of both channels are driven by a common control signal from the PFC controller device. In this case the 1-ns delay matching ensures that the paralleled MOSFETs are driven in a simultaneous fashion with the minimum of turnon delay difference. Yet another benefit of the tight matching between the two channels is that the two channels are connected together to effectively increase current drive capability, for example A and B channels may be combined into a single driver by connecting the INA and INB inputs together and the OUTA and OUTB outputs together. Then, a single signal controls the paralleled combination.

Caution must be exercised when directly connecting OUTA and OUTB pins together because there is the possibility that any delay between the two channels during turnon or turnoff may result in shoot-through current conduction as shown in Figure 21. While the two channels are inherently very well matched (4-ns Max propagation delay), note that there may be differences in the input threshold voltage level between the two channels which causes the delay between the two outputs especially when slow dV/dt input signals are employed. The following guidelines are recommended whenever the two driver channels are paralleled using direct connections between OUTA and OUTB along with INA and INB:

- Use very fast dV/dt input signals (20 V/µs or greater) on INA and INB pins to minimize impact of differences in input thresholds causing delays between the channels.
- INA and INB connections must be made as close to the device pins as possible.

Wherever possible, a safe practice would be to add an option in the design to have gate resistors in series with OUTA and OUTB. This allows the option to use 0-Ω resistors for paralleling outputs directly or to add appropriate series resistances to limit shoot-through current, should it become necessary.

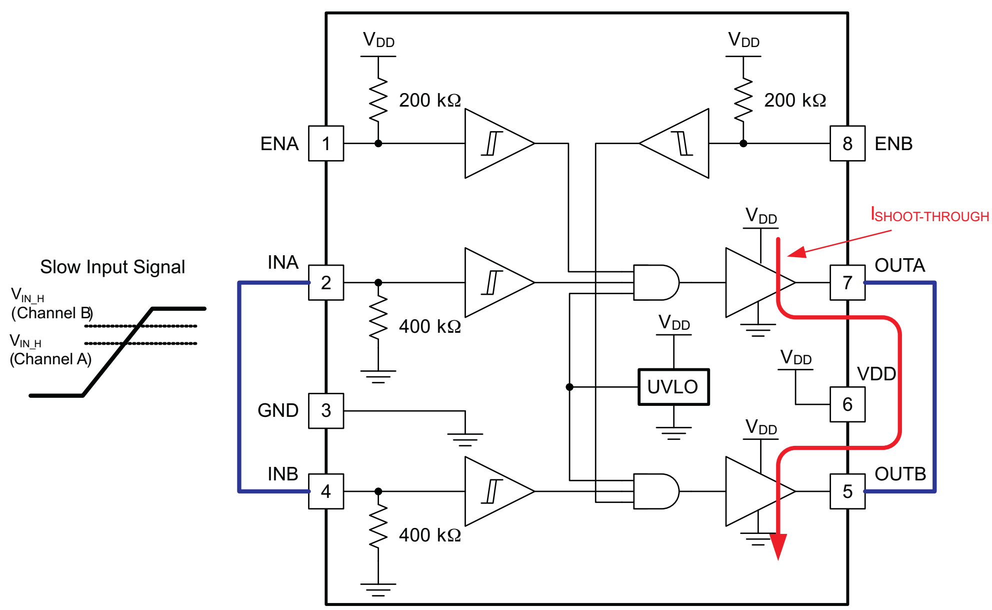


Figure 21. Slow Input Signal Can Cause Shoot-Through Between Channels During Paralleling (Recommended DV/DT is 20 V/Ms or Higher)

Feature Description (continued)

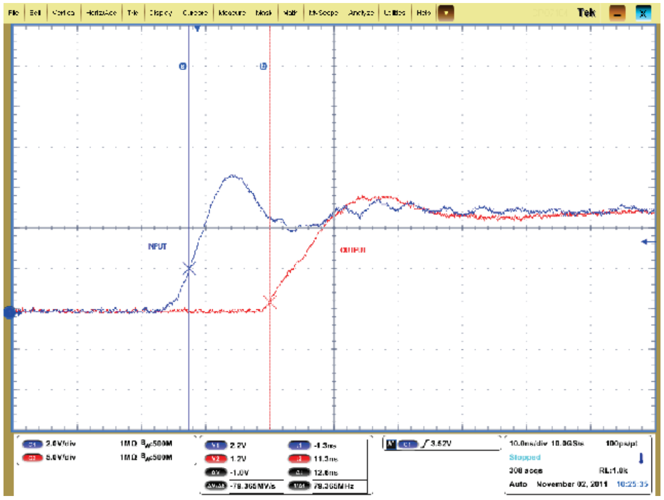


Figure 22. Turnon Propagation Delay
(C_L = 1.8 nF, VDD = 12 V)

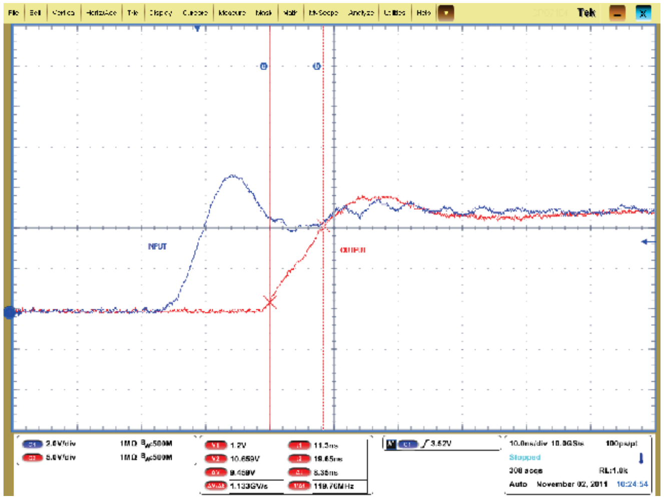


Figure 23. Turnon Rise Time
(C_L = 1.8 nF, VDD = 12 V)

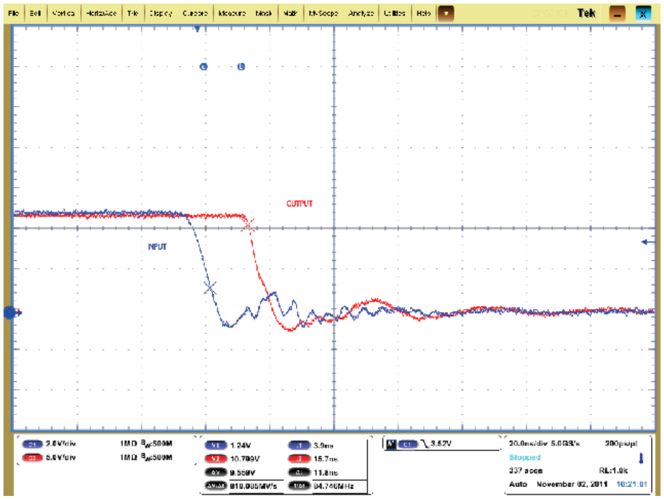


Figure 24. . Turnoff Propagation Delay
(C_L = 1.8 nF, VDD = 12 V)

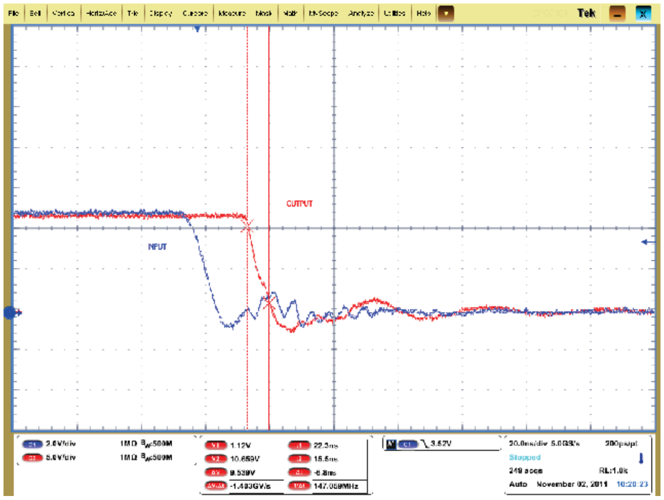


Figure 25. Turnoff Fall Time
(C_L = 1.8 nF, VDD = 12 V)

8.4 Device Functional Modes

Table 2. Device Logic Table

				UCC27524A	
ENA	**ENB**	**INA**	**INB**	**OUTA**	**OUTB**
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	x(1)	x(1)	L	L
x(1)	x(1)	L	L	L	L
x(1)	x(1)	L	H	L	H
x(1)	x(1)	H	L	H	L
x(1)	x(1)	H	H	H	H

(1) Floating condition.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

High-current gate-driver devices are required in switching power applications for a variety of reasons. In order to effect the fast switching of power devices and reduce associated switching-power losses, a powerful gate-driver device employs between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate-driver devices are indispensable when it is not feasible for the PWM controller device to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is required to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer-drive circuits based on NPN/PNP bipolar transistors in a totem-pole arrangement, as emitter-follower configurations, prove inadequate with digital power because the traditional buffer-drive circuits lack level-shifting capability. Gate-driver devices effectively combine both the level-shifting and buffer-drive functions. Gate-driver devices also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controller devices by moving gate-charge power losses into the controller. Finally, emerging wide band-gap power-device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving special requirements in terms of gate-drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays, tight delay matching and availability in compact, low-inductance packages with good thermal capability. In summary, gate-driver devices are an extremely important component in switching power combining benefits of high-performance, low-cost, component-count, board-space reduction, and simplified system design.

9.2 Typical Application

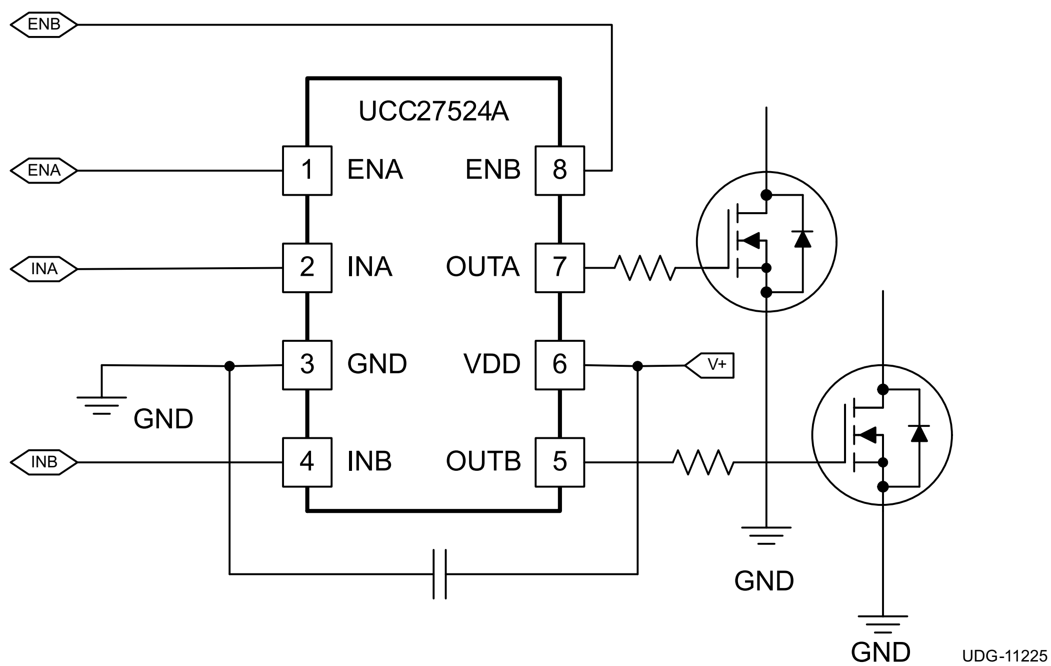


Figure 26. UCC27524A Typical Application Diagram

Typical Application (continued)

9.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some desiring considerations must be evaluated first in order to make the most appropriate selection. Among these considerations are VDD, UVLO, Drive current and power dissipation.

9.2.2 Detailed Design Procedure

9.2.2.1 VDD and Undervoltage Lockout

The UCC27524A device has an internal undervoltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. When VDD is rising and the level is still below UVLO threshold, this circuit holds the output low, regardless of the status of the inputs. The UVLO is typically 4.25 V with 350-mV typical hysteresis. This hysteresis prevents chatter when low VDD supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at low voltage levels such as below 5 V, along with best in class switching characteristics, is especially suited for driving emerging GaN power semiconductor devices.

For example, at power up, the UCC27524A driver-device output remains low until the V_{DD} voltage reaches the UVLO threshold if enable pin is active or floating. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. The non-inverting operation in Figure 27 shows that the output remains low until the UVLO threshold is reached, and then the output is in-phase with the input. The inverting operation in shows that the output remains low until the UVLO threshold is reached, and then the output is out-phase with the input.

Because the device draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1-µF ceramic capacitor must be located as close as possible to the VDD to GND pins of the gate-driver device. In addition, a larger capacitor (such as 1-µF) with relatively low ESR must be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

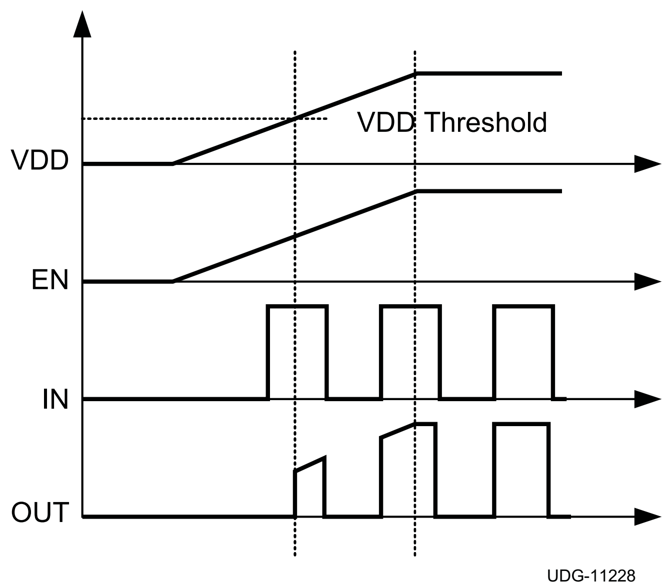


Figure 27. Power-Up Non-Inverting Driver

Typical Application (continued)

9.2.2.2 Drive Current and Power Dissipation

The UCC27524A driver is capable of delivering 5-A of current to a MOSFET gate for a period of several-hundred nanoseconds at VDD = 12 V. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground which repeats at the operating frequency of the power device. The power dissipated in the gate driver device package depends on the following factors:

- Gate charge required of the power MOSFET (usually a function of the drive voltage V_{GS}, which is very close to input bias supply voltage V_{DD} due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

Because UCC27524A features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver can be safely assumed to be negligible.

When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 1.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

where

- C_{LOAD} is the load capacitor
- V_{DD}^2 is the bias voltage feeding the driver (1)

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by Equation 2.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW}$$

where

- f_{SW} is the switching frequency (2)

With V_{DD} = 12 V, C_{LOAD} = 10 nF and f_{SW} = 300 kHz the power loss is calculated with Equation 3

$$P_G = 10\,nF \times 12\,V^2 \times 300\,kHz = 0.432\,W \quad (3)$$

Typical Application (continued)

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, the power that must be dissipated when charging a capacitor is determined which by using the equivalence $Q_g = C_{LOAD}V_{DD}$ to provide Equation 4 for power:

$$P_G = C_{LOAD}V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \quad (4)$$

Assuming that the UCC27524A device is driving power MOSFET with 60 nC of gate charge (Q_g = 60 nC at V_{DD} = 12 V) on each output, the gate charge related power loss is calculated with Equation 5.

$$P_G = 2 \text{x} 60\,\text{nC} \times 12\,\text{V} \times 300\,\text{kHz} = 0.432\,\text{W} \quad (5)$$

This power PG is dissipated in the resistive elements of the circuit when the MOSFET turns on or turns off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows (see Equation 6):

$$P_{SW} = 0.5 \times Q_G \times VDD \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right)$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pullup structure) = 1.5 x R_{OL} (6)

In addition to the above gate-charge related power dissipation, additional dissipation in the driver is related to the power associated with the quiescent bias current consumed by the device to bias all internal circuits such as input stage (with pullup and pulldown resistors), enable, and UVLO sections. As shown in Figure 4, the quiescent current is less than 0.6 mA even in the highest case. The quiescent power dissipation is calculated easily with Equation 7.

$$P_Q = I_{DD} V_{DD} \quad (7)$$

Assuming , I_{DD} = 6 mA, the power loss is:

$$P_Q = 0.6\text{ mA} \times 12\,\text{V} = 7.2\,\text{mW} \quad (8)$$

Clearly, this power loss is insignificant compared to gate charge related power dissipation calculated earlier.

With a 12-V supply, the bias current is estimated as follows, with an additional 0.6-mA overhead for the quiescent consumption:

$$I_{DD} \sim \frac{P_G}{V_{DD}} = \frac{0.432\text{ W}}{12\text{ V}} = 0.036\text{ A} \quad (9)$$

9.2.3 Application Curve

Figure 28 and Figure 29 show the typical switching characteristics of the UCC27524A device.

Typical Application (continued)

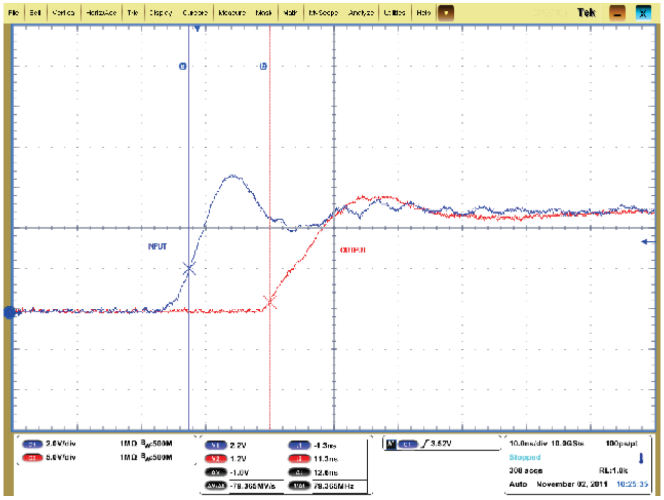


Figure 28. Typical Turnon Waveform (CL = 1.8 nF, VDD = 12 V)

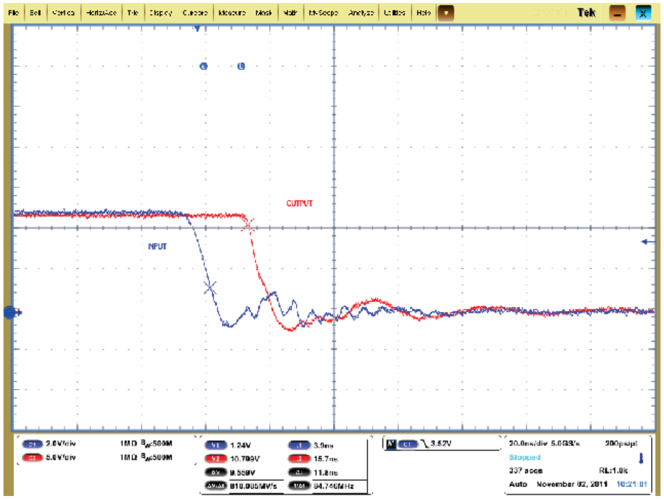


Figure 29. Typical Turnoff Waveform (CL = 1.8 nF, VDD = 12 V)

10 Power Supply Recommendations

The bias supply voltage range for which the UCC27524A device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the V_{ON} supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 2-V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 18 V.

The UVLO protection feature also involves a hysteresis function. This means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification VDD_H. Therefore, ensuring that, while operating at or near the 4.5-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the V_{OFF} threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup, the device does not begin operation until the V_{DD} pin voltage has exceeded above the V_{ON} threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUTA/B pin is also supplied through the same V_{DD} pin is important. As a result, every time a current is sourced out of the output pins, a corresponding current pulse is delivered into the device through the $VV_{DD}DD$ pin. Thus ensuring that local bypass capacitors are provided between the V_{DD} and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low ESR, ceramic surface mount capacitor is a must. TI recommends having 2 capacitors; a 100-nF ceramic surface-mount capacitor which can be nudged very close to the pins of the device and another surface-mount capacitor of few microfarads added in parallel.

11 Layout

11.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC27524A gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power MOSFET to facilitate voltage transitions very quickly. At higher VDD voltages, the peak current capability is even higher (5-A peak current is at VDD = 12 V). Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD during turnon of power MOSFET. The use of low inductance surface-mounted-device (SMD) components such as chip resistors and chip capacitors is highly recommended.
- The turnon and turnoff current loop paths (driver device, power MOSFET and VDD bypass capacitor) must be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances during turnon and turnoff transients which induces significant voltage transients on the output pin of the driver device and Gate of the power MOSFET.
- Wherever possible, parallel the source and return traces to take advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver is connected to the other circuit nodes such as source of power MOSFET and ground of PWM controller at one, single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground

Layout Guidelines (continued)

plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well

- In noisy environments, tying inputs of an unused channel of the UCC27524A device to VDD (in case of INx+) or GND (in case of INX–) using short traces in order to ensure that the output is enabled and to prevent noise from causing malfunction in the output may be necessary.
- Exercise caution when replacing the UCC2732x/UCC2742x devices with the UCC27524A device:
  - The UCC27524A device is a much stronger gate driver (5-A peak current versus 4-A peak current).
  - The UCC27524A device is a much faster gate driver (13-ns/13-ns rise and fall propagation delay versus 25-ns/35-ns rise and fall propagation delay).

11.2 Layout Example

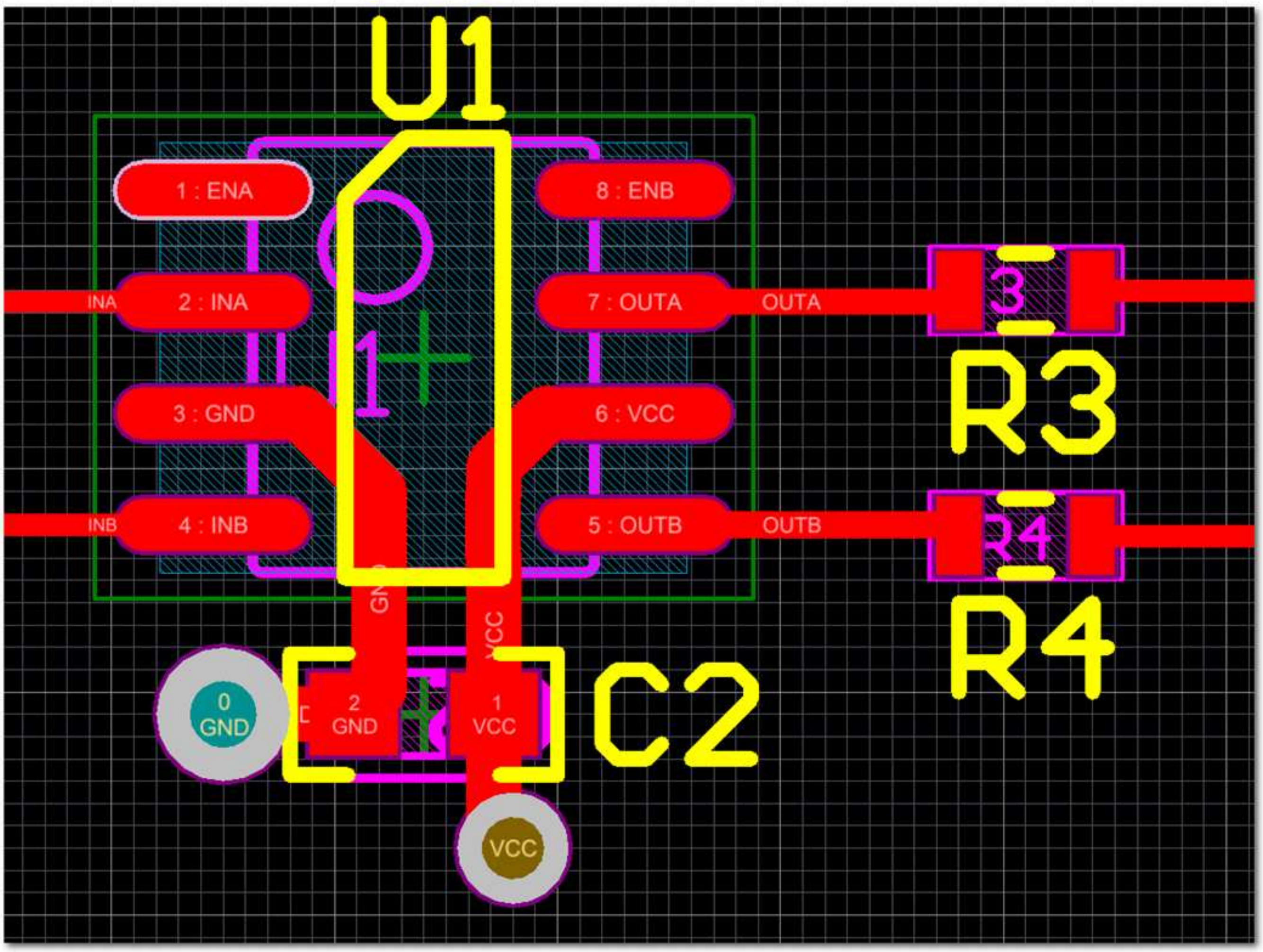


Figure 30. UCC27524A Layout Example

11.3 Thermal Protection

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a gate driver device to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. For detailed information regarding the thermal information table, please refer to Application Note from Texas Instruments entitled, *IC Package Thermal Metrics* (SPRA953).

Thermal Protection (continued)

Among the different package options available for the UCC27524A device, power dissipation capability of the DGN package is of particular mention. The MSOP PowerPAD-8 (DGN) package offers a means of removing the heat from the semiconductor junction through the bottom of the package. This package offers an exposed thermal pad at the base of the package. This pad is soldered to the copper on the printed circuit board directly underneath the device package, reducing the thermal resistance to a very low value. This allows a significant improvement in heat-sinking over that available in the D package. The printed circuit board must be designed with thermal lands and thermal vias to complete the heat removal subsystem. Note that the exposed pads in the MSOP-8 (PowerPAD) package are not directly connected to any leads of the package, however, the PowerPAD is electrically and thermally connected to the substrate of the device which is the ground of the device. TI recommends to externally connect the exposed pads to GND in PCB layout for better EMI immunity.

12 Device and Documentation Support

12.1 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27524AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27524A	Samples
UCC27524ADGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	524A	Samples
UCC27524ADGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	524A	Samples
UCC27524ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27524A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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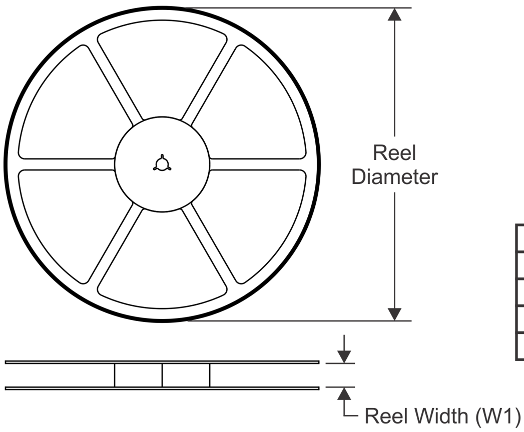
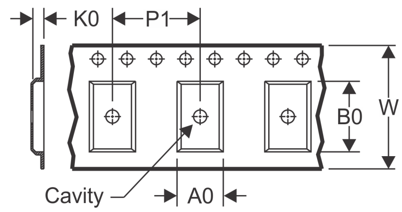
TAPE AND REEL INFORMATION

REEL DIMENSIONS

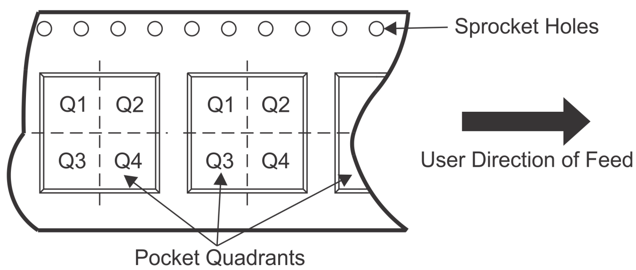


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

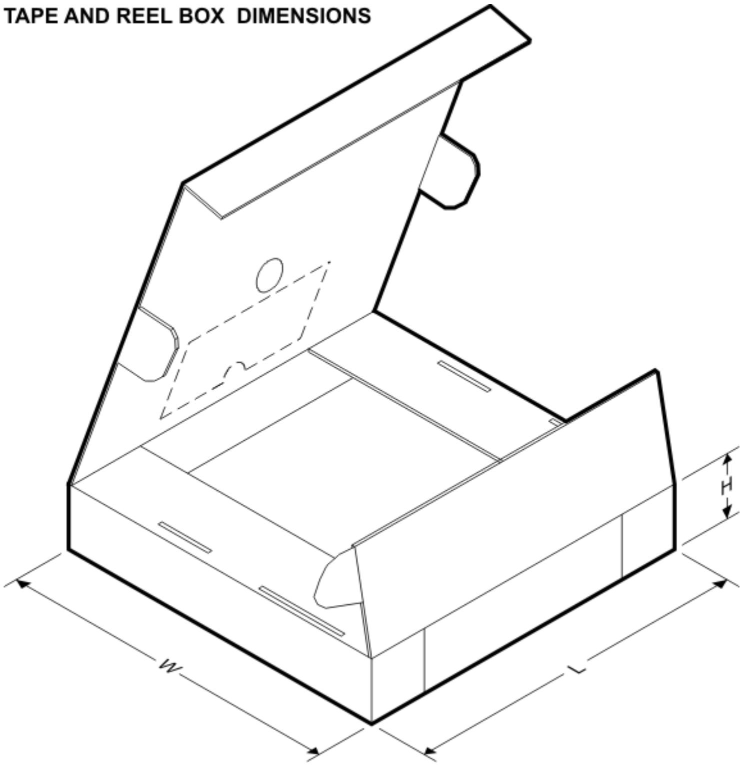
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27524ADGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27524ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

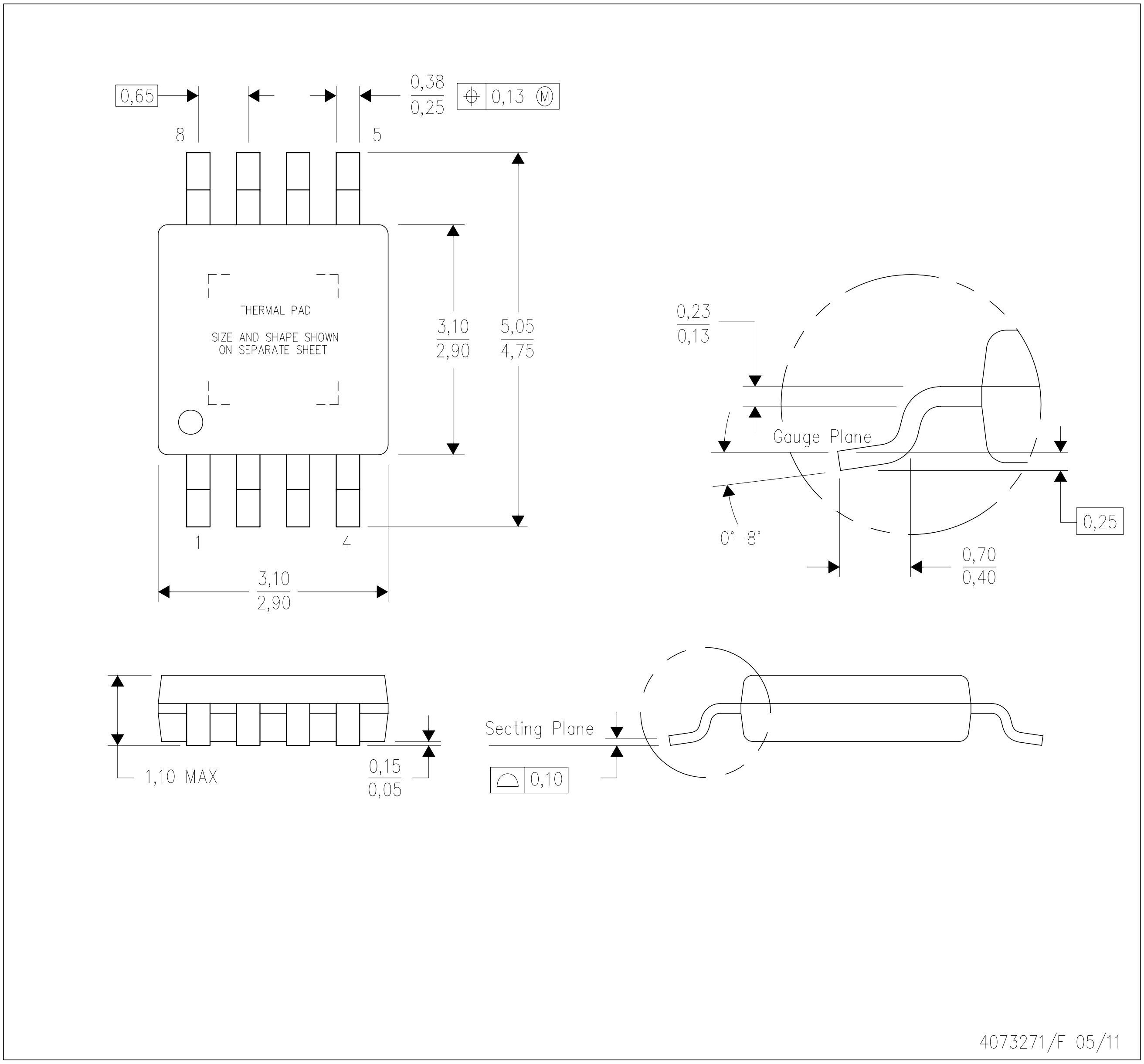
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27524ADGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
UCC27524ADR	SOIC	D	8	2500	367.0	367.0	35.0

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

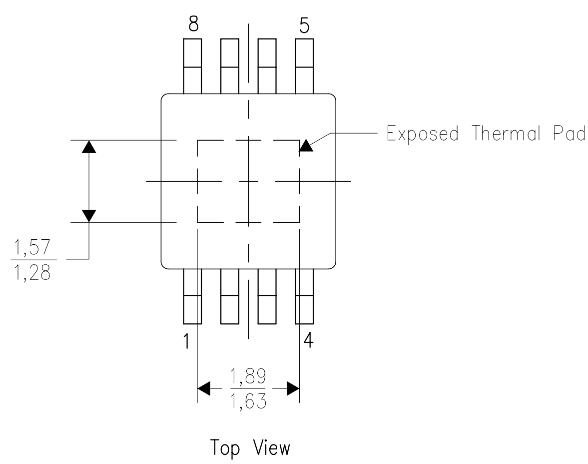
DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206323-2/I 12/11

NOTE: All linear dimensions are in millimeters

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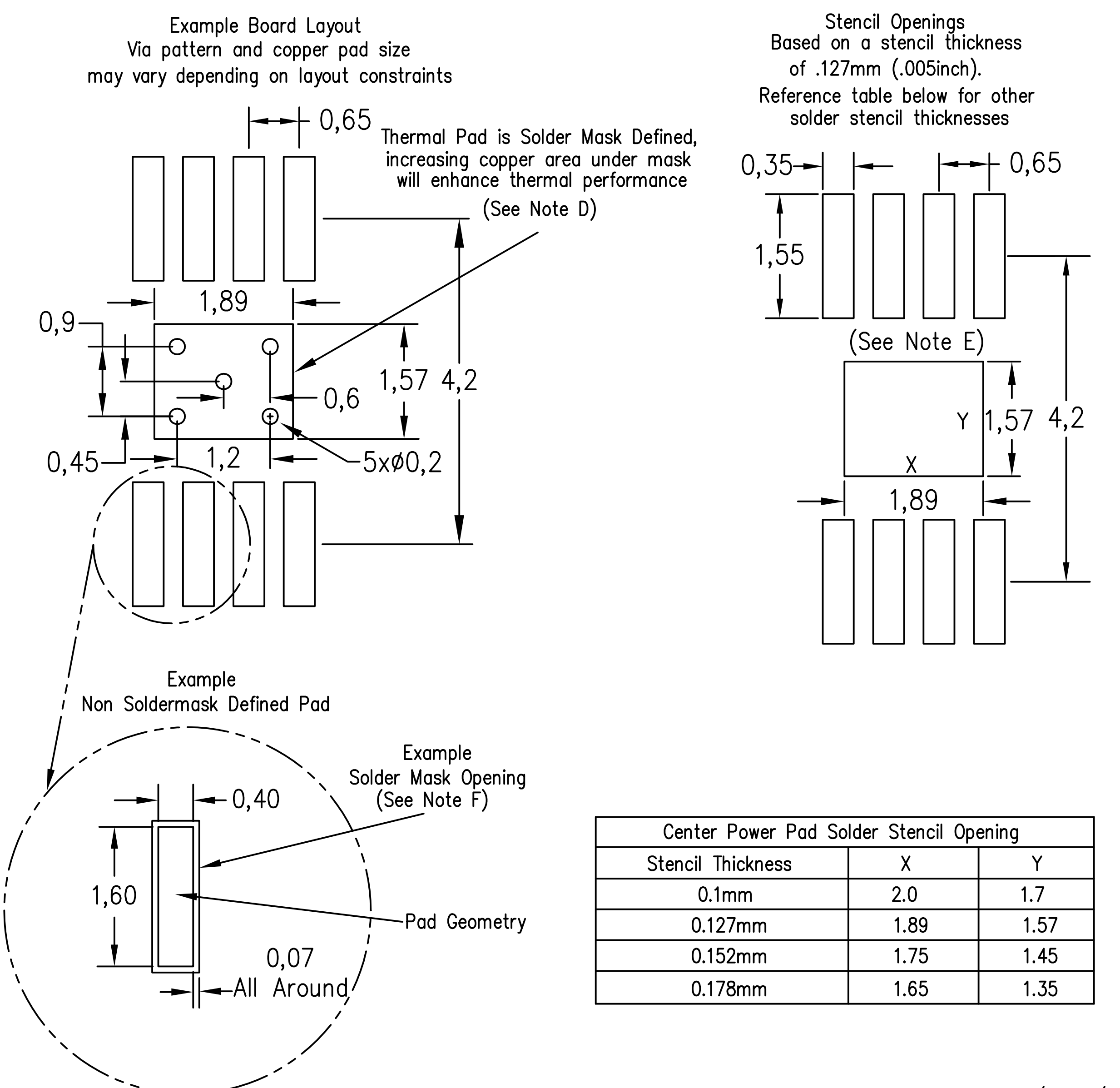
DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

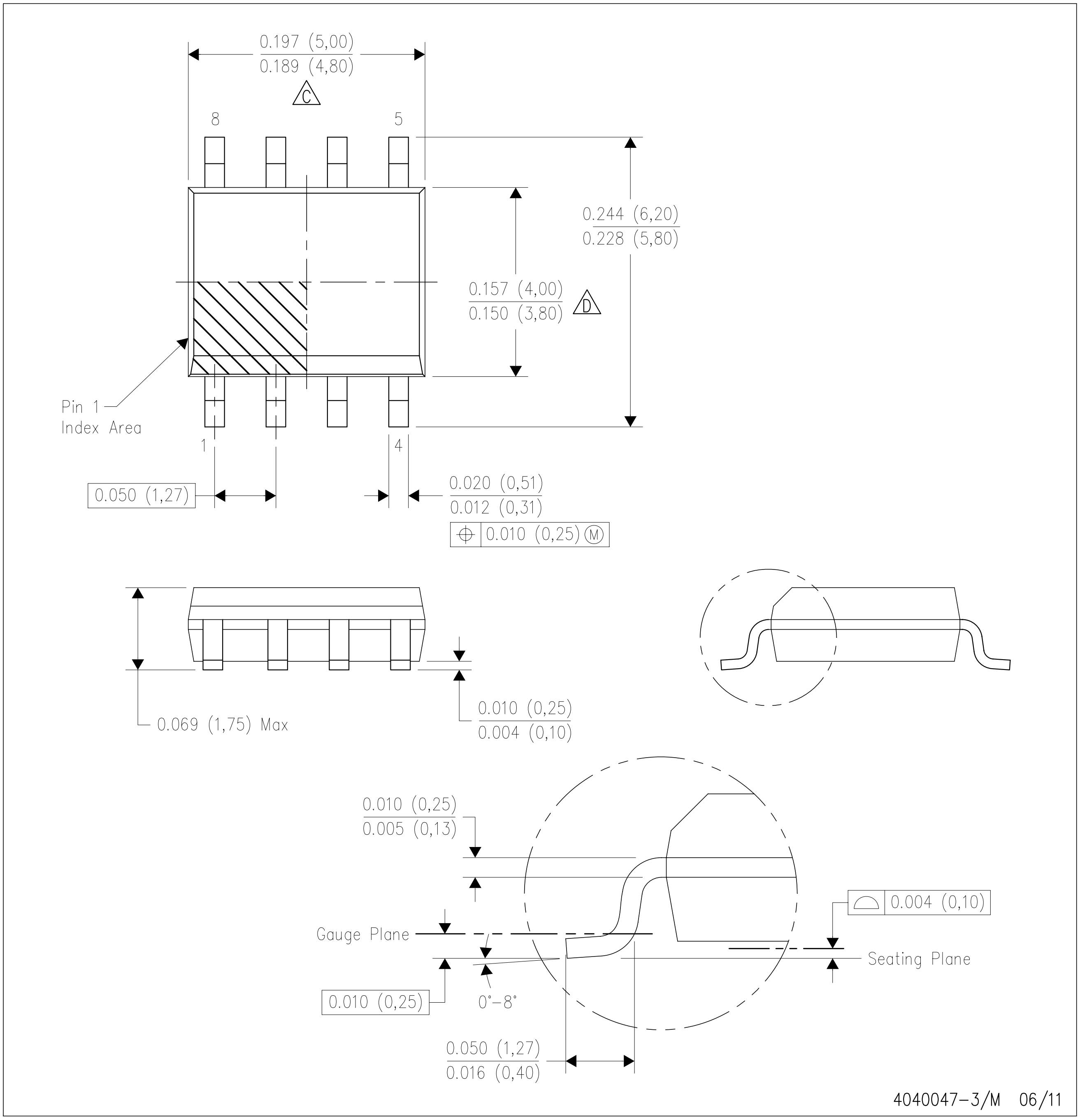


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737-2/F 02/13

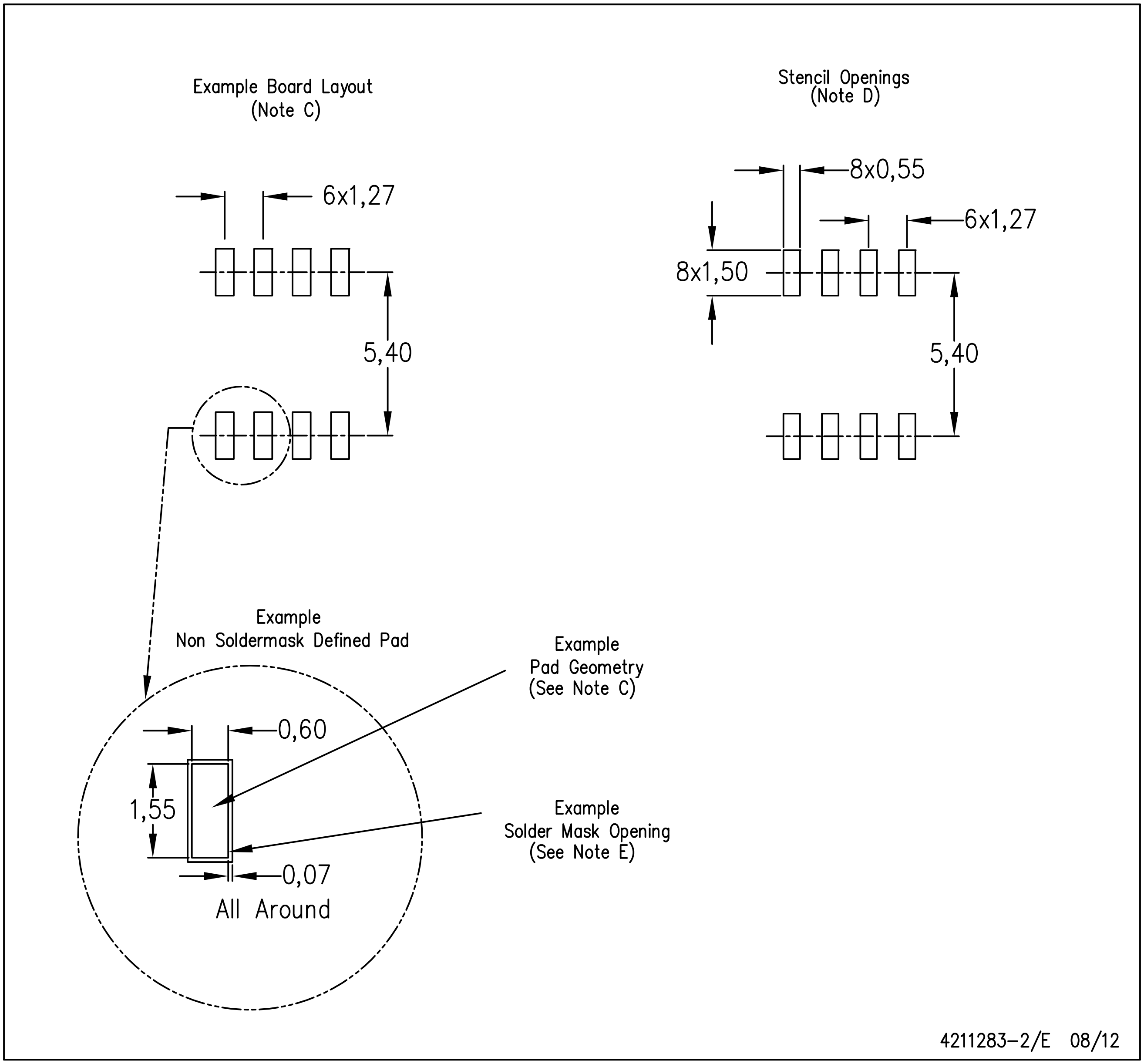
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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