



STL60N32N3LL

Dual N-channel 30 V, 0.005 Ω , 15 A PowerFLAT™ 5x6 asymmetrical double island, STripFET™ Power MOSFET

Features

Order code		V _{DSS}	R _{DS(on)}	I _D
STL60N32N3LL	Q ₁	30 V	< 0.0092 Ω	13.6 A
	Q ₂	30 V	< 0.0055 Ω	15 A

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

Application

- Switching applications

Description

This device is a dual N-channel Power MOSFET which utilizes the latest generation of design rules for ST's proprietary STripFET™ V and STripFET™ VI DeepGATE™ technology. The lowest available RDS(on)* Qg in this chip scale package renders the device suitable for the most demanding DC-DC converter applications, where high power density is required.

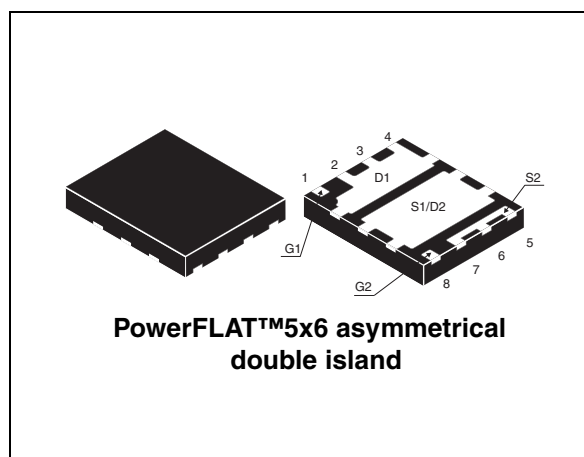


Figure 1. Internal schematic diagram

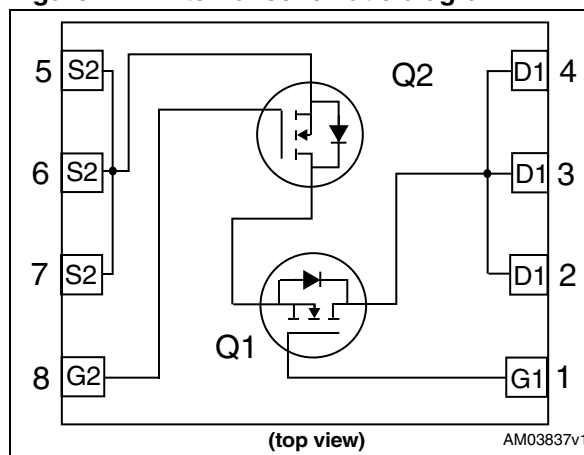


Table 1. Device summary

Order code	Marking	Package	Packaging
STL60N32N3LL	60N32N3LL	PowerFLAT™ 5x6 asymmetrical double island	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Type	Value	Unit
V_{DS}	Drain-source voltage	Q_1	30	V
		Q_2	30	V
V_{GS}	Gate- source voltage	Q_1	± 20	V
		Q_2	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	Q_1	32	A
		Q_2	60	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	Q_1	23	A
		Q_2	37	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	Q_1	13.6	A
		Q_2	15	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	Q_1	8.5	A
		Q_2	9.3	A
$I_{DM}^{(2),(3)}$	Drain current (pulsed)	Q_1	54.4	A
		Q_2	60	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	Q_1	23	W
		Q_2	50	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	Q_1	3.12	W
		Q_2	3.12	W
T_j	Operating junction temperature		-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature			

1. This value is according to R_{thj-c}
2. This value is according to $R_{thj-pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Type	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max		40	$^\circ\text{C/W}$
R_{thj-c}	Thermal resistance junction-case	Q_1	5.5	$^\circ\text{C/W}$
		Q_2	2.5	

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	Q_1 Q_2	30 30			V V
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = 30\ \text{V}$	Q_1 Q_2			1 1	μA μA
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = 30\ \text{V}$, $T_C = 125^{\circ}\text{C}$	Q_1 Q_2			10 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\ \text{V}$	Q_1 Q_2			± 100 ± 100	nA nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	Q_1 Q_2	1 1			V V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}$, $I_D = 6.8\ \text{A}$ $V_{GS} = 10\ \text{V}$, $I_D = 7.5\ \text{A}$	Q_1 Q_2		0.0085 0.005	0.0092 0.0055	Ω Ω
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 4.5\ \text{V}$, $I_D = 6.8\ \text{A}$ $V_{GS} = 4.5\ \text{V}$, $I_D = 7.5\ \text{A}$	Q_1 Q_2		0.0109 0.0065	0.012 0.0073	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$	Q_1 Q_2	- -	950 1690	- -	pF pF
C_{oss}	Output capacitance		Q_1 Q_2	- -	193 291	- -	pF pF
C_{rss}	Reverse transfer capacitance		Q_1 Q_2	- -	27.6 176	- -	pF pF
Q_g	Total gate charge	$V_{DD} = 15\ \text{V}$, $I_D = 15\ \text{A}$, $V_{GS} = 4.5\ \text{V}$ (see Figure 25)	Q_1 Q_2	- -	6.6 17	- -	nC nC
Q_{gs}	Gate-source charge		Q_1 Q_2	- -	3.3 8	- -	nC nC
Q_{gd}	Gate-drain charge		Q_1 Q_2	- -	2.4 6	- -	nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$, $I_D=7.5\text{ A}$, $R_G=4.7\ \Omega$	Q_1		10.8		ns
t_r	Rise time	$V_{GS}=4.5\text{ V}$ (see Figure 29)	Q_2	-	9.5	-	ns
			Q_1		15.6		ns
			Q_2		30		ns
$t_{d(off)}$	Turn-off delay time	$V_{DD}=15\text{ V}$, $I_D=7.5\text{ A}$, $R_G=4.7\ \Omega$	Q_1		14.2		ns
t_f	Fall time	$V_{GS}=4.5\text{ V}$ (see Figure 29)	Q_2	-	37	-	ns
			Q_1		6		ns
			Q_2		12		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current	$V_{DD}=15\text{ V}$, $I_D=7.5\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$	Q_1 Q_2	-		13.6 15	A A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)	$V_{DD}=15\text{ V}$, $I_D=7.5\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$	Q_1 Q_2	-		54.4 60	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=15\text{ A}$, $V_{GS}=0$	Q_1 Q_2	-		1.1 1.1	V V
t_{rr}	Reverse recovery time	$I_{SD}=15\text{ A}$, $V_{DD}=15\text{ V}$	Q_1 Q_2		20 24		ns ns
Q_{rr}	Reverse recovery charge	$di/dt=100\text{ A}/\mu\text{s}$, $T_j=150^\circ\text{C}$	Q_1 Q_2	-	10 16.8		nC nC
I_{RRM}	Reverse recovery current	(see Figure 29)	Q_1 Q_2		1 1.4		A A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

2.1.1 Graphs for Q1

Figure 2. Safe operating area

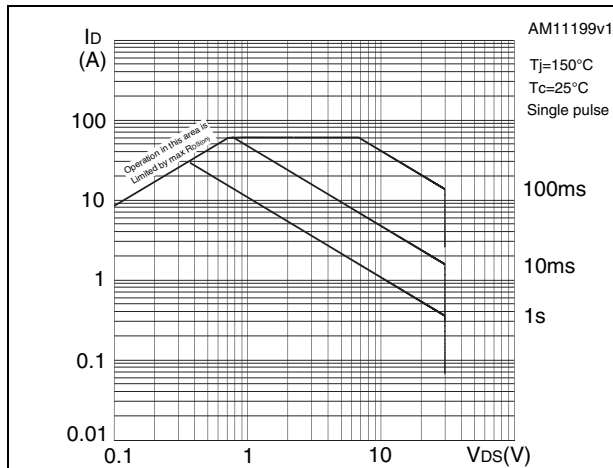


Figure 3. Thermal impedance

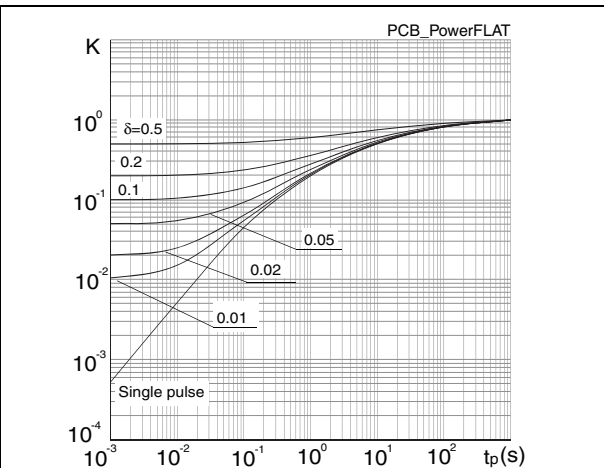


Figure 4. Output characteristics

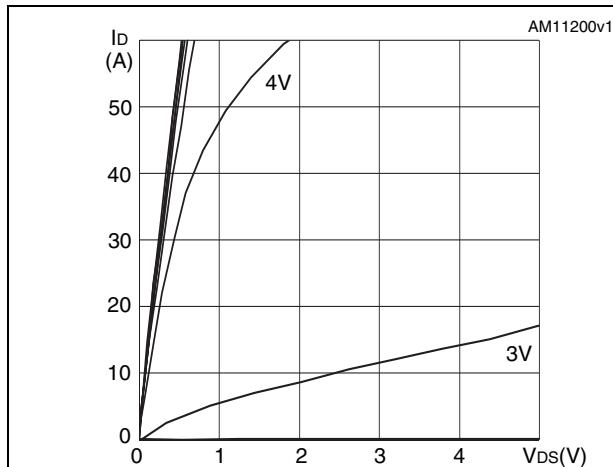


Figure 5. Transfer characteristics

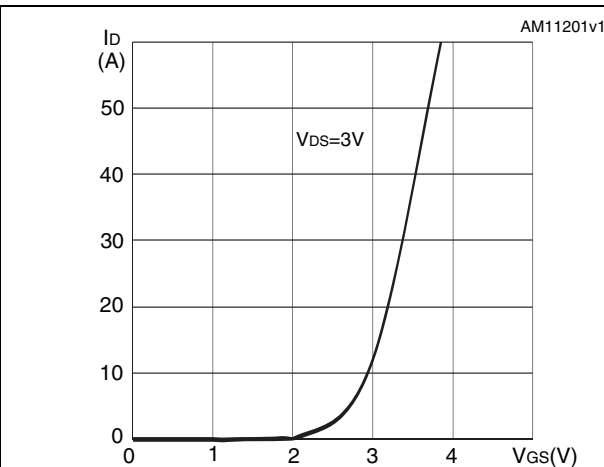


Figure 6. Normalized $B_{V_{DS}}$ vs temperature

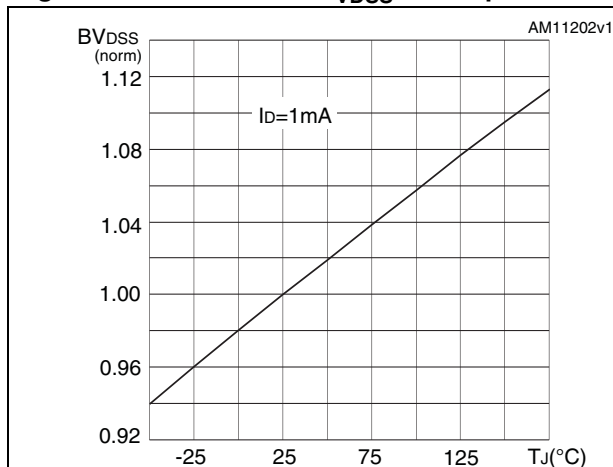


Figure 7. Static drain-source on resistance

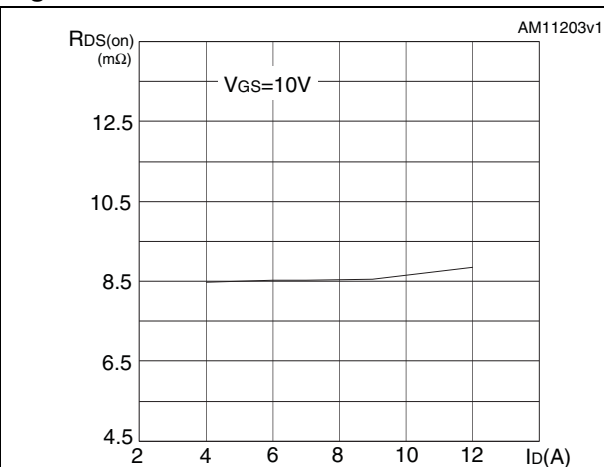


Figure 8. Gate charge vs gate-source voltage

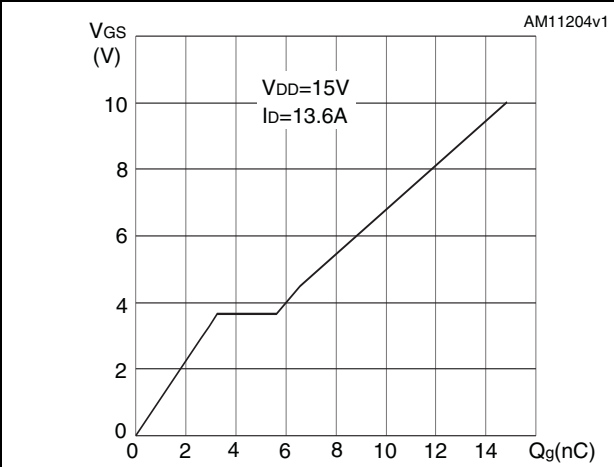


Figure 9. Capacitance variations

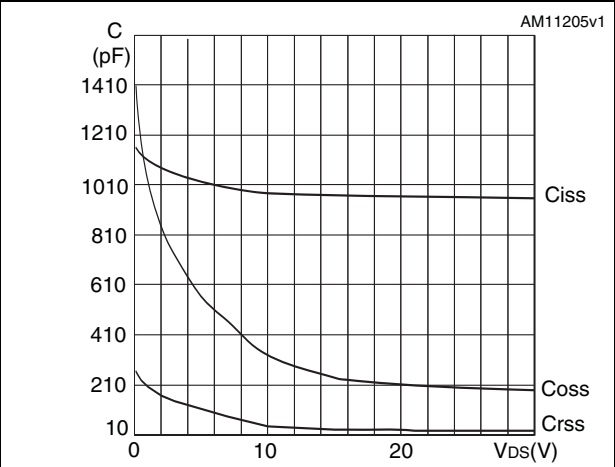


Figure 10. Normalized gate threshold voltage vs temperature

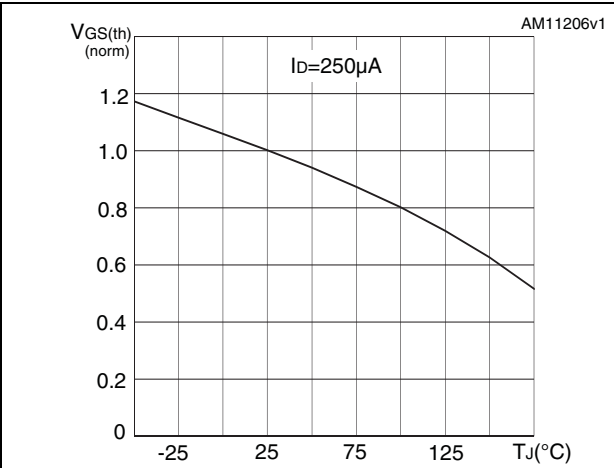


Figure 11. Normalized on resistance vs temperature

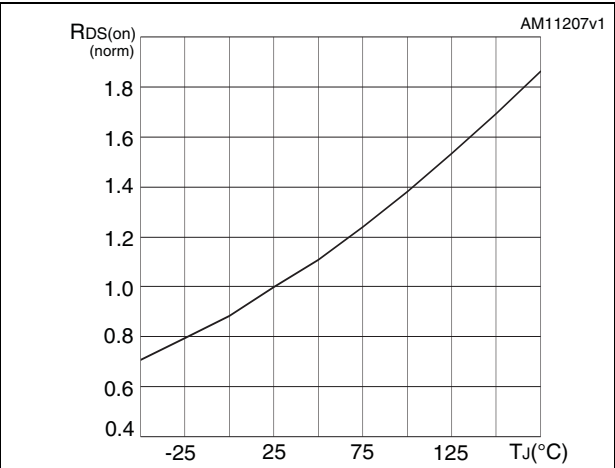
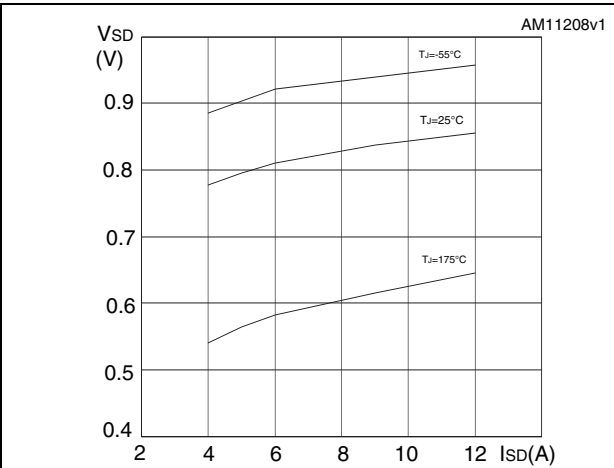


Figure 12. Source-drain diode forward characteristics



2.1.2 Graphs for Q2

Figure 13. Safe operating area

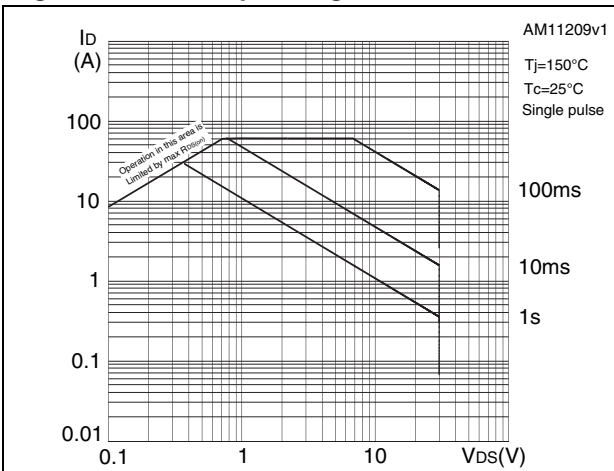


Figure 14. Thermal impedance

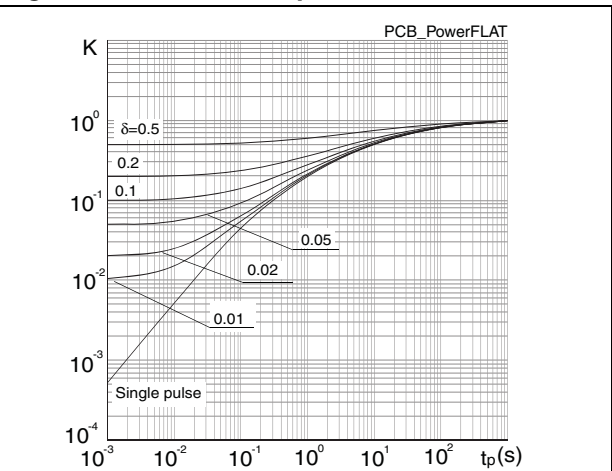


Figure 15. Output characteristics

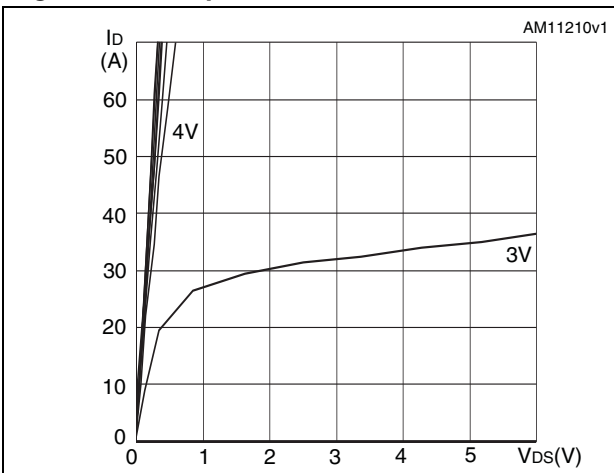


Figure 16. Transfer characteristics

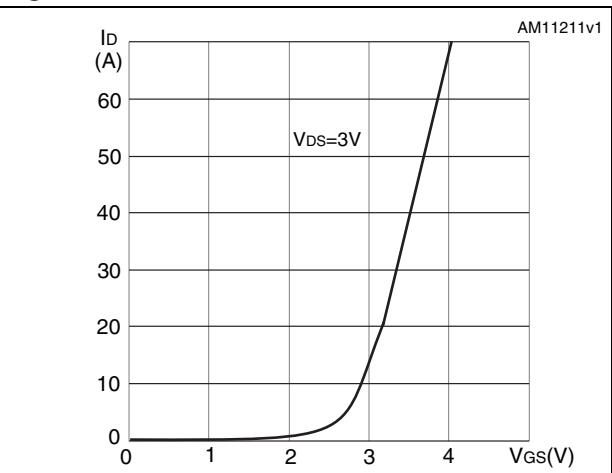


Figure 17. Normalized $B_{V_{DS}}$ vs temperature

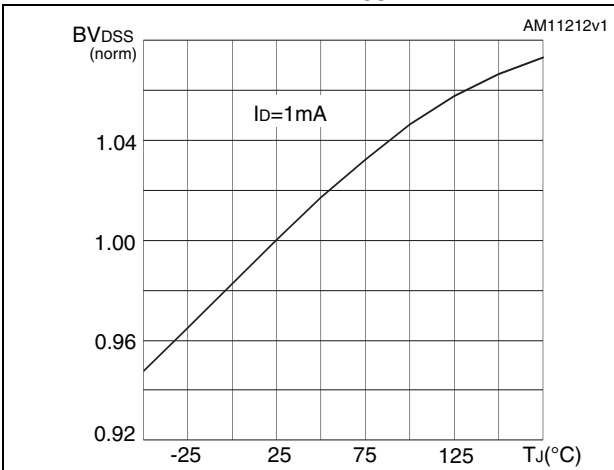


Figure 18. Static drain-source on resistance

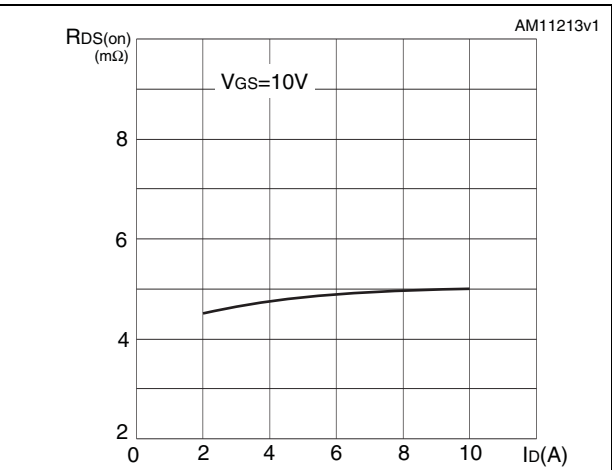


Figure 19. Gate charge vs gate-source voltage

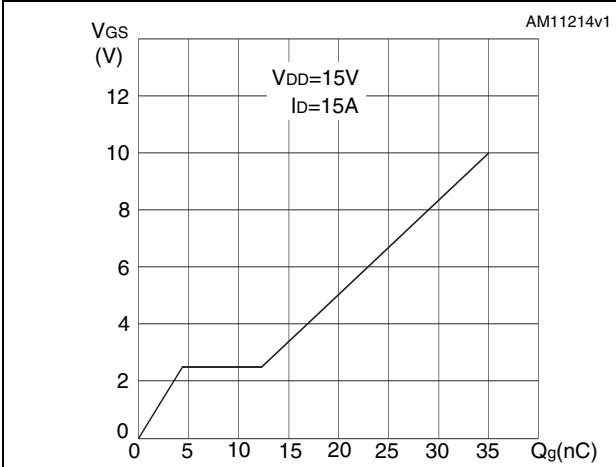


Figure 20. Capacitance variations

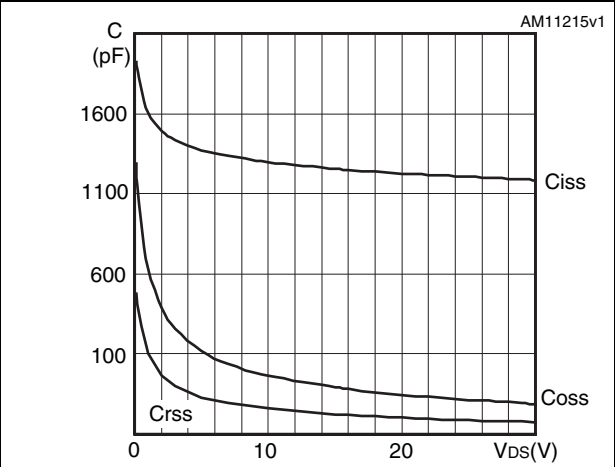


Figure 21. Normalized gate threshold voltage vs temperature

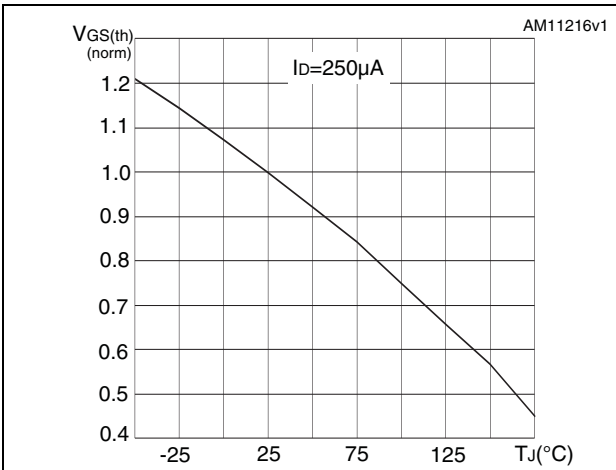


Figure 22. Normalized on resistance vs temperature

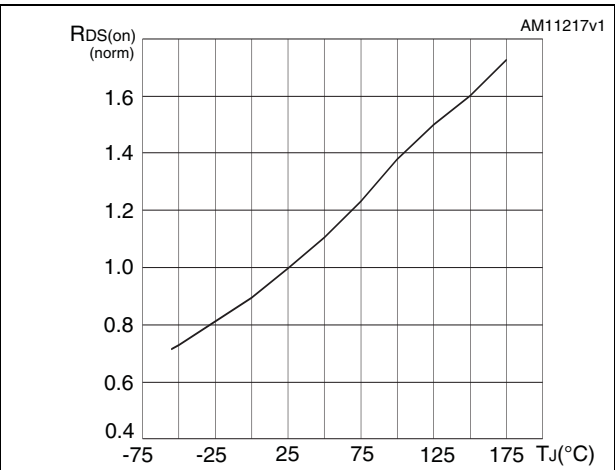
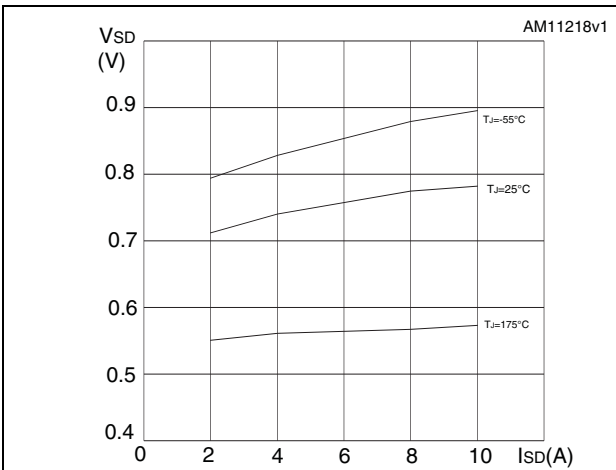


Figure 23. Source-drain diode forward characteristics



3 Test circuits

Figure 24. Switching times test circuit for resistive load

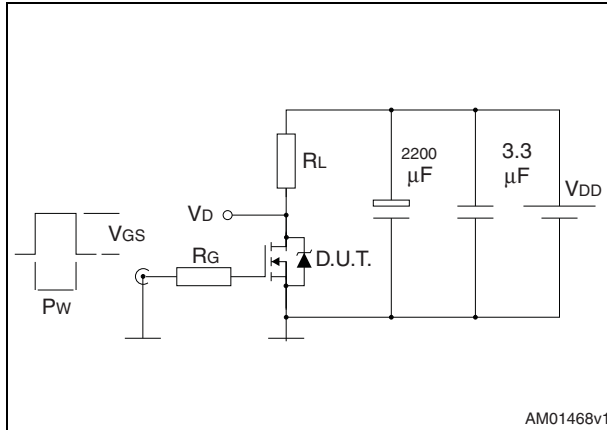


Figure 25. Gate charge test circuit

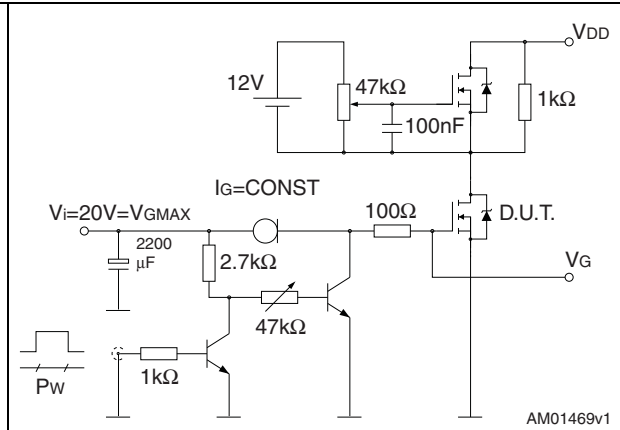


Figure 26. Test circuit for inductive load switching and diode recovery times

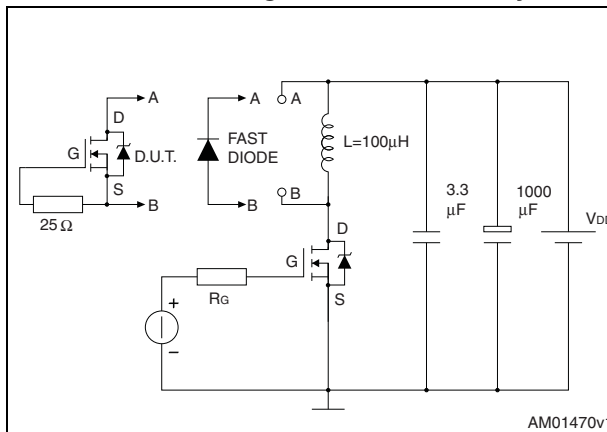


Figure 27. Unclamped inductive load test circuit

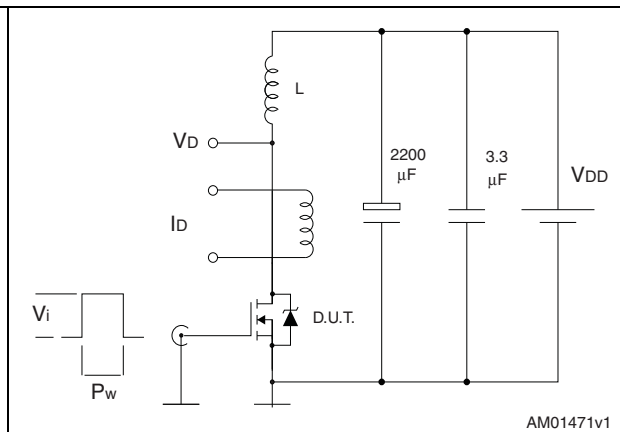


Figure 28. Unclamped inductive waveform

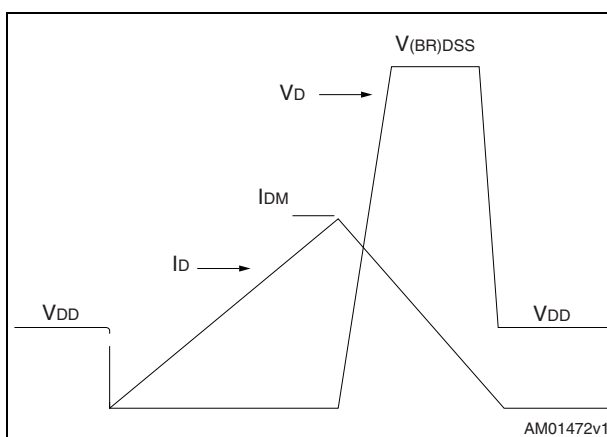
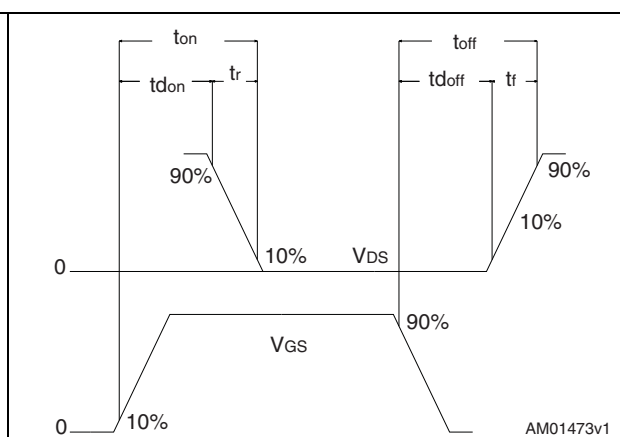


Figure 29. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 5x6 asymmetrical double island dimensions

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1			0.05
b	0.45		0.55
D	4.90	5.00	5.10
E	5.90	6.00	6.10
e		1.27	
L	0.40		0.60
aaa		0.10	
bbb		0.10	
ccc		0.10	

Technical drawing of a mechanical part, showing a cross-section with a hatched area. The drawing includes the following dimensions and features:

- Overall Dimensions:**
 - Top width: 5.1
 - Top width (inner): 3.11
 - Left height: 2.69
 - Right height: 6.1
 - Bottom width: 4.38
 - Bottom width (inner): 3.11
- Internal Features and Dimensions:**
 - Top left hole: diameter 0.57, distance from left edge 0.7.
 - Top right hole: diameter 0.92, distance from right edge 0.36.
 - Bottom left hole: diameter 0.57, distance from left edge 0.7.
 - Bottom right hole: diameter 0.36, distance from right edge 0.36.
 - Internal vertical hole: diameter 0.753, distance from left edge 0.753.
 - Internal vertical hole: diameter 0.753, distance from right edge 0.753.
 - Internal horizontal hole: diameter 0.95, distance from top edge 0.6, distance from left edge 0.3.
 - Internal horizontal hole: diameter 0.95, distance from bottom edge 1.348, distance from right edge 0.36.
 - Internal horizontal hole: diameter 0.95, distance from top edge 0.6, distance from right edge 0.36.
 - Internal horizontal hole: diameter 0.95, distance from bottom edge 1.348, distance from left edge 0.753.
- Other Features:**
 - 45° chamfer on the top left corner.
 - R0.1 fillet on the bottom left corner.

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
15-Mar-2010	1	First release
07-Feb-2011	2	Document status promoted from target specification to preliminary data.
21-Feb-2012	3	Document status promoted from preliminary data to datasheet. Section 2.1: Electrical characteristics (curves) has been added. Section 4: Package mechanical data has been updated. Minor text changes.

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