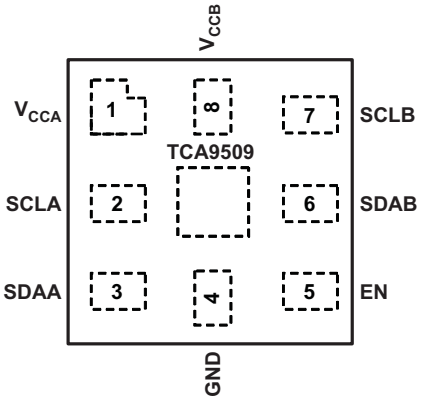
LEVEL-TRANSLATING I²C/SMBUS BUS REPEATER

Check for Samples: TCA9509

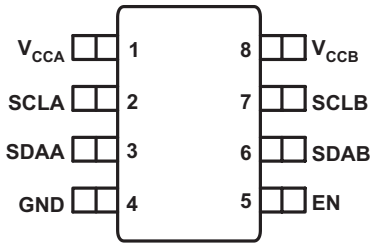
FEATURES

- **Two-Channel Bidirectional Buffer**
- **I²C Bus and SMBus Compatible**
- **Operating Supply Voltage Range of 2.7 V to 5.5 V on B side**
- **Operating Voltage Range of 0.9 V to V_{CCB} – 1V on A Side**
- **Voltage-Level Translation From 0.9 V to (V_{CCB} - 1V) and 2.7 V to 5.5 V**
- **Active-High Repeater-Enable Input**
- **Requires no external pull-up resistors on lower-voltage port-A**
- **Open-Drain I²C I/O**
- **5.5-V Tolerant I²C and Enable Input Support Mixed-Mode Signal Operation**
- **Lockup-Free Operation**
- **Accommodates Standard Mode and Fast Mode I²C Devices and Multiple Masters**
- **Supports Arbitration and Clock Stretching Across Repeater**
- **Powered-Off High-Impedance I²C bus pins**
- **Supports 400-kHz Fast I²C Bus operating speeds**
- **Available in**
  - **1.6mm x 1.6mm, 0.4mm height, 0.5mm pitch QFN pkg**
  - **3mm x 3mm industry standard MSOP pkg**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **1000-V Charged-Device Model (C101)**

RVH PACKAGE
(TOP VIEW)



DGK PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This TCA9509 integrated circuit is an I²C bus/SMBus Repeater for use in I²C/SMBus systems. It can also provide bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.5 V) in mixed-mode applications. This device enables I²C and similar bus systems to be extended, without degradation of performance even during level shifting.

The TCA9509 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I²C bus, thus allowing 400-pF bus capacitance on the B-side. This device can also be used to isolate two halves of a bus for voltage and capacitance.

The TCA9509 has two types of drivers – A-side drivers and B-side drivers. All inputs and B-side I/O's are overvoltage tolerant to 5.5V. The A-side I/O's are overvoltage tolerant to 5.5V when the device is unpowered (VCCB and/or VCCA=0V).

ORDERING INFORMATION

T_A	ORDERABLE PART NUMBERS	PACKAGES(1) (2)		TOP-SIDE MARKING
–40°C to 85°C	TCA9509RVHR	RVH - QFN	Tape and reel	7K
–40°C to 85°C	TCA9509DGKR	DGK - MSOP	Tape and reel	7KQ

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The bus port B drivers are compliant with SMBus I/O levels, while the A side uses a current sensing mechanism to detect the input or output LOW signal which prevents bus lock-up. The A side uses a 1 mA current source for pull-up and a 200 Ω pull-down driver. This results in a LOW on the A side accommodating smaller voltage swings. The output pull-down on the A side internal buffer LOW is set for approximately 0.2 V, while the input threshold of the internal buffer is set about 50 mV lower than that of the output voltage LOW. When the A side I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the B side drives a hard LOW and the input level is set at 0.3 of SMBus or I^2C-bus voltage level which enables B side to connect to any other I^2C-bus devices or buffer.

The TCA9509 drivers are not enabled unless V_{CCA} is above 0.8 V and V_{CCB} is above 2.5 V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.
an

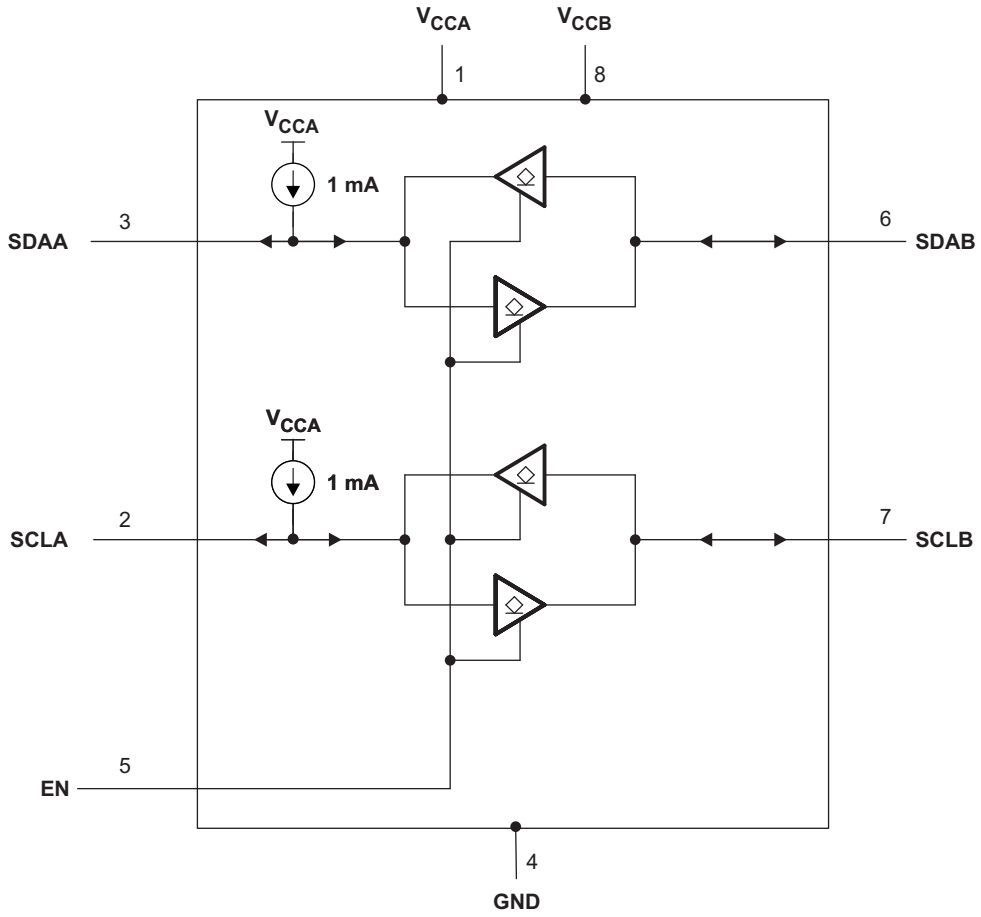
TERMINAL FUNCTIONS

NO.	NAME	DESCRIPTION
1	V_{CCA}	A-side supply voltage (0.9V to V_{CCB} - 1V)
2	SCLA	Serial clock bus, A side.
3	SDAA	Serial data bus, A side.
4	GND	Supply ground
5	EN	Active-high repeater enable input
6	SDAB	Serial data bus, B side. Connect to V_{CCB} through a pullup resistor.
7	SCLB	Serial clock bus, B side. Connect to V_{CCB} through a pullup resistor.
8	V_{CCB}	B-side and device supply voltage (2.7 V to 5.5 V)

Table 1. FUNCTION TABLE

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

Figure 1. FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage range		–0.5	6	V
V_{CCA}	Supply voltage range		–0.5	6	V
V_I	Enable input voltage range(2)		–0.5	6	V
$V_{I/O}$	I^2C bus voltage range(2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	
P_d	Max power dissipation			100	mW
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

THERMAL IMPEDANCE

over operating free-air temperature range (unless otherwise noted)

				UNIT
θ_{JA}	Package thermal impedance(1)	RVH package	208.99	°C/W
		DGK package	222.9	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CCA}	Supply voltage, A-side bus		0.9(1)	V_{CCB} - 1	V
V_{CCB}	Supply voltage, B-side bus		2.7	5.5	V
V_{IH}	High-level input voltage	SDAA, SCLA	0.7 × V_{CCA}	V_{CCA}	V
		SDAB, SCLB	0.7 × V_{CCB}	5.5	
		EN	0.7 × V_{CCA}	5.5	
V_{IL}	Low-level input voltage	SDAA, SCLA	–0.5	0.3	V
		SDAB, SCLB	–0.5	0.3 × V_{CCB}	
		EN	–0.5	0.3 × V_{CCA}	
I_{OL}	Low-level output current	SDAA, SCLA		10	µA
		SDAB, SCLB		6	mA
T_A	Operating free-air temperature		–40	85	°C

(1) Low-level supply voltage

ELECTRICAL CHARACTERISTICS

V_{CCB} = 2.7 V to 5.5 V, V_{CCA} = 0.9 V to (V_{CCB}-1), T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA	–1.5		–0.5	V
V_{OL}	Low-level output voltage	SDAA, SCLA	I_{OL} = 10 µA, V_{ILA} = V_{ILB} = 0 V, V_{CCA} = 0.9 to 1.2V		0.18	0.25	V
		SDAA, SCLA	I_{OL} = 20 µA, V_{ILA} = V_{ILB} = 0 V, 1.2V < V_{CCA} <= (V_{CCB} - 1V)		0.2	0.3	
$V_{OL} – V_{ILc}$	Low-level input voltage below low-level output voltage	SDAA, SCLA			50		mV
V_{ILc}	SDA and SCL low-level input voltage contention	SDAA, SCLA		–0.5	0.15		V
V_{OLB}	Low-level output voltage	SDAB, SCLB	I_{OL} = 6 mA		0.1	0.2	V
I_{CC}	Quiescent supply current for V_{CCA}		All port A Static high	0.25	0.45	0.9	mA
			All port A Static low	1.25	3	5	
I_{CC}	Quiescent supply current for V_{CCB}		All port B Static high	0.5	0.9	1.1	mA
I_I	Input leakage current	SDAB, SCLB	V_I = V_{CCB}			±1	µA
			V_I = 0.2 V			10	
		SDAA, SCLA	V_I = V_{CCA}			±1	
			V_I = 0.2 V			10	
		EN	V_I = V_{CCB}			±1	
			V_I = 0.2 V			–10	
I_{OH}	High-level output leakage current	SDAB, SCLB	V_O = 3.6 V			10	µA
		SDAA, SCLA				10	
C_{IOA}	I/O capacitance of A-side	SCLA, SDAA	V_I = 0 V	6	6.5	7	pF
C_{IOB}	I/O capacitance of B-side	SCLB, SDAB	V_I = 0 V	5.5	6	6.2	pF

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
t_{su}	Setup time, EN high before Start condition(1)	100		ns
t_h	Hold time, EN high after Stop condition(1)	100		ns

(1) EN should change state only when the global bus and the repeater port are in an idle state.

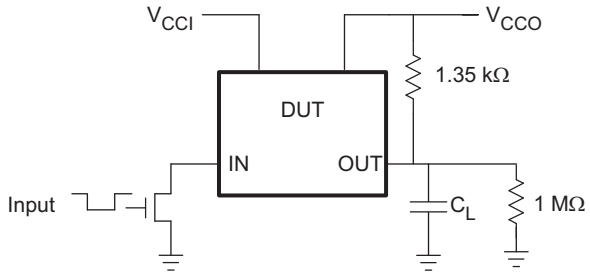
I²C INTERFACE TIMING REQUIREMENTS

T_A = –40°C to 85°C (unless otherwise noted)

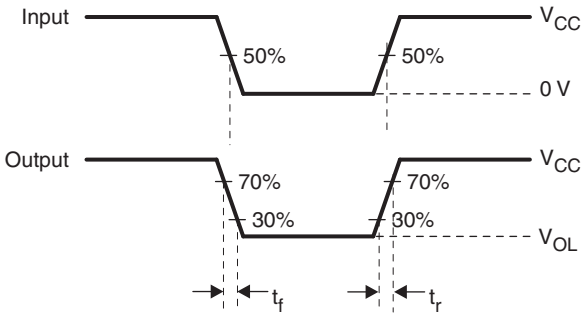
PARAMETER			V_{CCA} (INPUT)	V_{CCB} (OUTPUT)	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PHL}	Propagation delay	port A to port B	1.9 V	5.0 V	EN High	123.1	127.2	132.8	ns
		port B to port A				88.1	88.8	89.8	
t_{PLH}	Propagation delay	port A to port B	1.9 V	5.0 V	EN High	122.6	125.7	131.7	ns
		port B to port A				123.0	124.1	126.9	
t_{rise}	Transition time	port A	1.9 V	5.0 V	EN High	40.1	40.9	41.9	ns
		port B				57.3	57.5	58.4	
t_{fall}	Transition time	port A	1.9 V	5.0 V	EN High	14.5	16.4	17.9	ns
		port B				18.7	19.4	20.2	
t_{PLH2}	Propagation delay 50% of initial low on Port A to 1.5 V on Port B	port A to port B	1.9 V	5.0 V		176.0	177.3	178.0	ns
f_{MAX}	Maximum switching frequency					400			KHz

(1) Typical values were measured with V_{CCA} = V_{CCB} = 2.7 V at T_A = 25°C, unless otherwise noted.

PARAMETER MEASUREMENT INFORMATION



PIN	C_L
SCLA, SDAA (A side)	50 pF
SDAB, SCLB (B side)	50 pF



A. R_T termination resistance should be equal to Z_{OUT} of pulse generators.

B. C_L includes probe and jig capacitance.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

A typical application is shown in Figure 3. In this example, the system master is running on a 1.1-V I^2C bus, and the slave is connected to a 3.3-V bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

The TCA9509 is 5-V tolerant, so it does not require any additional circuitry to translate between 0.9-V to 5.5-V bus voltages and 2.7-V to 5.5-V bus voltages.

When the B side of the TCA9509 is pulled low by a driver on the I^2C bus and the falling edge goes below 0.3 V_{CCB}, it causes the internal driver on the A side to turn on, causing the A side to pull down to about 0.2 V. When the A side of the TCA9509 falls, first a comparator detects the falling edge and causes the internal driver on the B side to turn on and pull the B-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 4 and Figure 5. If the bus master in Figure 3 were to write to the slave through the TCA9509, waveforms shown in Figure 4 would be observed on the B bus. This looks like a normal I^2C bus transmission, except that the high level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the A-side bus of the TCA9509, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the TCA9509. After the eighth clock pulse, the data line is pulled to the V_{OL} of the master device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the TCA9509 for a short delay, while the B-bus side rises above 0.3 V_{CCB} and then continues high. It is important to note that any arbitration or clock stretching events require that the low level on the A-bus side at the input of the TCA9509 (V_{IL}) be at or below 0.15 V to be recognized by the TCA9509 and then transmitted to the B-bus side.

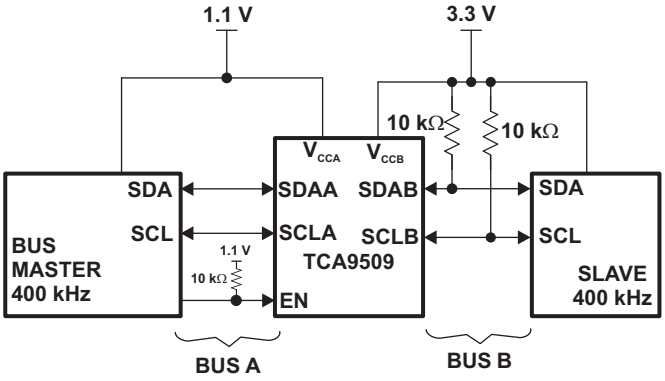


Figure 3. Typical Application

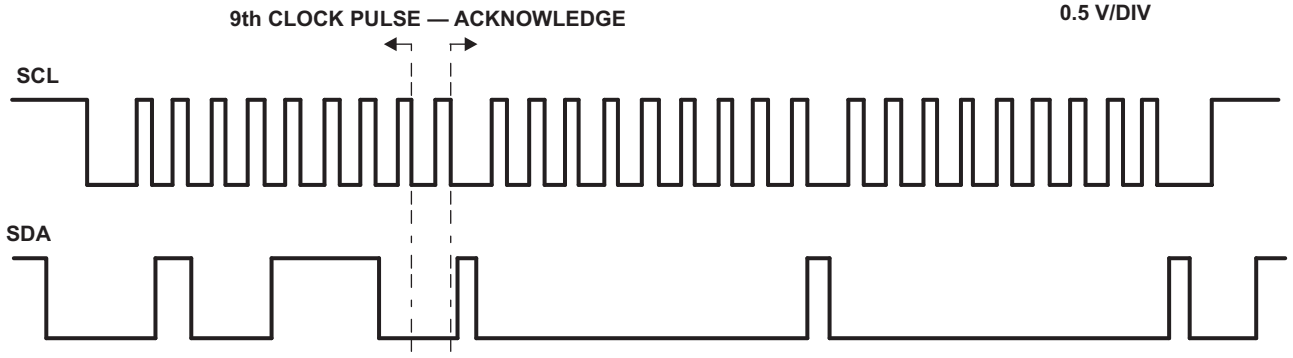


Figure 4. Bus A (0.9-V to 5.5-V Bus) Waveform

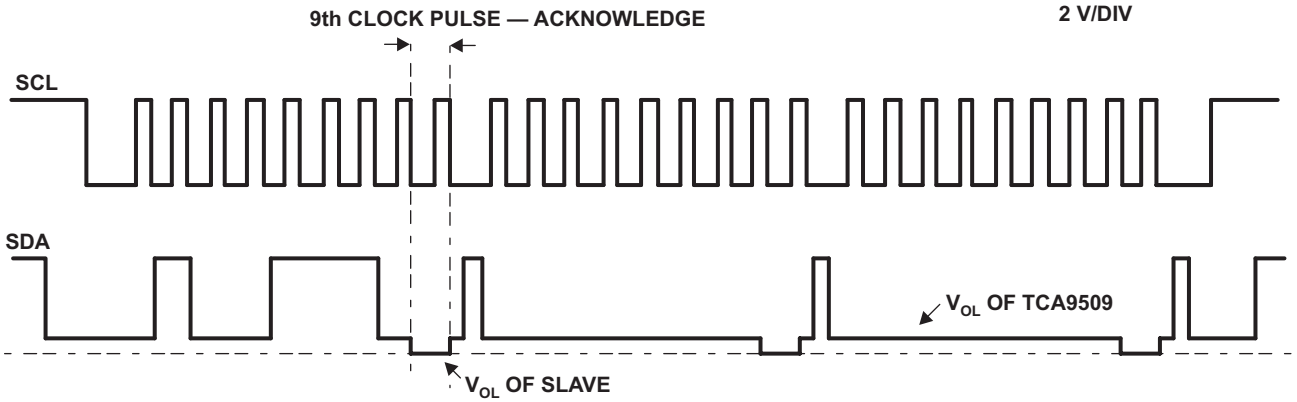


Figure 5. Bus B (2.7-V to 5.5-V Bus) Waveform

REVISION HISTORY

Changes from Original (August 2011) to Revision A **Page**

- Corrected V_{CCA} operating voltage lower limit, to 0.9V at multiple instances in document. 1
- Changed Operating Supply Voltage Range value error in FEATURES for B side. Changed from (0.9 V to 5.5 V on B side) to (2.7 V to 5.5 V on B side). 1
- Changed Operating Voltage Range value error in FEATURES for A side. Changed (2.7 V to V_{CCB} – 1 V on A side) to (0.9 V to V_{CCB} – 1 V on A side). 1

Changes from Revision A (October 2011) to Revision B **Page**

- Added DGK package and package information to datasheet. 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9509DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	7KQ	Samples
TCA9509RVHR	ACTIVE	X2QFN	RVH	8	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7K	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

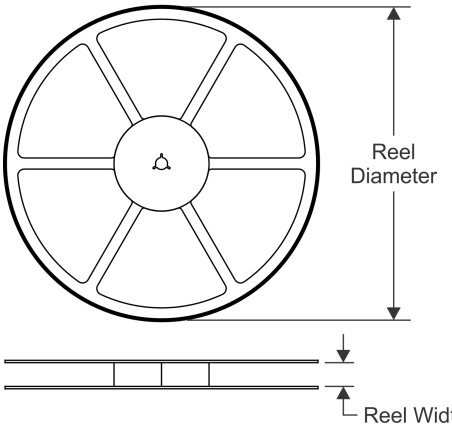
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

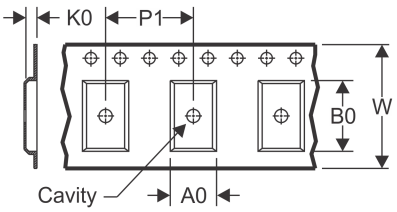
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

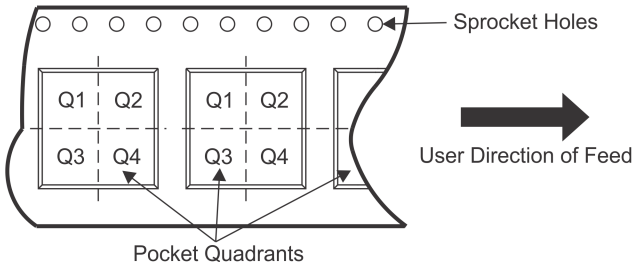


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

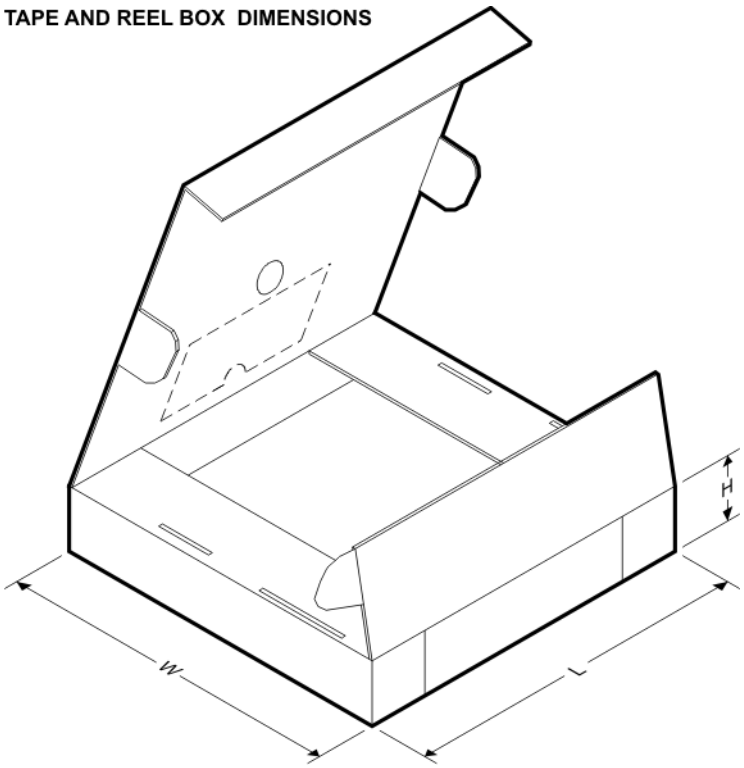
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9509DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TCA9509RVHR	X2QFN	RVH	8	5000	180.0	8.4	1.8	1.8	0.5	4.0	8.0	Q3

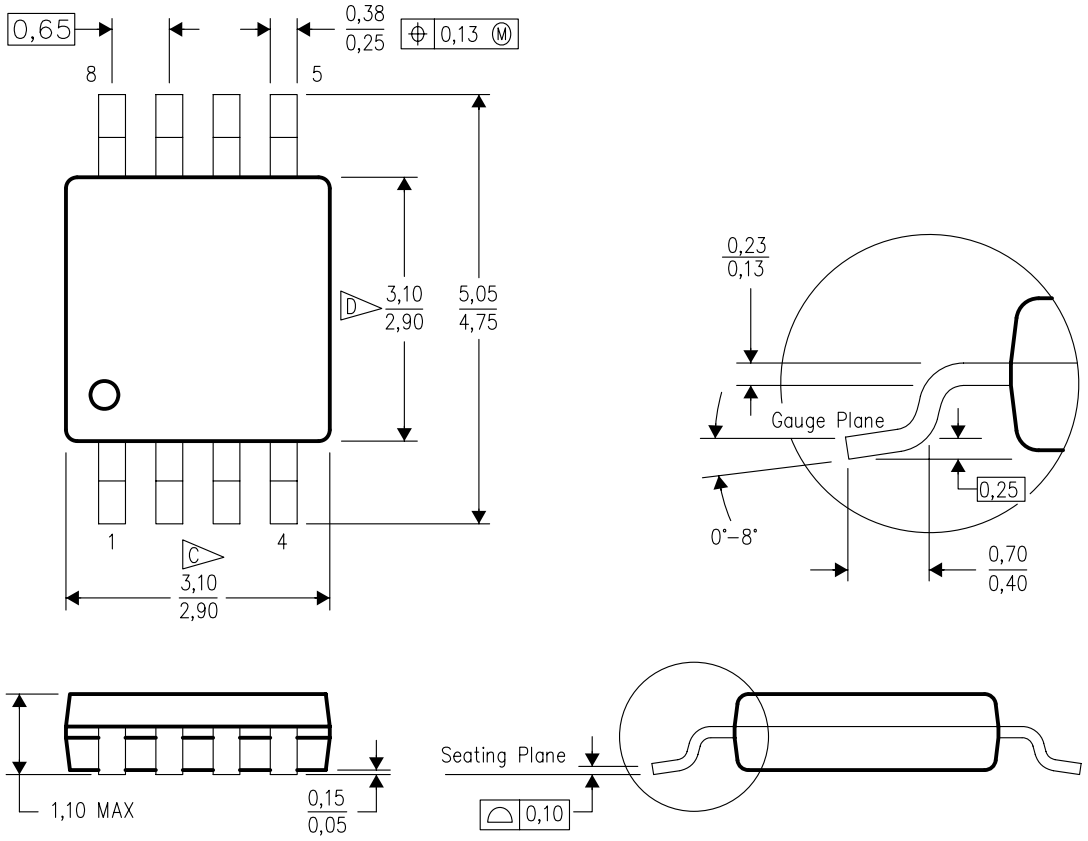
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9509DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TCA9509RVHR	X2QFN	RVH	8	5000	202.0	201.0	28.0

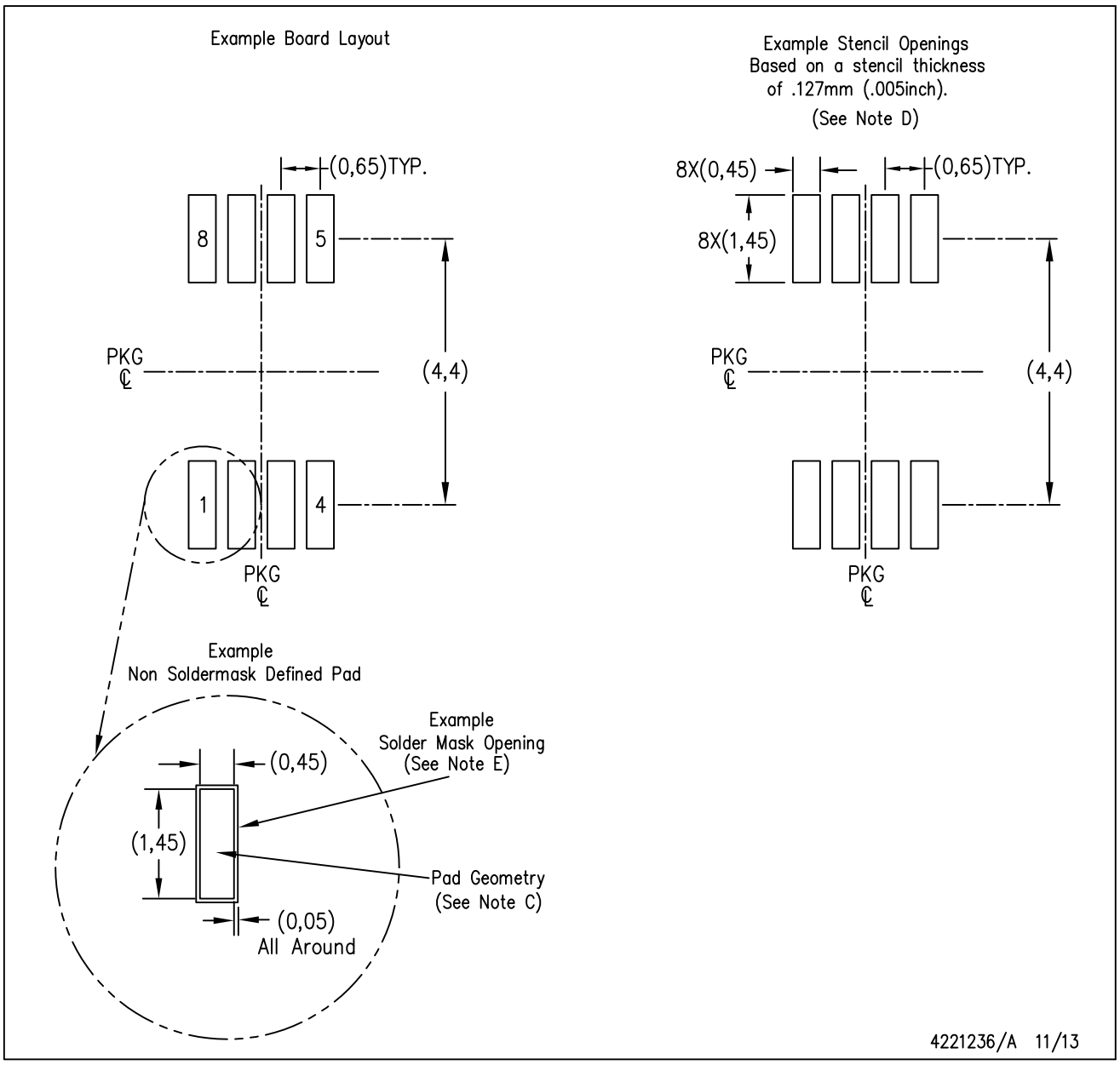
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

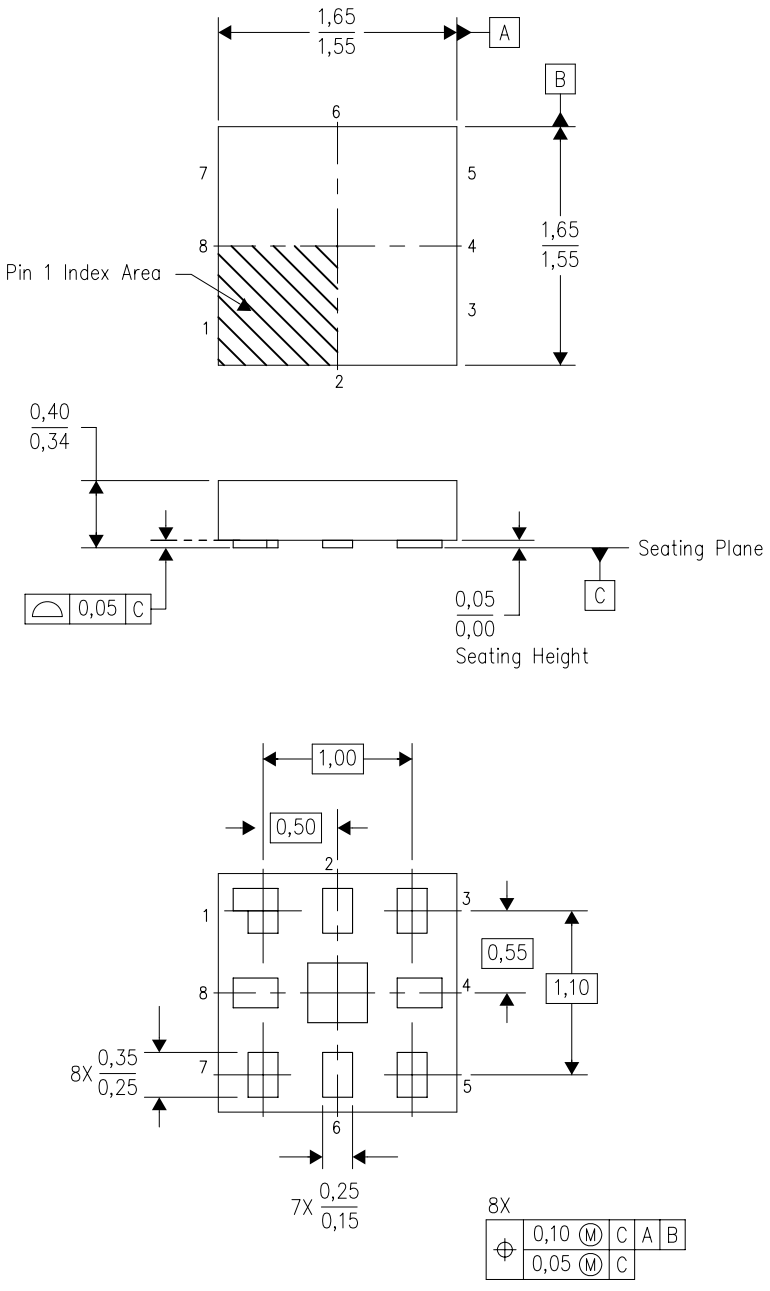
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RVH (S–PX2QFN–N8) PLASTIC QUAD FLATPACK NO–LEAD



4211402/B 01/11

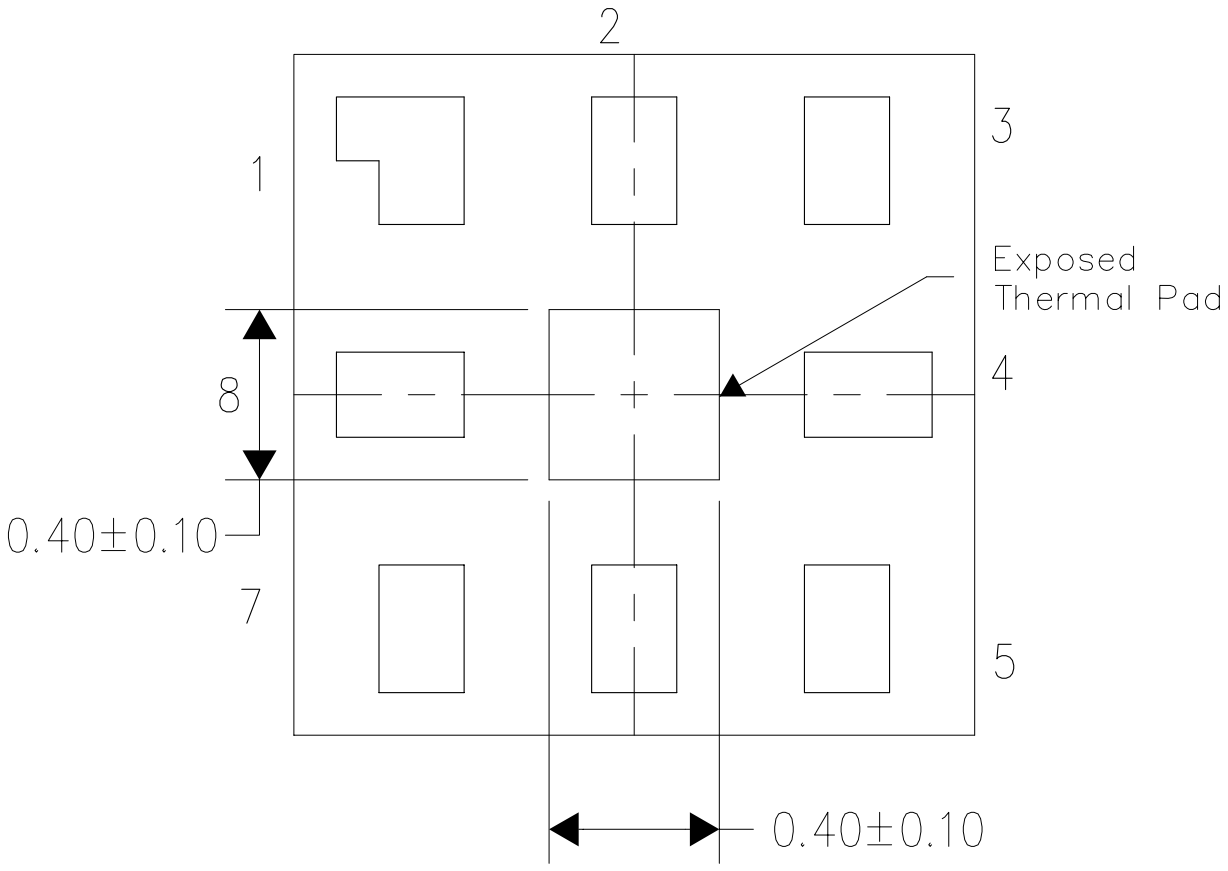
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–255.

RVH (S–PX2SON–N8) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

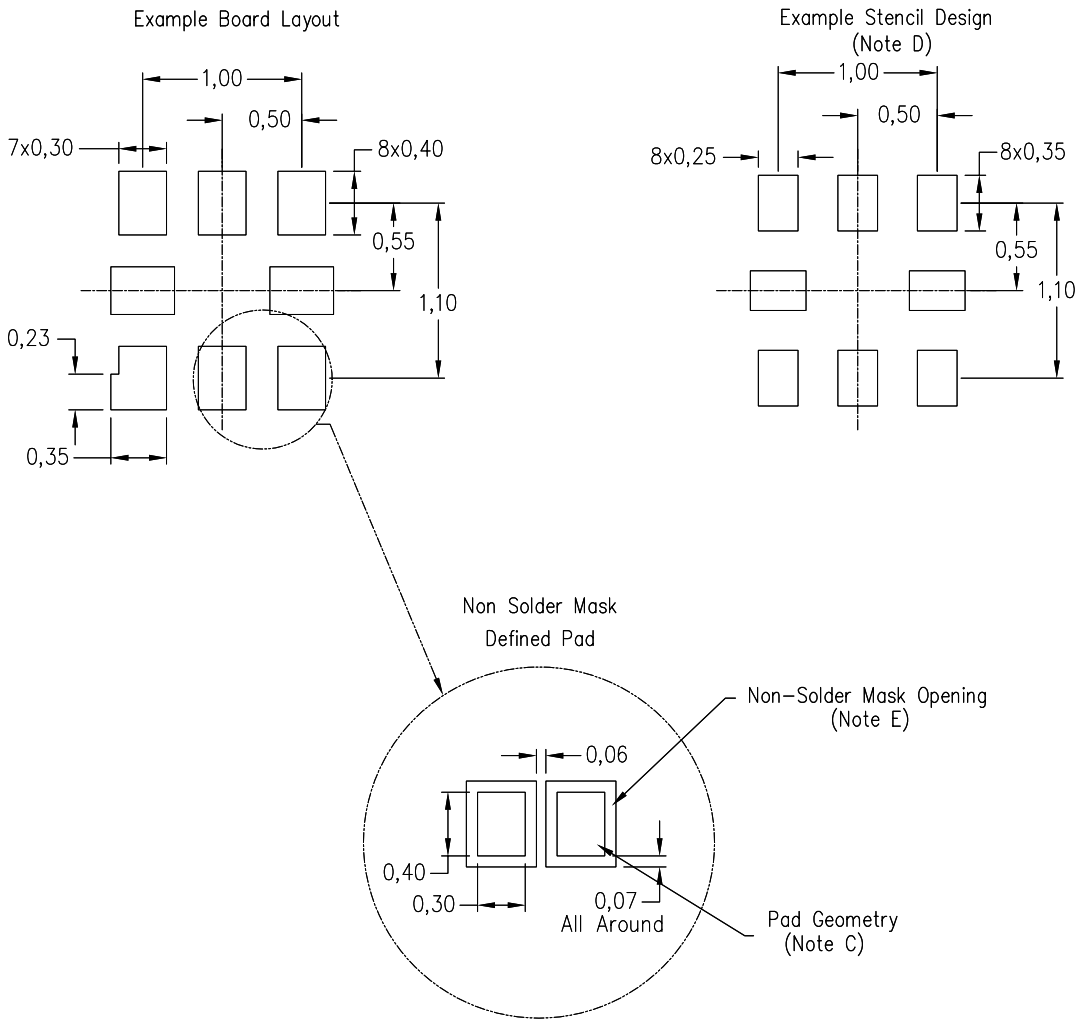
Exposed Thermal Pad Dimensions

4212275/B 12/11

NOTES:

A. All linear dimensions are in millimeters

RVH (S–PX2QFN–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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