Data Sheet | March 7, 2008 | FN9257.2

8V to 14V, Single-Phase Synchronous Buck Pulse-Width Modulation (PWM) Controller With Integrated Gate Drivers

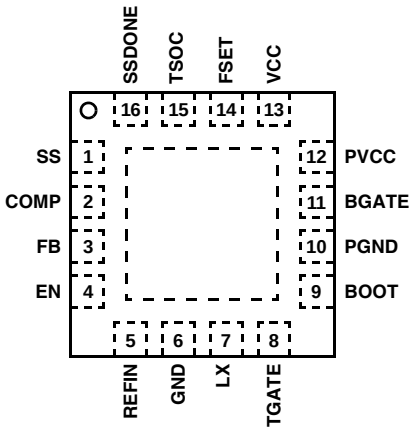
The ISL8104 is a 8V to 14V synchronous PWM controller with integrated MOSFET drivers. The controller features the ability to safely start-up into prebiased output loads and provides protection against overcurrent fault events. Overcurrent protection is implemented using top-side MOSFET $r_{DS(ON)}$ sensing, eliminating the need for a current sensing resistor.

The ISL8104 employs voltage-mode control with dual-edge modulation to achieve fast transient response. The operating frequency is adjustable from 50kHz to 1.5MHz with full (0% to 100%) PWM duty cycle capability. The error amplifier features a 15MHz (typ) gain-bandwidth product and 6V/µs slew rate enabling high converter bandwidth.

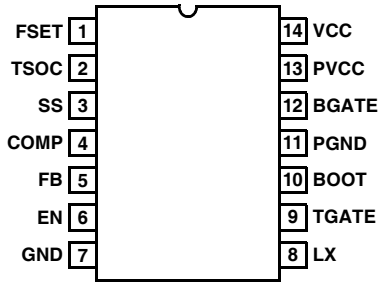
The output voltage of the converter can be regulated to as low as 0.597V with a tolerance of ±1.0% over the commercial temperature range (0°C to +70°C), and ±1.5% over industrial temperature range (-40°C to +85°C). Provided in the QFN package, a SS pin and REFIN pin enable supply sequencing and voltage tracking functionality.

Pinouts

ISL8104 (16 LD QFN)
TOP VIEW



ISL8104 (14 LD SOIC)
TOP VIEW



Features

- +8V ±5% to +14V ±10% Bias Voltage Range
  - 1.5V to 15.4V Input Voltage Range
- 0.597V Internal Reference Voltage
  - ±1.0% Over the Commercial Temperature Range
  - ±1.5% Over the Industrial Temperature Range
- Voltage-Mode PWM Control with Dual-Edge Modulation
- 14V High Speed N-Channel MOSFET Gate Drivers
  - 2.0A Source/3A Sink at 14V Bottom-Side Gate Drive
  - 1.25A Source/2A Sink at 14V Top-Side Gate Drive
- Fast Transient Response
  - 15MHz (typ) Gain-Bandwidth Error Amplifier with 6V/µs slew rate
  - Full 0% to 100% Duty Cycle Support
- Programmable Operating Frequency from 50kHz to 1.5MHz
- Lossless Programmable Overcurrent Protection
  - Top-Side MOSFET's $r_{DS(ON)}$ Sensing
  - ~120ns Blanking Time
- Sourcing and Sinking Current Capability
- Support for Start-Up into Prebiased Loads
- Soft-Start Done and an External Reference Pin for Tracking Applications are Available in the QFN Package
- Pb-free available (RoHS compliant)

Applications

- Test and Measurement Instruments
- Distributed DC/DC Power Architecture
- Industrial Applications
- Telecom/Datacom Applications

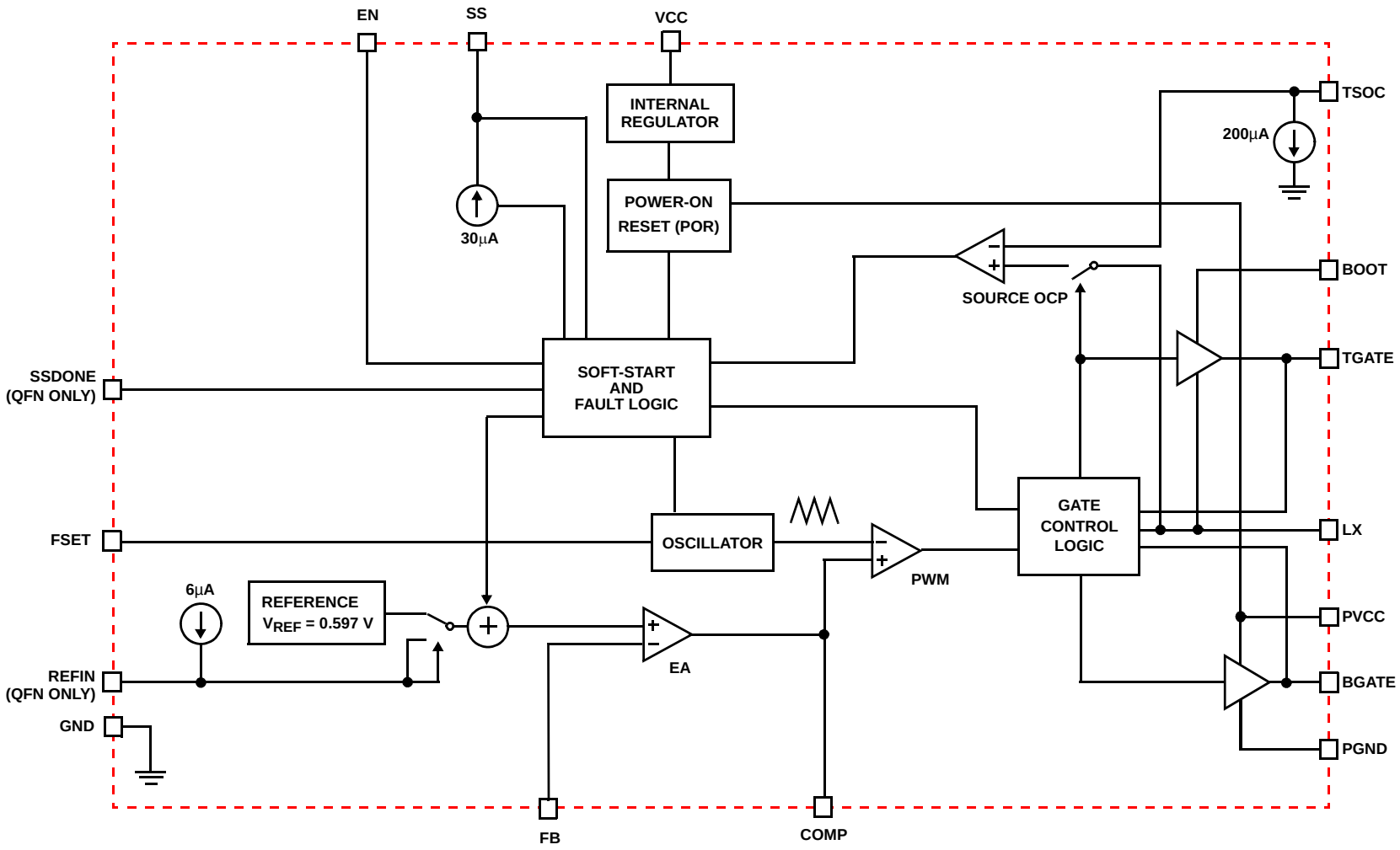
Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL8104CBZ*	8104CBZ	0 to +70	14 Ld SOIC	M14.15
ISL8104IBZ*	8104IBZ	-40 to +85	14 Ld SOIC	M14.15
ISL8104CRZ*	81 04CRZ	0 to +70	16 Ld 4x4 QFN	L16.4x4
ISL8104IRZ*	81 04IRZ	-40 to +85	16 Ld 4x4 QFN	L16.4x4
ISL8104EVAL1Z	Evaluation Board			
ISL8104EVAL2Z	Evaluation Board			

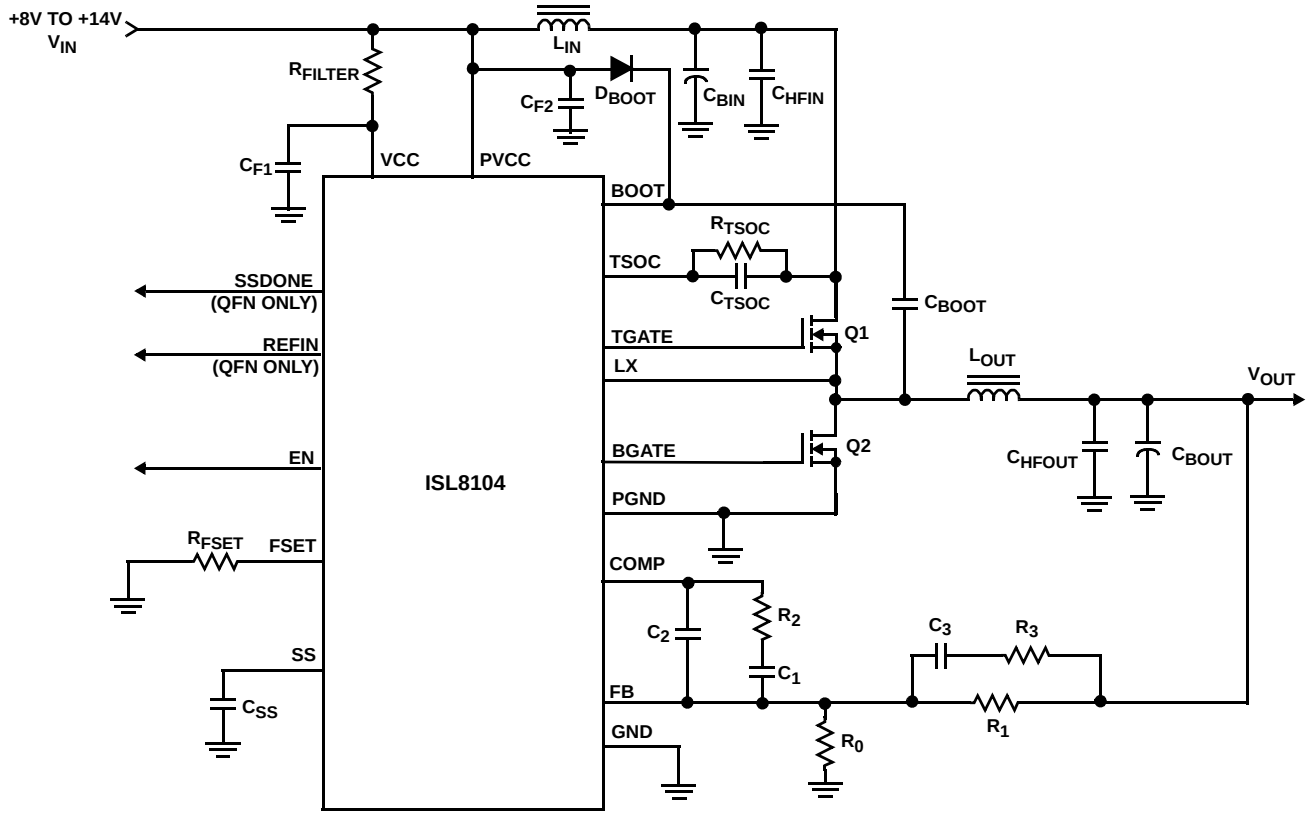
*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

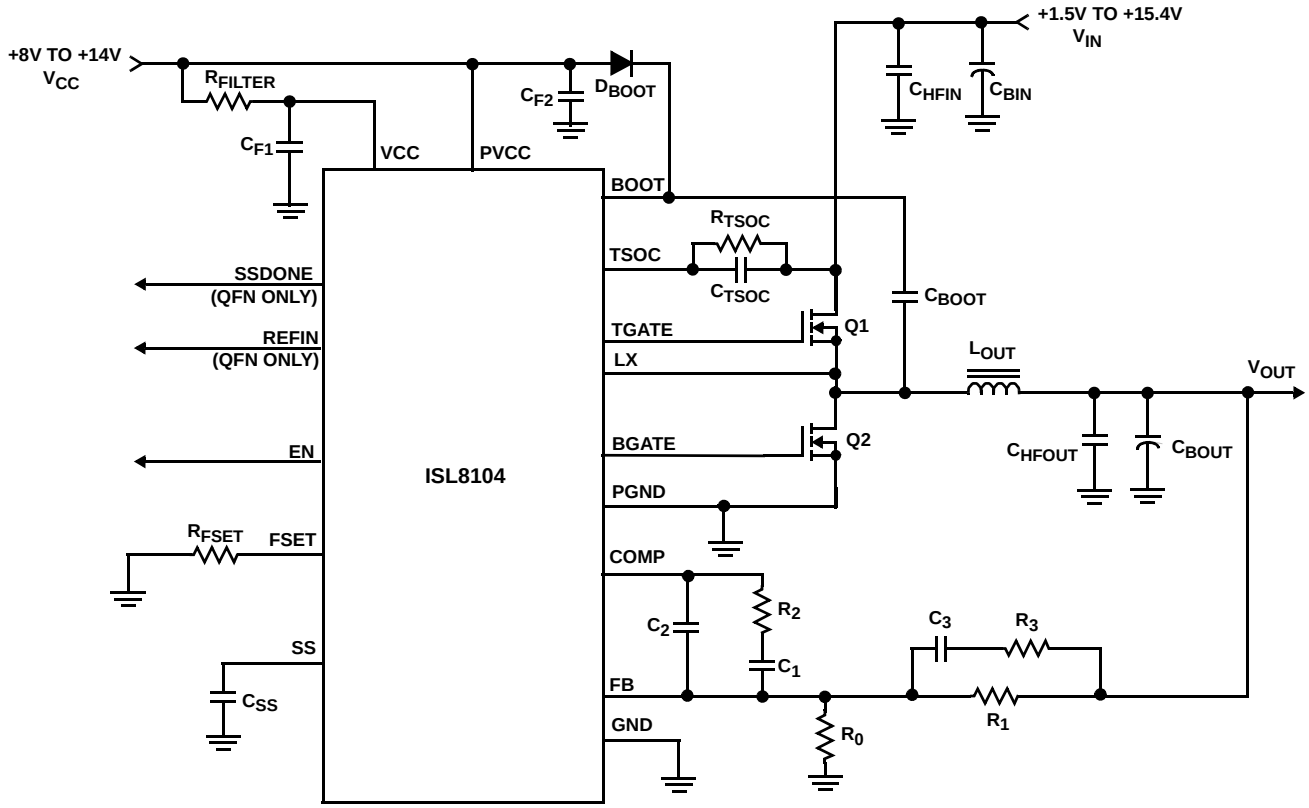
Block Diagram



Typical Application with Single Power Supply



Typical Application with Separated Power Supplies



Absolute Maximum Ratings

Supply Voltage, V_{PVCC}, V_{VCC} . . . . . GND - 0.3V to +16V
Enable Voltage, V_{EN} . . . . . GND - 0.3V to +16V
Soft-start Done Voltage, V_{SSDONE} . . . . . GND - 0.3V to +16V
TSOC Voltage, V_{TSOC} . . . . . GND - 0.3V to +16V
BOOT Voltage, V_{BOOT} . . . . . GND - 0.3V to +36V
LX Voltage, V_{LX} . . . . . V_{BOOT} - 16V to V_{BOOT} + 0.3V
All Other Pins . . . . . GND - 0.3V to 5.0V
ESD Rating
ESD Classification . . . . . Class 2

Operating Conditions

Supply Voltage, V_{VCC} . . . . . +8V ±5% to +14V ±10%
Supply Voltage, V_{PVCC} . . . . . +8V ±5% to +14V ±10%
Boot to Phase Voltage, V_{BOOT} - V_{LX} . . . . . <V_{PVCC}
Ambient Temperature Range, ISL8104C . . . . . 0°C to +70°C
Ambient Temperature Range, ISL8104I . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	95	N/A
QFN Package (Notes 2, 3)	47	8.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
4. Limits should be considered typical and are not production tested.

Electrical Specifications

Recommended Operating Conditions, unless otherwise noted, specifications in **bold** are valid for process, temperature, and line operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} SUPPLY CURRENT						
Shutdown Supply V_{CC}	I_{VCC}	SS/EN = 0V	3.5	6.1	8.5	mA
Shutdown Supply V_{PVCC}	I_{PVCC}	SS/EN = 0V	0.30	0.5	0.75	mA
POWER-ON RESET						
V_{CC}/V_{PVCC} Rising Threshold			6.45	7.10	7.55	V
V_{CC}/V_{PVCC} Hysteresis			170	250	500	mV
TSOC Rising Threshold			0.70	0.73	0.75	V
TSOC Hysteresis			180	200	220	mV
Enable - Rising Threshold			1.4	1.5	1.60	V
Enable - Hysteresis			175	250	325	mV
REFERENCE						
Reference Voltage		T_J = 0°C to +70°C	0.591	0.597	0.603	V
		T_J = -40°C to +85°C	0.588	0.597	0.606	V
System Accuracy		T_J = 0°C to +70°C	-1.0	-	1.0	%
		T_J = -40°C to +85°C	-1.5	-	1.5	%
REFIN Current Source (QFN Only)			-4	-6	-8	µA
REFIN Threshold (QFN Only)			2.10	-	3.50	V
REFIN Offset (QFN Only)			-3	-	3	mV

Electrical Specifications Recommended Operating Conditions, unless otherwise noted, specifications in **bold** are valid for process, temperature, and line operating conditions. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
Trim Test Frequency		R_{FSET} = OPEN V_{VCC} = 12	175	200	220	kHz
Total Variation (Note 4)		8kΩ < R_{FSET} to GND < 200kΩ	-	±15	-	%
Ramp Amplitude	ΔV_{OSC}	R_{FSET} = OPEN	1.7	1.9	2.15	V_{P-P}
Ramp Bottom (Note 4)			-	1	-	V
ERROR AMPLIFIER						
DC Gain (Note 4)		R_L = 10kΩ, C_L= 100pF	-	88	-	dB
Gain-Bandwidth Product (Note 4)	GBWP	R_L = 10kΩ, C_L= 100pF	-	15	-	MHz
Slew Rate (Note 4)	SR	R_L = 10kΩ, C_L= 100pF	-	6	-	V/µs
COMP Source Current (Note 4)	$I_{COMPSRC}$		-	2	-	mA
COMP Sink Current (Note 4)	$I_{COMPSNK}$		-	2	-	mA
GATE DRIVERS						
Top-side Drive Source Current (Note 4)	I_{T_SOURCE}	V_{BOOT} - V_{LX} = 14V, 3nF Load	-	1.25	-	A
Top-side Drive Source Impedance	R_{T_SOURCE}	90mA Source Current	-	2.0	-	Ω
Top-side Drive Sink Current (Note 4)	I_{T_SINK}	V_{BOOT} - V_{LX} = 14V, 3nF Load	-	2	-	A
Top-side Drive Sink Impedance	R_{T_SINK}	90mA Source Current	-	1.3	-	Ω
Bottom-side Drive Source Current (Note 4)	I_{B_SOURCE}	V_{PVCC} = 14V, 3nF Load	-	2	-	A
Bottom-side Drive Source Impedance	R_{B_SOURCE}	90mA Source Current	-	1.3	-	Ω
Bottom-side Drive Sink Current (Note 4)	I_{B_SINK}	V_{PVCC} = 14V, 3nF Load	-	3	-	A
Bottom-side Drive Sink Impedance	R_{B_SINK}	90mA Source Current	-	0.94	-	Ω
PROTECTION						
TSOC Current	I_{TSOC}	T_J = 0°C to +70°C	180	200	220	µA
		T_J = -40°C to +85°C	176	200	224	µA
TSOC Measurement Offset (Note 4)	OCP_{OFFSET}	TSOC = 1.5V to 15.4V	-	±10	-	mV
SOFT-START						
Soft-start Current	I_{SS}		22	30	38	µA
SSDONE Low Output Voltage (QFN ONLY)		I_{SSDONE} = 2mA	-	-	0.30	V

Functional Pin Description (QFN/SOIC)

SS (Pin 1/3)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 30µA current source, sets the soft-start interval of the converter.

COMP (Pin 2/4) and FB (Pin 3/5)

COMP and FB are the available external pins of the error amplifier. The FB pin is the inverting input of the error amplifier and the COMP pin is the error amplifier output. These pins are used to compensate the voltage-control feedback loop of the converter.

EN (Pin 4/6)

This pin is a TTL compatible input. Pull this pin below 0.8V to disable the converter. In shutdown the soft-start pin is discharged and the TGATE and BGATE pins are held low.

REFIN (QFN ONLY Pin 5)

Upon enable if REFIN is less than 2.2V, the external reference pin is used as the control reference instead of the internal 0.597V reference. An internal 6µA pull-up to 5V is provided for disabling this functionality.

GND (Pin 6/7)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

LX (Pin 7/8)

This pin connects to the source of the top-side MOSFET and the drain of the bottom-side MOSFET. This pin represents the return path for the top-side gate driver. During normal switching, this pin is used for top-side current sensing.

TGATE (Pin 8/9)

Connect TGATE to the top-side MOSFET gate. This pin provides the gate drive for the top-side MOSFET.

BOOT (Pin 9/10)

This pin provides bias to the top-side MOSFET driver. A bootstrap circuit may be used to create a BOOT voltage suitable to drive a standard N-Channel MOSFET.

PGND (Pin 10/11)

This is the power ground connection. Tie the bottom-side MOSFET source and board ground to this pin.

BGATE (Pin 11/12)

Connect BGATE to the bottom-side MOSFET gate. This pin provides the gate drive for the bottom-side MOSFET.

PVCC (Pin 12/13)

Provide an 8V to 14V bias supply for the bottom-side gate drive to this pin. This pin should be bypassed with a capacitor to PGND.

VCC (Pin 13/14)

Provide an 8V to 14V bias supply for the chip to this pin. The pin should be bypassed with a capacitor to GND.

FSET (Pin 14/1)

This pin provides oscillator switching frequency adjustment. By placing a resistor (R_{FSET}) from this pin to GND, the switching frequency is set from between 200kHz and 1.5MHz according to Equation 1:

$$R_{FSET}[k\Omega] \approx \left(\frac{6500}{F_s[kHz] - 200[kHz]} - 1.3\right) k\Omega \quad (R_{FSET} \text{ to GND})$$

(EQ. 1)

Alternately ISL8104's switching frequency can be lowered from 200kHz to 50kHz by connecting the FSET pin with a resistor to VCC according Equation 2:

$$R_{FSET}[k\Omega] \approx \left(\frac{55000}{200[kHz] - F_s[kHz]} + 70\right) k\Omega \quad (R_{FSET} \text{ to VCC})$$

(EQ. 2)

TSOC (Pin 15/2)

The current limit is programmed by connecting this pin with a resistor and capacitor to the drain of the top-side MOSEFT. A 200µA current source develops a voltage across the resistor which is then compared with the voltage developed across the top-side MOSFET. A blanking period of 120ns is provided for noise immunity.

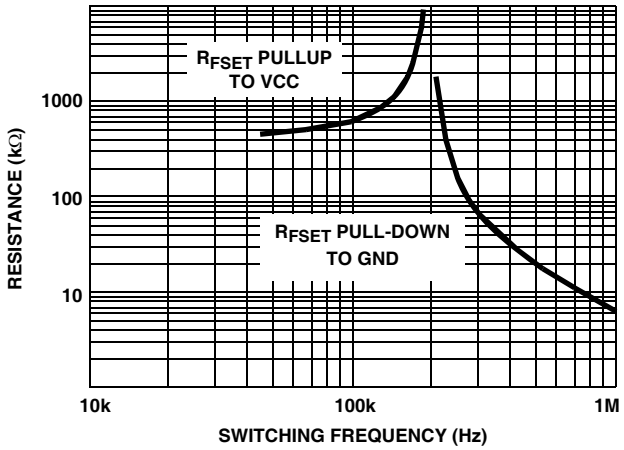


FIGURE 1. R_{FSET} RESISTANCE vs FREQUENCY

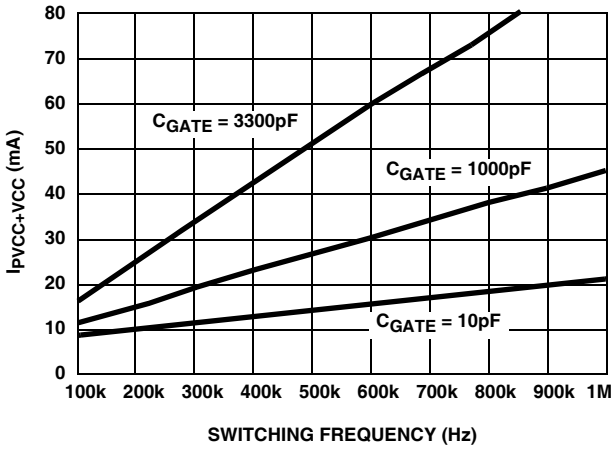


FIGURE 2. BIAS SUPPLY CURRENT vs FREQUENCY

SSDONE (QFN ONLY Pin 16)

Provides an open drain signal at the end of soft-start.

Functional Description

Initialization

The ISL8104 automatically initializes upon receipt of power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the bias voltage at the VCC pin and the driver input on the PVCC pin. When the voltages at VCC and PVCC exceed their rising POR thresholds, a 30µA current source driving the SS pin is enabled. Upon the SS pin exceeding 1V, the ISL8104 begins ramping the non-inverting input of the error amplifier from GND to the System Reference. During initialization the MOSFET drivers pull TGATE to LX and BGATE to PGND.

Soft-Start

During soft-start, an internal 30µA current source charges the external capacitor (C_{SS}) on the SS pin up to ~4V. If the ISL8104 is utilizing the internal reference, then as the SS pin's voltage ramps from 1V to 3V, the soft-start function scales the

reference input (positive terminal of error amp) from GND to VREF (0.597V nominal). If the ISL8104 is utilizing an externally supplied reference, when the voltage on the SS pin reaches 1V, the internal reference input (into the error amp) ramps from GND to the externally supplied reference at the same rate as the voltage on the SS pin. Figure 3 shows a typical soft-start interval. The rise time of the output voltage is, therefore, dependent upon the value of the soft-start capacitor, C_{SS}. If the internal reference is used, then the soft-start capacitance value can be calculated through Equation 3:

$$C_{SS} = \frac{30\mu A \cdot t_{SS}}{2V} \quad \text{(EQ. 3)}$$

If an external reference is used then the soft-start capacitance can be calculated through Equation 4:

$$C_{SS} = \frac{30\mu A \cdot t_{SS}}{V_{REFEXT}} \quad \text{(EQ. 4)}$$

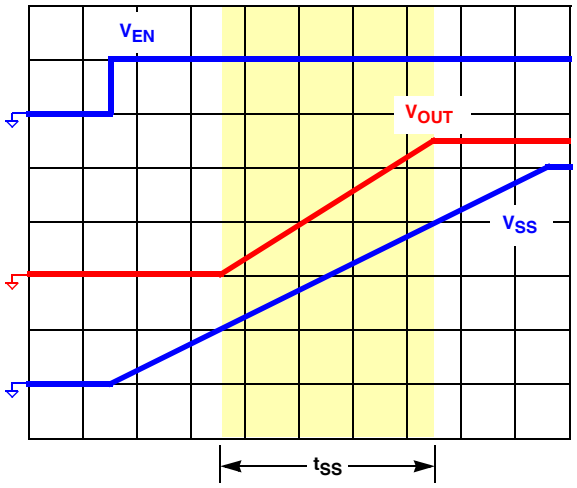


FIGURE 3. TYPICAL SOFT-START INTERVAL

Prebiased Load Start-up

Drivers are held in tri-state (TGATE pulled to LX, BGATE pulled to PGND) at the beginning of a soft-start cycle until two PWM pulses are detected. The bottom-side MOSFET is turned on first to provide for charging of the bootstrap capacitor. This method of driver activation provides support for start-up into prebiased loads by not activating the drivers until the control loop has entered its linear region, thereby substantially reducing output transients that would otherwise occur had the drivers been activated at the beginning of the soft-start cycle.

SSDONE

Soft-start done is only available in the 16 Ld QFN packaging option of the ISL8104. When the soft-start pin reaches 4V, an open drain signal is provided to support sequencing requirements. SSDONE is deasserted by disabling of the part, including pulling SS low, and by POR and OCP events.

Oscillator

The oscillator is a triangular waveform, providing for leading and falling edge modulation. The peak-to-peak of the ramp amplitude is set at 1.9V and varies as a function of frequency. At 50kHz the peak to peak amplitude is approximately 1.8V while at 1.5MHz it is approximately 2.2V. In the event the regulator operates at 100% duty cycle for 64 clock cycles an automatic boot cap refresh circuit will activate turning on BGATE for approximately 1/2 of a clock cycle.

Overcurrent Protection

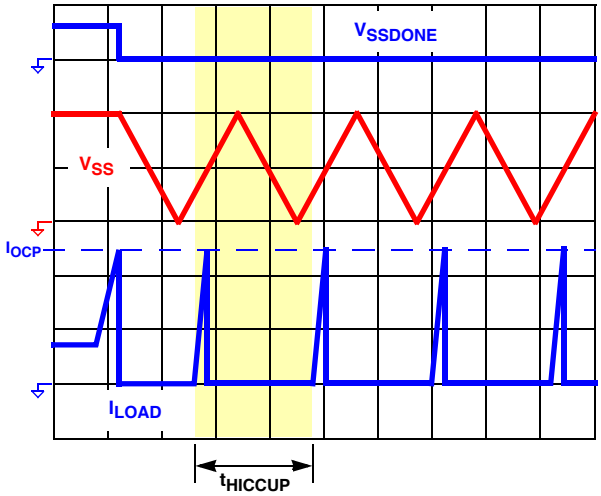


FIGURE 4. TYPICAL OVERCURRENT PROTECTION

The OCP function is enabled with the drivers at start-up. OCP is implemented via a resistor (R_{TSOC}) and a capacitor (C_{TSOC}) connecting the TSOC pin and the drain of the top-side MOSEFT. An internal 200mA current source develops a voltage across R_{TSOC}, which is then compared with the voltage developed across the top-side MOSFET at turn on as measured at the LX pin. When the voltage drop across the MOSFET exceeds the voltage drop across the resistor, a sourcing OCP event occurs. C_{TSOC} is placed in parallel with R_{TSOC} to smooth the voltage across R_{TSOC} in the presence of switching noise on the input bus.

A 120ns blanking period is used to reduce the current sampling error due to leading-edge switching noise. An additional simultaneous 120ns low pass filter is used to further reduce measurement error due to noise.

OCP faults cause the regulator to disable (top- and bottom-side drives disabled, SSDONE pulled low, soft-start capacitor discharged) itself for a fixed period of time, after which a normal soft-start sequence is initiated. If the voltage on the SS pin is already at 4V and an OCP is detected, a 30µA current sink is immediately applied to the SS pin. If an OCP is detected during soft-start, the 30µA current sink will not be applied until the voltage on the SS pin has reached 4V. This current sink discharges the C_{SS} capacitor in a linear fashion. Once the voltage on the SS pin has reached approximately 0V, the normal soft-start sequence is initiated. If the fault is still present on the subsequent restart, the ISL8104

will repeat this process in a hiccup mode. Figure 4 shows a typical reaction to a repeated overcurrent condition that places the regulator in a hiccup mode. If the regulator is repeatedly tripping overcurrent, the hiccup period can be approximated by Equation 5:

$$t_{HICCUP} = \frac{2 \cdot 4V \cdot C_{SS}}{30\mu A} \quad \text{(EQ. 5)}$$

The OCP trip point varies mainly due to MOSFET $r_{DS(ON)}$ variations and layout noise concerns. To avoid overcurrent tripping in the normal operating load range, find the R_{OCSET} resistor from the following equations with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature
2. The minimum I_{TSOC} from the specification table

Determine the overcurrent trip point greater than the maximum output continuous current at maximum inductor ripple current.

SIMPLE OCP EQUATION

$$R_{TSOC} = \frac{I_{OC\_SOURCE} \bullet r_{DS(ON)}}{200\mu A}$$

DETAILED OCP EQUATION

$$R_{TSOC} = \frac{\left(I_{OC\_SOURCE} + \frac{\Delta I}{2}\right) \bullet r_{DS(ON)}}{I_{TSOC} \bullet N_T}$$

N_T = NUMBER OF TOP-SIDE MOSFETs

$$\Delta I = \frac{V_{IN} - V_{OUT}}{f_{SW} \bullet L_{OUT}} \bullet \frac{V_{OUT}}{V_{IN}}$$

f_{SW} = Regulator Switching Frequency (EQ. 6)

High Speed MOSFET Gate Driver

The integrated driver has the same drive capability and feature as the Intersil's 12V gate driver, ISL6612. The PWM tri-state feature helps prevent a negative transient on the output voltage when the output is being shut down. This eliminates the Schottky diode that is used in some systems for protecting the loads from reversed-output-voltage damage. See the ISL6612 data sheet FN9153 for specification parameters that are not defined in the current ISL8104 "Electrical Specifications" table on page 4.

Reference Input

The REFIN pin allows the user to bypass the internal 0.597V reference with an external reference. If REFIN is NOT above ~2.2V, the external reference pin is used as the control reference instead of the internal 0.597V reference. When not using the external reference option, the REFIN pin should be left floating. An internal 6µA pull-up keeps this REFIN pin above 2.2V in this situation.

Internal Reference and System Accuracy

The Internal Reference is set to 0.597V. The total DC system accuracy of the system is to be within 1.5% over the industrial temperature range. System Accuracy includes Error Amplifier offset, and Reference Error. The use of REFIN may add up to 3mV of offset error into the system (as the Error Amplifier offset is trimmed out via the internal System reference).

Application Guidelines

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding.

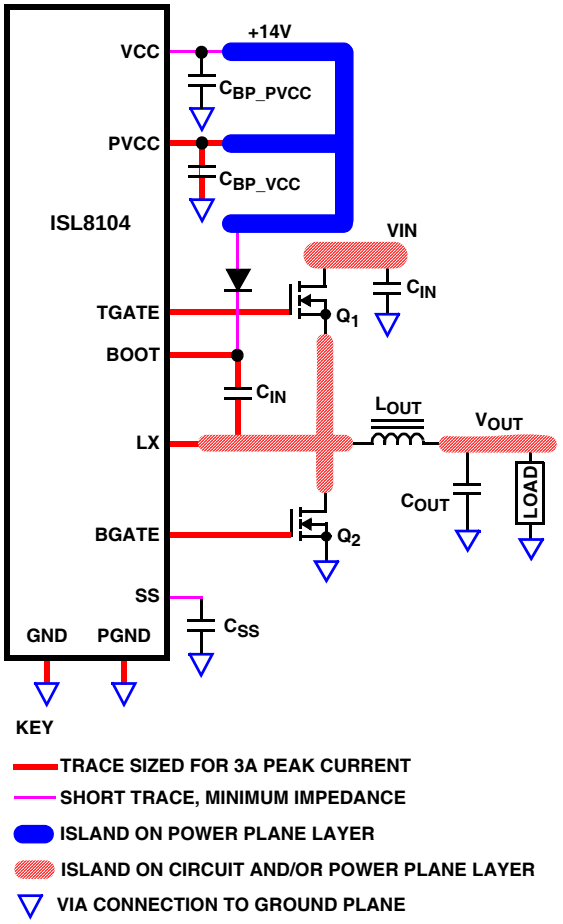


FIGURE 5. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

A multi-layer printed circuit board is recommended. Figure 5 shows the critical components of the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer (usually a middle layer of the PC board) for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the LX terminals to the output inductor short.

The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the LX nodes. Use the remaining printed circuit layers for small signal wiring.

Locate the ISL8104 within 2 to 3 inches of the MOSFETs, Q_1 and Q_2 (1 inch or less for 500kHz or higher operation). The circuit traces for the MOSFETs' gate and source connections from the ISL8104 must be sized to handle up to 3A peak current. Minimize any leakage current paths on the SS pin and locate the capacitor, C_{SS} close to the SS pin as the internal current source is only 30µA. Provide local V_{CC} decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT pin and the phase node.

Compensating the Converter

This section highlights the design consideration for a voltage mode controller requiring external compensation. To address a broad range of applications, a type-3 feedback network is recommended (see Figure 6).

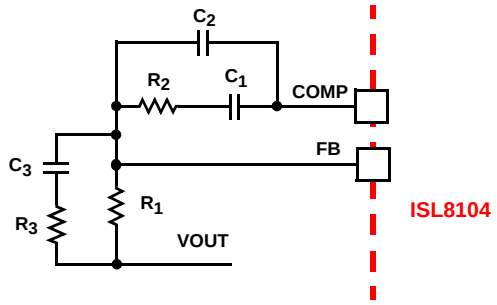


FIGURE 6. COMPENSATION CONFIGURATION FOR THE ISL8104 CIRCUIT

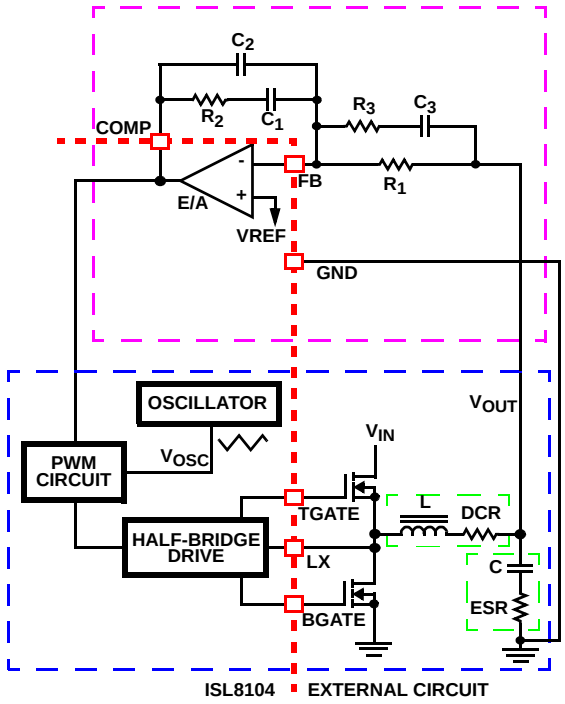


FIGURE 7. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

Figure 7 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage is regulated to the reference voltage level. The error amplifier output is compared with the oscillator triangle wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the LX node. The PWM wave is smoothed by the output filter. The output filter capacitor bank's equivalent series resistance is represented by the series resistor ESR.

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC gain and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{CE}. For the purpose of this analysis, L and DCR represent the output inductance and its DCR, while C and ESR represents the total output capacitance and its equivalent series resistance.

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \qquad F_{CE} = \frac{1}{2\pi \cdot C \cdot ESR} \qquad \text{(EQ. 7)}$$

The compensation network consists of the error amplifier (internal to the ISL8104) and the external R_1 to R_3, C_1 to C_3 components. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (F_0; typically 0.1 to 0.3 of f_{SW}) and adequate phase margin (better than 45°). Phase margin is the difference between the closed loop phase at F_{0dB} and 180°. The equations that follow relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figures 6 and 7. Use the following guidelines for locating the poles and zeros of the compensation network:

1. Select a value for R_1 (1kΩ to 10kΩ, typically). Calculate value for R_2 for desired converter bandwidth (F_0). If setting the output voltage to be equal to the reference set voltage as shown in Figure 7, the design procedure can be followed as presented in Equation 8.

$$R_2 = \frac{V_{OSC} \cdot R_1 \cdot F_0}{D_{MAX} \cdot V_{IN} \cdot F_{LC}} \qquad \text{(EQ. 8)}$$

As the ISL8104 supports 100% duty cycle, D_{MAX} equals 1. The ISL8104 uses a fixed ramp amplitude (V_{OSC}) of 1.9V, Equation 8 simplifies to Equation 9:

$$R_2 = \frac{1.9 \cdot R_1 \cdot F_0}{V_{IN} \cdot F_{LC}} \qquad \text{(EQ. 9)}$$

2. Calculate C_1 such that F_{Z1} is placed at a fraction of the F_{LC}, at 0.1 to 0.75 of F_{LC} (to adjust, change the 0.5 factor in Equation 10 to the desired number). The higher the quality factor of the output filter and/or the higher the ratio F_{CE}/F_{LC}, the lower the F_{Z1} frequency (to maximize phase boost at F_{LC}).

$$C_1 = \frac{1}{2\pi \cdot R_2 \cdot 0.5 \cdot F_{LC}} \qquad \text{(EQ. 10)}$$

3. Calculate C_2 such that F_{P1} is placed at F_{CE}.

$$C_2 = \frac{C_1}{2\pi \cdot R_2 \cdot C_1 \cdot F_{CE} - 1} \qquad \text{(EQ. 11)}$$

4. Calculate R_3 such that F_{Z2} is placed at F_{LC}. Calculate C_3 such that F_{P2} is placed below f_{SW} (typically, 0.3 to 1.0

times f_{SW}). f_{SW} represents the switching frequency of the regulator. Change the numerical factor (0.7) below to reflect desired placement of this pole. Placement of F_{P2} lower in frequency helps reduce the gain of the compensation network at high frequency, in turn reducing the HF ripple component at the COMP pin and minimizing resultant duty cycle jitter.

$$R_3 = \frac{R_1}{\frac{f_{SW}}{F_{LC}} - 1} \qquad \text{(EQ. 12)}$$

$$C_3 = \frac{1}{2\pi \cdot R_3 \cdot 0.7 \cdot f_{SW}}$$

It is recommended that a mathematical model be used to plot the loop response. Check the loop gain against the error amplifier's open-loop gain. Verify phase margin results and adjust as necessary. Equation 13 describes the frequency response of the modulator (G_{MOD}), feedback compensation (G_{FB}) and closed-loop response (G_{CL}):

$$G_{MOD}(f) = \frac{D_{MAX} \cdot V_{IN}}{V_{OSC}} \cdot \frac{1 + s(f) \cdot ESR \cdot C}{1 + s(f) \cdot (ESR + DCR) \cdot C + s^2(f) \cdot L \cdot C}$$

$$G_{FB}(f) = \frac{1 + s(f) \cdot R_2 \cdot C_1}{s(f) \cdot R_1 \cdot (C_1 + C_2)} \cdot \frac{1 + s(f) \cdot (R_1 + R_3) \cdot C_3}{(1 + s(f) \cdot R_3 \cdot C_3) \cdot \left(1 + s(f) \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)\right)}$$

$$G_{CL}(f) = G_{MOD}(f) \cdot G_{FB}(f) \qquad \text{where, } s(f) = 2\pi \cdot f \cdot j \qquad \text{(EQ. 13)}$$

COMPENSATION BREAK FREQUENCY EQUATIONS

$$F_{Z1} = \frac{1}{2\pi \cdot R_2 \cdot C_1} \qquad F_{P1} = \frac{1}{2\pi \cdot R_2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2}}$$

$$F_{Z2} = \frac{1}{2\pi \cdot (R_1 + R_3) \cdot C_3} \qquad F_{P2} = \frac{1}{2\pi \cdot R_3 \cdot C_3} \qquad \text{(EQ. 14)}$$

Figure 8 shows an asymptotic plot of the DC/DC converter's gain vs frequency. The actual Modulator Gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown. Using the previously mentioned guidelines should yield a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} against the capabilities of the error amplifier. The closed loop gain, G_{CL}, is constructed on the log-log graph of Figure 8 by adding the modulator gain, G_{MOD} (in dB), to the feedback compensation gain, G_{FB} (in dB). This is equivalent to multiplying the modulator transfer function and the compensation transfer function and then plotting the resulting gain.

A stable control loop has a gain crossing with close to a -20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin. The mathematical model presented makes a number of approximations and is generally not accurate at frequencies approaching or exceeding half the switching frequency. When designing compensation networks, select target crossover frequencies in the range of 10% to 30% of the switching frequency, f_{SW}.

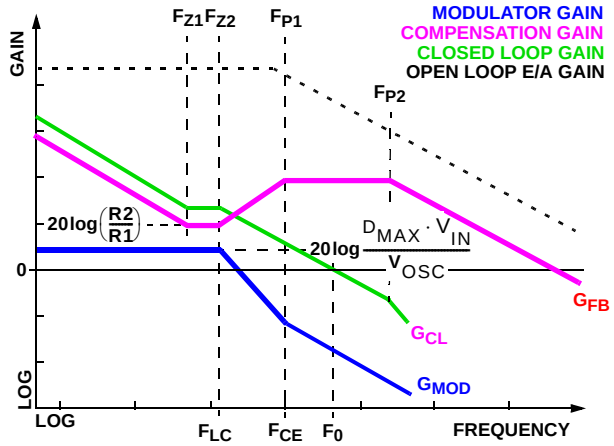


FIGURE 8. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

For applications that have transient load rates above 1A/ns, high frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate

transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by Equation 15:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{Fs \times L} \bullet \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR \qquad \text{(EQ. 15)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL8104 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient load is different for the application of load and the removal of load. Equation 16 gives the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}} \qquad \text{(EQ. 16)}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. With a +5V input source, the worst case response time can be either at the application or removal of load and dependent upon the output voltage setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q_1 and the source of Q_2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select a bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage, a voltage rating of 1.5 times greater is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

For a through hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection/Considerations

The ISL8104 requires at least 2 N-Channel power MOSFETs. These should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. At a 300kHz switching frequency, the conduction losses are the largest component of power dissipation for both the top-side and the bottom-side MOSFETs. These losses are distributed between the two MOSFETs according to duty factor (see the following equations). Only the top-side MOSFET exhibits switching losses, since the schottky rectifier clamps the switching node before the synchronous rectifier turns on.

$$P_{top\text{-}side} = I_O^2 \times r_{DS(ON)} \times D + \frac{1}{2} \times Io \times V_{IN} \times t_{SW} \times f_{SW}$$

$$P_{bottom\text{-}side} = I_O^2 \times r_{DS(ON)} \times (1 - D)$$

where: D is the duty cycle = V_O / V_{IN},
t_{SW} is the switching interval, and
f_{SW} is the switching frequency. (EQ. 17)

Equation 17 assumes linear voltage-current transitions and does not adequately model power loss due to the reverse-recovery of the bottom-side MOSFETs body diode. The gate-charge losses are dissipated by the ISL8104 and don't heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW} which increases the top-side MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

Standard-gate MOSFETs are normally recommended for use with the ISL8104. However, logic-level gate MOSFETs can be used under special circumstances. The input voltage, top-side gate drive level, and the MOSFETs absolute gate-to-source voltage rating determine whether logic-level MOSFETs are appropriate.

Figure 9 shows the top-side gate drive (BOOT pin) supplied by a bootstrap circuit from +14V. The boot capacitor, C_{BOOT} develops a floating supply voltage referenced to the LX pin. This supply is refreshed each cycle to a voltage of +14V less the boot diode drop (V_D) when the bottom-side MOSFET, Q_2 turns on. A MOSFET can only be used for Q_1 if the MOSFETs absolute gate-to-source voltage rating exceeds the maximum voltage applied to +14V. For Q_2, a logic-level MOSFET can be used if its absolute gate-to-source voltage rating also exceeds the maximum voltage applied to +14V.

Figure 10 shows the top-side gate drive supplied by a direct connection to +14V. This option should only be used in converter systems where the main input voltage is +5VDC or less. The peak top-side gate-to-source voltage is approximately +14V less the input supply. For +5V main power and +14VDC for the bias, the gate-to-source voltage of Q_1 is 9V. A logic-level MOSFET is a good choice for Q_1 and a logic-level MOSFET can be used for Q_2 if its absolute gate-to-source voltage rating exceeds the maximum voltage applied to PVCC. This method reduces the number of required external components, but does not provide for immunity to phase node ringing during turn on and may result in lower system efficiency.

Schottky Selection

Rectifier D2 is a clamp that catches the negative inductor swing during the dead time between turning off the bottomside MOSFET and turning on the top-side MOSFET. The diode must be a Schottky type to prevent the lossy parasitic MOSFET body diode from conducting. It is acceptable to omit the diode and let the body diode of the bottom-side MOSFET clamp the negative inductor swing, but efficiency could slightly decrease as a result. The diode's rated reverse breakdown voltage must be greater than the maximum input voltage.

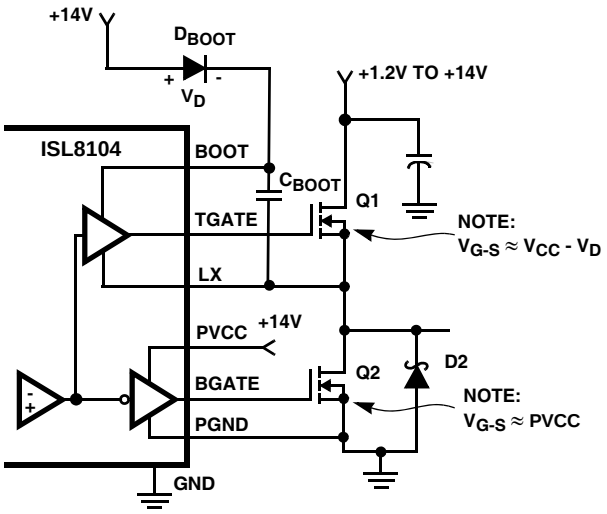


FIGURE 9. TOP-SIDE GATE DRIVE - BOOTSTRAP OPTION

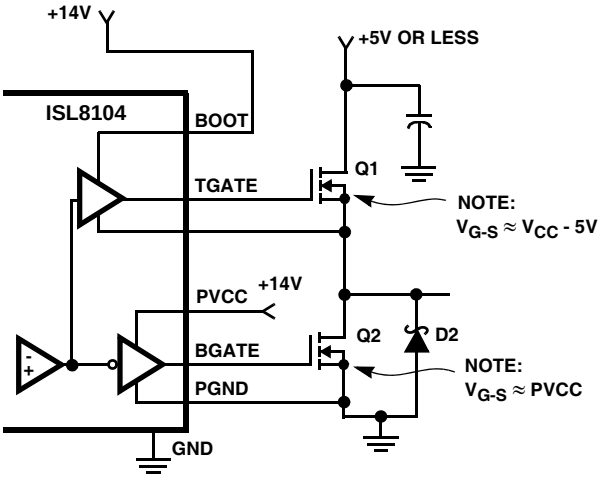
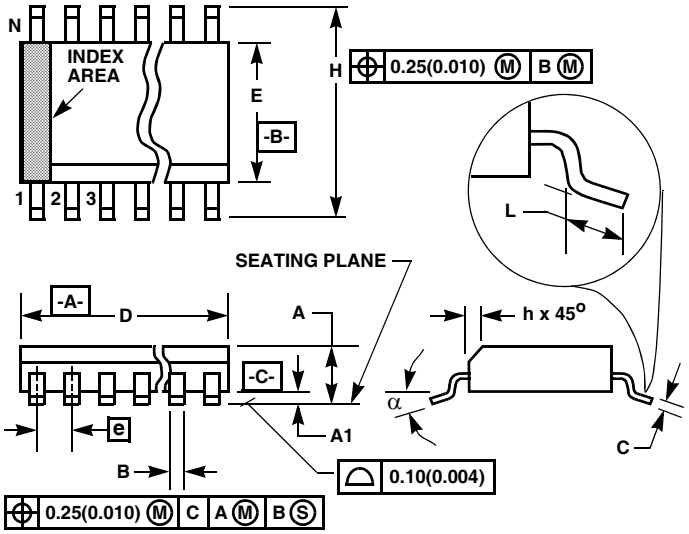


FIGURE 10. TOP-SIDE GATE DRIVE - DIRECT V_{CC} DRIVE OPTION

Small Outline Plastic Packages (SOIC)



NOTES:

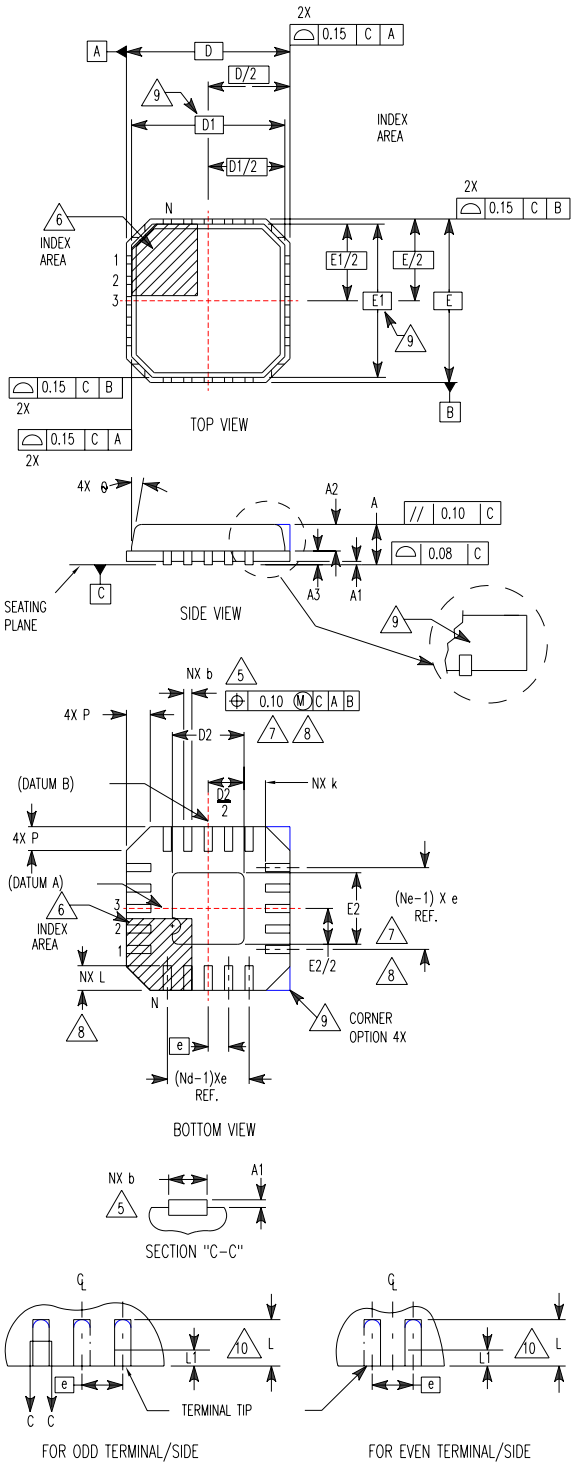
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 5 5/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

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