MC74LVX74

Dual D-Type Flip-Flop with Set and Clear

With 5.0 V−Tolerant Inputs

The MC74LVX74 is an advanced high speed CMOS D−type flip−flop. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

The signal level applied to the D input is transferred to O output during the positive going transition of the Clock pulse.

Clear ($\overline{CD}$) and Set ($\overline{SD}$) are independent of the Clock (CP) and are accomplished by setting the appropriate input Low.

Features

- High Speed: f_{max} = 145 MHz (Typ) at V_{CC} = 3.3 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
    Human Body Model > 2000 V;
    Machine Model > 200 V
- These Devices are Pb−Free and are RoHS Compliant
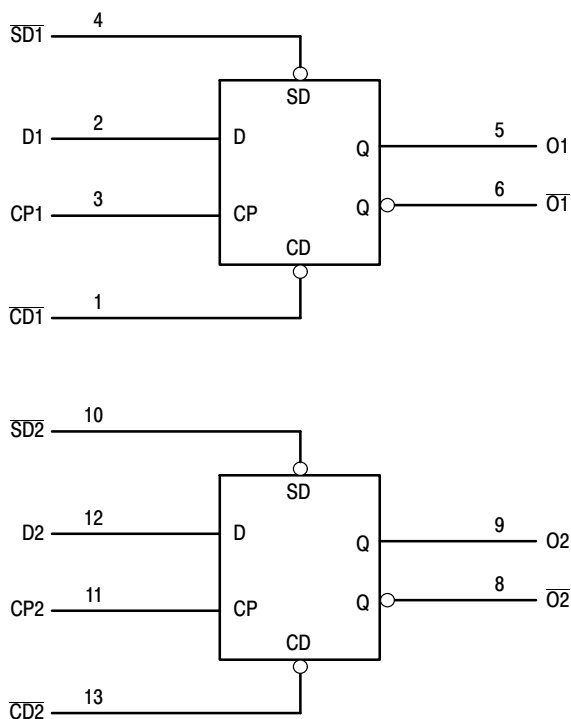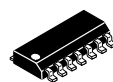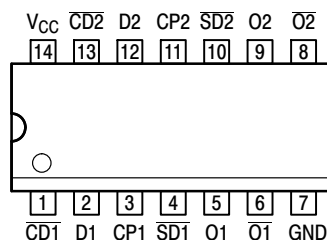
Figure 1. Logic Diagram

MC74LVX74

INPUTS				OUTPUTS		
$\overline{SDn}$	$\overline{CDn}$	CPn	Dn	On	$\overline{On}$	OPERATING MODE
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Clear
L	L	X	X	H	H	Undetermined
H	H	↑	h	H	L	Load and Read Register
H	H	↑	l	L	H	Load and Read Register
H	H	↕	X	NC	NC	Hold

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; NC = No Change; X = High or Low Voltage Level or Transitions are Acceptable; ↑ = Low–to–High Transition; ↕ = Not a Low–to–High Transition; For I_{CC} Reasons DO NOT FLOAT Inputs

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	−0.5 to +7.0	V
V_{in}	DC Input Voltage	−0.5 to +7.0	V
V_{out}	DC Output Voltage	−0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	−20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	−40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = − 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 / 3.0 / 3.6	1.5 / 2.0 / 2.4			1.5 / 2.0 / 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 / 3.0 / 3.6			0.5 / 0.8 / 0.8		0.5 / 0.8 / 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = −50µA / I_{OH} = −50µA / I_{OH} = −4mA	2.0 / 3.0 / 3.0	1.9 / 2.9 / 2.58	2.0 / 3.0		1.9 / 2.9 / 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50µA / I_{OL} = 50µA / I_{OL} = 4mA	2.0 / 3.0 / 3.0		0.0 / 0.0	0.1 / 0.1 / 0.36		0.1 / 0.1 / 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			2.0		20.0	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	Typ	Max	$T_A = -40$ to $85°C$ Min	Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay CP to O or $\overline{O}$	$V_{CC} = 2.7$V	$C_L = 15$pF $C_L = 50$pF		7.3 9.8	15.0 18.5	1.0 1.0	18.5 22.0	ns
		$V_{CC} = 3.3 \pm 0.3$V	$C_L = 15$pF $C_L = 50$pF		5.7 8.2	9.7 13.2	1.0 1.0	11.5 15.0	
t_{PLH}, t_{PHL}	Propagation Delay $\overline{SD}$ or $\overline{CD}$ to O or $\overline{O}$	$V_{CC} = 2.7$V	$C_L = 15$pF $C_L = 50$pF		8.4 10.9	15.6 19.1	1.0 1.0	18.5 22.0	ns
		$V_{CC} = 3.3 \pm 0.3$V	$C_L = 15$pF $C_L = 50$pF		6.6 9.1	10.1 13.6	1.0 1.0	12.0 15.5	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 2.7$V	$C_L = 15$pF $C_L = 50$pF	55 45	135 60		50 40		MHz
		$V_{CC} = 3.3 \pm 0.3$V	$C_L = 15$pF $C_L = 50$pF	95 60	145 85		80 50		
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1)	$V_{CC} = 2.7$V $V_{CC} = 3.3 \pm 0.3$V	$C_L = 50$pF $C_L = 50$pF			1.5 1.5		1.5 1.5	ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit $T_A = 25°C$	$T_A = -40$ to $85°C$	Unit
t_w	Minimum Pulse Width, CP	2.7V 3.3V ± 0.3	8.5 6.0	10.0 7.0	ns
t_w	Minimum Pulse Width, $\overline{CD}$ or $\overline{SD}$	2.7V 3.3V ± 0.3	8.5 6.0	10.0 7.0	ns
t_{su}	Minimum Setup Time, D to CP	2.7V 3.3V ± 0.3	8.0 5.5	9.5 6.5	ns
t_h	Minimum Hold Time, D to CP	2.7V 3.3V ± 0.3	0.5 0.5	0.5 0.5	ns
t_{rec}	Minimum Recovery Time, $\overline{SD}$ or $\overline{CD}$ to CP	2.7V 3.3V ± 0.3	6.5 5.0	7.5 5.0	ns

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	Typ	Max	$T_A = -40$ to $85°C$ Min	Max	Unit
Cin	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 2)		25				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/2$ (per flip–flop). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.3	-0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

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SWITCHING WAVEFORMS
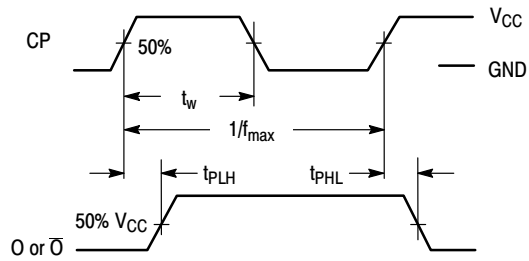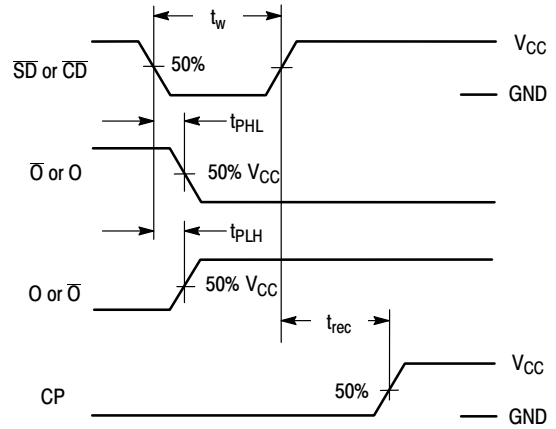
Figure 2.

Figure 3.

Figure 4.

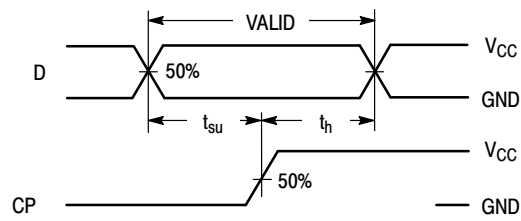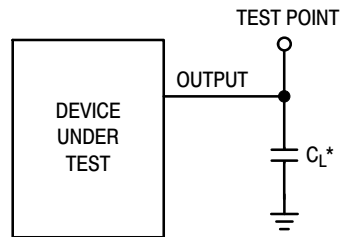## TEST CIRCUIT

*Includes all probe and jig capacitance

Figure 5.

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ORDERING INFORMATION
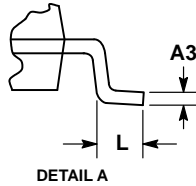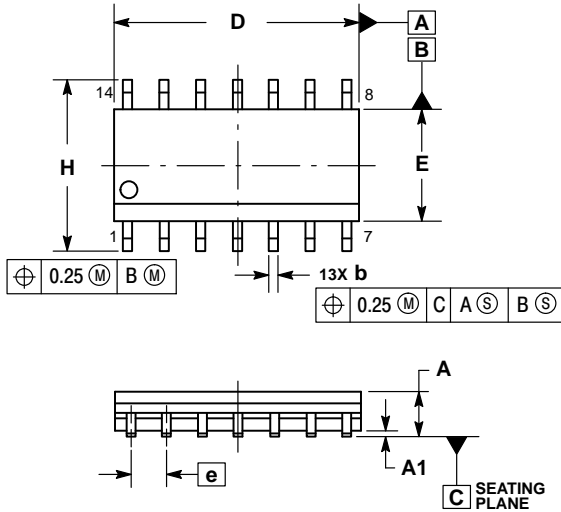
Device	Package	Shipping†
MC74LVX74DR2G	SOIC−14 NB (Pb−Free)	2500 Tape & Reel
MC74LVX74DTG	TSSOP−14 (Pb−Free)	96 Units / Rail
MC74LVX74DTR2G	TSSOP−14 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS
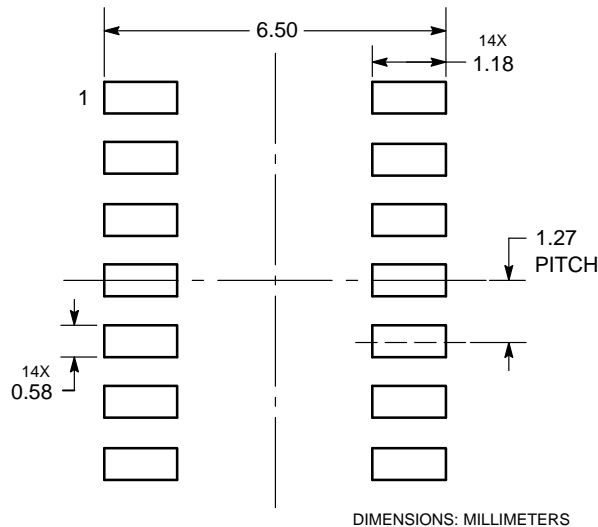
TSSOP−14
CASE 948G
ISSUE B

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*

7.06

1

0.65 PITCH

14X
0.36

14X
1.26

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

SOIC−14 NB
CASE 751A−03
ISSUE K
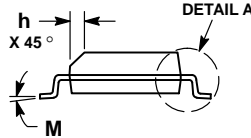
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

DETAIL A

13X b

SEATING PLANE

X 45 °

DETAIL A

SOLDERING FOOTPRINT*

6.50

14X
1.18

1.27 PITCH

14X
0.58

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

MC74LVX74/D

AMEYA360
Components Supply Platform

Authorized Distribution Brand：

Website：

Welcome to visit   www.ameya360.com

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➤ **Address：**

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Minhang District, Shanghai , China

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