

CTSLVEL16VR

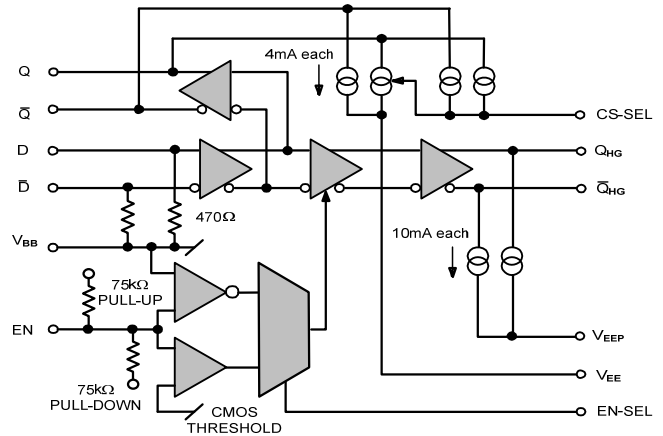
PECL/ECL Oscillator Gain Stage & Buffer with Selectable Enable

MLP8, MLP16

FEATURES

- Minimizes External Components
- Selectable Enable Polarity and Threshold (CMOS or PECL)
- High Bandwidth for $\geq 1\text{GHz}$
- Similar Operation as CTS100EL16
- -147 dBc/Hz Typical Noise Floor

BLOCK DIAGRAM



DESCRIPTION

The CTSLVEL16VR is a specialized oscillator gain stage with a high gain output buffer including an enable function. The $Q_{HG}/\bar{Q}_{HG}$ outputs have voltage gain several times greater than the $Q/\bar{Q}$ outputs. It provides a selectable $Q_{HG}/\bar{Q}_{HG}$ enable that allows continuous oscillator operation via the $Q/\bar{Q}$ outputs.

The CTSLVEL16VR provides adjustable internal pull-down current sources for the $Q/\bar{Q}$ outputs and optional 10mA current sources for the $Q_{HG}/\bar{Q}_{HG}$ outputs. Internal input biasing further reduces the number of needed external components.

ENGINEERING NOTES

Functionality of MLP16 Package (CTSLVEL16VRNLG)

The CTSLVEL16VRNLG provides a selectable $Q_{HG}/\bar{Q}_{HG}$ enable that allows continuous oscillator operation via the $Q/\bar{Q}$ outputs. Table 1 shows the operating modes. Leaving EN-SEL open (NC) selects PECL/ECL operation for the EN pad/pin. In this mode the $Q_{HG}/\bar{Q}_{HG}$ outputs are enabled when EN is left open (NC) or set to a PECL/ECL low.

Connecting EN-SEL to V_{CC} , V_{EE} or V_{BB} selects CMOS operation for the EN pad/pin. When EN-SEL is tied to V_{EE} , the $Q_{HG}/\bar{Q}_{HG}$ outputs are disabled when EN is left open (NC). When EN-SEL is tied to V_{CC} or V_{BB} , the $Q_{HG}/\bar{Q}_{HG}$ outputs are enabled when EN is left open. This default logic condition can be overridden by a $\leq 20\text{k}\Omega$ resistor connected to the opposite supply.

The CTSLVEL16VRNLG also provides a V_{BB} and 470Ω internal bias resistors from D to V_{BB} and $\bar{D}$ to V_{BB} . The V_{BB} pin supports 1.5mA sink/source current. V_{BB} should be bypassed to ground or V_{CC} with a $0.01\text{ }\mu\text{F}$ capacitor.

Outputs $Q/\bar{Q}$ each have a selectable on-chip pull-down current source. See Table 2 for the supported values. External resistors may also be used to increase pull-down current to a maximum total of 25mA for the $Q/\bar{Q}$ outputs.

Each of the $Q_{HG}/\bar{Q}_{HG}$ outputs has an optional on-chip pull-down current source of 10mA. When pad/pin V_{EEP} is left open (NC), the output current sources are disabled and the $Q_{HG}/\bar{Q}_{HG}$ operate as standard PECL/ECL. When V_{EEP} is connected to V_{EE} , the current sources are activated. The $Q_{HG}/\bar{Q}_{HG}$ pull-down current can be decreased by using a resistor between V_{EEP} and V_{EE} .

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Table 1 - Enable Truth Table

EN-SEL	EN	Q/ $\bar{Q}$	Q _{HG}	$\bar{Q}$ _{HG}
NC	PECL Low, V _{EE} or NC	Data	Data	Data
	PECL High or V _{CC}	Data	Low	High
V _{EE} ¹	CMOS Low, V _{EE} or NC	Data	Low	High
	CMOS High or V _{CC}	Data	Data	Data
V _{CC} or V _{BB} ^{1,2}	CMOS Low or V _{EE}	Data	Low	High
	CMOS High, V _{CC} or NC	Data	Data	Data

¹ EN-SEL connections must be $\leq 1\Omega$.

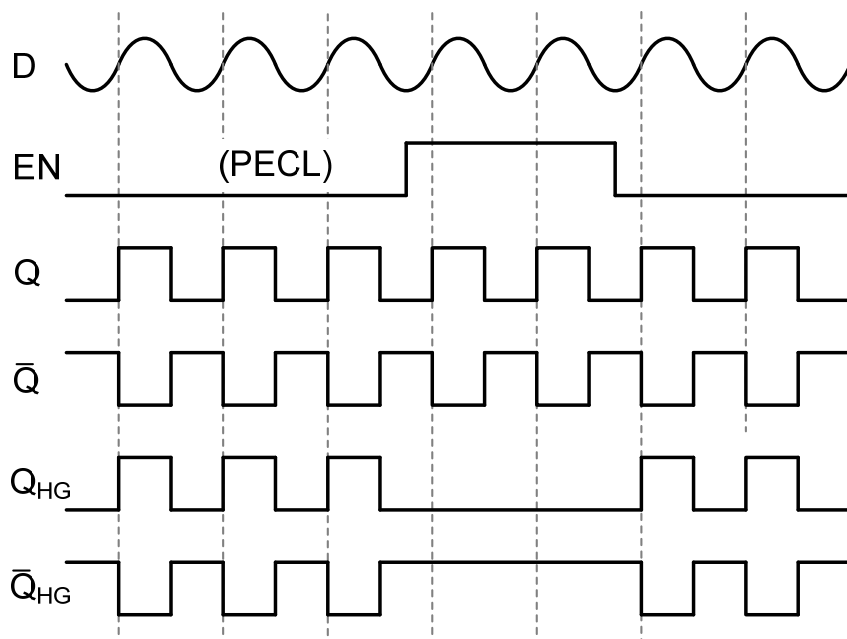
² Date codes prior to 0428 do not support this operating mode.

Table 2 - Current Source Truth Table

CS-SEL	Q	$\bar{Q}$
NC	4mA typ	4mA typ
V _{EE} ¹	8mA typ	8mA typ
V _{CC} ¹	0	4mA typ

¹ Connection must be less than 1Ω .

Figure below illustrates the timing sequences for the CTSLVEL16VRNLG in the MLP 16 package. It is shown here with the enable operating in active Low mode with a PECL threshold. This mode is determined by leaving the EN-SEL open (NC). An active High enable with a CMOS/TTL threshold is also an option.



CTSLVEL16VRNLG Timing Diagram

CTSLVEL16VR

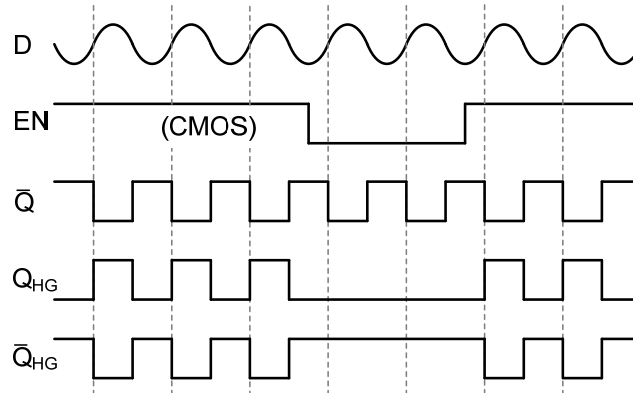
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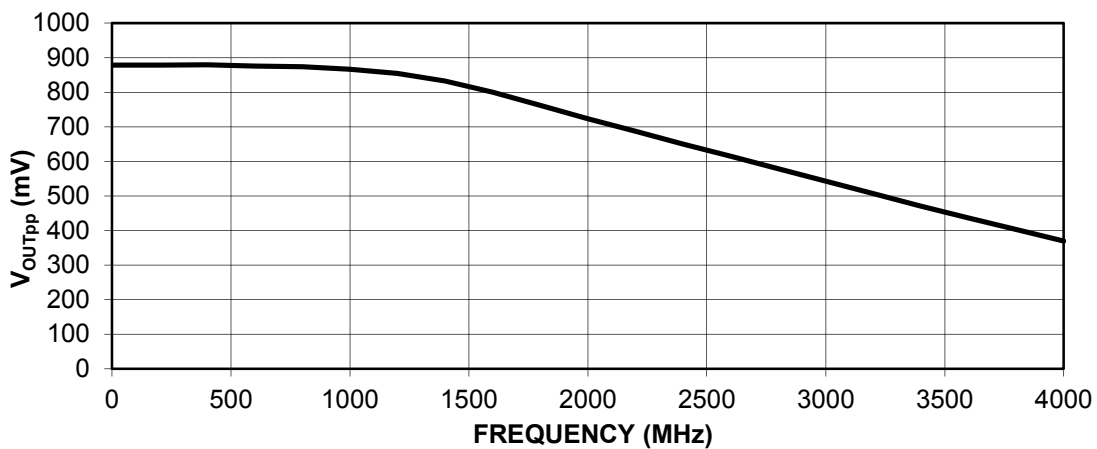
Functionality MLP8 Package (CTSLVEL16VRNNG)

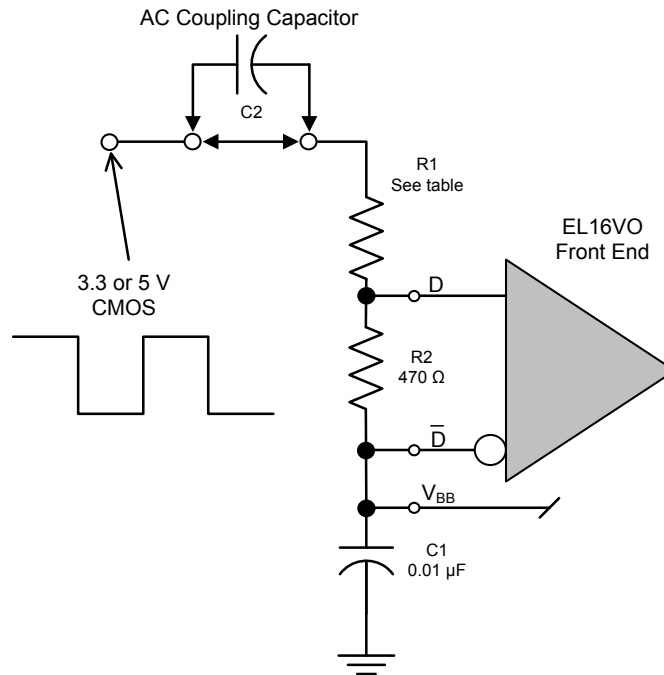
A CMOS enable input (EN) allows continuous oscillator operation. When the EN input is HIGH or left open (NC), the $\bar{Q}$ and $Q_{HG}/\bar{Q}_{HG}$ outputs follow the data input. When EN is LOW, the Q_{HG} output is forced high and the $\bar{Q}_{HG}$ output is forced low while $\bar{Q}$ continues to follow the data input. The $\bar{Q}$ output has an internal 4 mA current source to V_{EE} , in most cases eliminating the need for an external pull-down resistor.

The CTSLVEL16VRNNG also provides biasing. Data input D is tied to the VBB pin through a 470 Ω internal bias resistor while the inverting input $\bar{D}$ is connected directly to V_{BB} . The V_{BB} pin supports 1.5mA sink/source current. V_{BB} should be bypassed to ground with a 0.01 μ F capacitor.



CTSLVEL16VRNNG Timing





Application Circuit for CMOS Inputs

Recommended Component Values for CMOS Single Ended Inputs

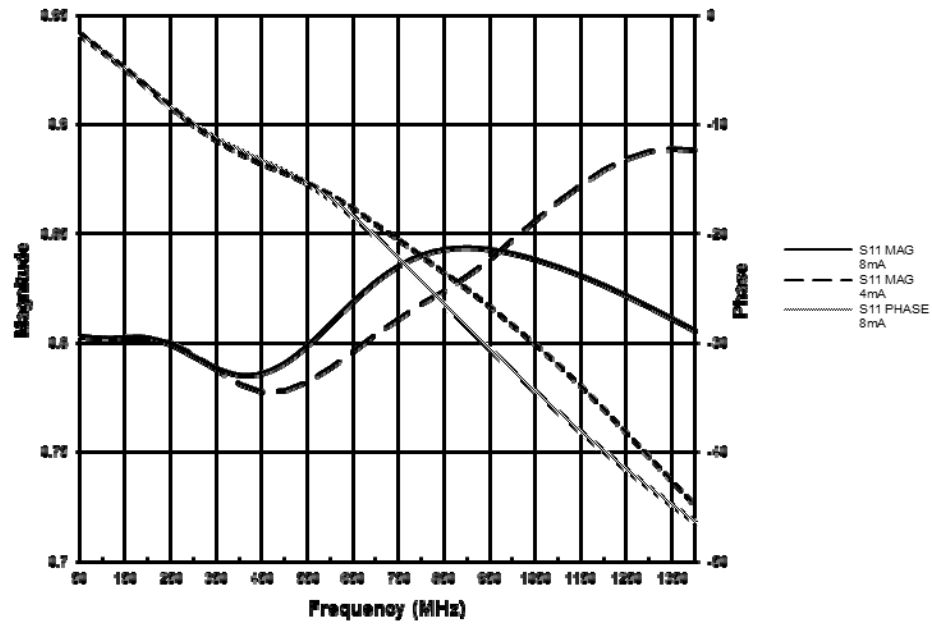
Input Type	R1 ¹ Value	
	AC Coupled (C2 in circuit)	DC Coupled (C2 shorted)
3.3V CMOS	1.1 kΩ	2.0 kΩ
5.0V CMOS	1.6 kΩ	3.3 kΩ

¹ R1 should be chosen so that the input swing on the D input with respect to $\bar{D}$ is in the range of ± 80 to ± 1000 mV, per the AC Characteristics table and the D input is $< \pm 750$ mV with respect to V_{BB}.

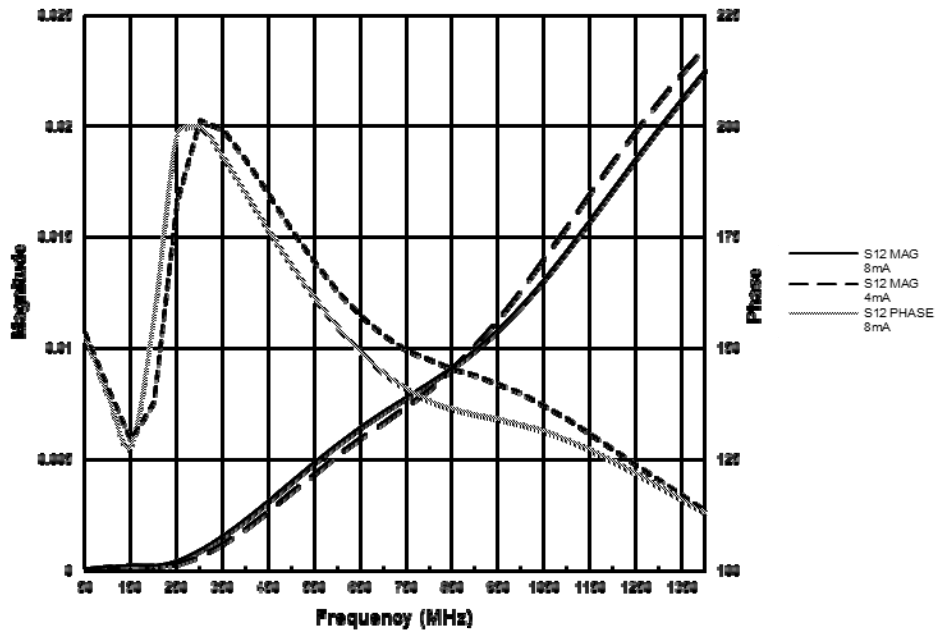
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S11 50Ω external AC, 4 & 8mA internal DC load

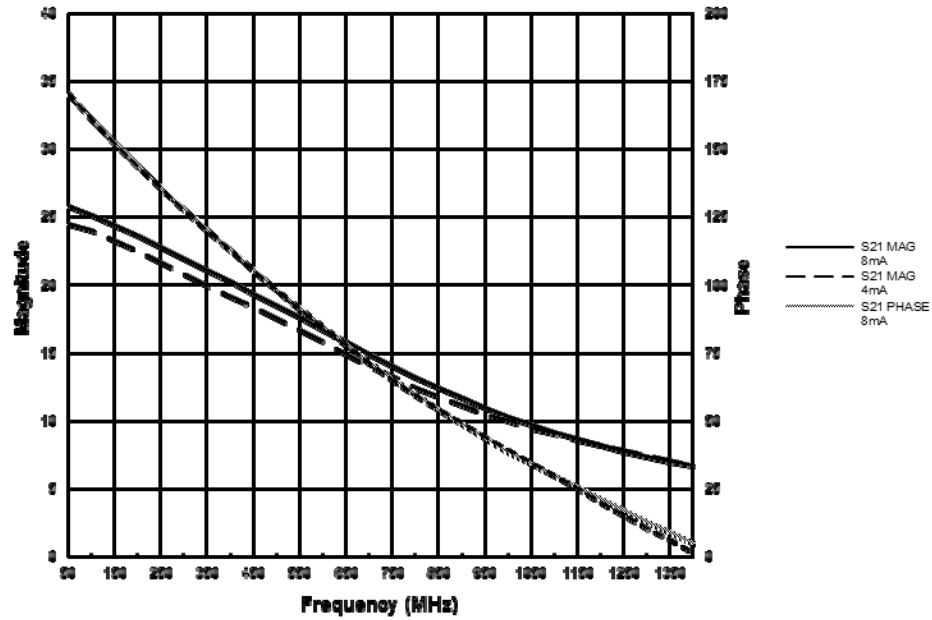


S12 50Ω external AC, 4 & 8mA internal DC load

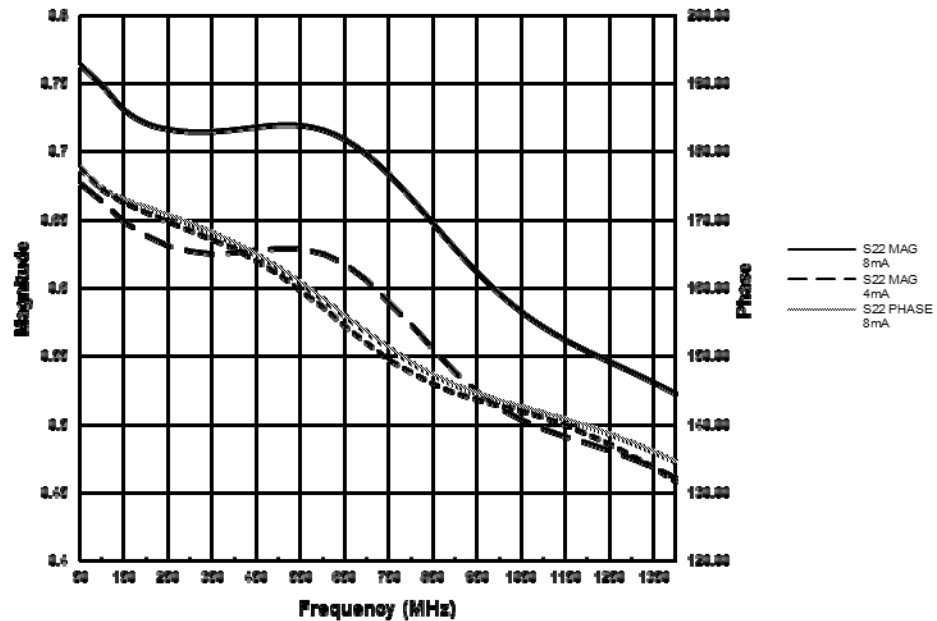
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PECL/ECL Oscillator Gain Stage & Buffer with Selectable Enable

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S21 50Ω external AC, 4 & 8mA internal DC load



S22 50Ω external AC, 4 & 8mA internal DC load

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ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V_{CC}	PECL Power Supply	$V_{EE} = 0V$	0 to + 6.0	V
V_{D_PECL}	PECL D Input Voltage	Referenced to V_{BB}	± 0.75	V
V_{EN_PECL}	PECL D Input Voltage	$V_{EE} = 0V$	0 to + 6.0	V
V_{EE}	ECL Power Supply	$V_{CC} = 0V$	-6.0 to 0	V
V_{D_ECL}	ECL D Input Voltage	Referenced to V_{BB}	± 0.75	V
V_{EN_ECL}	ECL D Input Voltage	$V_{CC} = 0V$	-6.0 to 0	V
I_{OUT}	Output Current	Continuous Q	25	mA
		Surge Q	50	
		Continuous Q_{HG}	50	
		Surge Q_{HG}	100	
T_A	Operating Temperature Range	-	-40 to +85	°C
T_{STG}	Storage Temperature Range	-	-65 to +150	°C
ESD_{HBM}	Human Body Model Electro Static Discharge	-	2500	V
ESD_{MM}	Machine Model Electro Static Discharge	-	200	V
ESD_{CDM}	Charged Device Model Electro Static Discharge	-	2000	V

ECL DC Characteristics ($V_{EE} = -3.0V$ to $-5.5V$, $V_{CC} = GND$)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage ¹	-1045	-835	-1025	-835	-1025	-835	-1025	-835	mV
V_{OL}	Output LOW Voltage ¹	-1925	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V_{IH}	Input HIGH Voltage D,EN (ECL) ²	-1165	-740	-1165	-740	-1165	-740	-1165	-740	mV
	Input HIGH Voltage EN (CMOS) ³	$V_{EE} + 2000$	V_{CC}	$V_{EE} + 2000$	V_{CC}	$V_{EE} + 2000$	V_{CC}	$V_{EE} + 2000$	V_{CC}	mV
V_{IL}	Input LOW Voltage D,EN (ECL) ²	-1900	-1475	-1900	-1475	-1900	-1475	-1900	-1475	mV
	Input LOW Voltage EN (CMOS) ³	V_{EE}	$V_{EE} + 800$	V_{EE}	$V_{EE} + 800$	V_{EE}	$V_{EE} + 800$	V_{EE}	$V_{EE} + 800$	mV
V_{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	μA
I_{IL}	Input LOW Current EN (ECL) ²	0.5		0.5		0.5		0.5		μA
	Input LOW Current EN (CMOS) ³	-150		-150		-150		-150		
I_{EE}	Power Supply Current ¹		48		48		48		54	mA

¹ Specified with each output terminated through 50Ω resistors to $V_{CC} - 2V$.

² EN-SEL = NC.

³ EN-SEL = V_{CC} or V_{EE} .

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AC Characteristics ($V_{EE} = -3.0V$ to $-5.5V$; $V_{CC}=GND$ or $V_{EE}=GND$; $V_{CC} = +3.0V$ to $+5.5V$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}/t_{PHL}	Propagation Delay													
	D to Q ¹			400			400			400			400	ps
	D to Q _{HG} ¹			450			450			450			450	ps
t_{SKEW}	Duty Cycle Skew ³		5	20		5	20		5	20		5	20	ps
V_{pp} (AC)	Input Swing ⁴ Differential	80		1000	80		1000	80		1000	80		1000	mV
t_r/t_f	Output Rise/Fall ^{1,2} (20% - 80%)	100		240	100		240	100		240	100		240	ps

¹ Specified with CS-SEL connected to V_{EE} , Q terminated with an AC coupled to 50Ω load.

² Specified with each output terminated through 50Ω resistors to $V_{CC} - 2V$.

³ Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

LVPECL DC Characteristics ($V_{EE} = GND$, $V_{CC} = +3.3V$)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage ^{1,2}	2255	2465	2275	2465	2275	2465	2275	2465	mV
V_{OL}	Output LOW Voltage ^{1,2}	1375	1745	1400	1680	1400	1680	1400	1680	mV
V_{IH}	Input HIGH Voltage D,EN (ECL) ³	2135	2560	2135	2560	2135	2560	2135	2560	mV
	Input HIGH Voltage EN (CMOS) ⁴	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	mV
V_{IL}	Input LOW Voltage D,EN (ECL) ³	1400	1825	1400	1825	1400	1825	1400	1825	mV
	Input LOW Voltage EN (CMOS) ⁴	GND	800	GND	800	GND	800	GND	800	mV
V_{BB}	Reference Voltage ¹	1910	2050	1910	2050	1910	2050	1910	2050	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	μA
I_{IL}	Input LOW Current EN (ECL) ³	0.5		0.5		0.5		0.5		μA
	Input LOW Current EN (CMOS) ⁴	-150		-150		-150		-150		
I_{EE}	Power Supply Current ²		48		48		48		54	mA

¹ For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.

² Specified with each output terminated through 50Ω resistors to $V_{CC} - 2V$.

³ EN-SEL = NC.

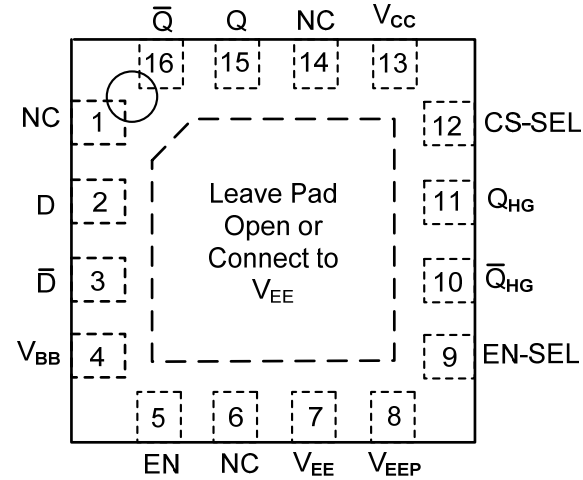
⁴ EN-SEL = V_{CC} or V_{EE} .

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PECL DC Characteristics ($V_{EE} = \text{GND}$, $V_{CC} = +5.0\text{V}$)

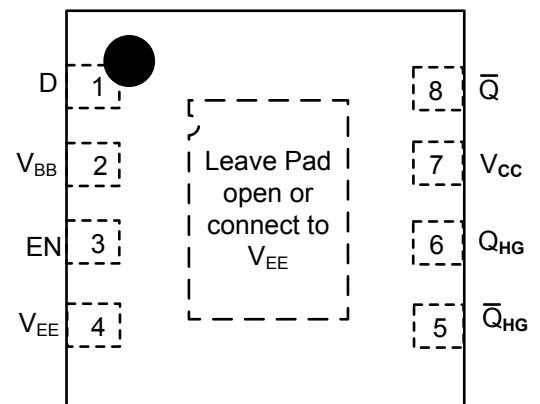
Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	3955	4165	3975	4165	3975	4165	3975	4165	mV
V_{OL}	Output LOW Voltage	3075	3445	3100	3380	3100	3380	3100	3380	mV
V_{IH}	Input HIGH Voltage D,EN (ECL)	3835	4260	3835	4260	3835	4260	3835	4260	mV
	Input HIGH Voltage EN (CMOS)	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	mV
V_{IL}	Input LOW Voltage D,EN (ECL)	3100	3525	3100	3525	3100	3525	3100	3525	mV
	Input LOW Voltage EN (CMOS)	GND	800	GND	800	GND	800	GND	800	mV
V_{BB}	Reference Voltage	3610	3750	3610	3750	3610	3750	3610	3750	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	μA
I_{IL}	Input LOW Current EN (ECL)	0.5		0.5		0.5		0.5		μA
	Input LOW Current EN (CMOS)	-150		-150		-150		-150		
I_{EE}	Power Supply Current		48		48		48		54	mA

CTSLVEL16VR
PECL/ECL Oscillator Gain Stage & Buffer with Selectable Enable
MLP8, MLP16
Pin Description and Configuration
Pin Assignments CTSLVEL16VRNLG

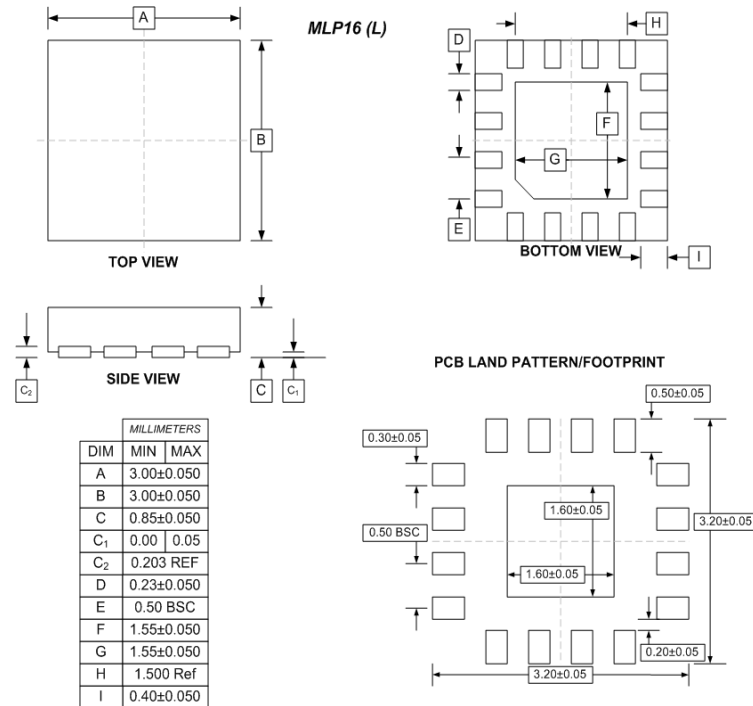
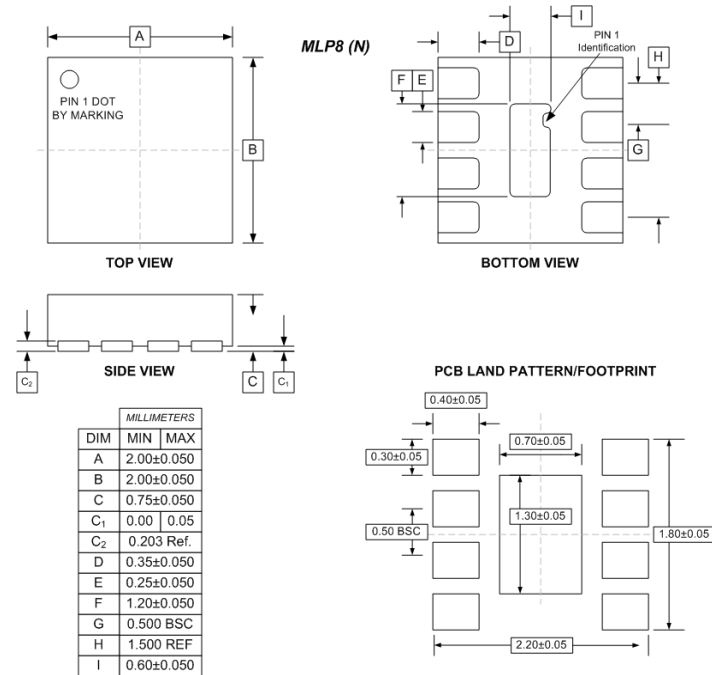
Pin	Name	Type	Function
1	NC	-	N/A
2	D	Input	Data Input
3	$\bar{D}$	Input	Inverting Data Input
4	V_{BB}	Output	Reference Voltage
5	EN	Input	Output Enable
6	NC	-	N/A
7	V_{EE}	Power	Negative Supply
8	V_{EEP}	Input	High Gain Current Source Enable
9	EN-SEL	Input	Enable Polarity Select
10	$\bar{Q}_{HG}$	Output	High Gain Inverting PECL Output
11	Q_{HG}	Output	High Gain PECL Output
12	CS-SEL	Input	Current Source Select
13	V_{CC}	Power	Positive Supply
14	NC	-	N/A
15	Q	Output	PECL Output
16	$\bar{Q}$	Output	Inverting PECL Output


Pin Configuration for CTSLVEL16VRNLG
Pin Description CTSLVEL16VRNNG

Pin	Name	Type	Function
1	D	Input	Data Input
2	V_{BB}	Output	Reference Voltage
3	EN	Input	Output Enable
4	V_{EE}	Power	Negative Supply
5	$\bar{Q}_{HG}$	Output	High Gain Inverting PECL Output
6	Q_{HG}	Output	High Gain PECL Output
7	V_{CC}	Power	Positive Supply
8	$\bar{Q}$	Output	Inverting PECL Output


Pin Configuration for CTSLVEL16VRNNG
PART ORDERING INFORMATION

Part Number	Package	Marking
CTSLVEL16VRNLG	MLP16	100G 16R YYWW
CTSLVEL16VRNNG	MLP8	R5G YYWW

CTSLVEL16VR
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MLP8, MLP16
PACKAGE DIMENSIONS


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