TPS25200 5V eFuse with Precision Adjustable Current Limit and Overvoltage Clamp

1 Features

- 2.5 V to 6.5 V Operation
- Input Withstands Up to 20 V
- 7.6 V Input Overvoltage Shutoff
- 5.25 V to 5.55 V Fixed Overvoltge Clamp
- 0.6-µs Overvoltage Lockout Response
- 3.5-µs Short Circuit Response
- Integrated 60-mΩ High-Side MOSFET
- Up to 2.5 A Continuous Load Current
- ±6% Current-Limit Accuracy at 2.9 A
- Reverse Current Blocking While Disabled
- Built-in Soft Start
- Pin-to-Pin Compatible with TPS2553

2 Applications

- USB Power Switch
- USB Slave Devices
- Cell/Smart Phones
- 3G, 4G Wireless Data-card
- Solid State Drives (SSD)
- 3 V or 5 V Adapter Powered Devices

3 Description

The TPS25200 is a 5V eFuse with precision current limit and overvoltage clamp. The device provides robust protection for load and source during overvoltage and overcurrent events.

The TPS25200 is an intelligent protected load switch with V_{IN} tolerant to 20 V. In the event that an incorrect voltage is applied at IN, the output will clamp to 5.4 V to protect the load. If the voltage at IN exceeds 7.6 V, the device disconnects the load to prevent damage to the device and/or load.

The TPS25200 has an internal 60 mΩ power switch and is intended for protecting source, device, and load under a variety of abnormal conditions. The device provides up to 2.5 A of continuous load current. Current limit is programmable from 85 mA to 2.9 A with a single resistor to ground. During overload events output current is limited to the level set by R_{ILIM}. If a persistent overload occurs the device will eventually go into thermal shutoff to prevent damage to the TPS25200.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
TPS25200DRV	SON (6)	2mm × 2mm

4 Simplified Schematic

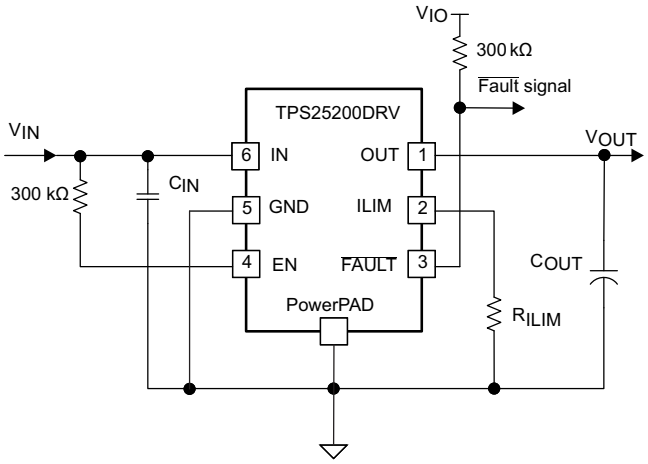
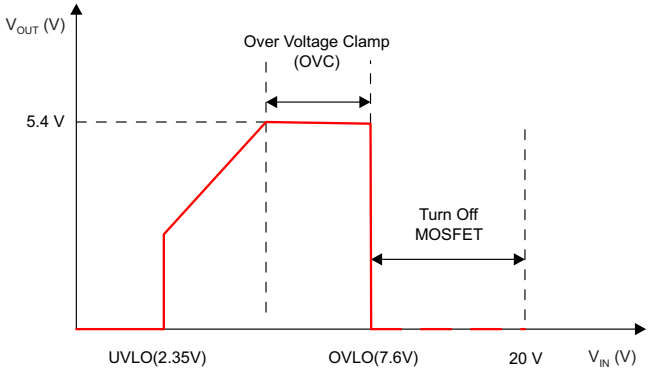


Figure 1. V_{OUT} vs V_{IN}



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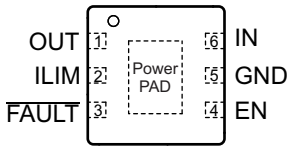
5 Revision History

Changes from Original (March 2014) to Revision A **Page**

- Changed the t_{off} TYP value From: 0.24 ms To: 0.22 ms ... 6
- Added condition: V_{EN} = V_{IN} = 0 V to Figure 4 ... 7
- Changed Figure 9 graph title From: Discharge Resistance To: V_{IN} ... 7
- Changed Equation 4 From = 2470 mA to = 2479 mA ... 17

6 Terminal Configuration and Functions

DRV PACKAGE
6 TERMINALS
TOP VIEW



Terminal Functions

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
EN	4	I	Logic-level control input. When is driven high, the power switch is enabled. When it is driven low, turn power switch off. This pin can not be left floating and it must be limited below the absolute maximum rating if tied to V_{IN}.
$\overline{\text{FAULT}}$	3	O	Active-low open-drain output, asserted during overcurrent, overvoltage or overtemperature. Connect a pull up resistor to the logic I/O voltage.
GND	5		Ground connection; connect externally to PowerPAD.
ILIM	2	O	External resistor used to set current-limit threshold; Recommended 33 kΩ ≤ R_{ILIM} ≤ 1100 kΩ.
IN	6	I	Input voltage; connect a 0.1 µF or greater ceramic capacitor from IN to GND as close to the IC as possible.
OUT	1	O	Protected power switch V_{OUT}.
PowerPAD™	PAD		Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND terminal externally.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, voltage are referenced to GND (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Voltage range on IN	–0.3	20	V
	Voltage range on OUT, EN, ILIM, $\overline{\text{FAULT}}$	–0.3	7	V
	Voltage range from IN to OUT	–7	20	V
I_O	Continuous output current	Thermally Limited		
	Continuous $\overline{\text{FAULT}}$ output sink current		25	mA
	Continuous ILIM output source current		150	µA
T_J	Operating junction temperature	Internally limited		

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	-65	150	°C
ESD(1)	Human Body Model (HBM) ESD stress voltage		2	kV
	Charging Device Model (CDM) ESD stress voltage		500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.

7.3 Recommended Operating Conditions

over operating free-air temperature range, voltage are referenced to GND (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage of IN	2.5	6.5	V
V_{EN}	Enable terminal voltage	0	6.5	V
$I_{\overline{\text{FAULT}}}$	Continuous $\overline{\text{FAULT}}$ sink current	0	10	mA
I_{OUT}	Continuous output current of OUT		2.5	A
R_{ILIM}	Current-limit set resistors	33	1100	kΩ
T_J	Operating junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS25200 DRV (6 TERMINALS)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	66.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	83.4	
θ_{JB}	Junction-to-board thermal resistance	36.1	
ψ_{JT}	Junction-to-top characterization parameter	1.6	
ψ_{JB}	Junction-to-board characterization parameter	36.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	7.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Conditions are –40°C ≤ T_J ≤ 125°C and 2.5 V ≤ V_{IN} ≤ 6.5 V. V_{EN} = V_{IN}, R_{ILIM} = 33kΩ. Positive current into terminals. Typical value is at 25°C. All voltages are with respect to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	IN–OUT resistance (1)	2.5 V ≤ V_{IN} ≤ 5 V, I_{OUT} = 2.5 A	T_J = 25°C		60	70	mΩ
			–40°C ≤ T_J ≤ 85°C		60	90	
			–40°C ≤ T_J ≤ 125°C		60	99	
ENABLE INPUT EN							
	EN terminal turn on threshold	Input rising				1.9	V
	EN terminal turn off threshold	Input falling		0.6			V
	Hyesteresis				330 (2)		mV
I_{EN}	Leakage current	V_{EN} = 0 V or 5.5 V		–2		2	µA
DISCHARGE							
R_{DCHG}	OUT Discharge Resistance	V_{OUT} = 5 V, V_{EN} = 0 V			480	625	Ω
CURRENT LIMIT							
I_{OS}	Current - limit, See Figure 13	R_{ILIM} = 33 kΩ		2773	2952	3127	mA
		R_{ILIM} = 40.2 kΩ		2270	2423	2570	
		R_{ILIM} = 56 kΩ		1620	1740	1860	
		R_{ILIM} = 80.6 kΩ		1110	1206	1300	
		R_{ILIM} = 150 kΩ		590	647	710	
		R_{ILIM} = 1100 kΩ		40	83	130	
OVERVOLTAGE LOCKOUT, IN							
$V_{(OVLO)}$	IN rising OVLO threshold voltage	IN rising		6.8	7.6	8.45	V
	Hysteresis				70 (2)		mV
VOLTAGE CLAMP, OUT							
$V_{(OVC)}$	OUT clamp voltage threshold	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 6.5V		5.25	5.4	5.55	V
SUPPLY CURRENT							
$I_{IN(off)}$	Supply current, low-level output	V_{EN} = 0 V, V_{IN} = 5 V			0.8	5	µA
		V_{EN} = 0 or 5 V, V_{IN} = 20 V			1000	1700	
$I_{IN(on)}$	Supply current, high-level output	V_{IN} = 5 V, No load on OUT	R_{ILIM} = 33 kΩ		143	200	µA
			R_{ILIM} = 150 kΩ		134	190	
I_{REV}	Reverse leakage current	V_{OUT} = 6.5V, V_{IN} = V_{EN} = 0 V, T_J = 25°C, Measure I_{OUT}			3.0	5	µA
UNDERVOLTAGE LOCKOUT, IN							
V_{UVLO}	IN rising UVLO threshold voltage	IN rising			2.35	2.45	V
	Hysteresis				30 (2)		mV
$\overline{\text{FAULT}}$ FLAG							
V_{OL}	Output low voltage, $\overline{\text{FAULT}}$	$I_{\overline{FAULT}}$ = 1 mA			50	180	mV
	Off-state leakage	$V_{\overline{FAULT}}$ = 6.5 V				1	µA
THERMAL SHUTDOWN							
	Thermal shutdown threshold, OTSD2			155			°C
	Thermal shutdown threshold only in current-limit, OTSD1			135			
	Hysteresis				20 (2)		

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.
(2) These parameters are provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

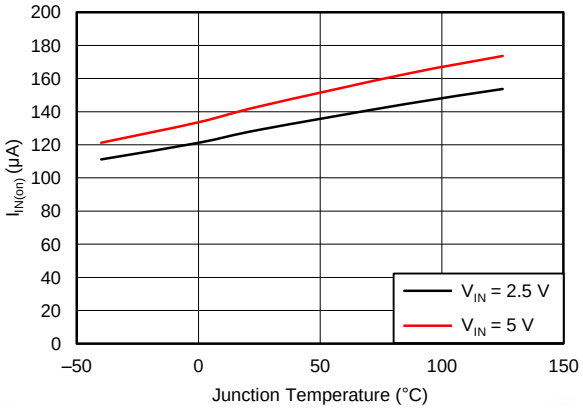
7.6 Timing Characteristics

Conditions are –40°C ≤ T_J ≤ 125°C and 2.5 V ≤ V_{IN} ≤ 6.5 V. V_{EN} = V_{IN}, R_{ILIM} = 33kΩ. Positive current are into terminals. Typical value is at 25°C. All voltages are with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
t_r	OUT voltage rise time	C_L = 1 µF, R_L = 100 Ω, (see Figure 11)		2.05	3.2	ms
t_f	OUT voltage fall time			0.18	0.2	ms
ENABLE INPUT EN						
t_{on}	Turn-on time	2.5 V ≤ V_{IN} ≤ 5 V, C_L = 1 µF, R_L = 100 Ω, (see Figure 11)		5.12	7.3	ms
t_{off}	Turn-off time			0.22	0.3	ms
CURRENT LIMIT						
$t_{(IOS)}$	Short-circuit response time	V_{IN} = 5 V (see Figure 13)		3.5 (1)		µs
OVERVOLTAGE LOCKOUT, IN						
$t_{(OVLO\_off\_delay)}$	Turn-Off Delay for OVLO	V_{IN} 5 V to 10 V with 1 V/µs ramp up rate, V_{OUT} with 100Ω load		0.6 (1)		µs
$\overline{\text{FAULT}}$ FLAG						
	$\overline{\text{FAULT}}$ deglitch	$\overline{\text{FAULT}}$ assertion or de-assertion due to overcurrent condition	5	8	12	ms

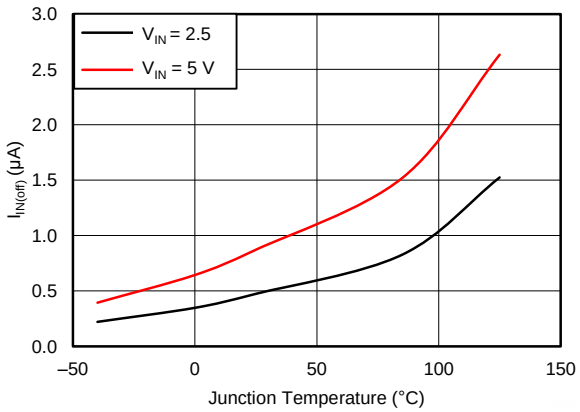
(1) This parameter is provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

7.7 Typical Characteristics



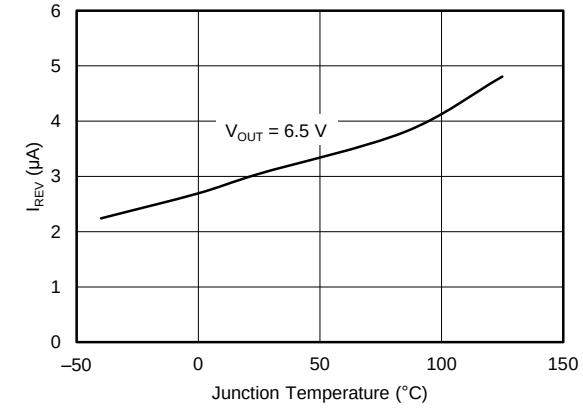
R_{ILIM} = 33 KΩ

Figure 2. $I_{IN(on)}$ vs Junction Temperature



R_{ILIM} = 33 KΩ

Figure 3. $I_{IN(off)}$ vs Junction Temperature



V_{EN} = V_{IN} = 0 V

Figure 4. I_{REV} vs Junction Temperature

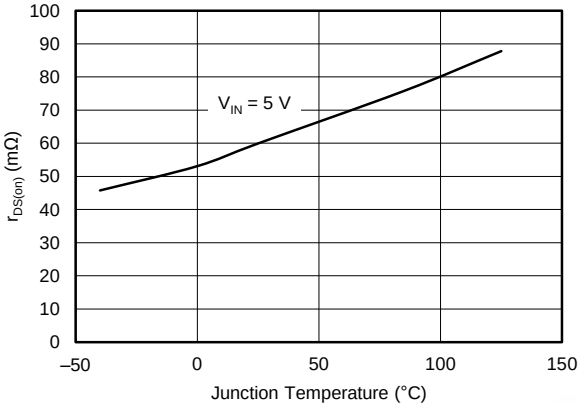
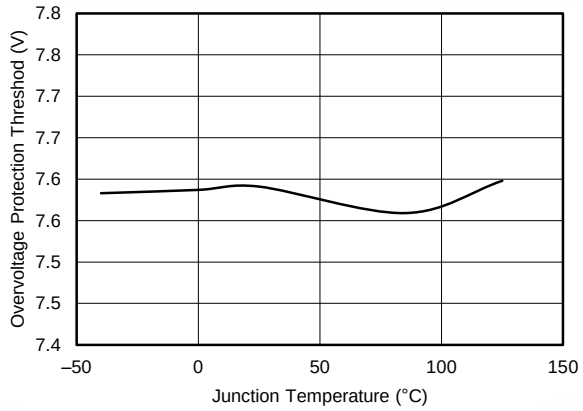
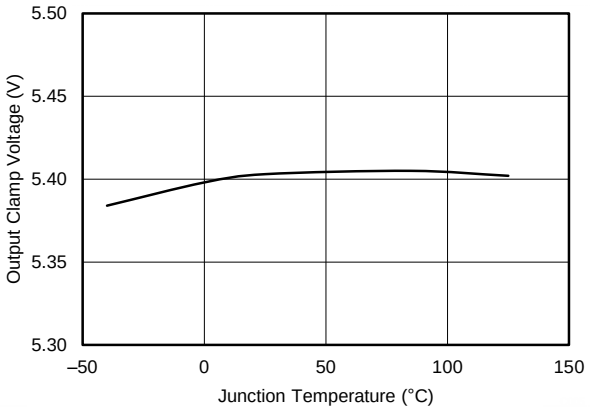


Figure 5. $r_{DS(ON)}$ vs Junction Temperature



V_{EN} = V_{IN} = 0 V

Figure 6. $V_{(OVLO)}$ vs Junction Temperature



C_L = 1µF R_L = 100 Ω V_{IN} = 6.5 V

Figure 7. $V_{O(VC)}$ vs Junction Temperature

Typical Characteristics (continued)

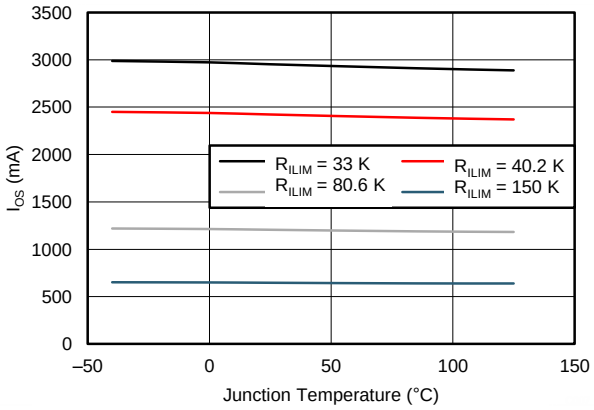


Figure 8. I_{OS} vs Junction Temperature

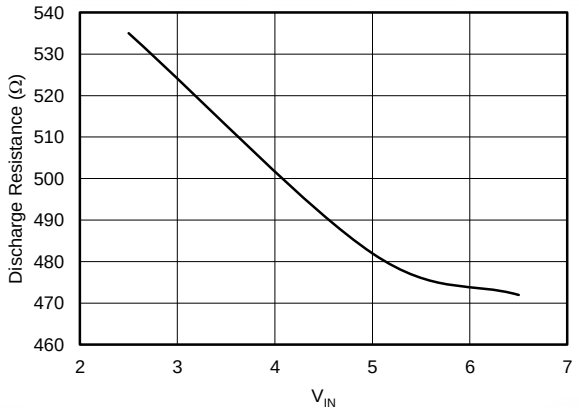


Figure 9. Discharge Resistance vs V_{IN}

8 Parameter Measurement Information

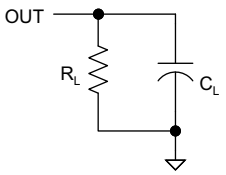


Figure 10. Output Rise/Fall Test Load

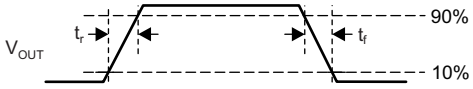


Figure 11. Power-On and Off Timing

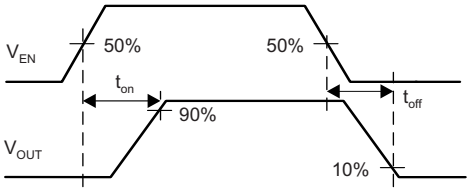


Figure 12. Enable Timing, Active High Enable

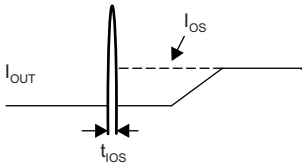


Figure 13. Output Short Circuit Parameters

9 Detailed Description

9.1 Overview

The TPS25200 is an intelligent low voltage switch or e-Fuse with robust overcurrent and overvoltage protection which are suitable for a variety of applications.

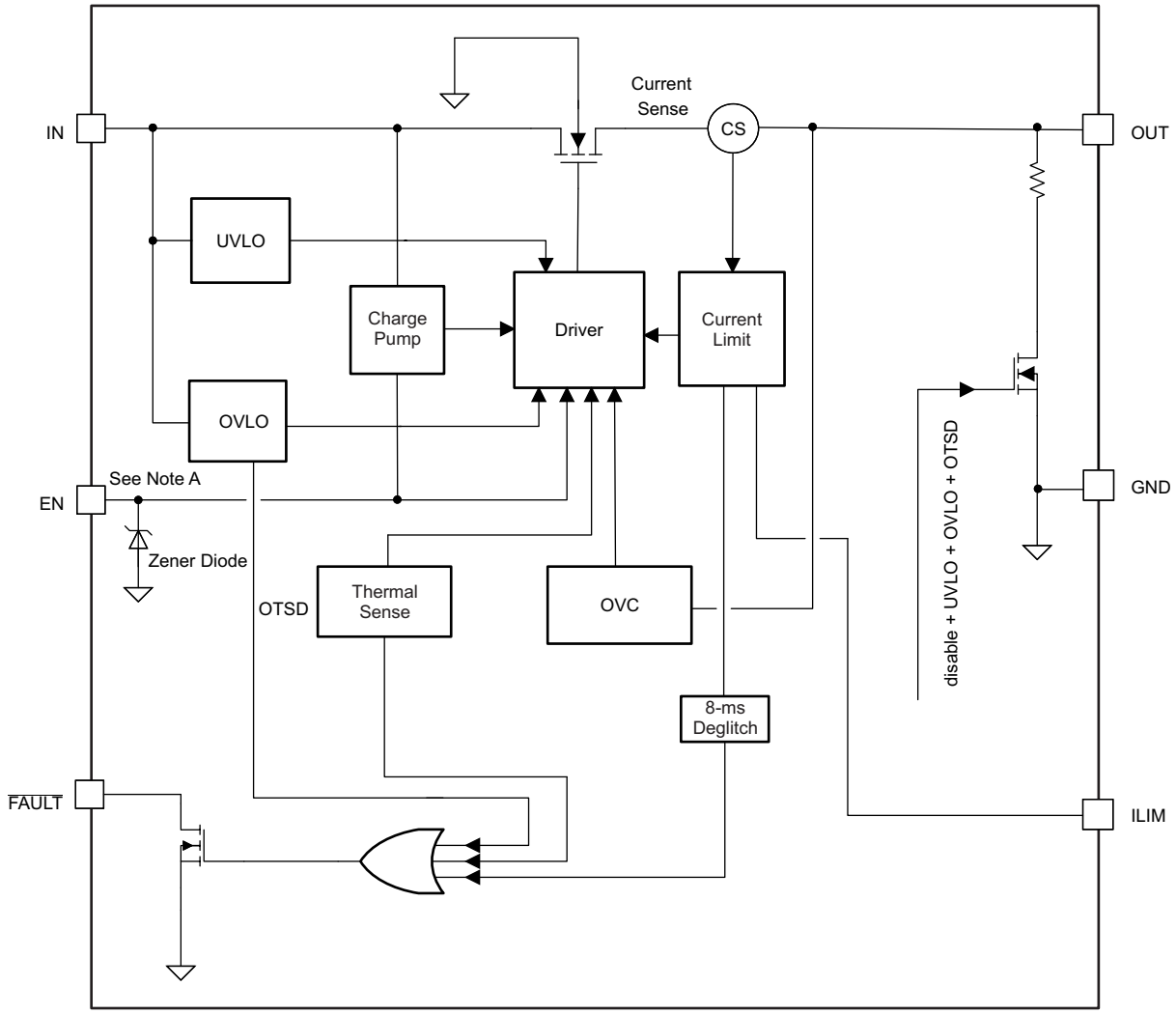
The TPS25200 current limited power switch uses N-channel MOSFETs in applications requiring up to 2.5 A of continuous load current. The device allows the user to program the current-limit threshold between 85 mA and 2.9 A (typ.) via an external resistor. The device enters constant-current mode when the load exceeds the current-limit threshold.

The TPS25200 Input can withstand 20 V DC voltage, but clamps V_{OUT} to a precision regulated 5.4 V and shuts down in the event V_{IN} exceeds 7.6 V. The device also integrates overcurrent and short circuit protection. The precision overcurrent limit helps to minimize over design of the input power supply while the fast response short circuit protection isolates the load when a short circuit is detected.

The additional features include:

- Enable the device can be put into a sleep mode for portable applications.
- Overtemperature protection to safely shutdown in the event of an overcurrent event or a slight overvoltage event where the V_{OUT} clamp is engaged over and extended period of time.
- Deglitched fault reporting to filter the Fault signal to ensure TPS25200 do not provide false fault alerts.
- Output discharge pull-down to help ensue a load is in fact off and not in some undefined operational state.
- Reverse blocking when disabled to prevent back-drive from an active load inadvertently causing undetermined behavior in the application.

9.2 Functional Block Diagram



A. 6.4 V typical clamp voltage

9.3 Feature Description

9.3.1 Enable

This logic enable input controls the power switch and device supply current. A logic high input on EN enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

EN can be tied to V_{IN} with a pull up resistor, and is protected with an integrated zener diode.Use a sufficiently large (300k) pull up resistor to ensure that the $V_{(EN)}$ is limited below the absolute maximum rating.

9.3.2 Thermal Sense

The TPS25200 self protects by using two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. The TPS25200 device operates in constant-current mode during an overcurrent condition, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor (OTSD1) turns off the power switch when the die temperature exceeds 135°C (min) and the part is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20°C.

Feature Description (continued)

The TPS25200 also has a second ambient thermal sensor (OTSD2). The ambient thermal sensor turns off the power switch when the die temperature exceeds 155°C (min) regardless of whether the power switch is in current limit and will turn on the power switch after the device has cooled approximately 20°C. The TPS25200 continues to cycle off and on until the fault is removed.

9.3.3 Overcurrent Protection

The TPS25200 will thermally protect itself by thermal cycling during an extended overcurrent condition. The device turns off when the junction temperature exceeds 135°C (typ) while in current limit. The device remains off until the junction temperature cools 20°C (typ) and then restarts. The TPS25200 cycles on/off until the overload is removed (see Figure 27 and Figure 30).

The TPS25200 responds to an overcurrent condition by limiting their output current to the I_{OS} levels shown in Figure 13. When an overcurrent condition is detected, the device maintains a constant output current and the output voltage is reduced accordingly. During an over current event, two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS25200 ramps the output current to I_{OS}. The TPS25200 devices will limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time t_{IOS} (see Figure 13). The current-sense amplifier is overdriven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier recovers and limits the output current to I_{OS}. Similar to the previous case, the TPS25200 will limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

9.3.4 $\overline{\text{FAULT}}$ Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an overcurrent, overtemperature or overvoltage condition. The TPS25200 asserts the $\overline{\text{FAULT}}$ signal until the fault condition is removed and the device resumes normal operation. The TPS25200 is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal delay "deglitch" circuit for overcurrent (8-ms typical) conditions without the need for external circuitry. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving current-limit induced fault conditions.

The $\overline{\text{FAULT}}$ signal is not deglitched when the MOSFET is disabled due to an overtemperature condition but is deglitched after the device has cooled and begins to turn on. This unidirectional deglitch prevents $\overline{\text{FAULT}}$ oscillation during an overtemperature event.

The $\overline{\text{FAULT}}$ signal is not deglitched when the MOSFET is disabled into OVLO or out of OVLO. The TPS25200 does not assert the $\overline{\text{FAULT}}$ during output voltage clamp mode.

Connect $\overline{\text{FAULT}}$ with a pull up resistor to a low voltage I/O rail.

9.3.5 Output Discharge

A 480 Ω (typical) output discharge will dissipate stored charge and leakage current on OUT when the TPS25200 is in UVLO, disabled or OVLO. The pull down capability decreases as V_{IN} decreases (Figure 9).

9.4 Device Functional Modes

TPS25200 V_{IN} can withstand up to 20 V. Within 0 V to 20 V range, it can be divided to four modes.

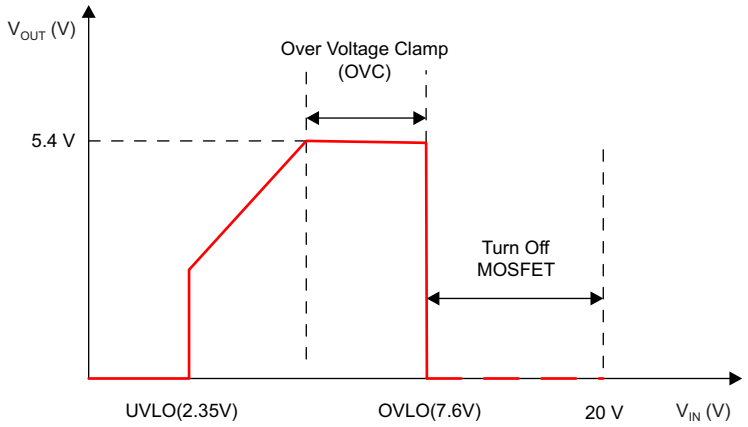


Figure 14. Output vs Input Voltage

9.4.1 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage droop during turn on.

9.4.2 Overcurrent Protection (OCP)

When 2.35 V < V_{IN} < 5.4 V, TPS25200 is a traditional power switch, providing overcurrent protection.

9.4.3 Overvoltage Clamp (OVC)

When 5.4 V < V_{IN} < 7.6 V, the overvoltage clamp (OVC) circuit clamps the output voltage to 5.4 V. Within this V_{IN} range, the overcurrent protection remains active.

9.4.4 Overvoltage Lockout (OVLO)

When V_{IN} exceeds 7.6 V, the overvoltage lockout (OVLO) circuit turns off the protected power switch.

10 Applications and Implementation

10.1 Application Information

The TPS25200 is a 5V eFuse with precision current limit and over-voltage clamp. When a slave device such as a mobile data-card device is hot plugged into a USB port as shown in Figure 15, an input transient voltage could damage the slave device due to the cable inductance. Placing TPS25200 at the input of mobile device as over-voltage and overcurrent protector can safeguard these slave devices. Input transients also occur when the current through the cable parasitic inductance changes abruptly. This can occur when the TPS25200 turns off the internal MOSFET in response to an overvoltage or overcurrent event. The TPS25200 can withstand the transient without a bypass bulk capacitor, or other external overvoltage protection components at input side. TPS25200 also can be used at host side as a traditional power switch pin-to-pin compatible with TPS2553.

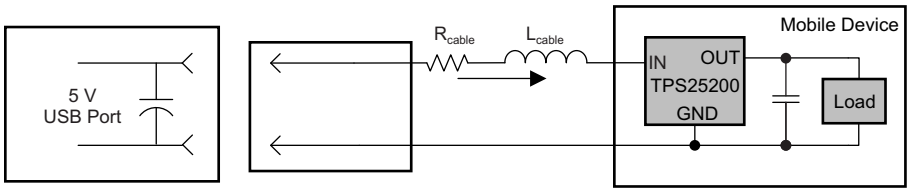


Figure 15. Hot Plug Into 5V USB port with Parasitic Cable Resistance and Inductance

10.2 Typical Application

10.2.1 Overvoltage and Overcurrent Protector

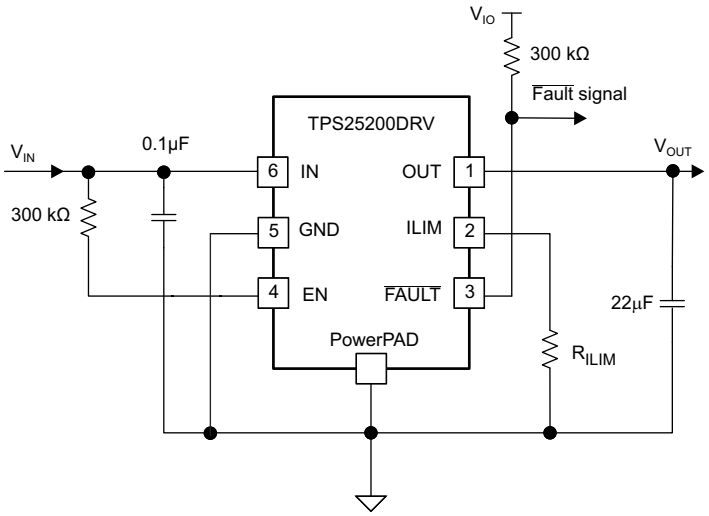


Figure 16. Typical Application Schematic

Use the I_{OS} in the Electrical Characteristics table or I_{OS} in the Equation 1 to select the R_{ILIM}.

10.2.1.1 Design Requirements

For this design example, use the following as the input parameters.

DESIGN PARAMETERS	EXAMPLE VALUE
Normal Input Operation Voltage	5 V
Output Transient Voltage	6.5 V
Minimum Current Limit	2.1 A
Maximum Currnt Limit	2.9 A

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Step by Step Design Produce

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Normal Input Operation Voltage
- Output transient voltage
- Minimum Current Limit
- Maximum Current Limit

10.2.1.2.2 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.1 µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.

When V_{IN} ramp up exceed 7.6 V, V_{OUT} will follow V_{IN} until TPS25200 turns off the internal MOSFET after $t_{(OVLO\_off\_delay)}$. Since $t_{(OVLO\_off\_delay)}$ largely depends on the V_{IN} ramp rate, V_{OUT} will see some peak voltage. Increasing the output capacitance can lower the output peak voltage as shown in Figure 17.

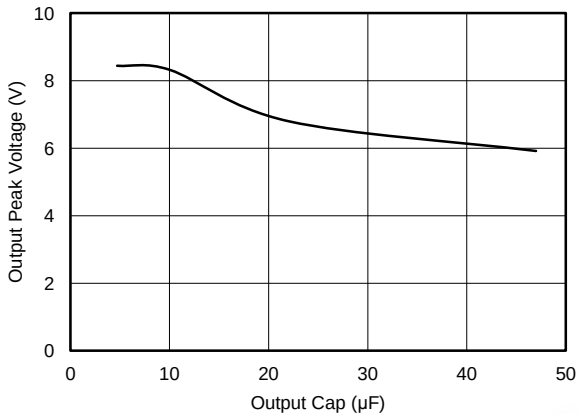


Figure 17. V_{OUT} Peak Voltage vs C_{OUT} (V_{IN} Step From 5 V to 15 V with 1V/us Ramp Up Rate)

10.2.1.2.3 Programming the Current-Limit Threshold

The overcurrent threshold is user programmable via an external resistor. The TPS25200 uses an internal regulation loop to provide a regulated voltage on the ILIM terminal. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for R_{ILIM} is 33 kΩ ≤ R_{ILIM} ≤ 1100 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIM}. The following equations approximate the resulting overcurrent threshold for a given external resistor value R_{ILIM}. Consult the Electrical Characteristics table for specific current limit settings. The traces routing the R_{ILIM} resistor to the TPS25200 should be as short as possible to reduce parasitic effects on the current-limit accuracy.

R_{ILIM} can be selected to provide a current-limit threshold that occurs 1) above a minimum load current or 2) below a maximum load current.

To design above a minimum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(min)}$ curve and choose a value of R_{ILIM} below this value. Programming the current limit above a minimum threshold is important to ensure start up into full load or heavy capacitive loads. The resulting maximum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{OS(max)}$ curve.

To design below a maximum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(max)}$ curve and choose a value of R_{ILIM} above this value. Programming the current limit below a maximum threshold is important to avoid current limiting upstream power supplies causing the input voltage bus to droop. The resulting minimum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{OS(min)}$ curve.

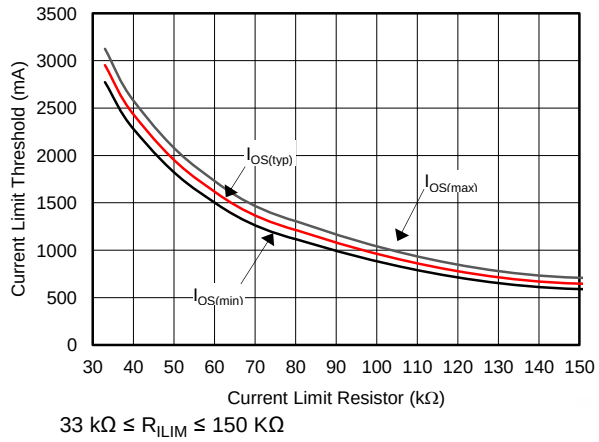
Current-Limit Threshold Equations (I_{OS}):

$$I_{OSmax}(mA) = \frac{96754V}{R_{ILIM}0.985_{k\Omega}} + 30$$

$$I_{OSnom}(mA) = \frac{98322V}{R_{ILIM}1.003k\Omega}$$

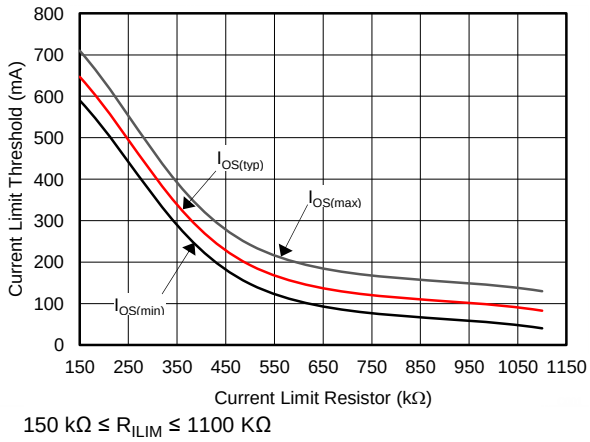
$$I_{OSmin}(mA) = \frac{97399}{R_{ILIM}1.015_{k\Omega}} - 30 \quad (1)$$

Where 33kΩ ≤ R_{ILIM} ≤ 1100kΩ.



33 kΩ ≤ R_{ILIM} ≤ 150 KΩ

Figure 18. Current-Limit Threshold vs R_{ILIM} I



150 kΩ ≤ R_{ILIM} ≤ 1100 KΩ

Figure 19. Current-Limit Threshold vs R_{ILIM} II

10.2.1.2.4 Design Above a Minimum Current Limit

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 2.1 A must be delivered to the load so that the minimum desired current-limit threshold is 2100 mA. Use the I_{OS} equations and Figure 18 to select R_{ILIM}.

$$I_{OS\,min}(mA) = 2100\ mA$$

$$I_{OS\,min}(mA) = \frac{97399V}{R_{ILIM}{}^{1.015}k\Omega} - 30$$

$$R_{ILIM}(k\Omega) = \left(\frac{97399}{I_{OS(min)} + 30}\right)^{\frac{1}{1.015}} = \left(\frac{97399}{2100 + 30}\right)^{\frac{1}{1.015}} = 43.22\ k\Omega \quad (2)$$

Select the closest 1% resistor less than the calculated value: R_{ILIM} = 42.2 kΩ. This sets the minimum current-limit threshold at 2130 mA.

$$I_{OS\,min}(mA) = \frac{97399V}{R_{ILIM}{}^{1.015}k\Omega} - 30 = \frac{97399}{(42.2\ x\ 1.01)^{1.015}} - 30 = 2130mA \quad (3)$$

Use the I_{OS} equations, Figure 18, and the previously calculated value for R_{ILIM} to calculate the maximum resulting current-limit threshold.

$$I_{OS\,max}(mA) = \frac{96754}{R_{ILIM}{}^{0.985}} + 30$$

$$I_{OS\,max}(mA) = \frac{96754}{(42.2 \times 0.99)^{0.985}} + 30 = 2479\ mA \quad (4)$$

The resulting current-limit threshold minimum is 2130 mA and maximum is 2479 mA with R_{ILIM} = 42.2kΩ ± 1%.

10.2.1.2.5 Design Below a Maximum Current Limit

Some applications require that current limiting must occur below a certain threshold. For this example, assume that 2.9 A must be delivered to the load so that the minimum desired current-limit threshold is 2900 mA. Use the I_{OS} equations and Figure 19 to select R_{ILIM}.

$$I_{OS\,max}(mA) = 2900mA$$

$$I_{OS\,max}(mA) = \frac{96754}{R_{ILIM}{}^{0.985}k\Omega} + 30$$

$$R_{ILIM}(k\Omega) = \left(\frac{96754}{I_{OS(max)} - 30}\right)^{\frac{1}{0.985}} = \left(\frac{96754}{2900 - 30}\right)^{\frac{1}{0.985}} = 35.57\ k\Omega \quad (5)$$

Select the closest 1% resistor greater than the calculated value: R_{ILIM} = 36 kΩ. This sets the maximum current-limit threshold at 2894 mA.

$$I_{OS\,max}(mA) = \frac{96754V}{R_{ILIM}{}^{0.985}k\Omega} + 30 = \frac{96754}{(36\ x\ 0.99)^{0.985}} + 30 = 2894mA \quad (6)$$

Use the I_{OS} equations, Figure 19, and the previously calculated value for R_{ILIM} to calculate the minimum resulting current-limit threshold.

$$I_{OS\,min}(mA) = \frac{97399}{R_{ILIM}{}^{1.015}} - 30$$

$$I_{OS\,min}(mA) = \frac{97399}{(36 \times 1.01)^{1.015}} - 30 = 2508mA \quad (7)$$

The resulting minimum current-limit threshold minimum is 2592 mA and maximum is 2894 mA with R_{ILIM} = 36kΩ ± 1%.

10.2.1.2.6 Power Dissipation and Junction Temperature

The low on-resistance of the internal N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph. When V_{IN} is lower than $V_{(OVC)}$, TPS2500 is an traditional power switch. Using this value, the power dissipation can be calculated by:

$$P_D = r_{DS(on)} \times I_{OUT}^2 \quad (8)$$

When V_{IN} exceed $V_{(OVC)}$, but lower than $V_{(OVLO)}$, TPS25200 clamp output to fixed $V_{(OVC)}$, the power dissipation can be calculated by:

$$P_D = (V_{IN} - V_{(OVC)}) \times I_{OUT}$$

where

- P_D = Total power dissipation (W)
- $r_{DS(on)}$ = Power switch on-resistance (Ω)
- $V_{(OVC)}$ = Overvoltage clamp voltage (V)
- I_{OUT} = Maximum current-limit threshold (A) (9)

This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature:

$$T_J = P_D \times \theta_{JA} + T_A$$

where

- T_A = Ambient temperature (°C)
- θ_{JA} = Thermal resistance (°C /W)
- P_D = Total power dissipation (W) (10)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined" $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance θ_{JA}, and thermal resistance is highly dependent on the individual package and board layout.

10.2.1.3 Application Curves

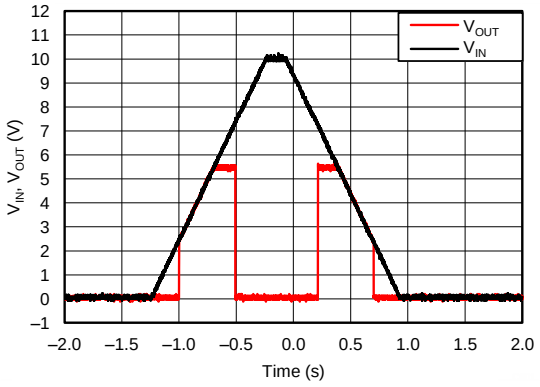


Figure 20. V_{OUT} vs V_{IN} (0 V to 10 V)

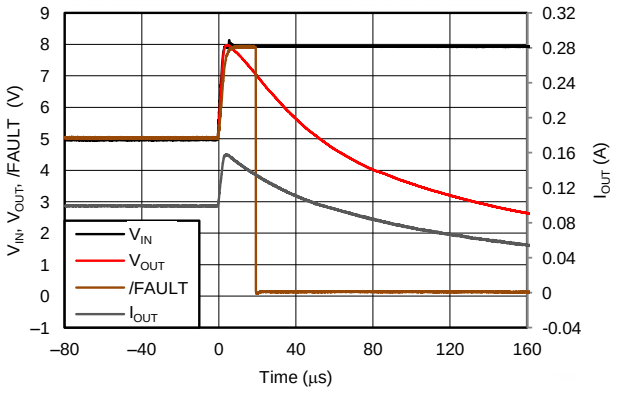


Figure 21. V_{IN} Step 5 V to 8 V With 4.7µF // 100Ω

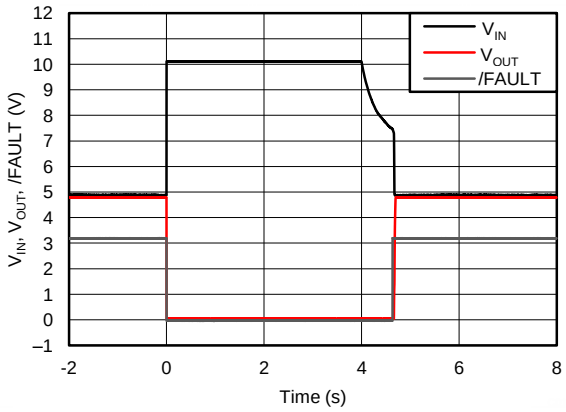


Figure 22. Pulse Overvoltage with 100Ω

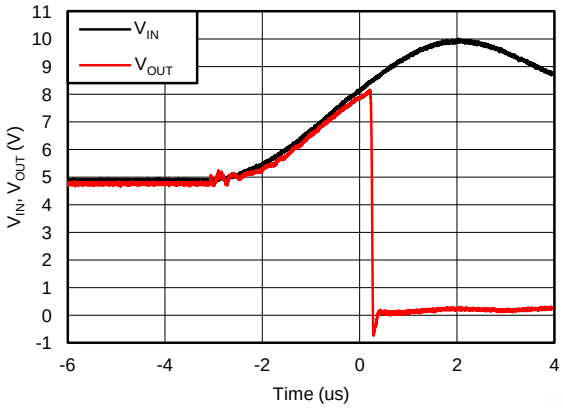


Figure 23. 5V to 10V OVLO Response Time

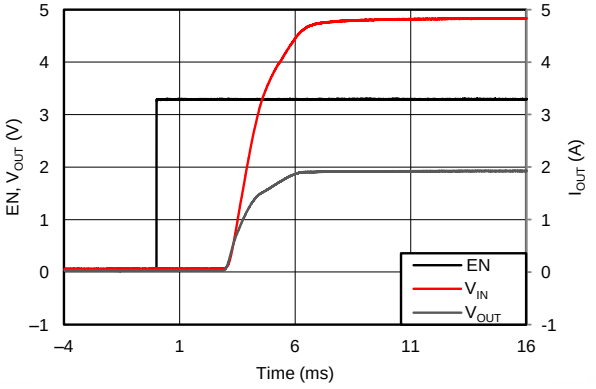


Figure 24. Turn On Delay and Rise Time 150µF || 2.5Ω

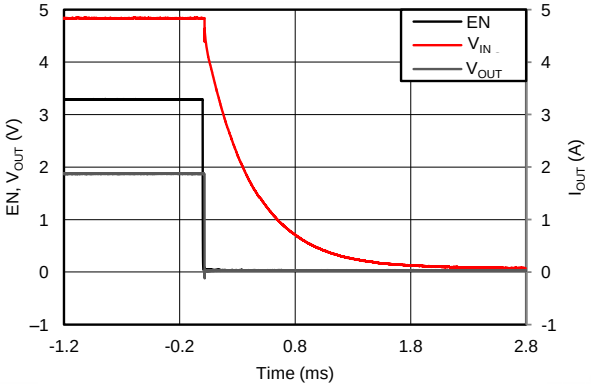


Figure 25. Turn Off Delay and Fall Time 150µF || 2.5Ω

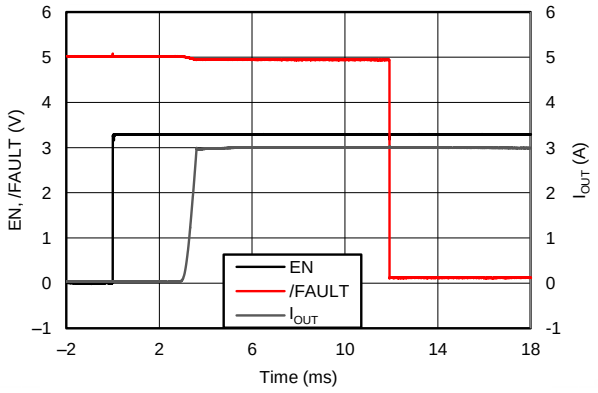


Figure 26. Enable into Output Short

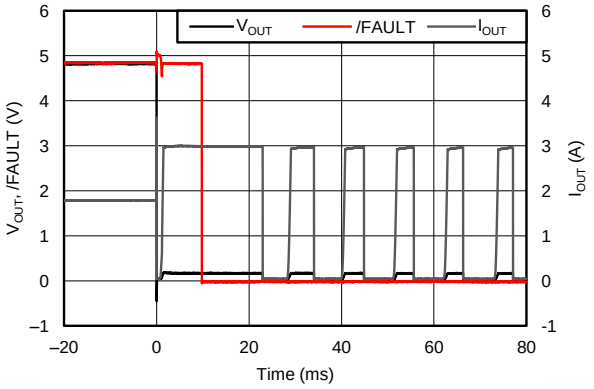


Figure 27. 2.5Ω to Output Short Transient Response

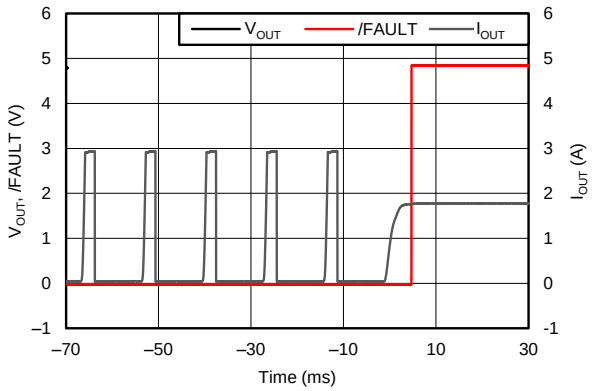


Figure 28. Output Short to 2.5Ω Load Recovery Response

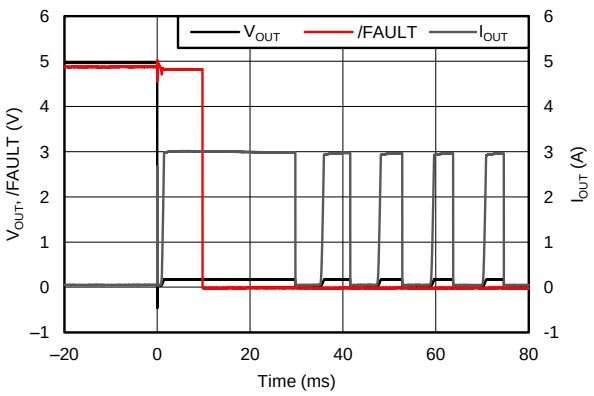


Figure 29. No Load to Output Short Transient Response

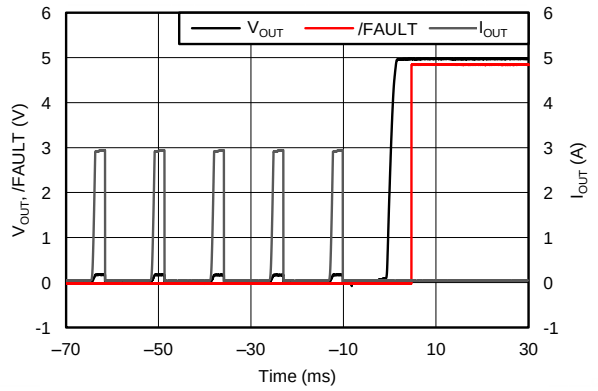


Figure 30. Output Short to No Load Recovery Response

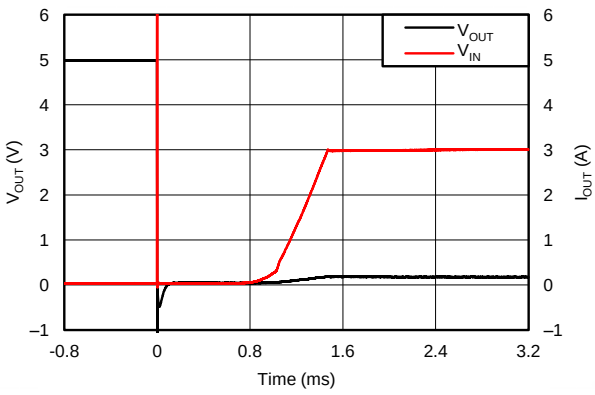


Figure 31. Hot-Short with 50mΩ

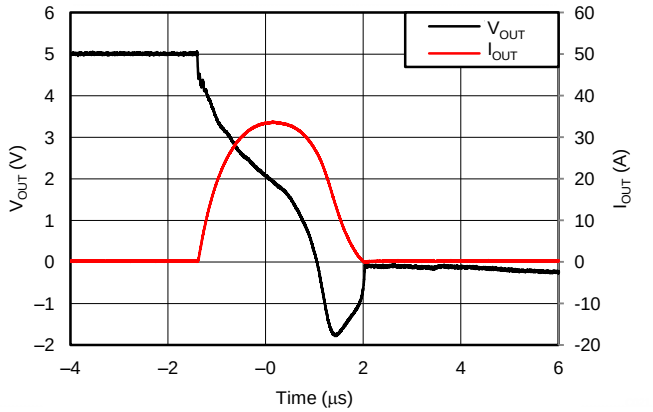


Figure 32. 50mΩ Hot-Short Response Time

11 Power Supply Recommendations

TPS25200 is designed for 2.7 V < V_{IN} < 5 V (typical) voltage rails. While there is a V_{OUT} clamp, it is not intended to be used to regulate V_{OUT} at ~5.4 V with 6 V < V_{IN} < 7 V. This is a protection feature only.

12 Layout

12.1 Layout Guidelines

- For all applications, a 0.1-µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.
- For output capacitance, refer to Figure 17, low ESR ceramic cap is recommended.
- The traces routing the R_{ILIM} resistor to the device should be as short as possible to reduce parasitic effects on the current limit accuracy.
- The PowerPAD should be directly connected to PCB ground plane using wide and short copper trace.

12.2 Layout Example

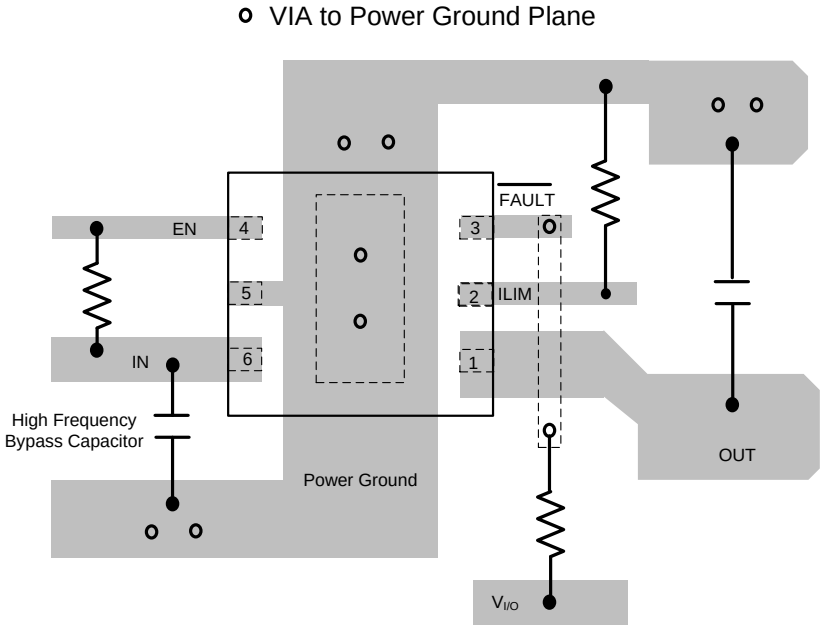


Figure 33. TPS25200 Board Layout

13 Device and Documentation Support

13.1 Trademarks

PowerPAD is a trademark of Texas Instruments.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS25200DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		SKB	Samples
TPS25200DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		SKB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

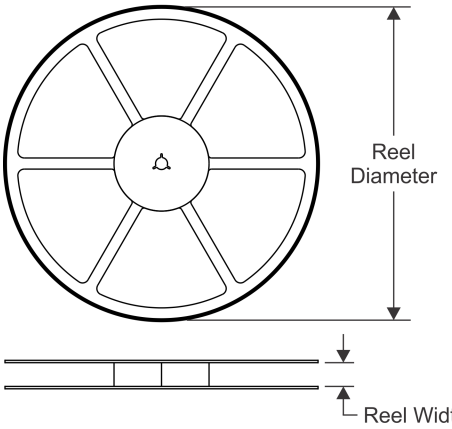
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

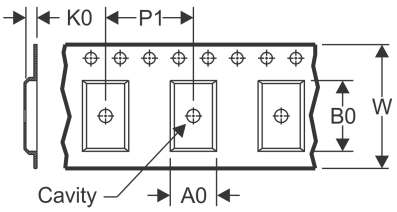
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

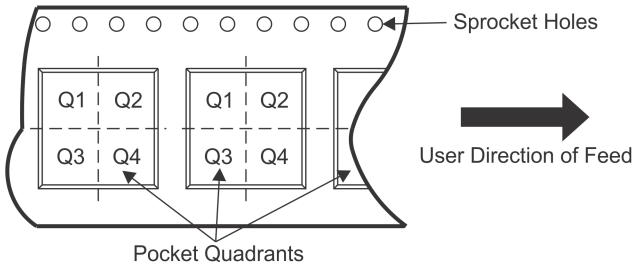


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

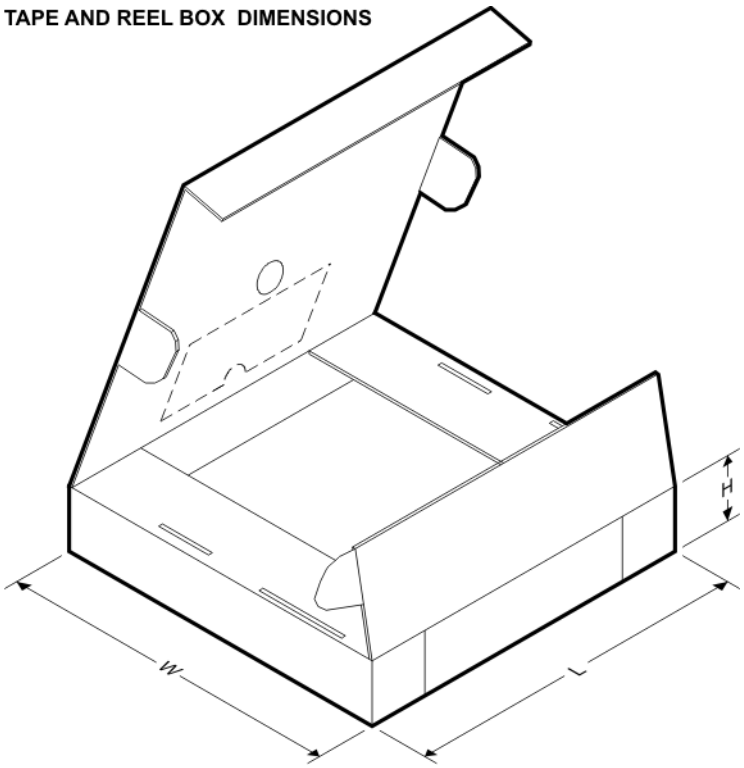
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25200DRVR	SON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS25200DRVT	SON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

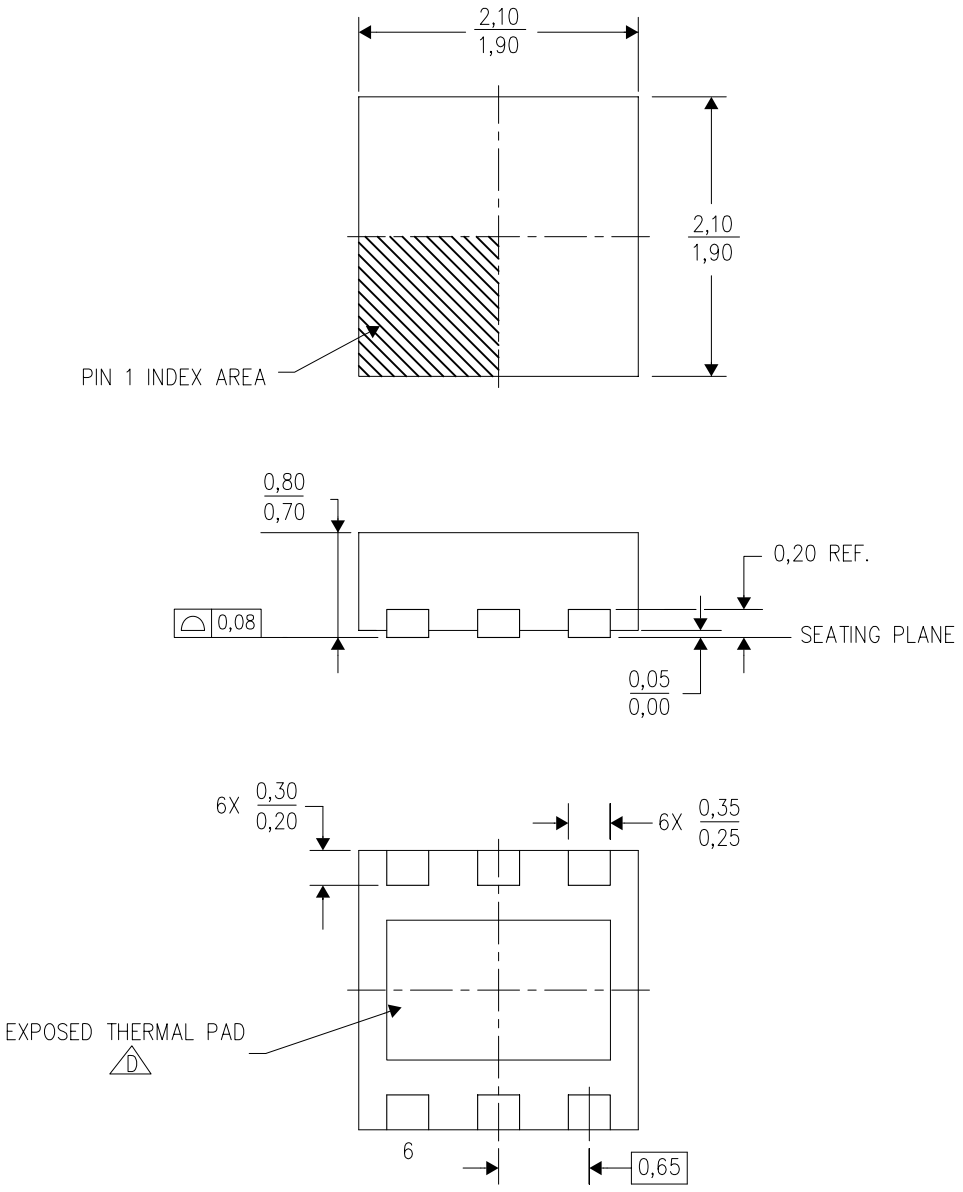
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25200DRVR	SON	DRV	6	3000	210.0	185.0	35.0
TPS25200DRVT	SON	DRV	6	250	210.0	185.0	35.0

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

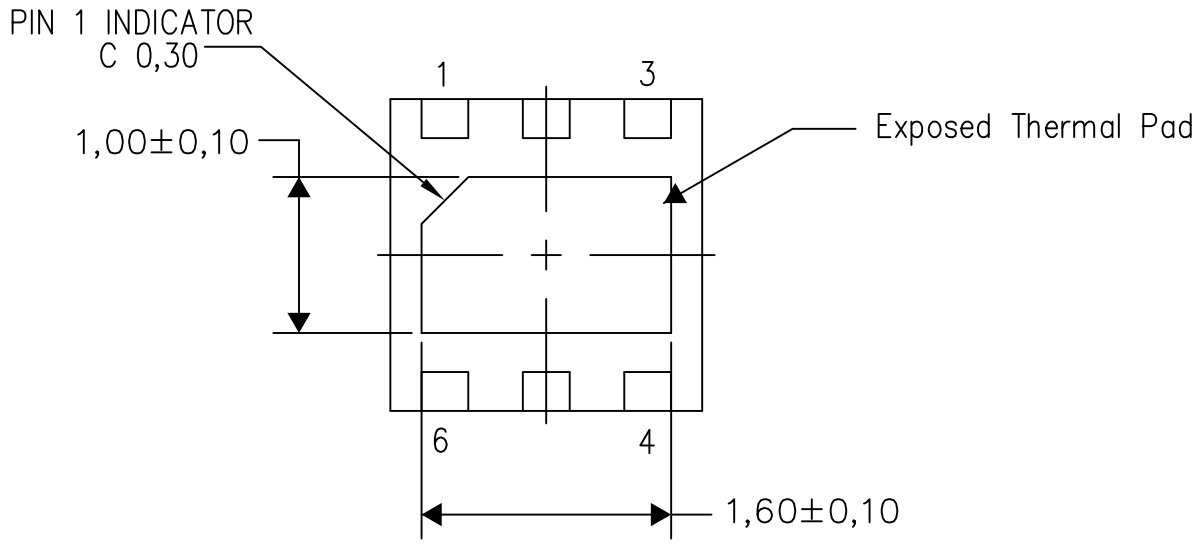
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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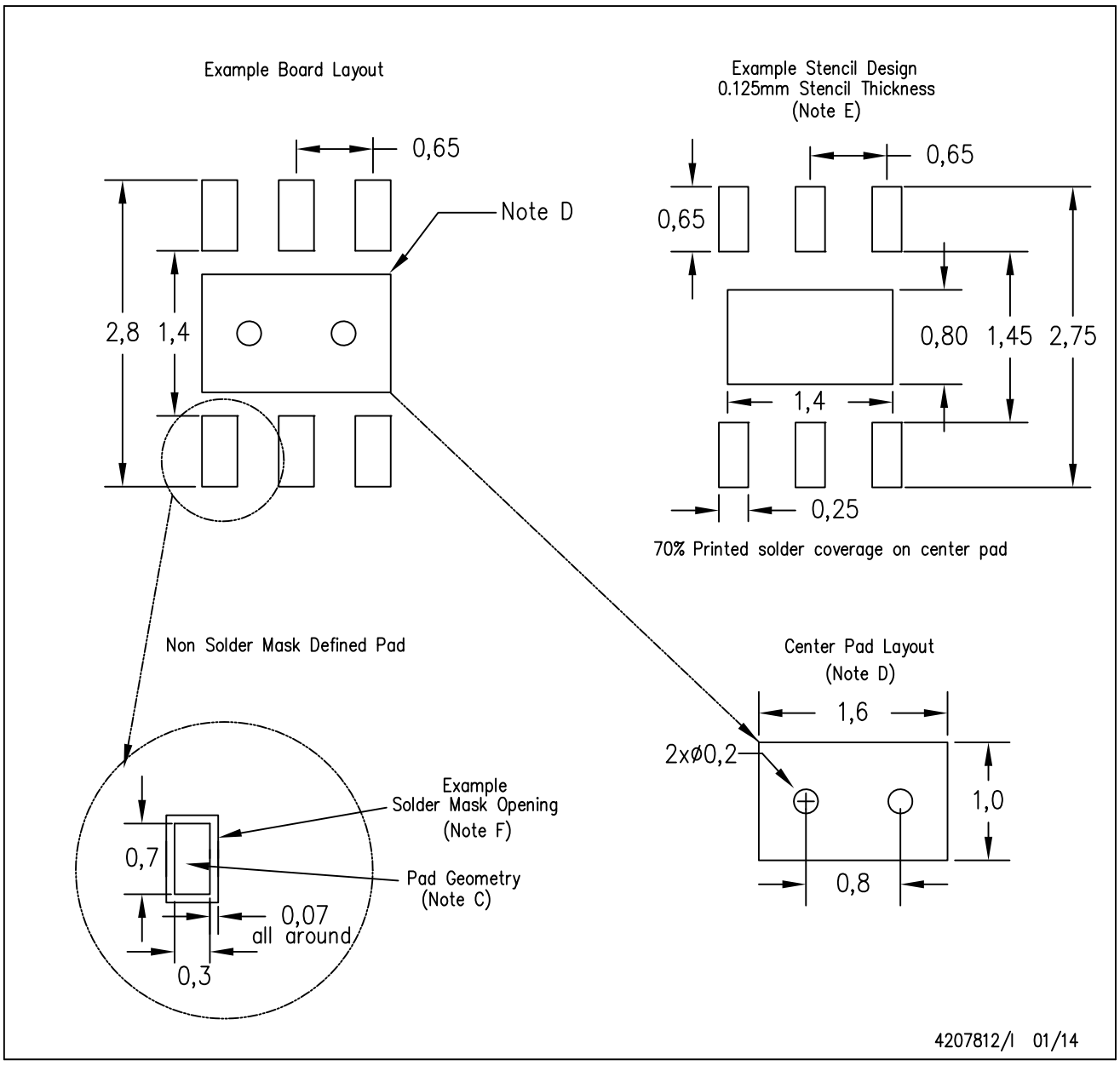
NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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