CYV15G0204TRB

Independent Clock HOTLink II™ Dual Serializer and Dual Reclocking Deserializer

Features

- Second-generation HOTLink® technology
- Compliant to SMPTE 292M and SMPTE 259M video standards
- Dual-channel video serializer plus dual channel video reclocking deserializer
  - 195- to 1500-Mbps serial data signaling rate
  - Simultaneous operation at different signaling rates
- Supports reception of either 1.485 or 1.485/1.001 Gbps data rate with the same training clock
- Supports half-rate and full-rate clocking
- Internal phase-locked loops (PLLs) with no external PLL components
- Selectable differential PECL-compatible serial inputs
  - Internal DC-restoration
- Redundant differential PECL-compatible serial outputs
  - No external bias resistors required
  - Signaling-rate controlled edge-rates
  - Internal source termination
- Synchronous LVTTL parallel interface
- JTAG boundary scan
- Built-In Self-Test (BIST) for at-speed link testing
- Link Quality Indicator
  - Analog signal detect
  - Digital signal detect
- Low-power 2.5 W at 3.3 V typical
- Single 3.3 V supply
- Thermally enhanced BGA
- Pb-free package option available
- 0.25 µ BiCMOS technology

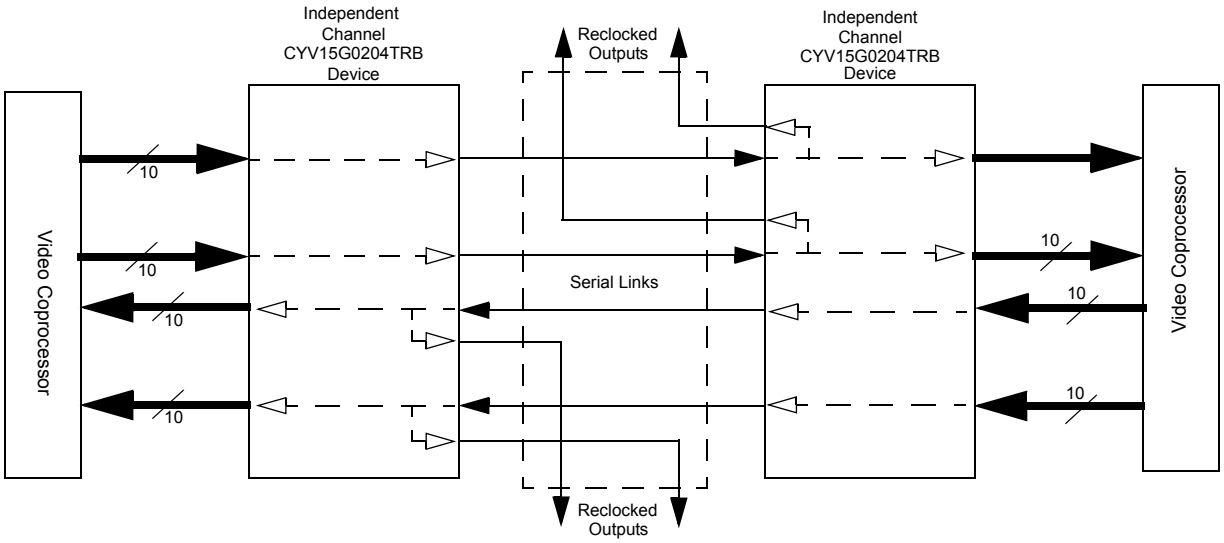
Functional Description

The CYV15G0204TRB Independent Clock HOTLink II™ Dual Serializer and Dual Reclocking Deserializer is a point-to-point or point-to-multipoint communications building block enabling transfer of data over a variety of high-speed serial links including SMPTE 292M and SMPTE 259M video applications. It supports signaling rates in the range of 195 to 1500 Mbps per serial link. All transmit and receive channels are independent and can operate simultaneously at different rates. Each transmit channel accepts 10-bit parallel characters in an Input Register and converts them to serial data. Each receive channel accepts serial data and converts it to 10-bit parallel characters and presents these characters to an Output Register. The received serial data can also be reclocked and retransmitted through the reclocker serial outputs. Figure 1 illustrates typical connections between independent video co-processors and corresponding CYV15G0204TRB chips.

The CYV15G0204TRB satisfies the SMPTE 259M and SMPTE 292M compliance as per SMPTE EG34-1999 Pathological Test Requirements.

As a second-generation HOTLink device, the CYV15G0204TRB extends the HOTLink family with enhanced levels of integration and faster data rates, while maintaining serial-link compatibility (data and BIST) with other HOTLink devices. Each transmit (TX) channel of the CYV15G0204TRB HOTLink II device accepts scrambled 10-bit transmission characters. These characters are serialized and output from dual Positive ECL (PECL) compatible differential transmission-line drivers at a bit-rate of either 10- or 20-times the input reference clock for that channel.

Figure 1. HOTLink II™ System Connections

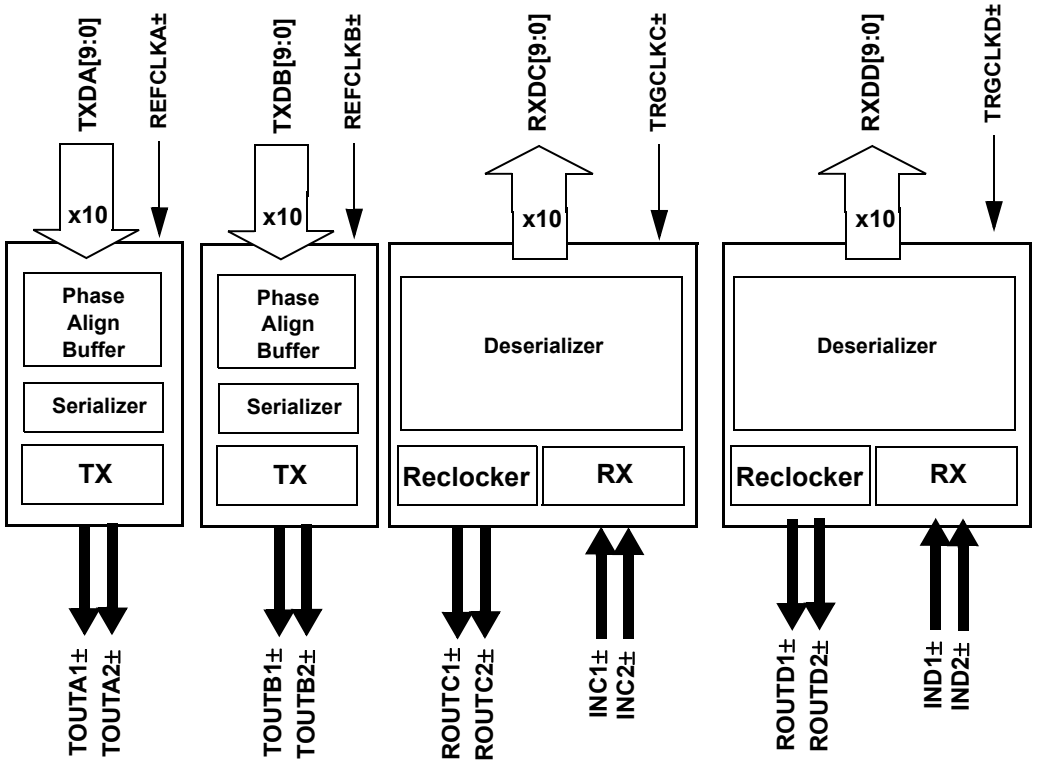


Each receive (RX) channel of the CYV15G0204TRB HOTLink II device accepts a serial bit-stream from one of two selectable PECL-compatible differential line receivers, and using a completely integrated Clock and Data Recovery PLL, recovers the timing information necessary for data reconstruction. The recovered bit-stream is reclocked and retransmitted through the reclocker serial outputs. Also, the recovered serial data is deserialized and presented to the destination host system.

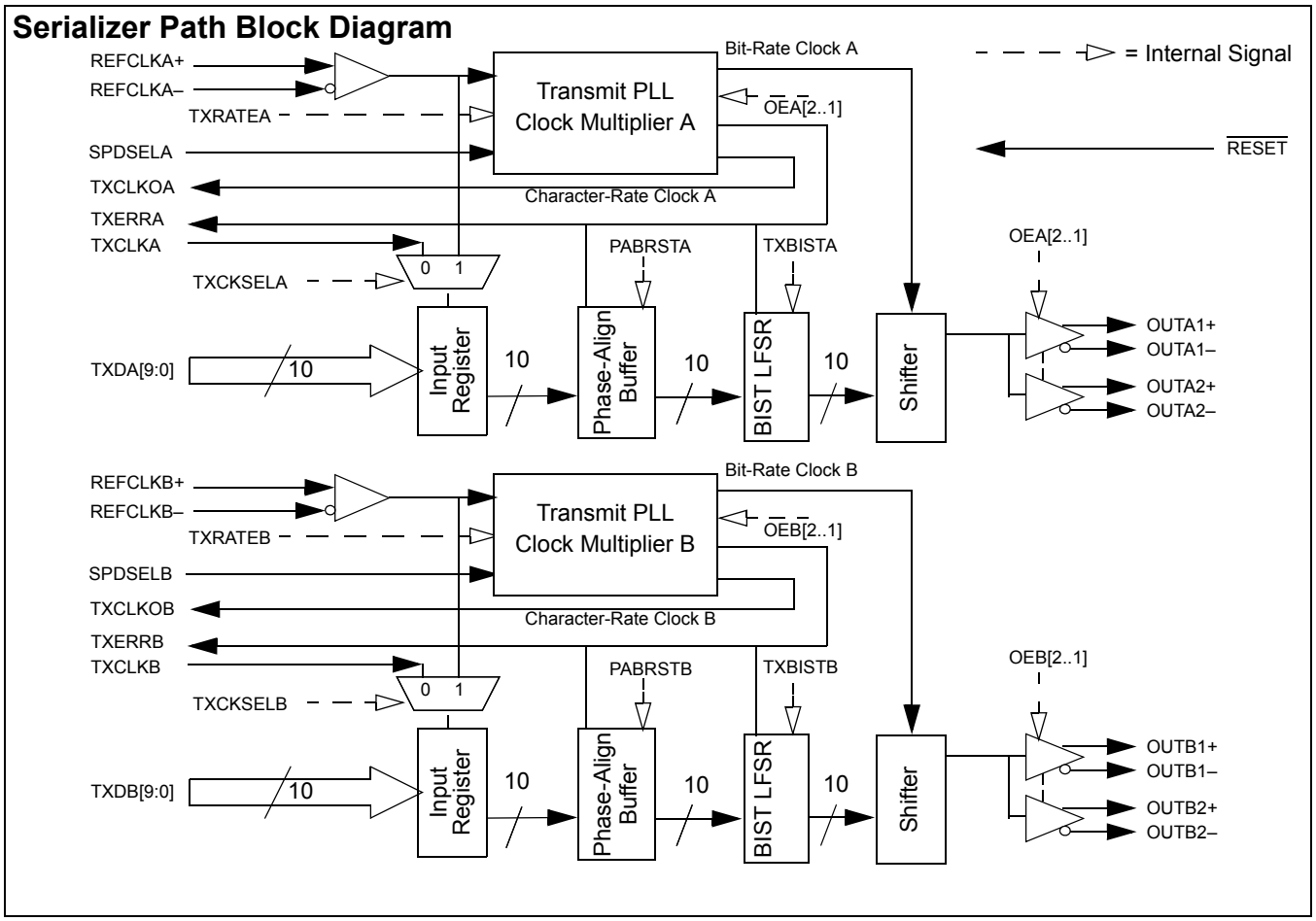
Each transmit and receive channel contains an independent BIST pattern generator and checker, respectively. This BIST hardware allows at-speed testing of the high-speed serial data paths in each transmit and receive section, and across the interconnecting links.

The CYV15G0204TRB is ideal for SMPTE applications where different data rates and serial interface standards are necessary for each channel. Some applications include multi-format routers, switchers, format converters, SDI monitors, cameras, and camera control units.

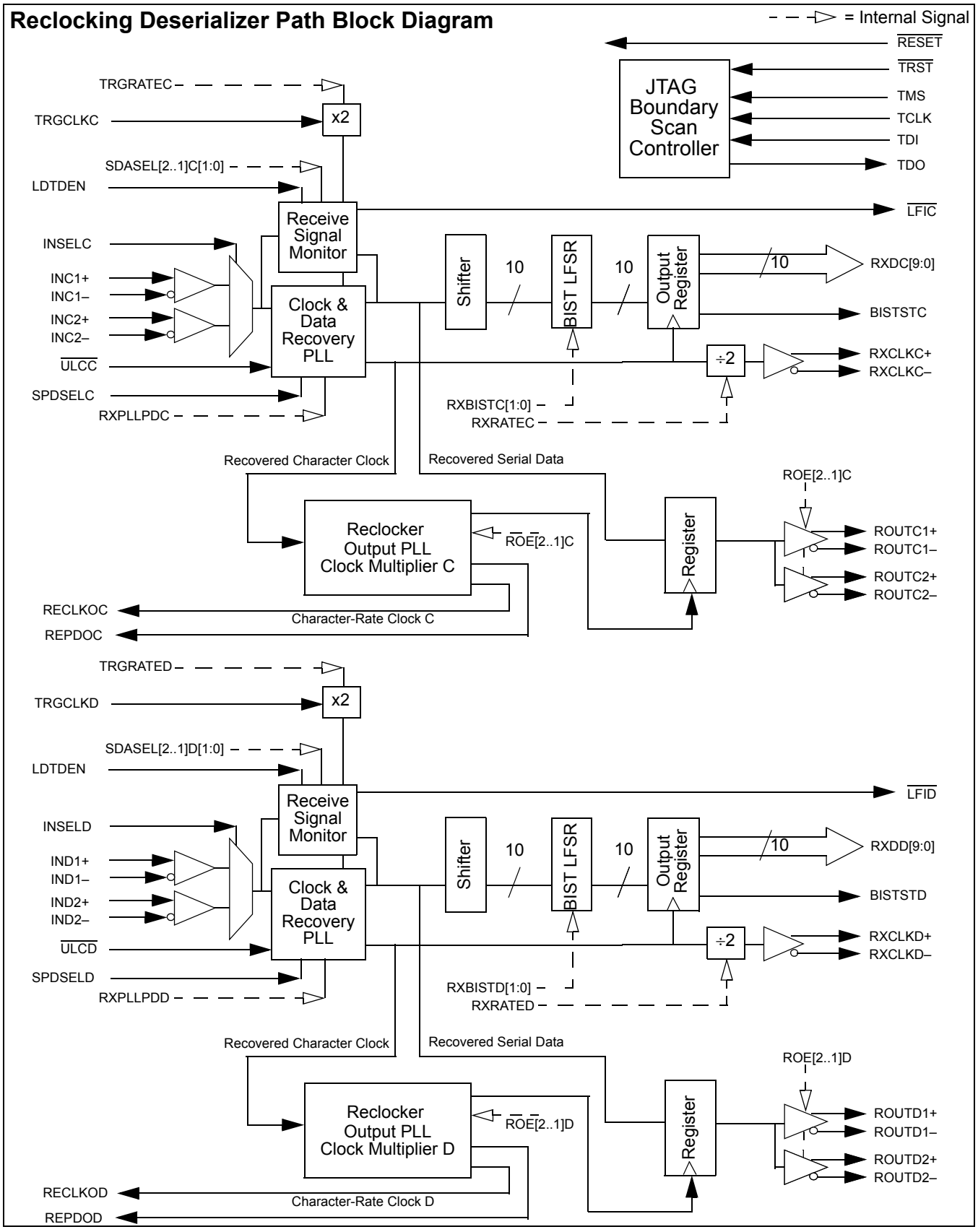
CYV15G0204TRB Logic Block Diagram



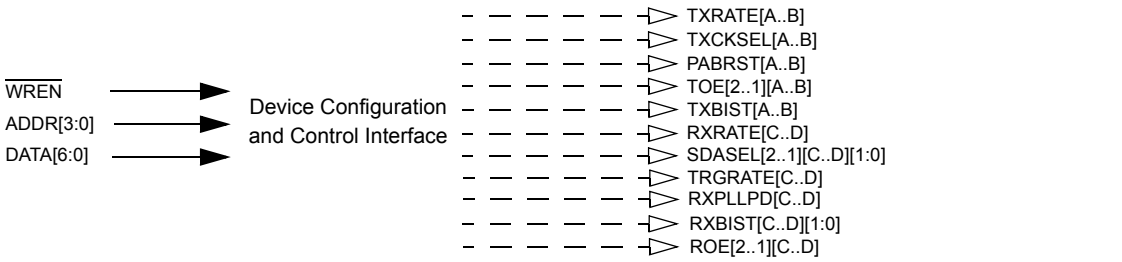
Serializer Path Block Diagram



Reclocking Deserializer Path Block Diagram



Device Configuration and Control Block Diagram



Contents

Pin Configuration (Top View)[1]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	IN C1–	ROUT C1–	IN C2–	ROUT C2–	V_{CC}	IN D1–	ROUT D1–	GND	IN D2–	ROUT D2–	GND	TOUT A1–	GND	GND	TOUT A2–	V_{CC}	V_{CC}	TOUT B1–	V_{CC}	TOUT B2–
B	IN C1+	ROUT C1+	IN C2+	ROUT C2+	V_{CC}	IN D1+	ROUT D1+	GND	IN D2+	ROUT D2+	NC	TOUT A1+	GND	NC	TOUT A2+	V_{CC}	NC	TOUT B1+	NC	TOUT B2+
C	TDI	TMS	INSELC	V_{CC}	V_{CC}	$\overline{\text{ULCD}}$	$\overline{\text{ULCC}}$	GND	DATA [6]	DATA [4]	DATA [2]	DATA [0]	GND	NC	SPD SELD	V_{CC}	LDTD EN	$\overline{\text{TRST}}$	GND	TDO
D	TCLK	$\overline{\text{RESET}}$	INSELD	V_{CC}	V_{CC}	V_{CC}	SPD SELC	GND	DATA [5]	DATA [3]	DATA [1]	GND	GND	GND	NC	V_{CC}	NC	V_{CC}	SCAN EN2	TMEN3
E	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
F	RX DC[8]	RX DC[9]	V_{CC}	V_{CC}													NC	NC	TX CLKOB	NC
G	GND	$\overline{\text{WREN}}$	GND	GND													SPD SELB	NC	SPD SELA	NC
H	GND	GND	GND	GND													GND	GND	GND	GND
J	GND	GND	GND	GND													NC	NC	NC	NC
K	RX DC[4]	TRG CLKC–	GND	GND													NC	NC	NC	NC
L	RX DC[5]	TRG CLKC+	$\overline{\text{LFIC}}$	GND													NC	NC	NC	TX DB[6]
M	RX DC[6]	RX DC[7]	V_{CC}	RE PDOC													REF CLKB+	REF CLKB–	TX ERRB	TX CLKB
N	GND	GND	GND	GND													GND	GND	GND	GND
P	RX DC[3]	RX DC[2]	RX DC[1]	RX DC[0]													TX DB[5]	TX DB[4]	TX DB[3]	TX DB[2]
R	BIST STC	RE CLKOC	RX CLKC+	RX CLKC–													TX DB[1]	TX DB[0]	TX DB[9]	TX DB[7]
T	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
U	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	RX DD[4]	RX DD[3]	GND	TX DA[9]	ADDR [0]	TRG CLKD–	TX DA[1]	GND	TX DA[4]	TX DA[8]	V_{CC}	NC	TX DB[8]	NC	NC
V	V_{CC}	V_{CC}	V_{CC}	RX DD[8]	V_{CC}	RX DD[5]	RX DD[1]	GND	BIST STD	ADDR [2]	TRG CLKD+	TX CLKOA	GND	TX DA[3]	TX DA[7]	V_{CC}	NC	NC	NC	NC
W	V_{CC}	V_{CC}	$\overline{\text{LFID}}$	RX CLKD–	V_{CC}	RX DD[6]	RX DD[0]	GND	ADDR [3]	ADDR [1]	NC	TX ERRA	GND	TX DA[2]	TX DA[6]	V_{CC}	NC	REF CLKA+	NC	NC
Y	V_{CC}	V_{CC}	RX DD[9]	RX CLKD+	V_{CC}	RX DD[7]	RX DD[2]	GND	RE CLKOD	NC	TX CLKA	NC	GND	TX DA[0]	TX DA[5]	V_{CC}	RE PDOD	REF CLKA–	NC	NC

Note
1. NC = Do not connect.

Pin Configuration (Bottom View)[1]

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	TOUT B2–	V_{CC}	TOUT B1–	V_{CC}	V_{CC}	TOUT A2–	GND	GND	TOUT A1–	GND	ROUT D2–	IN D2–	GND	ROUT D1–	IN D1–	V_{CC}	ROUT C2–	IN C2–	ROUT C1–	IN C1–
B	TOUT B2+	NC	TOUT B1+	NC	V_{CC}	TOUT A2+	NC	GND	TOUT A1+	NC	ROUT D2+	IN D2+	GND	ROUT D1+	IN D1+	V_{CC}	ROUT C2+	IN C2+	ROUT C1+	IN C1+
C	TDO	GND	$\overline{TRST}$	LDTD EN	V_{CC}	SPD SELD	NC	GND	DATA [0]	DATA [2]	DATA [4]	DATA [6]	GND	$\overline{ULCC}$	$\overline{ULCD}$	V_{CC}	V_{CC}	INSELC	TMS	TDI
D	TMEN3	SCAN EN2	V_{CC}	NC	V_{CC}	NC	GND	GND	GND	DATA [1]	DATA [3]	DATA [5]	GND	SPD SELC	V_{CC}	V_{CC}	V_{CC}	INSELD	$\overline{RESET}$	TCLK
E	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
F	NC	TX CLKOB	NC	NC													V_{CC}	V_{CC}	RX DC[9]	RX DC[8]
G	NC	SPD SELA	NC	SPD SELB													GND	GND	$\overline{WREN}$	GND
H	GND	GND	GND	GND													GND	GND	GND	GND
J	NC	NC	NC	NC													GND	GND	GND	GND
K	NC	NC	NC	NC													GND	GND	TRG CLKC–	RX DC[4]
L	TX DB[6]	NC	NC	NC													GND	$\overline{LFIC}$	TRG CLKC+	RX DC[5]
M	TX CLKB	TX ERRB	REF CLKB–	REF CLKB+													RE PDOC	V_{CC}	RX DC[7]	RX DC[6]
N	GND	GND	GND	GND													GND	GND	GND	GND
P	TX DB[2]	TX DB[3]	TX DB[4]	TX DB[5]													RX DC[0]	RX DC[1]	RX DC[2]	RX DC[3]
R	TX DB[7]	TX DB[9]	TX DB[0]	TX DB[1]													RX CLKC–	RX CLKC+	RE CLKOC	BIST STC
T	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
U	NC	NC	TX DB[8]	NC	V_{CC}	TX DA[8]	TX DA[4]	GND	TX DA[1]	TRG CLKD–	ADDR [0]	TX DA[9]	GND	RX DD[3]	RX DD[4]	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V	NC	NC	NC	NC	V_{CC}	TX DA[7]	TX DA[3]	GND	TX CLKOA	TRG CLKD+	ADDR [2]	BIST STD	GND	RX DD[1]	RX DD[5]	V_{CC}	RX DD[8]	V_{CC}	V_{CC}	V_{CC}
W	NC	NC	REF CLKA+	NC	V_{CC}	TX DA[6]	TX DA[2]	GND	TX ERRA	NC	ADDR [1]	ADDR [3]	GND	RX DD[0]	RX DD[6]	V_{CC}	RX CLKD–	$\overline{LFID}$	V_{CC}	V_{CC}
Y	NC	NC	REF CLKA–	RE PDOD	V_{CC}	TX DA[5]	TX DA[0]	GND	NC	TX CLKA	NC	RE CLKOD	GND	RX DD[2]	RX DD[7]	V_{CC}	RX CLKD+	RX DD[9]	V_{CC}	V_{CC}

Pin Definitions
CYV15G0204TRB HOTLink II Dual Serializer and Dual Reclocking Deserializer

Name	I/O Characteristics	Signal Description
Transmit Path Data and Status Signals		
TXDA[7:0] TXDB[7:0]	LVTTL Input, synchronous, sampled by the associated TXCLKx↑ or REFCLKx↑[2]	**Transmit Data Inputs**. TXDx[9:0] data inputs are captured on the rising edge of the transmit interface clock. The transmit interface clock is selected by the TXCKSELx latch via the device configuration interface.
TXERRA TXERRB	LVTTL Output, synchronous to REFCLKx↑ [3], asynchronous to transmit channel enable / disable, asynchronous to loss or return of REFCLKx±	**Transmit Path Error**. TXERRx is asserted HIGH to indicate detection of a transmit Phase-Align Buffer underflow or overflow. If an underflow or overflow condition is detected, TXERRx, for the channel in error, is asserted HIGH and remains asserted until the transmit Phase-Align Buffer is re-centered with the PABRSTx latch via the device configuration interface. When TXBISTx = 0, the BIST progress is presented on the associated TXERRx output. The TXERRx signal pulses HIGH for one transmit-character clock period to indicate a pass through the BIST sequence after every 511 character times. TXERRx is also asserted HIGH, when any of the following conditions is true: ■ The TXPLL for the associated channel is powered down. This occurs when OE2x and OE1x for a channel are both disabled by setting OE2x = 0 and OE1x = 0. ■ The absence of the REFCLKx± signal.
Transmit Path Clock Signals		
REFCLKA± REFCLKB±	Differential LVPECL or single-ended LVTTL input clock	**Reference Clock**. REFCLKx± clock inputs are used as the timing references for the transmit PLL. These input clocks may also be selected to clock the transmit parallel interface. When driven by a single-ended LVCMOS or LVTTL clock source, connect the clock source to either the true or complement REFCLKx input, and leave the alternate REFCLKx input open (floating). When driven by an LVPECL clock source, the clock must be a differential clock, using both inputs.
TXCLKA TXCLKB	LVTTL Clock Input, internal pull-down	**Transmit Path Input Clock**. When configuration latch TXCKSELx = 0, the associated TXCLKx input is selected as the character-rate input clock for the TXDx[9:0] input. In this mode, the TXCLKx input must be frequency-coherent to its associated TXCLKOx output clock, but may be offset in phase by any amount. After initialized, TXCLKx is allowed to drift in phase as much as ±180 degrees. If the input phase of TXCLKx drifts beyond the handling capacity of the Phase Align Buffer, TXERRx is asserted to indicate the loss of data, and remains asserted until the Phase Align Buffer is initialized. The phase of the TXCLKx input clock relative to its associated REFCLKx± is initialized when the configuration latch PABRSTx is written as 0. When the associated TXERRx is deasserted, the Phase Align Buffer is initialized and input characters are correctly captured.
TXCLKOA TXCLKOB	LVTTL Output	**Transmit Clock Output**. TXCLKOx output clock is synthesized by each channel's transmit PLL and operates synchronous to the internal transmit character clock. TXCLKOx operates at either the same frequency as REFCLKx± (TXRATEx = 0), or at twice the frequency of REFCLKx± (TXRATEx = 1). The transmit clock outputs have no fixed phase relationship to REFCLKx±.

Notes
2. When REFCLKx± is configured for half-rate operation, these inputs are sampled relative to both the rising and falling edges of the associated REFCLKx±.
3. When REFCLKx± is configured for half-rate operation, these outputs are presented relative to both the rising and falling edges of the associated REFCLKx±.

Pin Definitions (continued)
CYV15G0204TRB HOTLink II Dual Serializer and Dual Reclocking Deserializer

Name	I/O Characteristics	Signal Description
Receive Path Data and Status Signals		
RXDC[9:0] RXDD[9:0]	LVTTL Output, synchronous to the RXCLK± output	**Parallel Data Output**. RXDx[9:0] parallel data outputs change relative to the receive interface clock. If RXCLKx± is a full-rate clock, the RXCLKx± clock outputs are complementary clocks operating at the character rate. The RXDx[9:0] outputs for the associated receive channels follow rising edge of RXCLKx+ or falling edge of RXCLKx–. If RXCLKx± is a half-rate clock, the RXCLKx± clock outputs are complementary clocks operating at half the character rate. The RXDx[9:0] outputs for the associated receive channels follow both the falling and rising edges of the associated RXCLKx± clock outputs. When BIST is enabled on the receive channel, the BIST status is presented on the RXDx[1:0] and BISTSTx outputs. See Table 6 on page 22 for each status reported by the BIST state machine. Also, while BIST is enabled, the RXDx[9:2] outputs should be ignored.
BISTSTC BISTSTD	LVTTL Output, synchronous to the RXCLKx ± output	**BIST Status Output.** When RXBISTx[1:0] = 10, BISTSTx (along with RXDx[1:0]) displays the status of the BIST reception. See Table 6 on page 22 for the BIST status reported for each combination of BISTSTx and RXDx[1:0]. When RXBISTx[1:0] ≠ 10, BISTSTx should be ignored.
REPDOC REPDOD	Asynchronous to reclocker output channel enable / disable	**Reclocker Powered Down Status Output.** REPDOx is asserted HIGH, when the associated channel's reclocker output logic is powered down. This occurs when ROE2x and ROE1x are both disabled by setting ROE2x = 0 and ROE1x = 0.
Receive Path Clock Signals		
TRGCLKC± TRGCLKD±	Differential LVPECL or single-ended LVTTL input clock	**CDR PLL Training Clock**. TRGCLKx± clock inputs are used as the reference source for the frequency detector (Range Controller) of the associated receive PLL to reduce PLL acquisition time. In the presence of valid serial data, the recovered clock output of the receive CDR PLL (RXCLKx±) has no frequency or phase relationship with TRGCLKx±. When driven by a single-ended LVCMOS or LVTTL clock source, connect the clock source to either the true or complement TRGCLKx input, and leave the alternate TRGCLKx input open (floating). When driven by an LVPECL clock source, the clock must be a differential clock, using both inputs.
RXCLKC± RXCLKD±	LVTTL Output Clock	**Receive Clock Output**. RXCLKx± is the receive interface clock used to control timing of the RXDx[9:0] parallel outputs. These true and complement clocks are used to control timing of data output transfers. These clocks are output continuously at either the half-character rate (1/20th the serial bit-rate) or character rate (1/10th the serial bit-rate) of the data being received, as selected by RXRATEx.
RECLKOC RECLKOD	LVTTL Output	**Reclocker Clock Output**. RECLKOx output clock is synthesized by the associated reclocker output PLL and operates synchronous to the internal recovered character clock. RECLKOx operates at either the same frequency as RXCLKx± (RXRATEx = 0), or at twice the frequency of RXCLKx± (RXRATEx = 1).The reclocker clock outputs have no fixed phase relationship to RXCLKx±.
Device Control Signals		
$\overline{\text{RESET}}$	LVTTL Input, asynchronous, internal pull-up	**Asynchronous Device Reset**. $\overline{\text{RESET}}$ initializes all state machines, counters, and configuration latches in the device to a known state. $\overline{\text{RESET}}$ must be asserted LOW for a minimum pulse width. When the reset is removed, all state machines, counters and configuration latches are at an initial state. As per the JTAG specifications the device RESET cannot reset the JTAG controller. Therefore, the JTAG controller has to be reset separately. See "JTAG Support" on page 22 for the methods to reset the JTAG state machine. See Table 4 on page 18 for the initialize values of the device configuration latches.

Pin Definitions (continued)
CYV15G0204TRB HOTLink II Dual Serializer and Dual Reclocking Deserializer

Name	I/O Characteristics	Signal Description
LDTDEN	LVTTL Input, internal pull-up	**Level Detect Transition Density Enable**. When LDTDEN is HIGH, the Signal Level Detector, Range Controller, and Transition Density Detector are all enabled to determine if the RXPLL tracks TRGCLKx± or the selected input serial data stream. If the Signal Level Detector, Range Controller, or Transition Density Detector are out of their respective limits while LDTDEN is HIGH, the RXPLL locks to TRGCLKx± until such a time they become valid. The SDASEL[A..D][1:0] inputs are used to configure the trip level of the Signal Level Detector. The Transition Density Detector limit is one transition in every 60 consecutive bits. When LDTDEN is LOW, only the Range Controller is used to determine if the RXPLL tracks TRGCLKx± or the selected input serial data stream. It is recommended to set LDTDEN = HIGH.
$\overline{\text{ULCC}}$ ULCD	LVTTL Input, internal pull-up	**Use Local Clock**. When $\overline{\text{ULCx}}$ is LOW, the RXPLL is forced to lock to TRGCLKx± instead of the received serial data stream. While ULCx is LOW, the LFIx for the associated channel is LOW indicating a link fault. When $\overline{\text{ULCx}}$ is HIGH, the RXPLL performs Clock and Data Recovery functions on the input data streams. This function is used in applications in which a stable RXCLKx± is needed. In cases when there is an absence of valid data transitions for a long period of time, or the high-gain differential serial inputs (INx±) are left floating, there may be brief frequency excursions of the RXCLKx± outputs from TRGCLKx±.
SPDSELA SPDSELB SPDSELC SPDSELD	3-Level Select[4] static control input	**Serial Rate Select**. The SPDSELx inputs specify the operating signaling-rate range of each channel's transmit (channels A and B) or receive PLL (channels C and D). LOW = 195 – 400 MBd MID = 400 – 800 MBd HIGH = 800 – 1500 MBd.
INSELC INSELD	LVTTL Input, asynchronous	**Receive Input Selector**. The INSELx input determines which external serial bit stream is passed to the receiver's Clock and Data Recovery circuit. When INSELx is HIGH, the Primary Differential Serial Data Input, INx1±, is selected for the associated receive channel. When INSELx is LOW, the Secondary Differential Serial Data Input, INx2±, is selected for the associated receive channel.
$\overline{\text{LFIC}}$ LFID	LVTTL Output, asynchronous	**Link Fault Indication Output**. $\overline{\text{LFIx}}$ is an output status indicator signal. $\overline{\text{LFIx}}$ is the logical OR of six internal conditions. LFIx is asserted LOW when any of the following conditions is true: ■ Received serial data rate outside expected range ■ Analog amplitude below expected levels ■ Transition density lower than expected ■ Receive channel disabled ■ $\overline{\text{ULCx}}$ is LOW ■ Absence of TRGCLKx±.

Notes
4. 3-Level Select inputs are used for static configuration. These are ternary inputs that make use of logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC} (power). The MID level is usually implemented by not connecting the input (left floating), which allows it to self bias to the proper level.

Pin Definitions (continued)
CYV15G0204TRB HOTLink II Dual Serializer and Dual Reclocking Deserializer

Name	I/O Characteristics	Signal Description
Device Configuration and Control Bus Signals		
$\overline{\text{WREN}}$	LVTTL input, asynchronous, internal pull-up	**Control Write Enable**. The $\overline{\text{WREN}}$ input writes the values of the DATA[6:0] bus into the latch specified by the address location on the ADDR[3:0] bus.[5]
ADDR[3:0]	LVTTL input asynchronous, internal pull-up	**Control Addressing Bus**. The ADDR[3:0] bus is the input address bus used to configure the device. The $\overline{\text{WREN}}$ input writes the values of the DATA[6:0] bus into the latch specified by the address location on the ADDR[3:0] bus.[5] Table 4 on page 18 lists the configuration latches within the device, and the initialization value of the latches upon the assertion of $\overline{\text{RESET}}$. Table 5 on page 21 shows how the latches are mapped in the device.
DATA[6:0]	LVTTL input asynchronous, internal pull-up	**Control Data Bus**. The DATA[6:0] bus is the input data bus used to configure the device. The $\overline{\text{WREN}}$ input writes the values of the DATA[6:0] bus into the latch specified by address location on the ADDR[3:0] bus.[5] Table 4 on page 18 lists the configuration latches within the device, and the initialization value of the latches upon the assertion of $\overline{\text{RESET}}$. Table 5 on page 21 shows how the latches are mapped in the device.
Internal Device Configuration Latches		
RXRATE[C..D]	Internal Latch[6]	**Receive Clock Rate Select**.
SDASEL[2..1][C..D][1:0]	Internal Latch[6]	**Signal Detect Amplitude Select**.
TXCKSEL[A..B]	Internal Latch[6]	**Transmit Clock Select**.
TXRATE[A..B]	Internal Latch[6]	**Transmit PLL Clock Rate Select**.
TRGRATE[C..D]	Internal Latch[6]	**Reclocker Output PLL Clock Rate Select**.
RXPLLPD[C..D]	Internal Latch[6]	**Receive Channel Power Control**.
RXBIST[C..D][1:0]	Internal Latch[6]	**Receive Bist Disabled**.
TXBIST[A..B]	Internal Latch[6]	**Transmit Bist Disabled**.
TOE2[A..B]	Internal Latch[6]	**Transmitter Differential Serial Output Driver 2 Enable**.
TOE1[A..B]	Internal Latch[6]	**Transmitter Differential Serial Output Driver 1 Enable**.
ROE2[C..D]	Internal Latch[6]	**Reclocker Differential Serial Output Driver 2 Enable**.
ROE1[C..D]	Internal Latch[6]	**Reclocker Differential Serial Output Driver 1 Enable**.
PABRSTB[A..B]	Internal Latch[6]	**Transmit Clock Phase Alignment Buffer Reset**.
Factory Test Modes		
SCANEN2	LVTTL input, internal pull-down	**Factory Test 2.** SCANEN2 input is for factory testing only. This input may be left as a NO CONNECT, or GND only.
TMEN3	LVTTL input, internal pull-down	**Factory Test 3**. TMEN3 input is for factory testing only. This input may be left as a NO CONNECT, or GND only.

Notes
5. See *Device Configuration and Control Interface* for detailed information on the operation of the Configuration Interface.
6. See *Device Configuration and Control Interface* for detailed information on the internal latches.

Pin Definitions (continued)
CYV15G0204TRB HOTLink II Dual Serializer and Dual Reclocking Deserializer

Name	I/O Characteristics	Signal Description
Analog I/O		
TOUTA1± TOUTB1±	CML Differential Output	**Transmitter Primary Differential Serial Data Output**. The transmitter TOUTx1± PECL-compatible CML outputs (+3.3 V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules, and must be AC-coupled for PECL-compatible connections.
TOUTA2± TOUTB2±	CML Differential Output	**Transmitter Secondary Differential Serial Data Output**. The transmitter TOUTx2± PECL-compatible CML outputs (+3.3 V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules, and must be AC-coupled for PECL-compatible connections.
ROUTC1± ROUTD1±	CML Differential Output	**Reclocker Primary Differential Serial Data Output**. The reclocker ROUTx1± PECL-compatible CML outputs (+3.3 V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules, and must be AC-coupled for PECL-compatible connections.
ROUTC2± ROUTD2±	CML Differential Output	**Reclocker Secondary Differential Serial Data Output**. The reclocker ROUTx2± PECL-compatible CML outputs (+3.3 V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules, and must be AC-coupled for PECL-compatible connections.
INC1± IND1±	Differential Input	**Primary Differential Serial Data Input**. The INx1± input accepts the serial data stream for deserialization. The INx1± serial stream is passed to the receive CDR circuit to extract the data content when INSELx = HIGH.
INC2± IND2±	Differential Input	**Secondary Differential Serial Data Input**. The INx2± input accepts the serial data stream for deserialization. The INx2± serial stream is passed to the receiver CDR circuit to extract the data content when INSELx = LOW.
JTAG Interface		
TMS	LVTTL Input, internal pull-up	**Test Mode Select**. Used to control access to the JTAG Test Modes. If maintained high for ≥5 TCLK cycles, the JTAG test controller is reset.
TCLK	LVTTL Input, internal pull-down	**JTAG Test Clock**.
TDO	3-State LVTTL Output	**Test Data Out**. JTAG data output buffer. High-Z while JTAG test mode is not selected.
TDI	LVTTL Input, internal pull-up	**Test Data In**. JTAG data input port.
$\overline{\text{TRST}}$	LVTTL Input, internal pull-up	**JTAG reset signal**. When asserted (LOW), this input asynchronously resets the JTAG test access port controller.
Power		
V_{CC}		**+3.3 V Power**.
GND		**Signal and Power Ground for all internal circuits**.

CYV15G0204TRB HOTLink II Operation

The CYV15G0204TRB is a highly configurable, independent clocking, device designed to support reliable transfer of large quantities of digital video data, using high-speed serial links from multiple sources to multiple destinations.

CYV15G0204TRB Transmit Data Path

Input Register

The parallel input bus TXDx[9:0] can be clocked in using TXCLKx (TXCKSELx = 0) or REFCLKx (TXCKSELx = 1).

Phase-Align Buffer

Data from each Input Register is passed to the associated Phase-Align Buffer, when the TXDx[9:0] input registers are clocked using TXCLKx (TXCKSELx = 0 and TXRATEx = 0). When the TXDx[9:0] input registers are clocked using REFCLKx± (TXCKSELx = 1) and REFCLKx± is a full-rate clock, the associated Phase Alignment Buffer in the transmit path is bypassed. These buffers are used to absorb clock phase differences between the TXCLKx input clock and the internal character clock for that channel.

After initialized, TXCLKx is allowed to drift in phase as much as ±180 degrees. If the input phase of TXCLKx drifts beyond the handling capacity of the Phase Align Buffer, TXERRx is asserted to indicate the loss of data, and remains asserted until the Phase Align Buffer is initialized. The phase of the TXCLKx relative to its associated internal character rate clock is initialized when the configuration latch PABRSTx is written as 0. When the associated TXERRx is deasserted, the Phase Align Buffer is initialized and input characters are correctly captured.

If the phase offset, between the initialized location of the input clock and REFCLKx, exceeds the skew handling capabilities of the Phase-Align Buffer, an error is reported on that channel's TXERRx output. This output indicates an error continuously until the Phase-Align Buffer for that channel is reset. While the error remains active, the transmitter for that channel outputs a continuous "1001111000" character to indicate to the remote receiver that an error condition is present in the link.

Transmit BIST

Each transmit channel contains an internal pattern generator that can be used to validate both the link and device operation. These generators are enabled by the associated TXBISTx latch via the device configuration interface. When enabled, a register in the associated transmit channel becomes a signature pattern generator by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Receiver(s).

A device reset ($\overline{\text{RESET}}$ sampled LOW) presets the BIST Enable Latches to disable BIST on both channels.

All data present at the associated TXDx[9:0] inputs are ignored when BIST is active on that channel.

Transmit PLL Clock Multiplier

Each Transmit PLL Clock Multiplier accepts a character-rate or half-character-rate external clock at the associated REFCLKx± input, and that clock is multiplied by 10 or 20 (as selected by TXRATEx) to generate a bit-rate clock for use by the transmit shifter. It also provides a character-rate clock used by the transmit paths, and outputs this character rate clock as TXCLKOx.

Each clock multiplier PLL can accept a REFCLKx± input between 19.5 MHz and 150 MHz, however, this clock range is limited by the operating mode of the CYV15G0204TRB clock multiplier (TXRATEx) and by the level on the associated SPDSELx input.

SPDSELx are 3-level select[7] inputs that select one of three operating ranges for the serial data outputs and inputs of the associated channel. The operating serial signaling-rate and allowable range of REFCLKx± frequencies are listed in Table 1.

Table 1. Operating Speed Settings

SPDSELx	TXRATEx	REFCLKx± Frequency (MHz)	Signaling Rate (Mbps)
LOW	1	reserved	195–400
	0	19.5–40	
MID (Open)	1	20–40	400–800
	0	40–80	
HIGH	1	40–75	800–1500
	0	80–150	

The REFCLKx± inputs are differential inputs with each input internally biased to 1.4 V. If the REFCLKx+ input is connected to a TTL, LVTTL, or LVCMOS clock source, the input signal is recognized when it passes through the internally biased reference point. When driven by a single-ended TTL, LVTTL, or LVCMOS clock source, connect the clock source to either the true or complement REFCLKx input, and leave the alternate REFCLKx input open (floating).

When both the REFCLKx+ and REFCLKx– inputs are connected, the clock source must be a differential clock. This can either be a differential LVPECL clock that is DC-or AC-coupled or a differential LVTTL or LVCMOS clock.

By connecting the REFCLKx– input to an external voltage source, it is possible to adjust the reference point of the REFCLKx+ input for alternate logic levels. When doing so, it is necessary to ensure that the input differential crossing point remains within the parametric range supported by the input.

Transmit Serial Output Drivers

The serial output interface drivers use differential Current Mode Logic (CML) drivers to provide source-matched drivers for 50Ω transmission lines. These drivers accept data from the Transmit Shifters. These drivers have signal swings equivalent to that of standard PECL drivers, and are capable of driving AC-coupled optical modules or transmission lines.

Notes

7. 3-Level Select inputs are used for static configuration. These are ternary inputs that make use of logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC} (power). The MID level is usually implemented by not connecting the input (left floating), which allows it to self bias to the proper level.

Transmit Channels Enabled

Each driver can be enabled or disabled separately via the device configuration interface.

When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. A device reset ($\overline{\text{RESET}}$ sampled LOW) disables all output drivers.

Note. When a disabled transmit channel (that is, both outputs disabled) is re-enabled:

- data on the serial outputs may not meet all timing specifications for up to 250 µs
- the state of the phase-align buffer cannot be guaranteed, and a phase-align reset is required if the phase-align buffer is used

CYV15G0204TRB Receive Data Path

Serial Line Receivers

Two differential Line Receivers, INx1± and INx2±, are available on each channel for accepting serial data streams. The active Serial Line Receiver on a channel is selected using the associated INSELx input. The Serial Line Receiver inputs are differential, and can accommodate wire interconnect and filtering losses or transmission line attenuation greater than 16 dB. For normal operation, these inputs should receive a signal of at least VI_{DIFF} > 100 mV, or 200 mV peak-to-peak differential. Each Line Receiver can be DC- or AC-coupled to +3.3 V powered fiber-optic interface modules (any ECL/PECL family, not limited to 100K PECL) or AC-coupled to +5 V powered optical modules. The common-mode tolerance of these line receivers accommodates a wide range of signal termination voltages. Each receiver provides internal DC-restoration, to the center of the receiver's common mode range, for AC-coupled signals.

Signal Detect/Link Fault

Each selected Line Receiver (that is, that routed to the clock and data recovery PLL) is simultaneously monitored for

- analog amplitude above amplitude level selected by SDASELx
- transition density above the specified limit
- range controls report the received data stream inside normal frequency range (±1500 ppm[9])
- receive channel enabled
- Presence of reference clock
- $\overline{\text{ULCx}}$ is not asserted.

All of these conditions must be valid for the Signal Detect block to indicate a valid signal is present. This status is presented on the $\overline{\text{LFIx}}$ (Link Fault Indicator) output associated with each receive channel, which changes synchronous to the receive interface clock.

Analog Amplitude

While most signal monitors are based on fixed constants, the analog amplitude level detection is adjustable to allow operation with highly attenuated signals, or in high-noise environments. The analog amplitude level detection is set by the SDASELx latch via device configuration interface. The SDASELx latch sets the trip point for the detection of a valid signal at one of three levels, as listed in Table 2. This control input affects the analog monitors for both receive channels. The Analog Signal Detect monitors are active for the Line Receiver as selected by the associated INSELx input.

Table 2. Analog Amplitude Detect Valid Signal Levels[8]

SDASEL	Typical Signal with Peak Amplitudes Above
00	Analog Signal Detector is disabled
01	140 mV p-p differential
10	280 mV p-p differential
11	420 mV p-p differential

Transition Density

The Transition Detection logic checks for the absence of transitions spanning greater than six transmission characters (60 bits). If no transitions are present in the data received, the Detection logic for that channel asserts $\overline{\text{LFIx}}$.

Range Controls

The CDR circuit includes logic to monitor the frequency of the PLL Voltage Controlled Oscillator (VCO) used to sample the incoming data stream. This logic ensures that the VCO operates at, or near the rate of the incoming data stream for two primary cases:

- when the incoming data stream resumes after a time in which it has been "missing."
- when the incoming data stream is outside the acceptable signaling rate range.

To perform this function, the frequency of the RXPLL VCO is periodically compared to the frequency of the TRGCLKx± input. If the VCO is running at a frequency beyond ±1500 ppm[9] as defined by the TRGCLKx± frequency, it is periodically forced to the correct frequency (as defined by TRGCLKx±, SPDSELx, and TRGRATEx) and then released in an attempt to lock to the input data stream.

The sampling and relock period of the Range Control is calculated as follows: RANGE_CONTROL_ SAMPLING_PERIOD = (RECOVERED BYTE CLOCK PERIOD) * (4096).

During the time that the Range Control forces the RXPLL VCO to track TRGCLKx±, the $\overline{\text{LFIx}}$ output is asserted LOW. After a valid serial data stream is applied, it may take up to one RANGE CONTROL SAMPLING PERIOD before the PLL locks to the input data stream, after which $\overline{\text{LFIx}}$ should be HIGH.

The operating serial signaling-rate and allowable range of TRGCLK± frequencies are listed in Table 3.

Notes

8. The peak amplitudes listed in this table are for typical waveforms that have generally 3–4 transitions for every ten bits. In a worse case environment the signals may have a sine-wave appearance (highest transition density with repeating 0101...). Signal peak amplitudes levels within this environment type could increase the values in the table above by approximately 100 mV.
9. TRGCLKx± has no phase or frequency relationship with the recovered clock(s) and only acts as a centering reference to reduce clock synchronization time. TRGCLKx± must be within ±1500 PPM (±0.15%) of the transmitter PLL reference (REFCLKx±) frequency. Although transmitting to a HOTLink II receiver channel necessitates the frequency difference between the transmitter and receiver reference clocks to be within ±1500-PPM, the stability of the crystal needs to be within the limits specified by the appropriate standard when transmitting to a remote receiver that is compliant to that standard.

Table 3. Operating Speed Settings

SPDSELx	TRGRATEx	TRGCLKx± Frequency (MHz)	Signaling Rate (Mbps)
LOW	1	reserved	195 – 400
	0	19.5–40	
MID (Open)	1	20–40	400–800
	0	40–80	
HIGH	1	40–75	800–1500
	0	80–150	

Receive Channel Enabled

The CYV15G0204TRB contains two receive channels that can be independently enabled and disabled. Each channel can be enabled or disabled separately through the RXPLLPDx input latch as controlled by the device configuration interface. When the RXPLLPDx latch = 0, the associated PLL and analog circuitry of the channel is disabled. Any disabled channel indicates a constant link fault condition on the LFIx output. When RXPLLPDx = 1, the associated PLL and receive channel is enabled to receive a serial stream.

When a disabled receive channel is reenabled, the status of the associated LFIx output and data on the parallel outputs for the associated channel may be indeterminate for up to 2 ms.

Clock/Data Recovery

The extraction of a bit-rate clock and recovery of bits from each received serial stream is performed by a separate CDR block within each receive channel. The clock extraction function is performed by an integrated PLL that tracks the frequency of the transitions in the incoming bit stream and align the phase of the internal bit-rate clock to the transitions in the selected serial data stream.

Each CDR accepts a character-rate (bit-rate ÷ 10) or half-character-rate (bit-rate ÷ 20) training clock from the associated TRGCLKx± input. This TRGCLKx± input is used to

- ensure that the VCO (within the CDR) is operating at the correct frequency (rather than a harmonic of the bit-rate)
- reduce PLL acquisition time
- limit unlocked frequency excursions of the CDR VCO when there is no input data present at the selected Serial Line Receiver.

Regardless of the type of signal present, the CDR attempts to recover a data stream from it. If the signalling rate of the recovered data stream is outside the limits set by the range control monitors, the CDR tracks TRGCLKx± instead of the data stream. After the CDR output (RXCLK±) frequency returns back close to TRGCLKx± frequency, the CDR input is switched back to the input data stream. If no data is present at the selected line receiver, this switching behavior may result in brief RXCLK± frequency excursions from TRGCLKx±. However, the validity of the input data stream is indicated by the LFIx output. The frequency of TRGCLKx± is required to be within ±1500 ppm[10] of the frequency of the clock that drives the REFCLKx± input of the *remote* transmitter to ensure a lock to the incoming data stream. This large ppm tolerance allows the CDR PLL to reliably receive a 1.485 or 1.485/1.001 Gbps SMPTE HD-SDI data stream with a constant TRGCLK frequency.

For systems using multiple or redundant connections, the $\overline{\text{LFIx}}$ output can be used to select an alternate data stream. When an $\overline{\text{LFIx}}$ indication is detected, external logic can toggle selection of the associated INx1± and INx2± input through the associated INSELx input. When a port switch takes place, it is necessary for the receive PLL for that channel to reacquire the new serial stream.

Reclocker

Each receive channel performs a reclocker function on the incoming serial data. To do this, the Clock and Data Recovery PLL first recovers the clock from the data. The data is retimed by the recovered clock and then passed to an output register. Also, the recovered character clock from the receive PLL is passed to the reclocker output PLL which generates the bit clock that is used to clock the retimed data into the output register. This data stream is then transmitted through the differential serial outputs.

Reclocker Serial Output Drivers

The serial output interface drivers use differential Current Mode Logic (CML) drivers to provide source-matched drivers for 50Ω transmission lines. These drivers accept data from the reclocker output register in the reclocker channel. These drivers have signal swings equivalent to that of standard PECL drivers, and are capable of driving AC-coupled optical modules or transmission lines.

Reclocker Output Channels Enabled

Each driver can be enabled or disabled separately via the device configuration interface.

When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both reclocker serial drivers for a channel are in this disabled state, the associated internal reclocker logic is also powered down. The deserialization logic and parallel outputs remain enabled. A device reset ($\overline{\text{RESET}}$ sampled LOW) disables all output drivers.

Note. When the disabled reclocker function (that is, both outputs disabled) is re-enabled, the data on the reclocker serial outputs may not meet all timing specifications for up to 250 μs.

Output Bus

The receive channel presents a 10-bit data signal (and a BIST status signal when RXBISTx[1:0] = 10).

Receive BIST Operation

Each receiver channel contains an internal pattern checker that can be used to validate both device and link operation. These pattern checkers are enabled by the associated RXBISTx[1:0] latch via the device configuration interface. When enabled, a register in the associated receive channel becomes a signature

Note

10. TRGCLKx± has no phase or frequency relationship with the recovered clock(s) and only acts as a centering reference to reduce clock synchronization time. TRGCLKx± must be within ±1500 PPM (±0.15%) of the transmitter PLL reference (REFCLKx±) frequency. Although transmitting to a HOTLink II receiver channel necessitates the frequency difference between the transmitter and receiver reference clocks to be within ±1500-PPM, the stability of the crystal needs to be within the limits specified by the appropriate standard when transmitting to a remote receiver that is compliant to that standard.

pattern generator and checker by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Transmitter(s). When synchronized with the received data stream, the associated Receiver checks each character from the deserializer with each character generated by the LFSR and indicates compare errors and BIST status at the RXDx[1:0] and BISTSTx bits of the Output Register.

The BIST status bus {BISTSTx, RXDx[0], RXDx[1]} indicates 010b or 100b for one character period per BIST loop to indicate loop completion. This status can be used to check test pattern progress.

If the number of invalid characters received ever exceeds the number of valid characters by 16, the receive BIST state machine aborts the compare operations and resets the LFSR to look for the start of the BIST sequence again.

A device reset ($\overline{\text{RESET}}$ sampled LOW) presets the BIST Enable Latches to disable BIST on both channels.

BIST Status State Machine

When a receive path is enabled to look for and compare the received data stream with the BIST pattern, the {BISTSTx, RXDx[0], RXDx[1]} bits identify the present state of the BIST compare operation.

The BIST state machine has multiple states, as shown in Figure 2 on page 23 and Table 6 on page 22. When the receive PLL detects an out-of-lock condition, the BIST state is forced to the Start-of-BIST state, regardless of the present state of the BIST state machine. If the number of detected errors ever exceeds the number of valid matches by greater than 16, the state machine is forced to the WAIT_FOR_BIST state where it monitors the receive path for the first character of the next BIST sequence.

Power Control

The CYV15G0204TRB supports user control of the powered up or down state of each transmit and receive channel. The receive channels are controlled by the RXPLLPDx latch via the device configuration interface. When RXPLLPDx = 0, the associated PLL and analog circuitry of the channel is disabled. The transmit channels are controlled by the TOE1x and the TOE2x latches via the device configuration interface. The reclocker function is controlled by the ROE1x and the ROE2x latches via the device configuration interface. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. When the reclocker serial drivers are disabled, the reclocker function is disabled, but the deserialization logic and parallel outputs remain enabled.

Device Reset State

When the CYV15G0204TRB is reset by assertion of $\overline{\text{RESET}}$, all state machines, counters, and configuration latches in the device are initialized to a reset state. Additionally, the JTAG controller must also be reset for valid operation (even if JTAG testing is not performed). See "JTAG Support" on page 22 for JTAG state machine initialization. See Table 4 on page 18 for the initialize values of the configuration latches.

Following a device reset, it is necessary to enable the receive channels used for normal operation. This can be done by sequencing the appropriate values on the device configuration interface.[11]

Device Configuration and Control Interface

The CYV15G0204TRB is highly configurable via the configuration interface. The configuration interface allows each channel to be configured independently. Table 4 on page 18 lists the configuration latches within the device including the initialization value of the latches upon the assertion of $\overline{\text{RESET}}$. Table 5 on page 21 shows how the latches are mapped in the device. Each row in the Table 5 maps to a 7-bit latch bank. There are 12 such write-only latch banks. When $\overline{\text{WREN}}$ = 0, the logic value in the DATA[7:0] is latched to the latch bank specified by the values in ADDR[3:0]. The second column of Table 5 specifies the channels associated with the corresponding latch bank. For example, the first three latch banks (0,1 and 2) consist of configuration bits for channel A.

Latch Types

There are two types of latch banks: static (S) and dynamic (D). Each channel is configured by 2 static and 1 dynamic latch banks. The S type contain those settings that normally do not change for an application, whereas the D type controls the settings that could change during the application's lifetime. The first and second rows of each channel (address numbers 0, 1, 3, 4, 6, 7, 9, and 10) are the static control latches. The third row of latches for each channel (address numbers 2, 5, 8, and 11) are the dynamic control latches that are associated with enabling dynamic functions within the device.

Static Latch Values

There are some latches in the table that have a static value (that is, 1, 0, or X). The latches that have a '1' or '0' must be configured with their corresponding value each time that their associated latch bank is configured. The latches that have an 'X' are don't cares and can be configured with any value.

Table 4. Device Configuration and Control Latch Descriptions

Name	Signal Description
TXCKSELA TXCKSELB	**Transmit Clock Select**. The initialization value of the TXCKSELx latch = 1. TXCKSELx selects the clock source used to write data into the Transmit Input Register. When TXCKSELx = 1, the associated input register TXDx[9:0] is clocked by REFCLKx↑. In this mode, the phase alignment buffer in the transmit path is bypassed. When TXCKSELx = 0, the associated TXCLKx↑ is used to clock in the input register TXDx[9:0].

Note
11. See *Device Configuration and Control Interface* for detailed information on the operation of the Configuration Interface.

Table 4. Device Configuration and Control Latch Descriptions (continued)

Name	Signal Description
TXRATEA TXRATEB	**Transmit PLL Clock Rate Select**. The initialization value of the TXRATEx latch = 0. TXRATEx is used to select the clock multiplier for the Transmit PLL. When TXRATEx = 0, each transmit PLL multiples the associated REFCLKx± input by 10 to generate the serial bit-rate clock. When TXRATEx = 0, the TXCLKOx output clocks are full-rate clocks and follow the frequency and duty cycle of the associated REFCLKx± input. When TXRATEx = 1, each Transmit PLL multiplies the associated REFCLKx± input by 20 to generate the serial bit-rate clock. When TXRATEx = 1, the TXCLKOx output clocks are twice the frequency rate of the REFCLKx± input. When TXCLKSELx = 1 and TXRATEx = 1, the Transmit Data Inputs are captured using both the rising and falling edges of REFCLKx. TXRATEx = 1 and SPDSELx = LOW, is an invalid state and this combination is reserved.
TXBISTA TXBISTB	**Transmit Bist Disabled**. The initialization value of the TXBISTx latch = 1. TXBISTx selects if the transmit BIST is disabled or enabled. When TXBISTx = 1, the transmit BIST function is disabled. When TXBISTx = 0, the transmit BIST function is enabled.
TOE2A TOE2B	**Secondary Differential Serial Data Output Driver Enable**. The initialization value of the TOE2x latch = 0. TOE2x selects if the TOUTx2± secondary differential output drivers are enabled or disabled. When TOE2x = 1, the associated serial data output driver is enabled allowing data to be transmitted from the transmit shifter. When TOE2x = 0, the associated serial data output driver is disabled. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. A device reset (RESET sampled LOW) disables all output drivers.
TOE1A TOE1B	**Primary Differential Serial Data Output Driver Enable**. The initialization value of the TOE1x latch = 0. TOE1x selects if the TOUTx1± primary differential output drivers are enabled or disabled. When TOE1x = 1, the associated serial data output driver is enabled allowing data to be transmitted from the transmit shifter. When TOE1x = 0, the associated serial data output driver is disabled. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. A device reset (RESET sampled LOW) disables all output drivers.
PABRSTA PABRSTB	**Transmit Clock Phase Alignment Buffer Reset**. The initialization value of the PABRSTx latch = 1. The PABRSTx is used to re-center the Transmit Phase Align Buffer. When the configuration latch PABRSTx is written as a 0, the phase of the TXCLKx input clock relative to its associated REFCLKx+/- is initialized. PABRST is an asynchronous input, but is sampled by each TXCLKx↑ to synchronize it to the internal clock domain. PABRSTx is a self clearing latch. This eliminates the requirement of writing a 1 to complete the initialization of the Phase Alignment Buffer.
RXRATEC RXRATED	**Receive Clock Rate Select**. The initialization value of the RXRATEx latch = 1. RXRATEx is used to select the rate of the RXCLKx± clock output. When RXRATEx = 1, the RXCLKx± clock outputs are complementary clocks that follow the recovered clock operating at half the character rate. Data for the associated receive channels should be latched alternately on the rising edge of RXCLKx+ and RXCLKx–. When RXRATEx = 0, the RXCLKx± clock outputs are complementary clocks that follow the recovered clock operating at the character rate. Data for the associated receive channels should be latched on the rising edge of RXCLKx+ or falling edge of RXCLKx–.
SDASEL1C[1:0] SDASEL1D[1:0]	**Primary Serial Data Input Signal Detector Amplitude Select**. The initialization value of the SDASEL1x[1:0] latch = 10. SDASEL1x[1:0] selects the trip point for the detection of a valid signal for the INx1± Primary Differential Serial Data Inputs. When SDASEL1x[1:0] = 00, the Analog Signal Detector is disabled. When SDASEL1x[1:0] = 01, the typical p-p differential voltage threshold level is 140 mV. When SDASEL1x[1:0] = 10, the typical p-p differential voltage threshold level is 280 mV. When SDASEL1x[1:0] = 11, the typical p-p differential voltage threshold level is 420 mV.
SDASEL2C[1:0] SDASEL2D[1:0]	**Secondary Serial Data Input Signal Detector Amplitude Select**. The initialization value of the SDASEL2x[1:0] latch = 10. SDASEL2x[1:0] selects the trip point for the detection of a valid signal for the INx2± Secondary Differential Serial Data Inputs. When SDASEL2x[1:0] = 00, the Analog Signal Detector is disabled When SDASEL2x[1:0] = 01, the typical p-p differential voltage threshold level is 140 mV. When SDASEL2x[1:0] = 10, the typical p-p differential voltage threshold level is 280 mV. When SDASEL2x[1:0] = 11, the typical p-p differential voltage threshold level is 420 mV.

Table 4. Device Configuration and Control Latch Descriptions (continued)

Name	Signal Description
TRGRATEC TRGRATED	**Training Clock Rate Select**. The initialization value of the TRGRATEx latch = 0. TRGRATEx is used to select the clock multiplier for the training clock input to the associated CDR PLL. When TRGRATEx = 0, the TRGCLKx± input is not multiplied before it is passed to the CDR PLL. When TRGRATEx = 1, the TRGCLKx± input is multiplied by 2 before it is passed to the CDR PLL. TRGRATEx = 1 and SPDSELx = LOW is an invalid state and this combination is reserved.
RXPLLPDC RXPLLPDD	**Receive Channel Enable**. The initialization value of the RXPLLPDx latch = 0. RXPLLPDx selects if the associated receive channel is enabled or powered-down. When RXPLLPDx = 0, the associated receive PLL and analog circuitry are powered-down. When RXPLLPDx = 1, the associated receive PLL and analog circuitry are enabled.
RXBISTC[1:0] RXBISTD[1:0]	**Receive Bist Disable / SMPTE Receive Enable**. The initialization value of the RXBISTx[1:0] latch = 11. For SMPTE data reception, RXBISTx[1:0] should not remain in this initialization state (11). RXBISTx[1:0] selects if receive BIST is disabled or enabled and sets the associated channel for SMPTE data reception. When RXBISTx[1:0] = 01, the receiver BIST function is disabled and the associated channel is set to receive SMPTE data. When RXBISTx[1:0] = 10, the receive BIST function is enabled and the associated channel is set to receive BIST data. RXBISTx[1:0] = 00 and RXBISTx[1:0] = 11 are invalid states.
ROE2C ROE2D	**Reclocker Secondary Differential Serial Data Output Driver Enable**. The initialization value of the ROE2x latch = 0. ROE2x selects if the ROUTx2± secondary differential output drivers are enabled or disabled. When ROE2x = 1, the associated serial data output driver is enabled allowing data to be transmitted from the transmit shifter. When ROE2x = 0, the associated serial data output driver is disabled. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. A device reset (RESET sampled LOW) disables all output drivers.
ROE1C ROE1D	**Reclocker Primary Differential Serial Data Output Driver Enable**. The initialization value of the ROE1x latch = 0. ROE1x selects if the ROUTx1± primary differential output drivers are enabled or disabled. When ROE1x = 1, the associated serial data output driver is enabled allowing data to be transmitted from the transmit shifter. When ROE1x = 0, the associated serial data output driver is disabled. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. A device reset (RESET sampled LOW) disables all output drivers.

Device Configuration Strategy

The following is a series of ordered events needed to load the configuration latches on a per channel basis:

1. Pulse $\overline{\text{RESET}}$ Low after device power-up. This operation resets all four channels. Initialize the JTAG state machine to its reset state as detailed in "JTAG Support" on page 22.
2. Set the static latch banks for the target channel.
3. Set the dynamic bank of latches for the target channel. Enable the Receive PLLs and transmit channels. If a receive channel is enabled, set the channel for SMPTE data reception (RXBISTA[1:0] = 01) or BIST data reception (RXBISTA[1:0] = 10).
4. Reset the Phase Alignment Buffer for the target channel. [Optional if phase align buffer is bypassed.]

Table 5. Device Control Latch Configuration Table

ADDR	Channel	Type	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	Reset Value
0 (0000b)	A	S	X	X	X	X	X	0	X	1011111
1 (0001b)	A	S	X	X	X	X	0	TXCKSELA	TXRATEA	1010110
2 (0010b)	A	D	X	X	X	TXBISTA	OE2A	OE1A	PABRSTA	1011001
3 (0011b)	B	S	X	X	X	X	X	0	X	1011111
4 (0100b)	B	S	X	X	X	X	0	TXCKSELB	TXRATEB	1010110
5 (0101b)	B	D	X	X	X	TXBISTB	OE2B	OE1B	PABRSTB	1011001
6 (0110b)	C	S	1	0	X	X	0	0	RXRATEC	1011111
7 (0111b)	C	S	SDASEL2C[1]	SDASEL2C[0]	SDASEL1C[1]	SDASEL1C[0]	X	X	TRGRATEC	1010110
8 (1000b)	C	D	RXBISTC[1]	RXPLLPDC	RXBISTC[0]	X	ROE2C	ROE1C	X	1011001
9 (1001b)	D	S	1	0	X	X	0	0	RXRATED	1011111
10 (1010b)	D	S	SDASEL2D[1]	SDASEL2D[0]	SDASEL1D[1]	SDASEL1D[0]	X	X	TRGRATED	1010110
11 (1011b)	D	D	RXBISTD[1]	RXPLLPDD	RXBISTD[0]	X	ROE2D	ROE1D	X	1011001
12 (1100b)			INTERNAL TEST REGISTERS DO NOT WRITE TO THESE ADDRESSES							
13 (1101b)										
14 (1110b)										
15 (1111b)										

JTAG Support

The CYV15G0204TRB contains a JTAG port to allow system level diagnosis of device interconnect. Of the available JTAG modes, boundary scan, and bypass are supported. This capability is present only on the LVTTL inputs and outputs, the REFCLKx± clock inputs, and the TRGCLKx± clock inputs. The high-speed serial inputs and outputs are not part of the JTAG test chain.

To ensure valid device operation after power-up (including non-JTAG operation), the JTAG state machine should also be initialized to a reset state. This should be done in addition to the device reset (using RESET). The JTAG state machine can be initialized using TRST (asserting it LOW and de-asserting it or leaving it asserted), or by asserting TMS HIGH for at least 5 consecutive TCLK cycles. This is necessary to ensure that the JTAG controller does not enter any of the test modes after device power-up. In this JTAG reset state, the rest of the device is in normal operation.

Note. The order of device reset (using $\overline{\text{RESET}}$) and JTAG initialization does not matter.

3-Level Select Inputs

Each 3-Level select inputs reports as two bits in the scan register. These bits report the LOW, MID, and HIGH state of the associated input as 00, 10, and 11 respectively

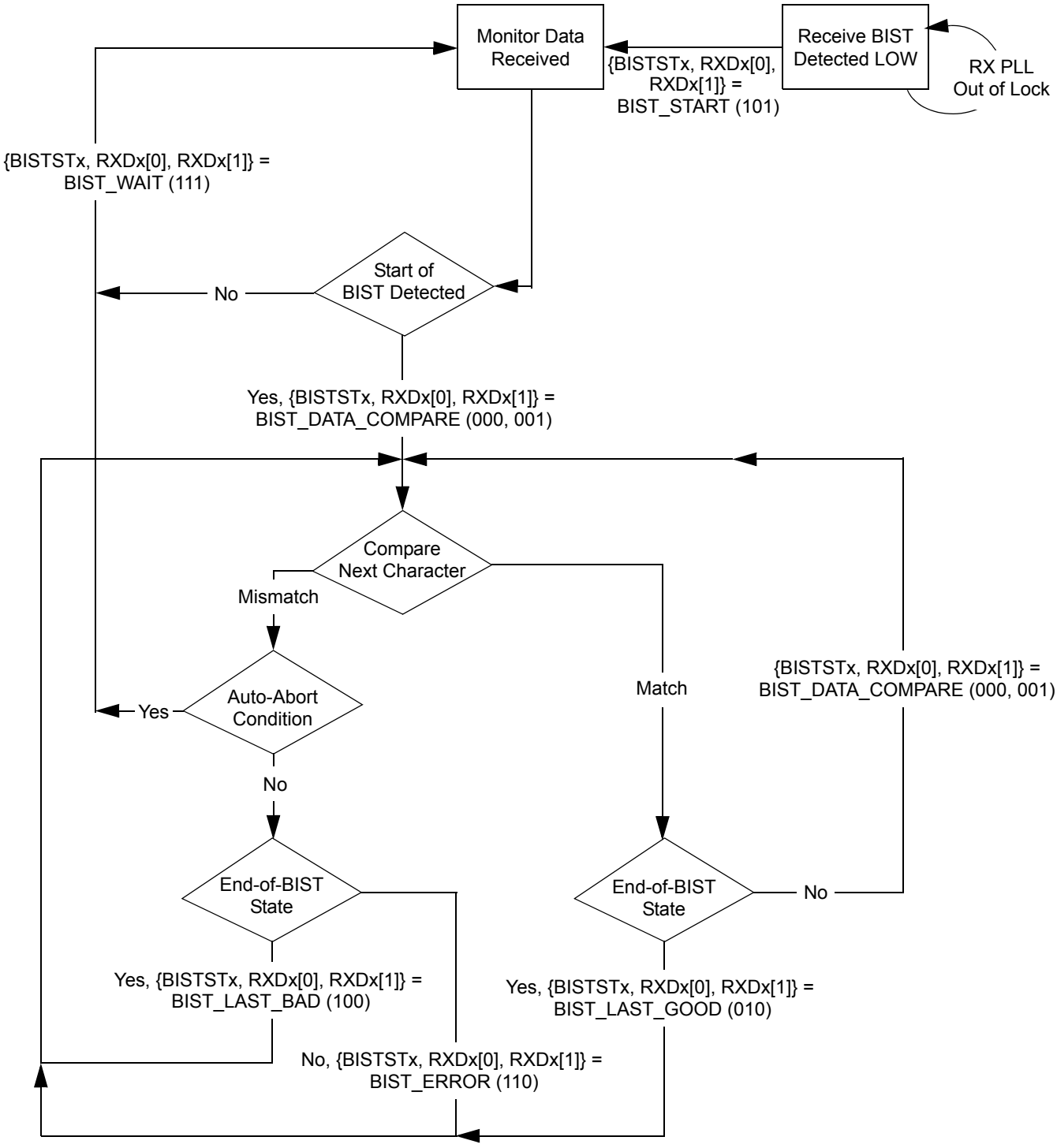
JTAG ID

The JTAG device ID for the CYV15G0204TRB is ‘0C811069’x

Table 6. Receive Character Status Bits

{BISTSTx, RXDx[0], RXDx[1]}	Description
	Receive BIST Status (Receive BIST = Enabled)
000, 001	**BIST Data Compare**. Character compared correctly.
010	**BIST Last Good**. Last Character of BIST sequence detected and valid.
011	Reserved.
100	**BIST Last Bad**. Last Character of BIST sequence detected invalid.
101	**BIST Start**. Receive BIST is enabled on this channel, but character compares have not yet commenced. This also indicates a PLL Out of Lock condition.
110	**BIST Error**. While comparing characters, a mismatch was found in one or more of the character bits.
111	**BIST Wait**. The receiver is comparing characters. but has not yet found the start of BIST character to enable the LFSR.

Figure 2. Receive BIST State Machine



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.5 V to +3.8 V

DC voltage applied to LVTTL outputs in high-Z state ..... –0.5 V to V_{CC} + 0.5 V

Output current into LVTTL outputs (LOW) ..... 60 mA

DC input voltage ..... –0.5 V to V_{CC} + 0.5 V

Static discharge voltage ..... > 2000 V (per MIL-STD-883, Method 3015)

Latch-up current ..... > 200 mA

Power-up Requirements

The CYV15G0204TRB requires one power-supply. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	+3.3 V ±5%

CYV15G0204TRB DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
LVTTL-compatible Outputs					
V_{OHT}	Output HIGH Voltage	I_{OH} = – 4 mA, V_{CC} = Min	2.4	–	V
V_{OLT}	Output LOW Voltage	I_{OL} = 4 mA, V_{CC} = Min	–	0.4	V
I_{OST}	Output Short Circuit Current	V_{OUT} = 0 V[12], V_{CC} = 3.3 V	–20	–100	mA
I_{OZL}	High-Z Output Leakage Current	V_{OUT} = 0 V, V_{CC}	–20	20	µA
LVTTL-compatible Inputs					
V_{IHT}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{ILT}	Input LOW Voltage		–0.5	0.8	V
I_{IHT}	Input HIGH Current	REFCLKx Input, V_{IN} = V_{CC}	–	1.5	mA
		Other Inputs, V_{IN} = V_{CC}	–	+40	µA
I_{ILT}	Input LOW Current	REFCLKx Input, V_{IN} = 0.0 V	–	–1.5	mA
		Other Inputs, V_{IN} = 0.0 V	–	–40	µA
I_{IHPDT}	Input HIGH Current with internal pull-down	V_{IN} = V_{CC}	–	+200	µA
I_{ILPUT}	Input LOW Current with internal pull-up	V_{IN} = 0.0 V	–	–200	µA
LVDIFF Inputs: REFCLKx±					
V_{DIFF}[13]	Input Differential Voltage		400	V_{CC}	mV
V_{IHHP}	Highest Input HIGH Voltage		1.2	V_{CC}	V
V_{ILLP}	Lowest Input LOW voltage		0.0	V_{CC}/2	V
V_{COMREF}[14]	Common Mode Range		1.0	V_{CC} – 1.2 V	V
3-Level Inputs					
V_{IHH}	Three-Level Input HIGH Voltage	Min ≤ V_{CC} ≤ Max	0.87 * V_{CC}	V_{CC}	V
V_{IMM}	Three-Level Input MID Voltage	Min ≤ V_{CC} ≤ Max	0.47 * V_{CC}	0.53 * V_{CC}	V
V_{ILL}	Three-Level Input LOW Voltage	Min ≤ V_{CC} ≤ Max	0.0	0.13 * V_{CC}	V
I_{IHH}	Input HIGH Current	V_{IN} = V_{CC}	–	200	µA
I_{IMM}	Input MID current	V_{IN} = V_{CC}/2	–50	50	µA
I_{ILL}	Input LOW current	V_{IN} = GND	–	–200	µA

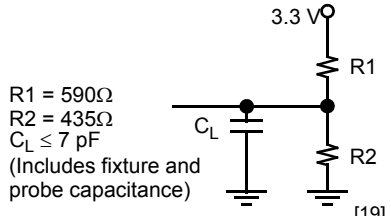
Notes

12. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
13. This is the minimum difference in voltage between the true and complement inputs required to ensure detection of a logic-1 or logic-0. A logic-1 exists when the true (+) input is more positive than the complement (–) input. A logic-0 exists when the complement (–) input is more positive than true (+) input.
14. The common mode range defines the allowable range of REFCLKx+ and REFCLKx– when REFCLKx+ = REFCLKx–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.

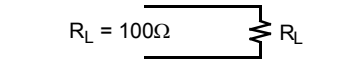
CYV15G0204TRB DC Electrical Characteristics (continued)

Parameter	Description	Test Conditions		Min	Max	Unit
Differential CML Serial Outputs: TOUTA1±, TOUTA2±, TOUTB1±, TOUTB2±, ROUTC1±, ROUTC2±, ROUTD1±, ROUTD2±						
V_{OHC}	Output HIGH Voltage (V_{cc} Referenced)	100 Ω differential load		V_{CC} – 0.5	V_{CC} – 0.2	V
		150 Ω differential load		V_{CC} – 0.5	V_{CC} – 0.2	V
V_{OLC}	Output LOW Voltage (V_{CC} Referenced)	100 Ω differential load		V_{CC} – 1.4	V_{CC} – 0.7	V
		150 Ω differential load		V_{CC} – 1.4	V_{CC} – 0.7	V
V_{ODIF}	Output Differential Voltage |(OUT+) – (OUT–)|	100 Ω differential load		450	900	mV
		150 Ω differential load		560	1000	mV
Differential Serial Line Receiver Inputs: INC1±, INC2±, IND1±, IND2±						
V_{DIFFs}[15]	Input Differential Voltage |(IN+) – (IN–)|			100	1200	mV
V_{IHE}	Highest Input HIGH Voltage				V_{CC}	V
V_{ILE}	Lowest Input LOW Voltage			V_{CC} – 2.0		V
I_{IHE}	Input HIGH Current	$V_{IN} = V_{IHE}$ Max			1350	µA
I_{ILE}	Input LOW Current	$V_{IN} = V_{ILE}$ Min		–700		µA
VI_{COM}[16]	Common Mode input range	((V_{CC} – 2.0 V)+0.5)min, (V_{CC} – 0.5 V) Max		+1.25	+3.1	V
Power Supply				**Typ**	**Max**	
I_{CC}[17, 18]	Max Power Supply Current	REFCLKx = MAX	Commercial	810	990	mA
I_{CC}[17, 18]	Typical Power Supply Current	REFCLKx = 125 MHz	Commercial	770	950	mA

AC Test Loads and Waveforms

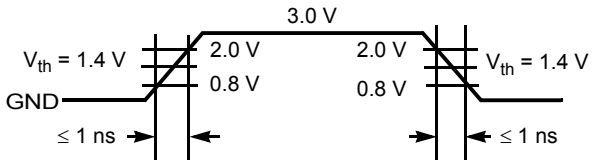


(a) LVTTL Output Test Load[19]

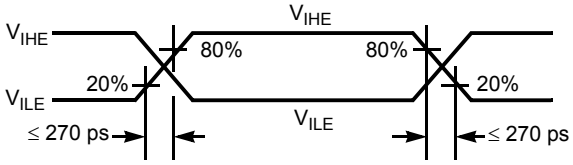


(Includes fixture and
probe capacitance)

(b) CML Output Test Load[19]



(c) LVTTL Input Test Waveform[20]



(d) CML/LVPECL Input Test Waveform

Notes

15. This is the minimum difference in voltage between the true and complement inputs required to ensure detection of a logic-1 or logic-0. A logic-1 exists when the true (+) input is more positive than the complement (–) input. A logic-0 exists when the complement (–) input is more positive than true (+) input.
16. The common mode range defines the allowable range of INPUT+ and INPUT– when INPUT+ = INPUT–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.
17. Maximum I_{CC} is measured with V_{CC} = MAX, T_A = 25 °C, with all channels and Serial Line Drivers enabled, sending a continuous alternating 01 pattern, and outputs unloaded.
18. Typical I_{CC} is measured under similar conditions except with V_{CC} = 3.3 V, T_A = 25 °C, with all channels enabled and one Serial Line Driver per transmit channel sending a continuous alternating 01 pattern. The redundant outputs on each channel are powered down and the parallel outputs are unloaded.
19. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
20. The LVTTL switching threshold is 1.4 V. All timing references are made relative to where the signal edges cross the threshold voltage.

CYV15G0204TRB AC Electrical Characteristics

Parameter	Description	Min	Max	Unit
CYV15G0204TRB Transmitter LVTTL Switching Characteristics Over the Operating Range				
f_{TS}	TXCLKx Clock Cycle Frequency	19.5	150	MHz
t_{TXCLK}	TXCLKx Period=1/f_{TS}	6.66	51.28	ns
t_{TXCLKH}[21]	TXCLKx HIGH Time	2.2	–	ns
t_{TXCLKL}[21]	TXCLKx LOW Time	2.2	–	ns
t_{TXCLKR}[21, 22, 23, 24]	TXCLKx Rise Time	0.2	1.7	ns
t_{TXCLKF}[21, 22, 23, 24]	TXCLKx Fall Time	0.2	1.7	ns
t_{TXDS}	Transmit Data Set-up Time to TXCLKx↑ (TXCKSELx = 0)	2.2	–	ns
t_{TXDH}	Transmit Data Hold Time from TXCLKx↑ (TXCKSELx = 0)	1.0	–	ns
f_{TOS}	TXCLKOx Clock Frequency = 1x or 2x REFCLKx Frequency	19.5	150	MHz
t_{TXCLKO}	TXCLKOx Period=1/f_{TOS}	6.66	51.28	ns
$t_{TXCLKOD}$	TXCLKO Duty Cycle centered at 60% HIGH time	–1.9	0	ns
CYV15G0204TRB Receiver LVTTL Switching Characteristics Over the Operating Range				
f_{RS}	RXCLKx± Clock Output Frequency	9.75	150	MHz
t_{RXCLKP}	RXCLKx± Period = 1/f_{RS}	6.66	102.56	ns
t_{RXCLKD}	RXCLKx± Duty Cycle Centered at 50% (Full Rate and Half Rate)	–1.0	+1.0	ns
t_{RXCLKR}[21]	RXCLKx± Rise Time	0.3	1.2	ns
t_{RXCLKF}[21]	RXCLKx± Fall Time	0.3	1.2	ns
t_{RXDv-}[25]	Status and Data Valid Time to RXCLKx± (RXRATEx = 0) (Full Rate)	5UI–2.0[26]	–	ns
	Status and Data Valid Time to RXCLKx± (RXRATEx = 1) (Half Rate)	5UI–1.3[26]	–	ns
t_{RXDv+}[25]	Status and Data Valid Time to RXCLKx± (RXRATEx = 0)	5UI–1.8[26]	–	ns
	Status and Data Valid Time to RXCLKx± (RXRATEx = 1)	5UI–2.6[26]	–	ns
f_{ROS}	RECLKOx Clock Frequency	19.5	150	MHz
t_{RECLKO}	RECLKOx Period=1/f_{ROS}	6.66	51.28	ns
$t_{RECLKOD}$	RECLKOx Duty Cycle centered at 60% HIGH time	–1.9	0	ns
CYV15G0204TRB REFCLKx Switching Characteristics Over the Operating Range				
f_{REF}	REFCLKx Clock Frequency	19.5	150	MHz
t_{REFCLK}	REFCLKx Period = 1/f_{REF}	6.6	51.28	ns
t_{REFH}	REFCLKx HIGH Time (TXRATEx = 1)(Half Rate)	5.9	–	ns
	REFCLKx HIGH Time (TXRATEx = 0)(Full Rate)	2.9[21]	–	ns
t_{REFL}	REFCLKx LOW Time (TXRATEx = 1)(Half Rate)	5.9	–	ns
	REFCLKx LOW Time (TXRATEx = 0)(Full Rate)	2.9[21]	–	ns
t_{REFD}[27]	REFCLKx Duty Cycle	30	70	%
t_{REFR}[21, 22, 23, 24]	REFCLKx Rise Time (20%–80%)	–	2	ns
t_{REFF}[21, 22, 23, 24]	REFCLKx Fall Time (20%–80%)	–	2	ns

Notes
21. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
22. The ratio of rise time to falling time must not vary by greater than 2:1.
23. For an operating frequency, neither rise or fall specification can be greater than 20% of the clock-cycle period or the data sheet maximum time.
24. All transmit AC timing parameters measured with 1-ns typical rise time and fall time.
25. Parallel data output specifications are only valid if all outputs are loaded with similar DC and AC loads.
26. Receiver UI (Unit Interval) is calculated as 1/(f_{REF} * 20) (when TRGRATEx = 1) or 1/(f_{REF} * 10) (when TRGRATEx = 0). In an operating link this is equivalent to t_B.
27. The duty cycle specification is a simultaneous condition with the t_{REFH} and t_{REFL} parameters. This means that at faster character rates the REFCLKx± duty cycle cannot be as large as 30%–70%.
28. TRGCLKx± has no phase or frequency relationship with the recovered clock(s) and only acts as a centering reference to reduce clock synchronization time. TRGCLKx± must be within ±1500 PPM (±0.15%) of the transmitter PLL reference (REFCLKx±) frequency. Although transmitting to a HOTLink II receiver channel necessitates the frequency difference between the transmitter and receiver reference clocks to be within ±1500-PPM, the stability of the crystal needs to be within the limits specified by the appropriate standard when transmitting to a remote receiver that is compliant to that standard.

CYV15G0204TRB AC Electrical Characteristics (continued)

Parameter	Description	Min	Max	Unit
t_{REFRX}[34]	TRGCLKx Frequency Referenced to Received Clock Period	–0.15	+0.15	%
t_{TREFDS}	Transmit Data Set-up Time to REFCLKx - Full Rate (TXRATEx = 0, TXCKSELx = 1)	2.4	–	ns
	Transmit Data Set-up Time to REFCLKx - Half Rate (TXRATEx = 1, TXCKSELx = 1)	2.3	–	ns
t_{TREFDH}	Transmit Data Hold Time from REFCLKx - Full Rate (TXRATEx = 0, TXCKSELx = 1)	1.0	–	ns
	Transmit Data Hold Time from REFCLKx - Half Rate (TXRATEx = 1, TXCKSELx = 1)	1.6	–	ns
CYV15G0204TRB TRGCLKx Switching Characteristics Over the Operating Range				
f_{REF}	TRGCLKx Clock Frequency	19.5	150	MHz
t_{REFCLK}	TRGCLKx Period = $1/f_{REF}$	6.6	51.28	ns
t_{REFH}	TRGCLKx HIGH Time (TXRATEx = 1)(Half Rate)	5.9	–	ns
	TRGCLKx HIGH Time (TXRATEx = 0)(Full Rate)	2.9[21]	–	ns
t_{REFL}	TRGCLKx LOW Time (TXRATEx = 1)(Half Rate)	5.9	–	ns
	TRGCLKx LOW Time (TXRATEx = 0)(Full Rate)	2.9[21]	–	ns
t_{REFD}[33]	TRGCLKx Duty Cycle	30	70	%
t_{REFR}[29, 30, 31, 32]	TRGCLKx Rise Time (20%–80%)	–	2	ns
t_{REFF}[29, 30, 31, 32]	TRGCLKx Fall Time (20%–80%)	–	2	ns
t_{REFRX}[34]	TRGCLKx Frequency Referenced to Received Clock Frequency	–0.15	+0.15	%
CYV15G0204TRB Bus Configuration Write Timing Characteristics Over the Operating Range				
t_{DATAH}	Bus Configuration Data Hold	0	–	ns
t_{DATAS}	Bus Configuration Data Setup	10	–	ns
t_{WRENP}	Bus Configuration WREN Pulse Width	10	–	ns
CYV15G0204TRB JTAG Test Clock Characteristics Over the Operating Range				
f_{TCLK}	JTAG Test Clock Frequency	–	20	MHz
t_{TCLK}	JTAG Test Clock Period	50	–	ns
CYV15G0204TRB Device RESET Characteristics Over the Operating Range				
t_{RST}	Device RESET Pulse Width	30	–	ns

Notes
29. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
30. The ratio of rise time to falling time must not vary by greater than 2:1.
31. For an operating frequency, neither rise or fall specification can be greater than 20% of the clock-cycle period or the data sheet maximum time.
32. All transmit AC timing parameters measured with 1-ns typical rise time and fall time.
33. The duty cycle specification is a simultaneous condition with the t_{REFH} and t_{REFL} parameters. This means that at faster character rates the REFCLKx± duty cycle cannot be as large as 30%–70%.
34. TRGCLKx± has no phase or frequency relationship with the recovered clock(s) and only acts as a centering reference to reduce clock synchronization time. TRGCLKx± must be within ±1500 PPM (±0.15%) of the transmitter PLL reference (REFCLKx±) frequency. Although transmitting to a HOTLink II receiver channel necessitates the frequency difference between the transmitter and receiver reference clocks to be within ±1500-PPM, the stability of the crystal needs to be within the limits specified by the appropriate standard when transmitting to a remote receiver that is compliant to that standard.

CYV15G0204TRB AC Electrical Characteristics (continued)

Parameter	Description		Min	Max	Unit
CYV15G0204TRB Transmitter and Reclocker Serial Output Characteristics Over the Operating Range					
Parameter	**Description**	**Condition**	**Min**	**Max**	**Unit**
t_B	Bit Time		660	5128	ps
t_{RISE}[35]	CML Output Rise Time 20–80% (CML Test Load)	SPDSELx = HIGH	50	270	ps
		SPDSELx= MID	100	500	ps
		SPDSELx =LOW	180	1000	ps
t_{FALL}[35]	CML Output Fall Time 80–20% (CML Test Load)	SPDSELx = HIGH	50	270	ps
		SPDSELx = MID	100	500	ps
		SPDSELx =LOW	180	1000	ps

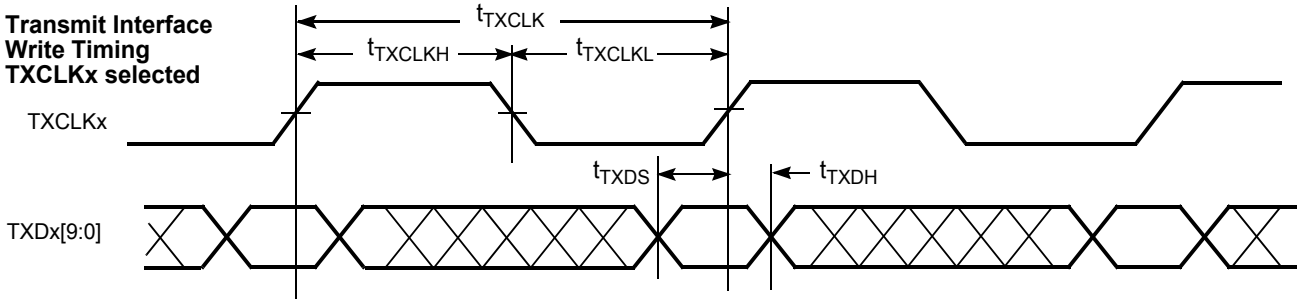
PLL Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
CYV15G0204TRB Transmitter Output PLL Characteristics						
$t_{JTGENSD}$[35, 36]	Transmit jitter generation - SD data rate	REFCLKx = 27 MHz	–	200	–	ps
$t_{JTGENHD}$[35, 36]	Transmit jitter generation - HD data rate	REFCLKx = 148.5 MHz	–	76	–	ps
t_{TXLOCK}	Transmit PLL lock to REFCLKx±		–		200	µs
CYV15G0204TRB Reclocker Output PLL Characteristics						
$t_{JRGENSD}$[35, 37]	Reclocker jitter generation - SD data rate	TRGCLKx = 27 MHz	–	133	–	ps
$t_{JRGENHD}$[35, 37]	Reclocker jitter generation - HD data rate	TRGCLKx = 148.5 MHz	–	107	–	ps
CYV15G0204TRB Receive PLL Characteristics Over the Operating Range						
t_{RXLOCK}	Receive PLL lock to input data stream (cold start)		–	–	376k	UI
	Receive PLL lock to input data stream		–	–	376k	UI
$t_{RXUNLOCK}$	Receive PLL unlock rate		–	–	46	UI

Capacitance[21]

Parameter	Description	Test Conditions	Max	Unit
C_{INTTL}	TTL input capacitance	T_A = 25 °C, f_0 = 1 MHz, V_{CC} = 3.3 V	7	pF
C_{INPECL}	PECL input capacitance	T_A = 25 °C, f_0 = 1 MHz, V_{CC} = 3.3 V	4	pF

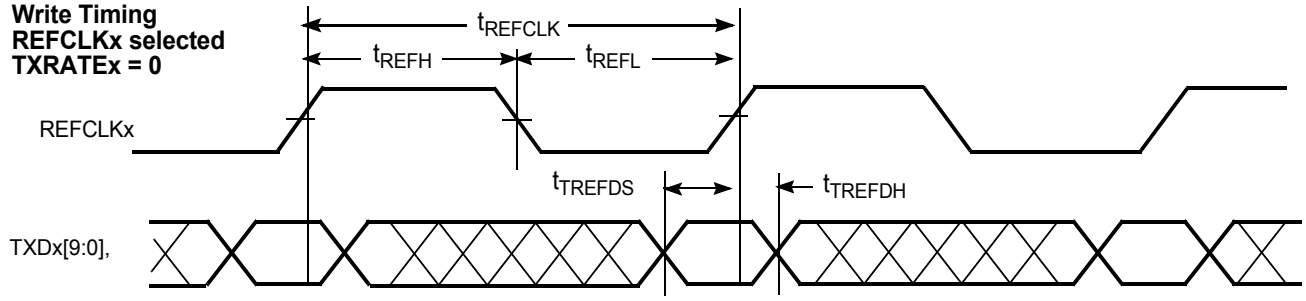
CYV15G0204TRB HOTLink II Transmitter Switching Waveforms



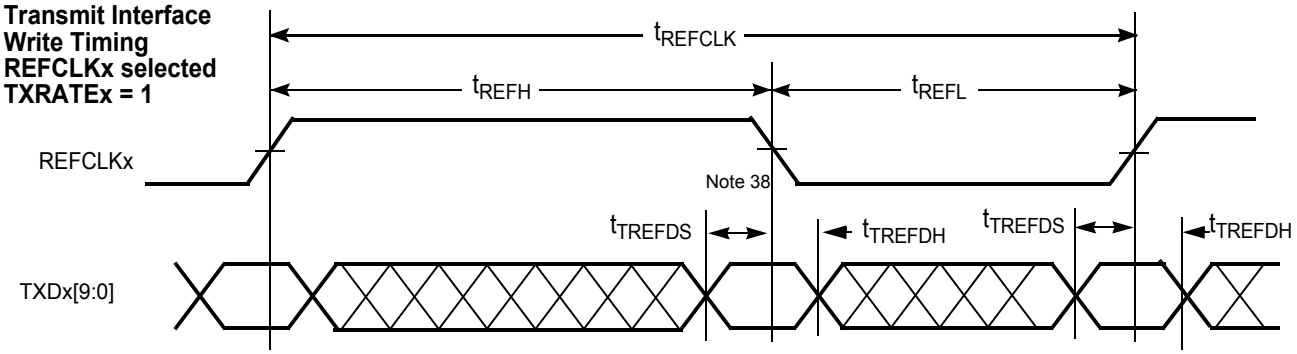
Notes
35. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
36. While sending BIST data at the corresponding data rate, after 10,000 histogram hits, time referenced to REFCLKx± input.
37. Receiver input stream is BIST data from the transmit channel. This data is reclocked and output to a wide-bandwidth digital sampling oscilloscope. The

CYV15G0204TRB HOTLink II Transmitter Switching Waveforms (continued)

Transmit Interface Write Timing REFCLKx selected TXRATEx = 0

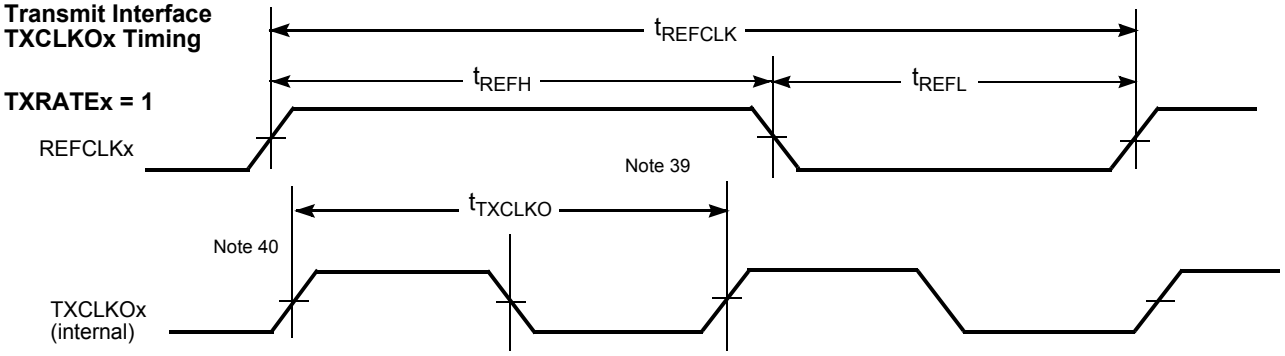


Transmit Interface Write Timing REFCLKx selected TXRATEx = 1



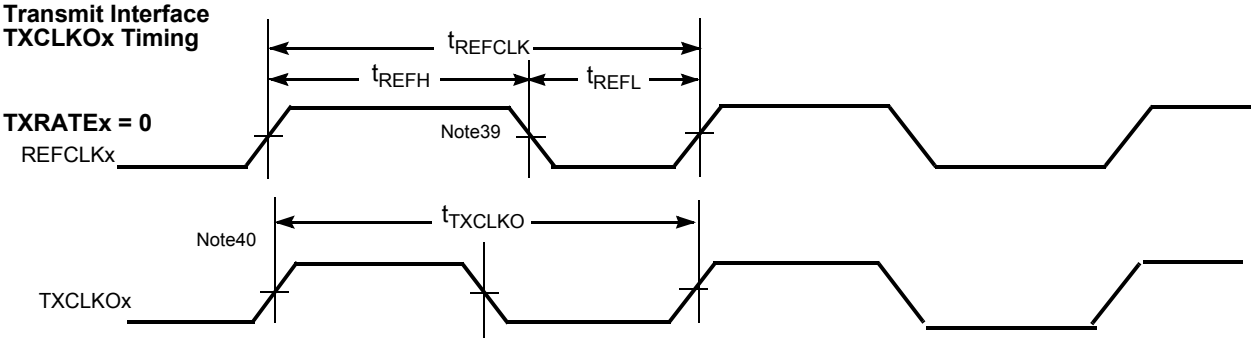
Transmit Interface TXCLKOx Timing

TXRATEx = 1



Transmit Interface TXCLKOx Timing

TXRATEx = 0

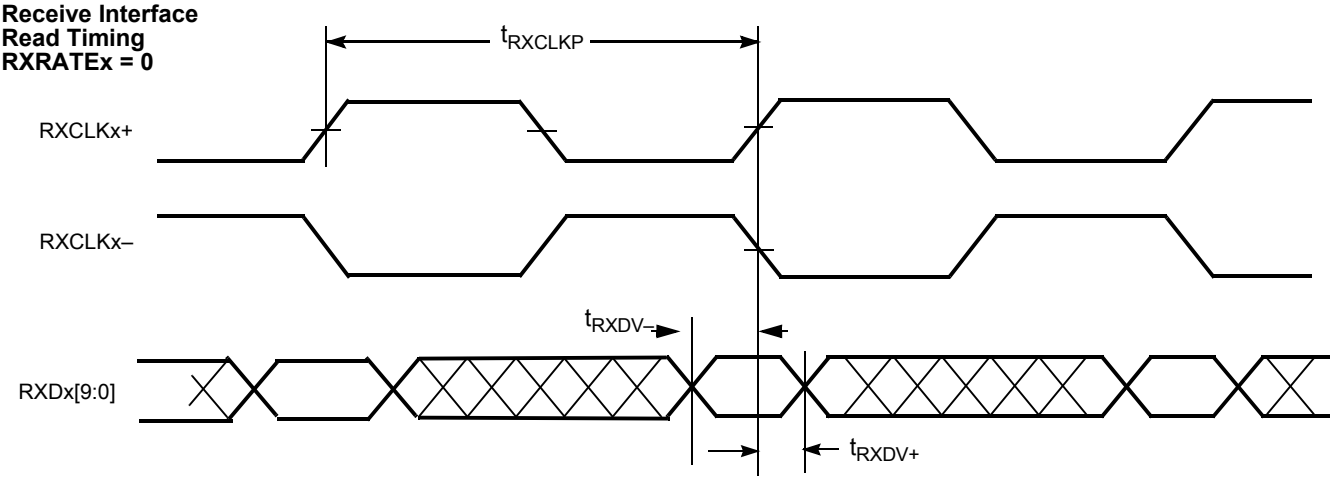


Notes

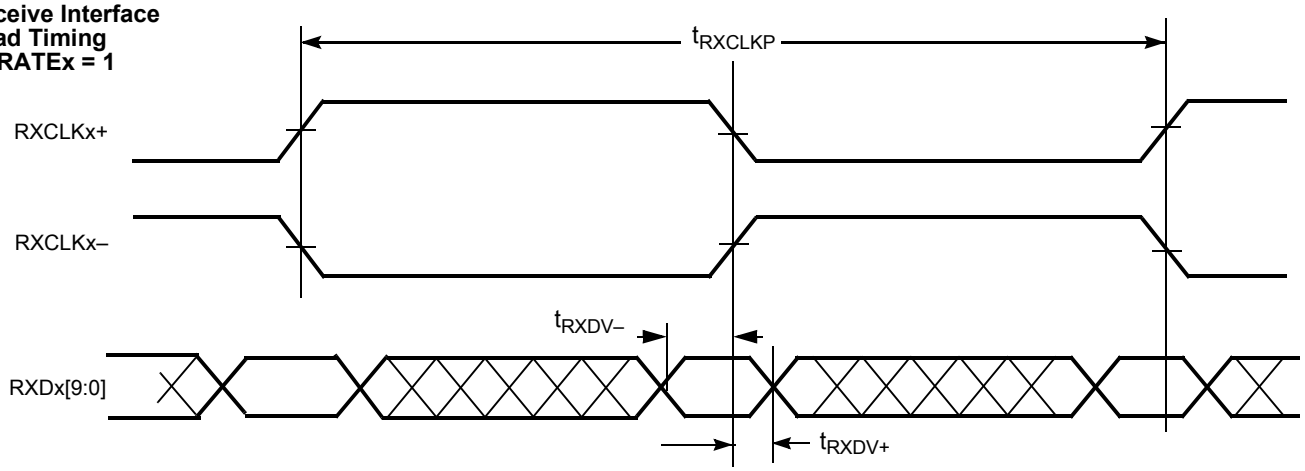
38. When REFCLKx± is configured for half-rate operation (TXRATEx = 1) and data is captured using REFCLKx instead of a TXCLKx clock. Data is captured using both the rising and falling edges of REFCLKx.
39. The TXCLKOx output remains at the character rate regardless of the state of TXRATEx and does not follow the duty cycle of REFCLKx±.
40. The rising edge of TXCLKOx output has no direct phase relationship to the REFCLKx± input.

Switching Waveforms for the CYV15G0204TRB HOTLink II Receiver

Receive Interface Read Timing RXRATEx = 0



Receive Interface Read Timing RXRATEx = 1



Bus Configuration Write Timing

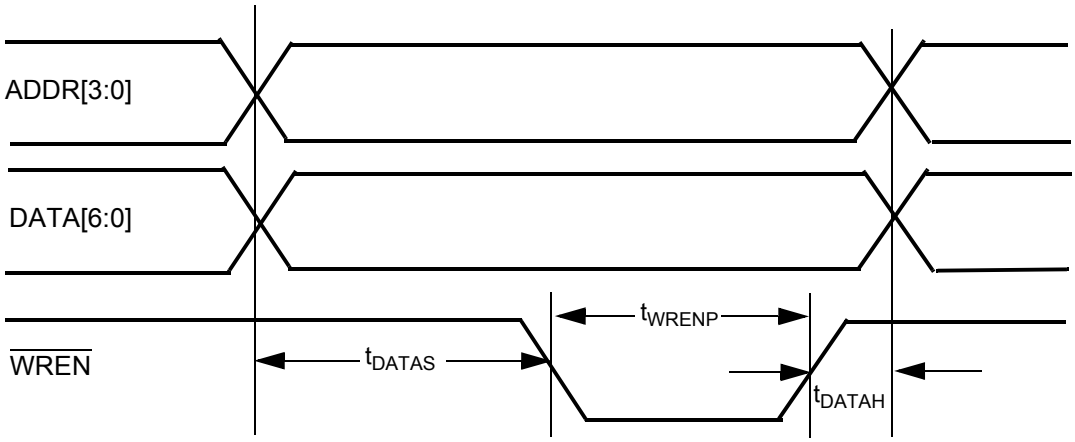


Table 7. Package Coordinate Signal Allocation

Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type
A01	INC1–	CML IN	C07	ULCC	LVTTL IN PU	F17	NC	NO CONNECT
A02	ROUTC1–	CML OUT	C08	GND	GROUND	F18	NC	NO CONNECT
A03	INC2–	CML IN	C09	DATA[6]	LVTTL IN PU	F19	TXCLKOB	LVTTL OUT
A04	ROUTC2–	CML OUT	C10	DATA[4]	LVTTL IN PU	F20	NC	NO CONNECT
A05	VCC	POWER	C11	DATA[2]	LVTTL IN PU	G01	GND	GROUND
A06	IND1–	CML IN	C12	DATA[0]	LVTTL IN PU	G02	$\overline{\text{WREN}}$	LVTTL IN PU
A07	ROUTD1–	CML OUT	C13	GND	GROUND	G03	GND	GROUND
A08	GND	GROUND	C14	NC	NO CONNECT	G04	GND	GROUND
A09	IND2–	CML IN	C15	SPDSELD	3-LEVEL SEL	G17	SPDSELB	3-LEVEL SEL
A10	ROUTD2–	CML OUT	C16	VCC	POWER	G18	NC	NO CONNECT
A11	GND	GROUND	C17	LDTDEN	LVTTL IN PU	G19	SPDSELA	3-LEVEL SEL
A12	TOUTA1–	CML OUT	C18	TRST	LVTTL IN PU	G20	NC	NO CONNECT
A13	GND	GROUND	C19	GND	GROUND	H01	GND	GROUND
A14	GND	GROUND	C20	TDO	LVTTL 3-S OUT	H02	GND	GROUND
A15	TOUTA2–	CML OUT	D01	TCLK	LVTTL IN PD	H03	GND	GROUND
A16	VCC	POWER	D02	RESET	LVTTL IN PU	H04	GND	GROUND
A17	VCC	POWER	D03	INSELD	LVTTL IN	H17	GND	GROUND
A18	TOUTB1–	CML OUT	D04	VCC	POWER	H18	GND	GROUND
A19	VCC	POWER	D05	VCC	POWER	H19	GND	GROUND
A20	TOUTB2–	CML OUT	D06	VCC	POWER	H20	GND	GROUND
B01	INC1+	CML IN	D07	SPDSELC	3-LEVEL SEL	J01	GND	GROUND
B02	ROUTC1+	CML OUT	D08	GND	GROUND	J02	GND	GROUND
B03	INC2+	CML IN	D09	DATA[5]	LVTTL IN PU	J03	GND	GROUND
B04	ROUTC2+	CML OUT	D10	DATA[3]	LVTTL IN PU	J04	GND	GROUND
B05	VCC	POWER	D11	DATA[1]	LVTTL IN PU	J17	NC	NO CONNECT
B06	IND1+	CML IN	D12	GND	GROUND	J18	NC	NO CONNECT
B07	ROUTD1+	CML OUT	D13	GND	GROUND	J19	NC	NO CONNECT
B08	GND	GROUND	D14	GND	GROUND	J20	NC	NO CONNECT
B09	IND2+	CML IN	D15	NC	NO CONNECT	K01	RXDC[4]	LVTTL OUT
B10	ROUTD2+	CML OUT	D16	VCC	POWER	K02	TRGCLKC–	PECL IN
B11	NC	NO CONNECT	D17	NC	NO CONNECT	K03	GND	GROUND
B12	TOUTA1+	CML OUT	D18	VCC	POWER	K04	GND	GROUND
B13	GND	GROUND	D19	SCANEN2	LVTTL IN PD	K17	NC	NO CONNECT
B14	NC	NO CONNECT	D20	TMEN3	LVTTL IN PD	K18	NC	NO CONNECT
B15	TOUTA2+	CML OUT	E01	VCC	POWER	K19	NC	NO CONNECT
B16	VCC	POWER	E02	VCC	POWER	K20	NC	NO CONNECT
B17	NC	NO CONNECT	E03	VCC	POWER	L01	RXDC[5]	LVTTL OUT
B18	TOUTB1+	CML OUT	E04	VCC	POWER	L02	TRGCLKC+	PECL IN
B19	NC	NO CONNECT	E17	VCC	POWER	L03	LFIC	LVTTL OUT
B20	TOUTB2+	CML OUT	E18	VCC	POWER	L04	GND	GROUND
C01	TDI	LVTTL IN PU	E19	VCC	POWER	L17	NC	NO CONNECT
C02	TMS	LVTTL IN PU	E20	VCC	POWER	L18	NC	NO CONNECT
C03	INSELC	LVTTL IN	F01	RXDC[8]	LVTTL OUT	L19	NC	NO CONNECT

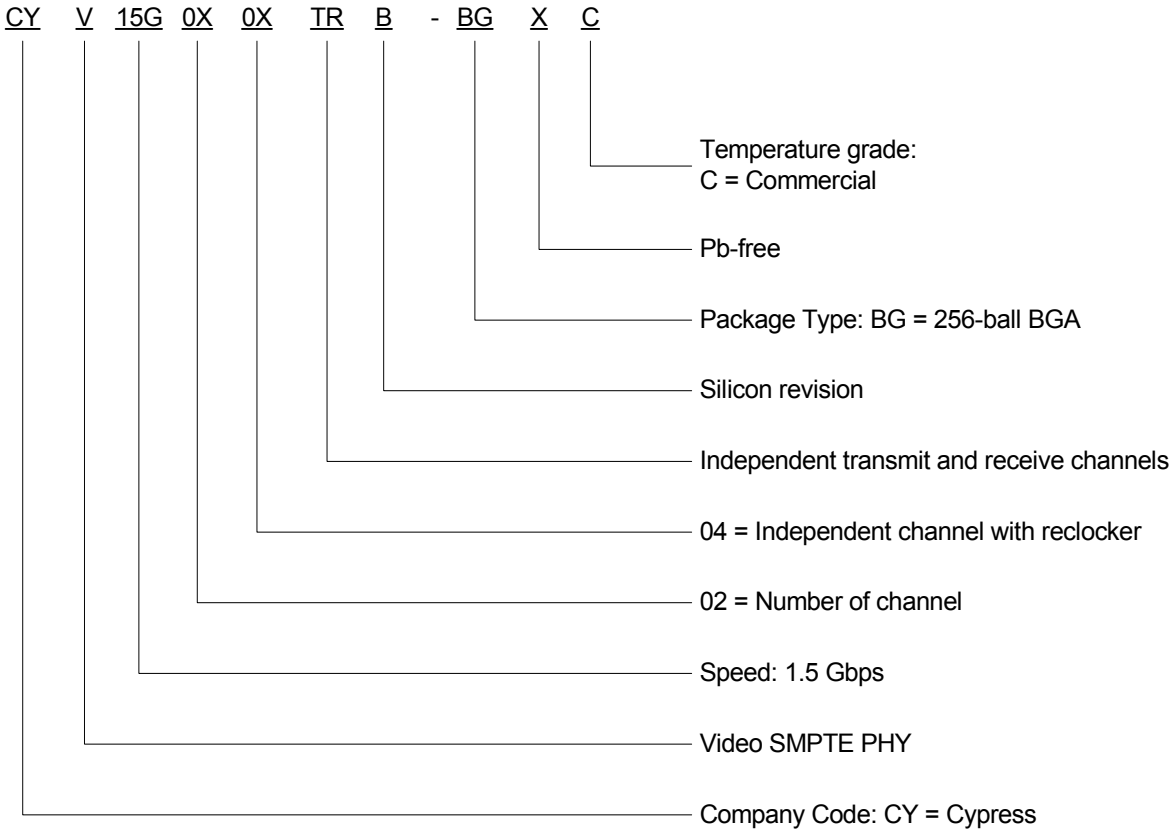
Table 7. Package Coordinate Signal Allocation (continued)

Ball ID	Signal Name	Signal Type
C04	VCC	POWER
C05	VCC	POWER
C06	ULCD	LVTTL IN PU
M03	VCC	POWER
M04	REPDOC	LVTTL OUT
M17	REFCLKB+	PECL IN
M18	REFCLKB–	PECL IN
M19	TXERRB	LVTTL OUT
M20	TXCLKB	LVTTL IN PD
N01	GND	GROUND
N02	GND	GROUND
N03	GND	GROUND
N04	GND	GROUND
N17	GND	GROUND
N18	GND	GROUND
N19	GND	GROUND
N20	GND	GROUND
P01	RXDC[3]	LVTTL OUT
P02	RXDC[2]	LVTTL OUT
P03	RXDC[1]	LVTTL OUT
P04	RXDC[0]	LVTTL OUT
P17	TXDB[5]	LVTTL IN
P18	TXDB[4]	LVTTL IN
P19	TXDB[3]	LVTTL IN
P20	TXDB[2]	LVTTL IN
R01	BISTSTC	LVTTL OUT
R02	RECLKOC	LVTTL OUT
R03	RXCLKC+	LVTTL OUT
R04	RXCLKC–	LVTTL OUT
R17	TXDB[1]	LVTTL IN
R18	TXDB[0]	LVTTL IN
R19	TXDB[9]	LVTTL IN
R20	TXDB[7]	LVTTL IN
T01	VCC	POWER
T02	VCC	POWER
T03	VCC	POWER
T04	VCC	POWER
T17	VCC	POWER
T18	VCC	POWER
T19	VCC	POWER
T20	VCC	POWER
U01	VCC	POWER
U02	VCC	POWER
F02	RXDC[9]	LVTTL OUT
F03	VCC	POWER
F04	VCC	POWER
U03	VCC	POWER
U04	VCC	POWER
U05	VCC	POWER
U06	RXDD[4]	LVTTL OUT
U07	RXDD[3]	LVTTL OUT
U08	GND	GROUND
U09	TXDA[9]	LVTTL IN
U10	ADDR [0]	LVTTL IN PU
U11	TRGCLKD–	PECL IN
U12	TXDA[1]	LVTTL IN
U13	GND	GROUND
U14	TXDA[4]	LVTTL IN
U15	TXDA[8]	LVTTL IN
U16	VCC	POWER
U17	NC	NO CONNECT
U18	TXDB[8]	LVTTL IN
U19	NC	NO CONNECT
U20	NC	NO CONNECT
V01	VCC	POWER
V02	VCC	POWER
V03	VCC	POWER
V04	RXDD[8]	LVTTL OUT
V05	VCC	POWER
V06	RXDD[5]	LVTTL OUT
V07	RXDD[1]	LVTTL OUT
V08	GND	GROUND
V09	BISTSTD	LVTTL OUT
V10	ADDR [2]	LVTTL IN PU
V11	TRGCLKD+	PECL IN
V12	TXCLKOA	LVTTL OUT
V13	GND	GROUND
V14	TXDA[3]	LVTTL IN
V15	TXDA[7]	LVTTL IN
V16	VCC	POWER
V17	NC	NO CONNECT
V18	NC	NO CONNECT
V19	NC	NO CONNECT
V20	NC	NO CONNECT
W01	VCC	POWER
W02	VCC	POWER
L20	TXDB[6]	LVTTL IN
M01	RXDC[6]	LVTTL OUT
M02	RXDC[7]	LVTTL OUT
W03	$\overline{\text{LFID}}$	LVTTL OUT
W04	RXCLKD–	LVTTL OUT
W05	VCC	POWER
W06	RXDD[6]	LVTTL OUT
W07	RXDD[0]	LVTTL OUT
W08	GND	GROUND
W09	ADDR [3]	LVTTL IN PU
W10	ADDR [1]	LVTTL IN PU
W11	NC	NO CONNECT
W12	TXERRA	LVTTL OUT
W13	GND	GROUND
W14	TXDA[2]	LVTTL IN
W15	TXDA[6]	LVTTL IN
W16	VCC	POWER
W17	NC	NO CONNECT
W18	REFCLKA+	PECL IN
W19	NC	NO CONNECT
W20	NC	NO CONNECT
Y01	VCC	POWER
Y02	VCC	POWER
Y03	RXDD[9]	LVTTL OUT
Y04	RXCLKD+	LVTTL OUT
Y05	VCC	POWER
Y06	RXDD[7]	LVTTL OUT
Y07	RXDD[2]	LVTTL OUT
Y08	GND	GROUND
Y09	RECLKOD	LVTTL OUT
Y10	NC	NO CONNECT
Y11	TXCLKA	LVTTL IN PD
Y12	NC	NO CONNECT
Y13	GND	GROUND
Y14	TXDA[0]	LVTTL IN
Y15	TXDA[5]	LVTTL IN
Y16	VCC	POWER
Y17	REPDOD	LVTTL OUT
Y18	REFCLKA–	PECL IN
Y19	NC	NO CONNECT
Y20	NC	NO CONNECT

Ordering Information

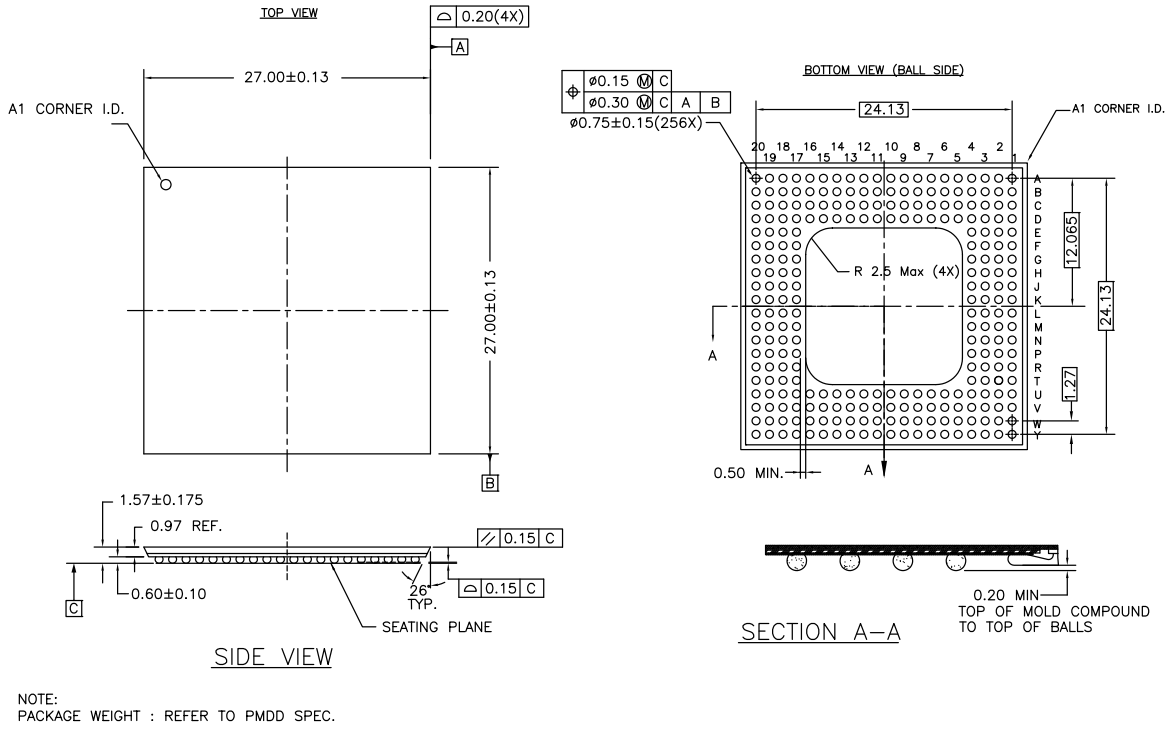
Speed	Ordering Code	Package Name	Package Type	Operating Range
Standard	CYV15G0204TRB-BGXC	BJ256	Pb-free 256-ball thermally enhanced ball grid array	Commercial

Ordering Code Definitions



Package Diagram

Figure 3. 256-pin L2 Ball Grid Array (27 × 27 × 1.57 mm) BJ256



NOTE:
PACKAGE WEIGHT : REFER TO PMDD SPEC.

51-85123 *I

Acronyms

The following table lists the acronyms that are used in this document.

Table 8. Acronyms Used in this Datasheet

Acronym	Description
BGA	ball grid array
BIST	built-in self test
I/O	input/output
JTAG	joint test action group
PLL	phase-locked loop
TMS	test mode select
TDO	test data out
TDI	test data in

Document Conventions

Units of Measure

Table 9. Units of Measure

Acronym	Description
°C	degree Celsius
kΩ	Kilo ohm
µA	microampere
µs	microsecond
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CYV15G0204TRB, Independent Clock HOTLink II™ Dual Serializer and Dual Reclocking Deserializer Document Number: 38-02101				
Revision	**ECN**	**Origin of Change**	**Submission Date**	**Description of Change**
**	244348	FRE	See ECN	New data sheet
*A	338721	SUA	See ECN	Added Pb-free package option availability
*B	384307	AGT	See ECN	Revised setup and hold times (t_{TXDH}, t_{TREFDS}, t_{TREFDH}, t_{RXDv-}, t_{RXDv+})
*C	1034060	UKK	See ECN	Added clarification for the necessity of JTAG controller reset and the methods to implement it.
*D	2897032	CGX	03/19/10	Removed inactive parts from Ordering Information. Updated Packaging Information
*E	3334793	SAAC	08/23/11	Added ordering code definitions. Added acronyms, and units of measure. Package name changed from BL256 to BJ256. Updated package diagram spec 51-85123 from *F to *G revision. Updated template according to current Cypress standards.
*F	4497471	YLIU	09/09/2014	Updated Package Diagram: spec 51-85123 – Changed revision from *G to *I. Updated in new template. Completing Sunset Review.

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