CSD17559Q5 30-V N-Channel NexFET™ Power MOSFET

1 Features

- Extremely Low Resistance
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5 mm × 6 mm Plastic Package

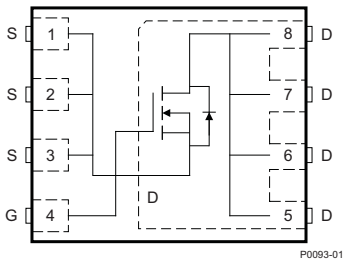
2 Applications

- Point of Load Synchronous Buck in Networking, Telecom, and Computing Systems
- Synchronous Rectification
- Active ORing and Hotswap Applications

3 Description

This 30 V, 0.95 mΩ, 5 × 6 mm SON NexFET™ power MOSFET is designed to minimize losses in synchronous rectification and other power conversion applications.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5 V)	39		nC
Q_{gd}	Gate Charge Gate-to-Drain	9.3		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V	1.15	mΩ
		V_{GS} = 10 V	0.95	mΩ
$V_{GS(th)}$	Threshold Voltage	1.4		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD17559Q5	2500	13-Inch Reel	SON 5 × 6 mm Plastic Package	Tape and Reel
CSD17559Q5T	250	13-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

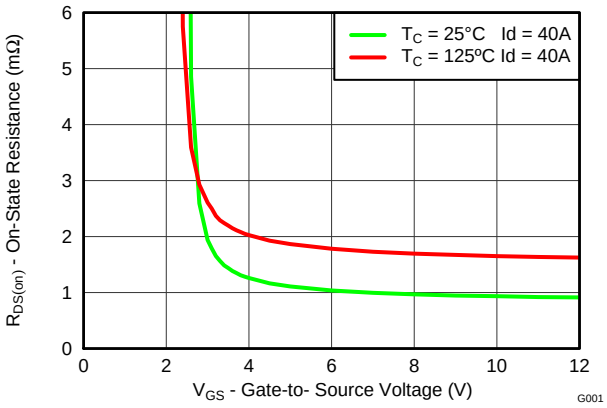
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	100	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	257	A
	Continuous Drain Current(1)	40	A
I_{DM}	Pulsed Drain Current(2)	400	A
P_D	Power Dissipation(1)	3.2	W
	Power Dissipation, T_C = 25°C	96	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 104 A, L = 0.1m H, R_G = 25 Ω	541	mJ

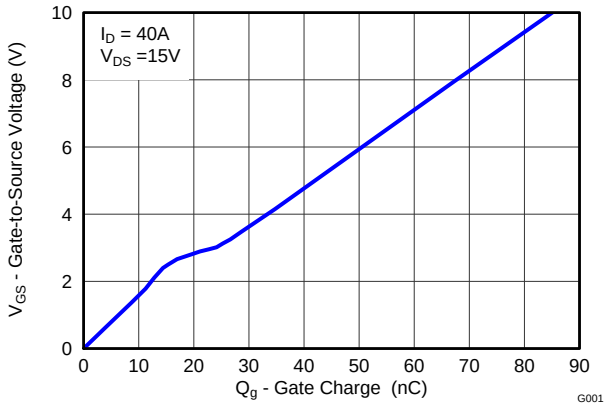
(1) Typical $R_{\theta JA}$ = 40°C/W on 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 0.06 inch (1.52 mm) thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 1.2°C/W, pulse duration ≤100 µs, duty cycle ≤1%

$R_{DS(on)}$ vs V_{GS}



Gate Charge



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4 Revision History

Changes from Original (Novermber 2012) to Revision A	Page
•	1
• Added small reel information	1
• Increased max pulsed drain current to 400 A	1
• Added line for max power dissipation with case temperature held to 25º	1
• Updated max pulsed current conditions	1
• Updated Figure 1 to a normalized $R_{\theta JC}$ curve	4
• Updated the SOA in Figure 10	6

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

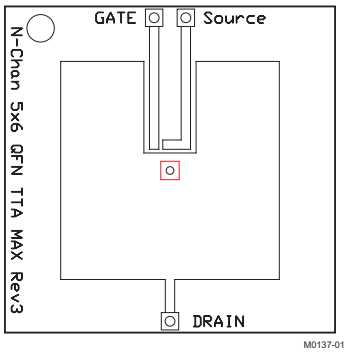
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = 250 µA	30			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 24 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	1.2	1.4	1.7	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V, I_{DS} = 40 A		1.15	1.5	mΩ
		V_{GS} = 10 V, I_{DS} = 40 A		0.95	1.15	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_{DS} = 40 A		235		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		7070	9200	pF
C_{oss}	Output Capacitance			1780	2314	pF
C_{rss}	Reverse Transfer Capacitance			87	113	pF
R_G	Series Gate Resistance			1.2	2.4	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 15 V, I_{DS} = 40 A		39	51	nC
Q_{gd}	Gate Charge Gate-to-Drain			9.3		nC
Q_{gs}	Gate Charge Gate-to-Source			14.4		nC
$Q_{g(th)}$	Gate Charge at V_{th}			8.3		nC
Q_{oss}	Output Charge	V_{DS} = 15 V, V_{GS} = 0 V		50		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 40 A, R_G = 2 Ω		20		ns
t_r	Rise Time			41		ns
$t_{d(off)}$	Turn Off Delay Time			32		ns
t_f	Fall Time			14		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 40 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD}= 15 V, I_F = 40 A, di/dt = 300 A/µs		80		nC
t_{rr}	Reverse Recovery Time			37		ns

5.2 Thermal Information

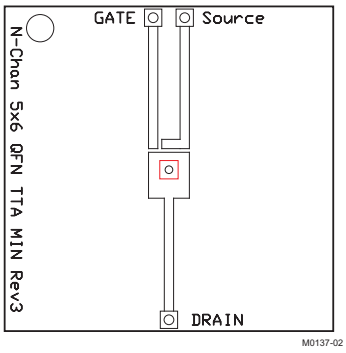
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance(1)			1.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)(2)			50	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

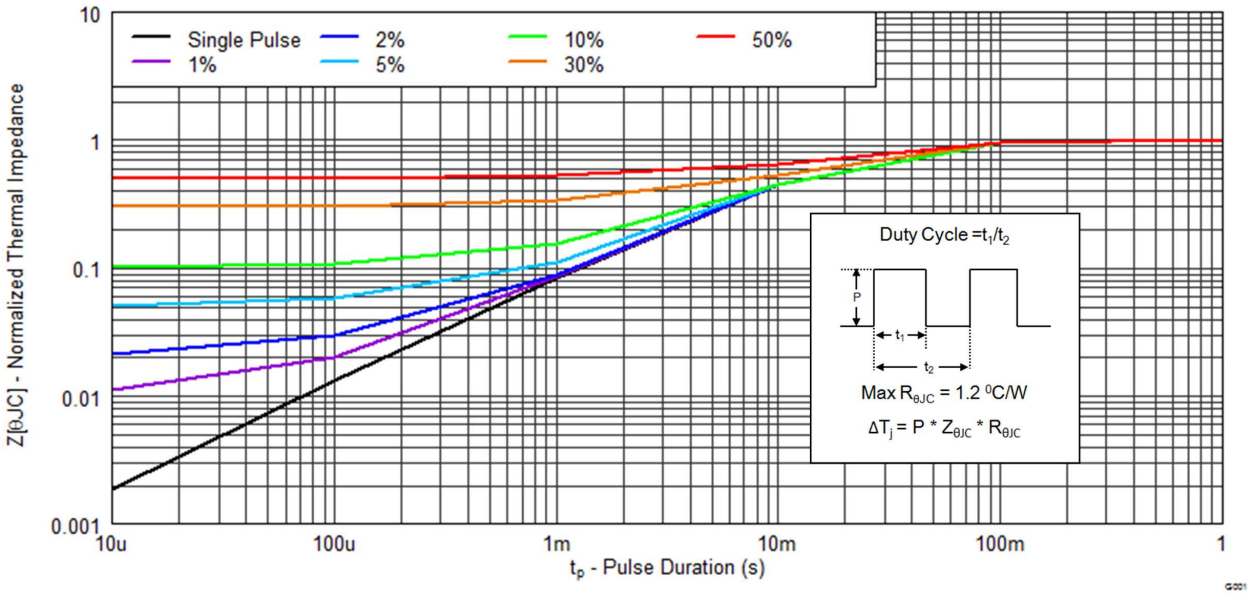


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

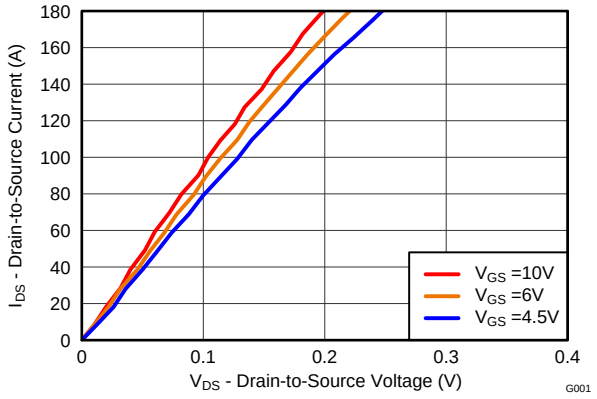


Figure 2. Saturation Characteristics

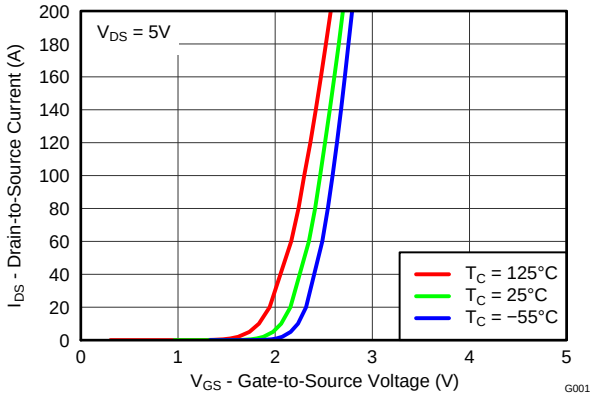


Figure 3. Transfer Characteristics

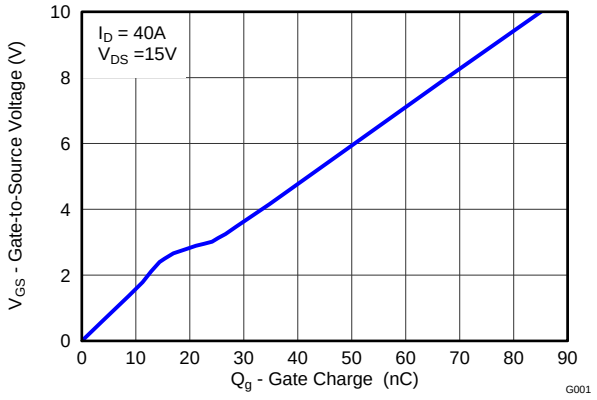


Figure 4. Gate Charge

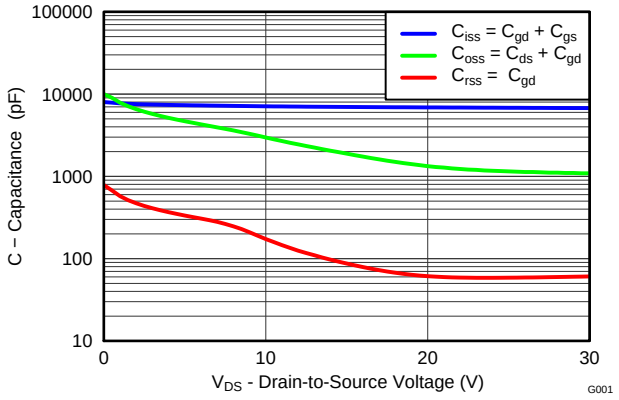


Figure 5. Capacitance

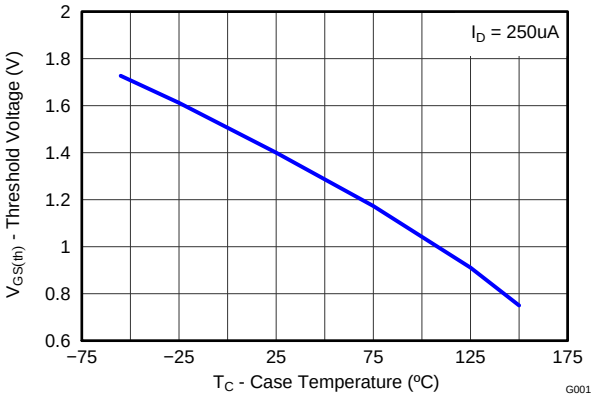


Figure 6. Threshold Voltage vs Temperature

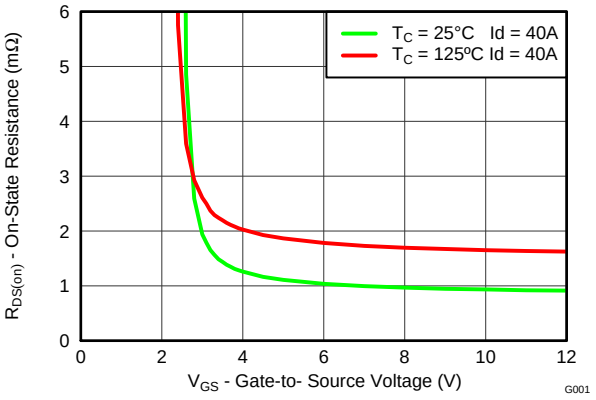


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

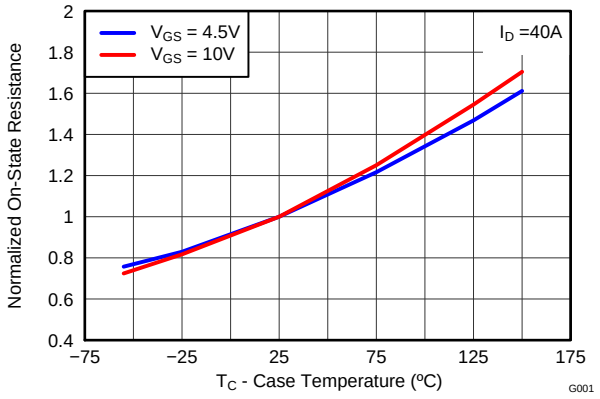


Figure 8. Normalized On-State Resistance vs Temperature

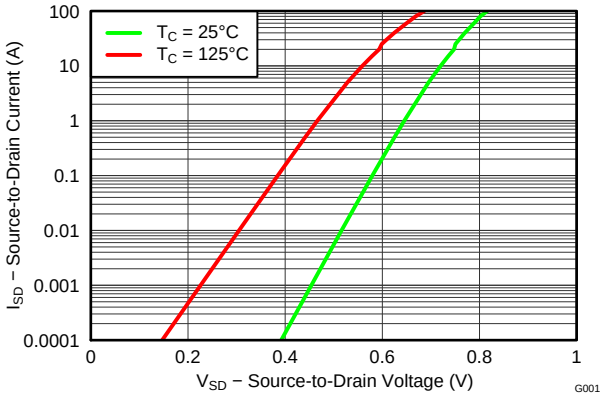


Figure 9. Typical Diode Forward Voltage

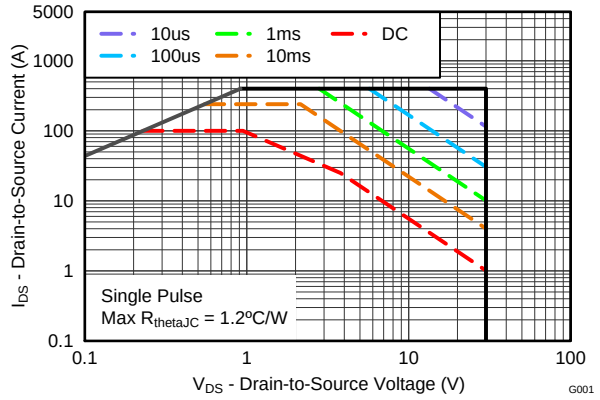


Figure 10. Safety Operating Area

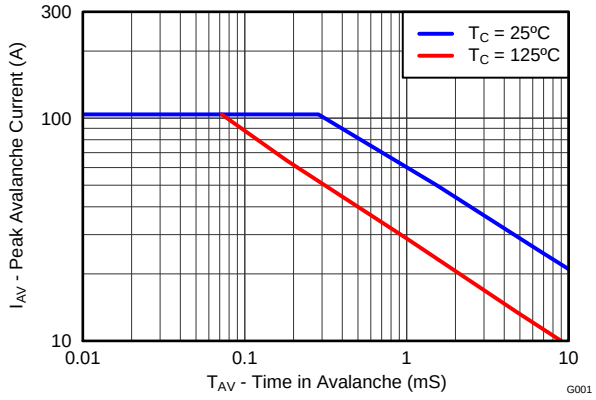


Figure 11. Single Pulse Unclamped Inductive Switching

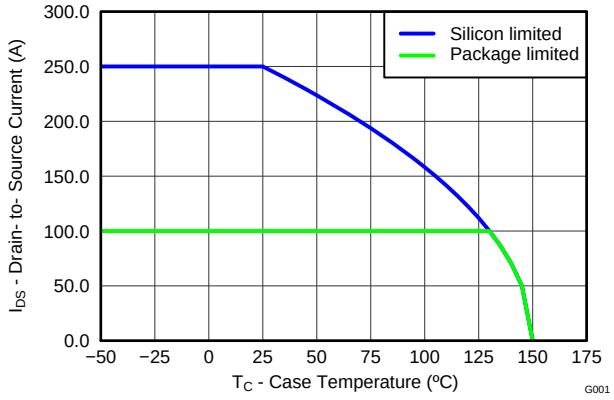


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

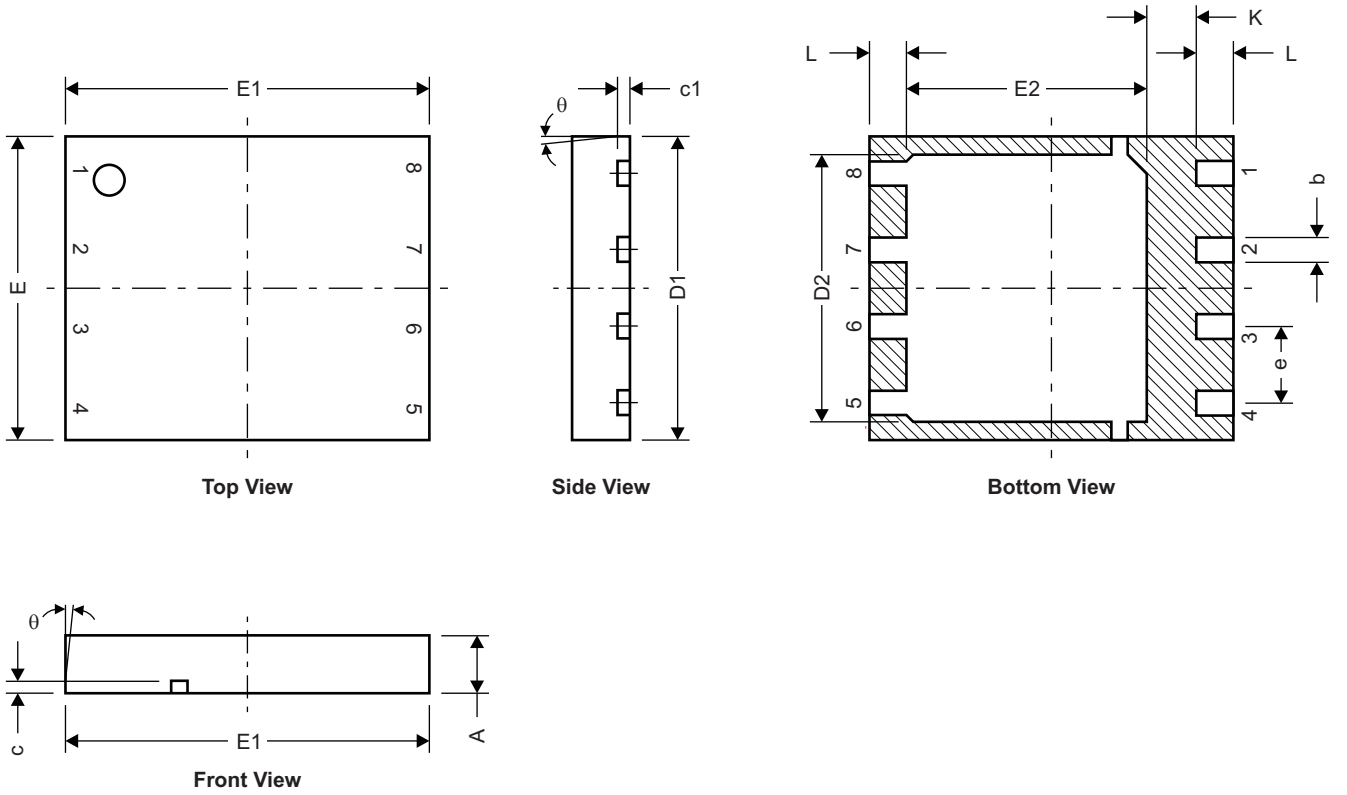
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

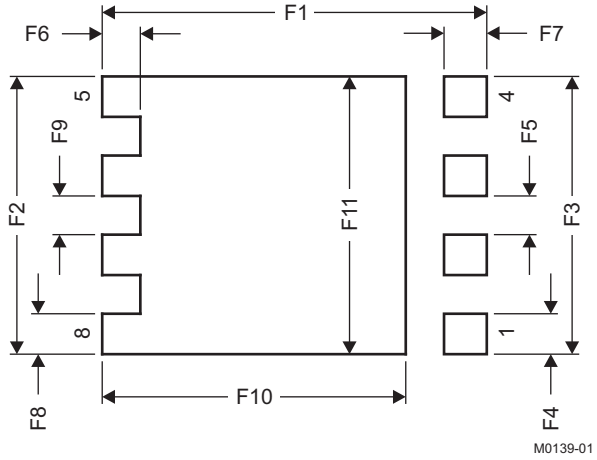
7.1 Q5 Package Dimensions



M0140-01

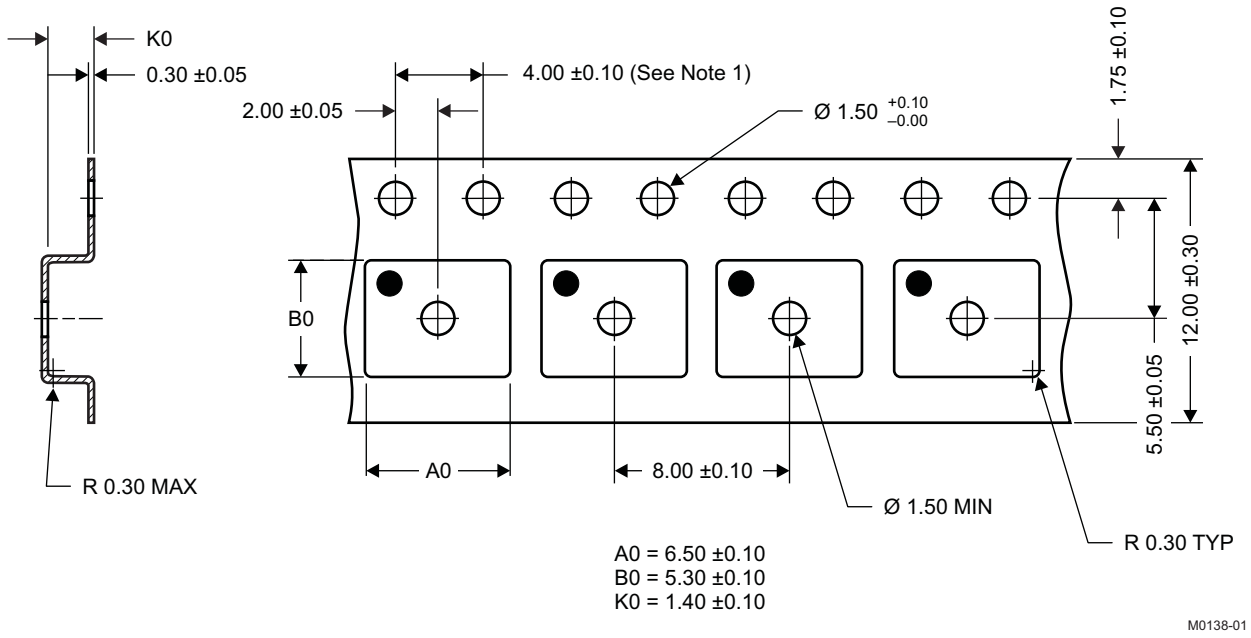
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
K	0.760		0.030	
L	0.510	0.710	0.020	0.028
θ	0.00	—	—	—

Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.460	4.560	0.176	0.180
F3	4.460	4.560	0.176	0.180
F4	0.650	0.700	0.026	0.028
F5	0.620	0.670	0.024	0.026
F6	0.630	0.680	0.025	0.027
F7	0.700	0.800	0.028	0.031
F8	0.650	0.700	0.026	0.028
F9	0.620	0.670	0.024	0.026
F10	4.900	5.000	0.193	0.197
F11	4.460	4.560	0.176	0.180

7.2 Q5 Tape and Reel Information

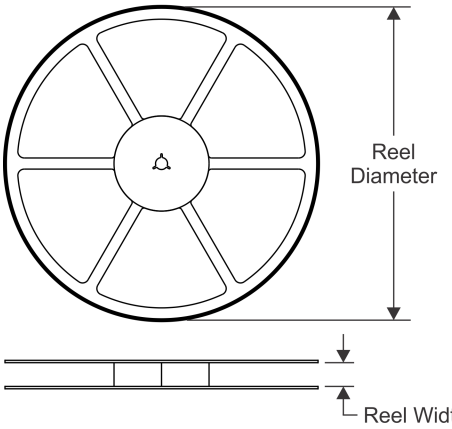


Notes:

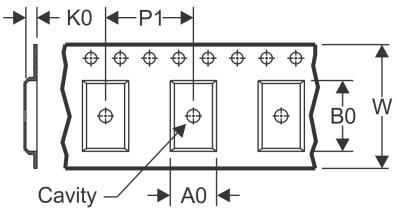
1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm, unless otherwise specified.
5. Thickness: 0.30 ±0.05 mm
6. MSL1 260°C (IR and convection) PbF-reflow compatible.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

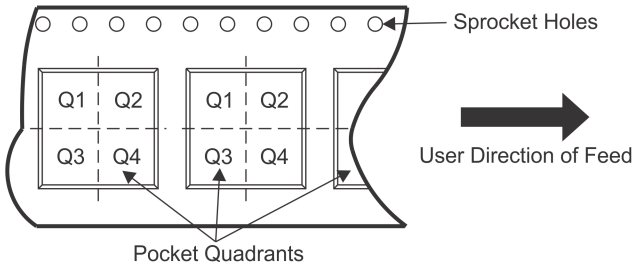


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

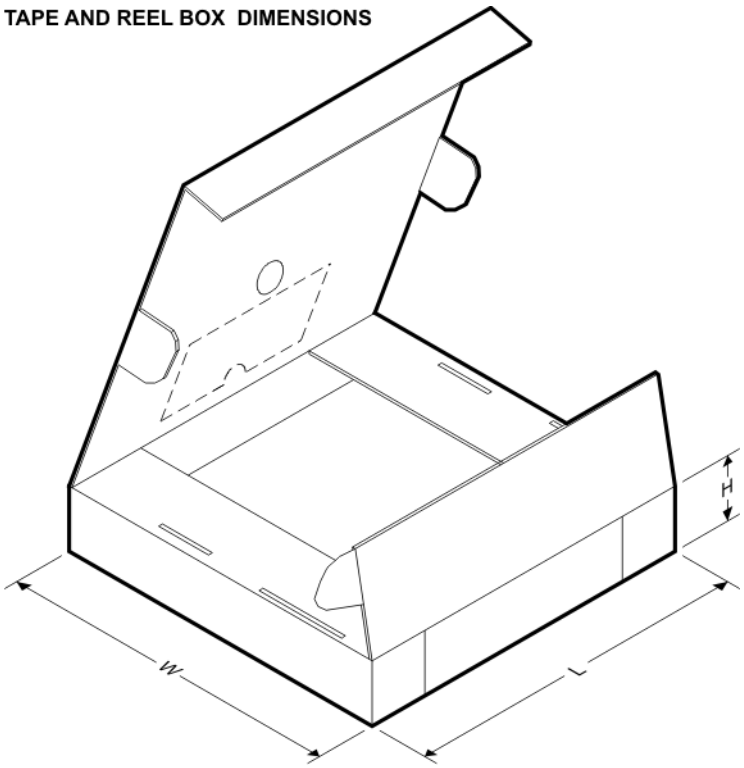
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17559Q5T	VSON-CLIP	DQH	8	250	330.0	12.8	6.5	5.3	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17559Q5T	VSON-CLIP	DQH	8	250	335.0	335.0	32.0

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