

# SN74LVTH162244-EP

## 3.3-V ABT 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCBS781 – NOVEMBER 2003

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Member of the Texas Instruments Widebus™ Family**
- **Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )**
- **Supports Unregulated Battery Operation Down To 2.7 V**
- **Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **$I_{off}$  and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

DGG PACKAGE  
(TOP VIEW)

1OE	1	48	2OE
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
$V_{CC}$	7	42	$V_{CC}$
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
$V_{CC}$	18	31	$V_{CC}$
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4OE	24	25	3OE

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

### description/ordering information

The SN74LVTH162244 is a 16-bit buffer and line driver designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. This device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.



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### description/ordering information (continued)

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

### ORDERING INFORMATION

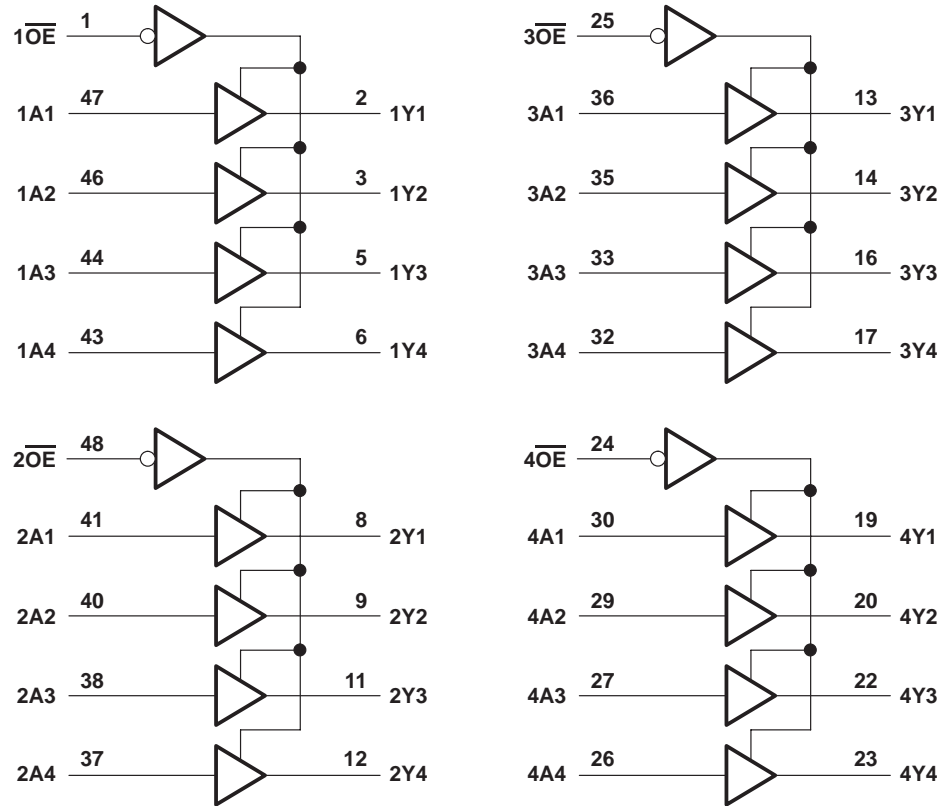
$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	CLVTH162244IDGGREP	LH162244EP

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_O$	30 mA
Current into any output in the high state, $I_O$ (see Note 2)	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3)	70°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  3. The package thermal impedance is calculated in accordance with JESD 51-7.

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### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage		5.5	V
$I_{OH}$	High-level output current		-12	mA
$I_{OL}$	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10 ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		$\mu$ s/V
$T_A$	Operating free-air temperature	-40	85	$^{\circ}$ C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 2.7$ V,	$I_I = -18$ mA			-1.2	V
$V_{OH}$	$V_{CC} = 3$ V,	$I_{OH} = -12$ mA	2			V
$V_{OL}$	$V_{CC} = 3$ V,	$I_{OL} = 12$ mA			0.8	V
$I_I$	Control inputs	$V_{CC} = 0$ or 3.6 V,			10	$\mu$ A
		$V_I = 5.5$ V				
		$V_{CC} = 3.6$ V,			$\pm 1$	
		$V_I = V_{CC}$ or GND				
	Data inputs	$V_{CC} = 3.6$ V			1	$\mu$ A
		$V_I = 0$			-5	
$I_{off}$	$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to 4.5 V			$\pm 100$	$\mu$ A
$I_{I(hold)}$	Data inputs	$V_{CC} = 3$ V		75		$\mu$ A
				-75		
		$V_{CC} = 3.6$ V‡,			500 -750	
		$V_I = 0$ to 3.6 V				
$I_{OZH}$	$V_{CC} = 3.6$ V,	$V_O = 3$ V			5	$\mu$ A
$I_{OZL}$	$V_{CC} = 3.6$ V,	$V_O = 0.5$ V			-5	$\mu$ A
$I_{OZPU}$	$V_{CC} = 0$ to 1.5 V, $V_O = 0.5$ V to 3 V, $\overline{OE} =$ don't care				$\pm 100$	$\mu$ A
$I_{OZPD}$	$V_{CC} = 1.5$ V to 0, $V_O = 0.5$ V to 3 V, $\overline{OE} =$ don't care				$\pm 100$	$\mu$ A
$I_{CC}$	$V_{CC} = 3.6$ V, $I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high			0.19	mA
		Outputs low			5	
		Outputs disabled			0.19	
$\Delta I_{CC}^{\S}$	$V_{CC} = 3$ V to 3.6 V, One input at $V_{CC} - 0.6$ V, Other inputs at $V_{CC}$ or GND				0.2	mA
$C_i$	$V_I = 3$ V or 0			4		pF
$C_o$	$V_O = 3$ V or 0			9		pF

† All typical values are at  $V_{CC} = 3.3$  V,  $T_A = 25^{\circ}$ C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.



switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$		UNIT
			MIN	TYP†	MAX	MIN	MAX	
$t_{PLH}$	A	Y	1.4	3.4	4	4.8		ns
$t_{PHL}$			1.2	2.9	3.6	4.1		
$t_{PZH}$	$\overline{OE}$	Y	1.2	3.9	5.1	6.5		ns
$t_{PZL}$			1.4	3.8	4.5	5.8		
$t_{PHZ}$	$\overline{OE}$	Y	2.2	4.4	5	5.4		ns
$t_{PLZ}$			2	4.2	5	5.4		
$t_{sk(o)}$					0.5			ns

† All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

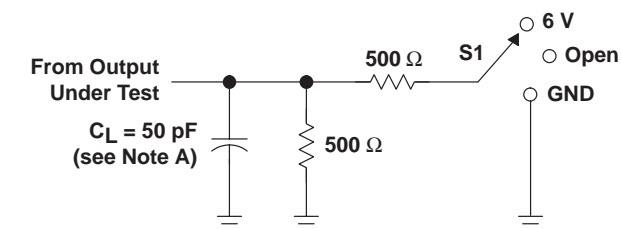
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### WITH 3-STATE OUTPUTS

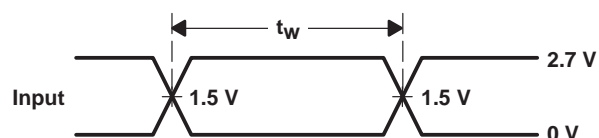
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#### PARAMETER MEASUREMENT INFORMATION

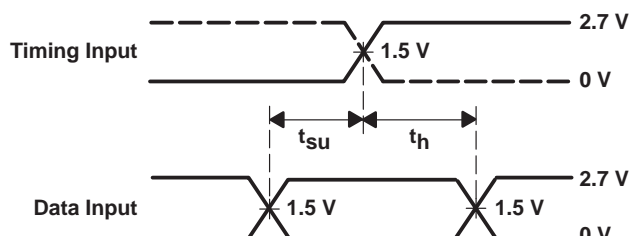


LOAD CIRCUIT

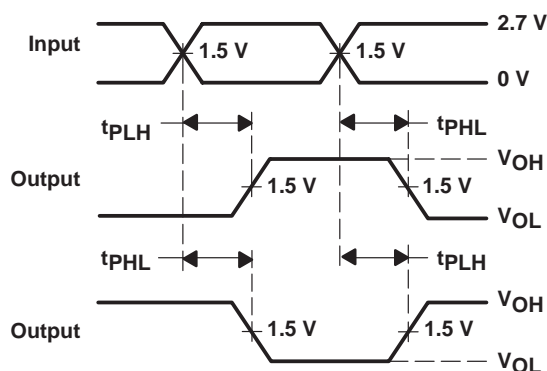
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



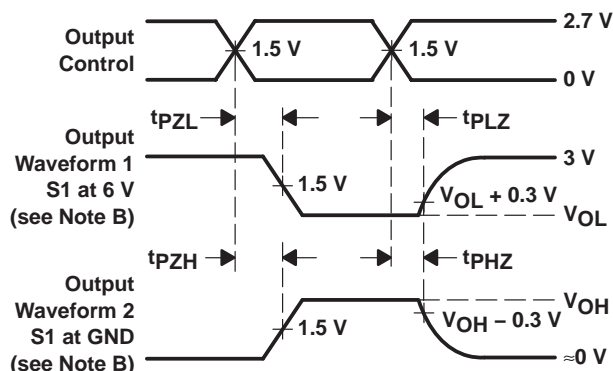
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CLVTH162244IDGGREP	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04708-01XE	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- Catalog: [SN74LVTH162244](#)
- Military: [SN54LVTH162244](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

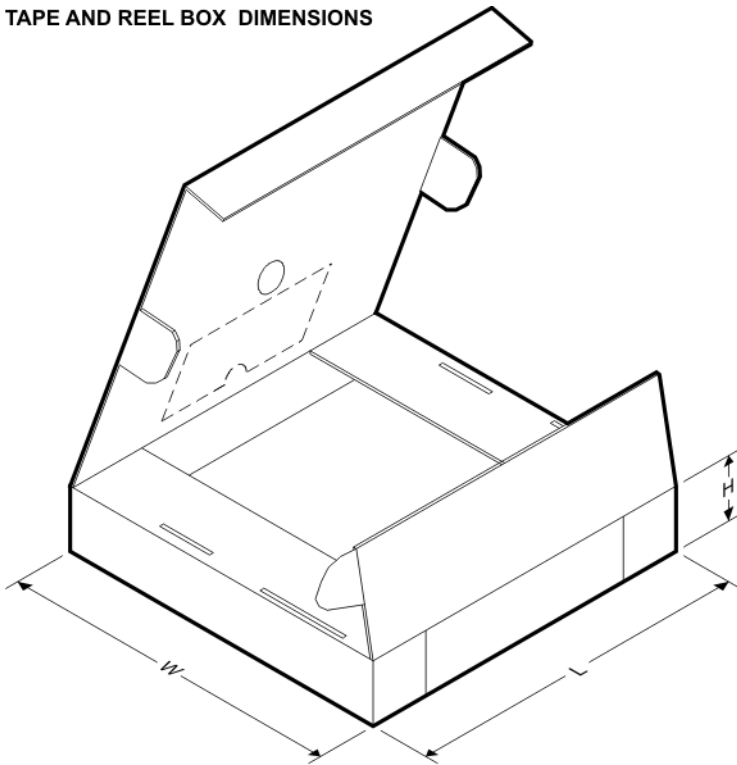


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVTH162244IDGGREP	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVTH162244IDGGREP	TSSOP	DGG	48	2000	346.0	346.0	41.0

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