

IR1168S
DUAL SMART RECTIFIER DRIVER IC

Features

- Secondary-side high speed controller for synchronous rectification in resonant half bridge topologies
- 200V proprietary IC technology
- Max 500KHz switching frequency
- Anti-bounce logic and UVLO protection
- 4A peak turn off drive current
- Micropower start-up & ultra low quiescent current
- 10.7V gate drive clamp
- 70ns turn-off propagation delay
- Wide Vcc operating range
- Direct sensing for both Synchronous Rectifiers
- Minimal component count
- Simple design
- Lead-free

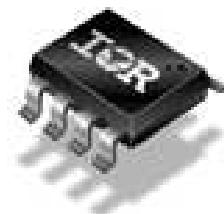
Typical Applications

- LCD & PDP TV, Telecom SMPS, AC-DC adapters

Product Summary

Topology	LLC Half-bridge
VD	200V
V _{OUT}	10.7V Clamped
I _{o+} & I _{o-} (typical)	+1A & -4A
Turn on Propagation Delay	60ns (typical)
Turn off Propagation Delay	70ns (typical)

Package Options



8-Lead SOIC

Typical Connection Diagram

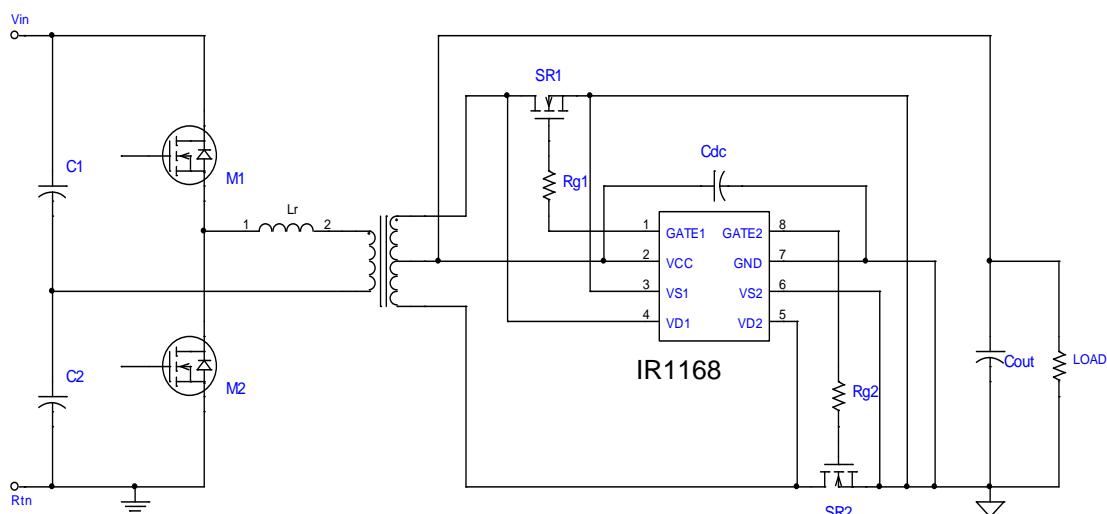


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Description

IR1168 is dual smart secondary-side rectifier driver IC designed to drive two N-Channel power MOSFETs used as synchronous rectifiers in resonant converter applications. The IC can control one or more paralleled N MOSFETs to emulate the behavior of Schottky diode rectifiers. The drain to source for each rectifier MOSFET voltage is sensed differentially to determine the level of the current and the power switch is turned ON and OFF in close proximity of the zero current transition. Ruggedness and noise immunity are accomplished using an advanced blanking scheme and double-pulse suppression that allows reliable operation in fixed and variable frequency applications.

Qualification Information[†]

Qualification Level		Industrial ^{††}	
Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.			
Moisture Sensitivity Level		SOIC8N	MSL2 ^{†††} 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class B (per JEDEC standard JESD22-A115)	
	Human Body Model	Class 2 (per EIA/JEDEC standard EIA/JESD22-A114)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

[†] Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

^{††} Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

^{†††} Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Parameters	Symbol	Min.	Max.	Units	Remarks
Supply Voltage	V_{CC}	-0.3	20	V	
Cont. Drain Sense Voltage	V_D	-3	200	V	
Pulse Drain Sense Voltage	V_D	-5	200	V	
Source Sense Voltage	V_S	-3	20	V	
Gate Voltage	V_{GATE}	-0.3	20	V	$V_{CC}=20V$, Gate off
Operating Junction Temperature	T_J	-40	150	°C	
Storage Temperature	T_S	-55	150	°C	
Thermal Resistance	$R_{\theta JA}$		128	°C/W	SOIC-8
Package Power Dissipation	P_D		970	mW	SOIC-8, $T_{AMB}=25°C$
Switching Frequency	fsw		500	kHz	

Electrical Characteristics

The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_J from -25°C to 125°C . Typical values represent the median values, which are related to 25°C . If not otherwise stated, a supply voltage of $V_{CC} = 15\text{ V}$ is assumed for test condition.

Supply Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Supply Voltage Operating Range	V_{CC}	8.6		18	V	GBD
V_{CC} Turn On Threshold	$V_{CC\ ON}$	7.5	8.1	8.5	V	
V_{CC} Turn Off Threshold (Under Voltage Lock Out)	$V_{CC\ UVLO}$	7	7.6	8	V	
V_{CC} Turn On/Off Hysteresis	$V_{CC\ HYST}$		0.5		V	
Operating Current	I_{CC}		14	18	mA	$C_{LOAD} = 1\text{nF}$, $f_{SW} = 400\text{kHz}$
			48	60	mA	$C_{LOAD} = 4.7\text{nF}$, $f_{SW} = 400\text{kHz}$
Quiescent Current	I_{QCC}		2.6	3.8	mA	
Start-up Current	$I_{CC\ START}$			140	μA	$V_{CC} = V_{CC\ ON} - 0.1\text{V}$

Comparator Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Turn-off Threshold	V_{TH1}	-12	-6	0	mV	
Turn-on Threshold	V_{TH2}	-220	-140	-80	mV	
Hysteresis	V_{HYST}		141		mV	
Input Bias Current	I_{IBIAS1}		1	10	μA	$V_D = -50\text{mV}$
Input Bias Current	I_{IBIAS2}		10	50	μA	$V_D = 200\text{V}$
Comparator Input Offset	V_{OFFSET}			2	mV	GBD

One-Shot Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Blanking pulse duration	t_{BLANK}	9	17	25	μs	
Reset Threshold	V_{TH3}		2.5		V	$V_{CC} = 10\text{V} - \text{GBD}$
			5.4		V	$V_{CC} = 20\text{V} - \text{GBD}$
Hysteresis	V_{HYST3}		40		mV	$V_{CC} = 10\text{V} - \text{GBD}$

Minimum On Time Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Minimum on time	T_{ONmin}	500	750	1000	ns	

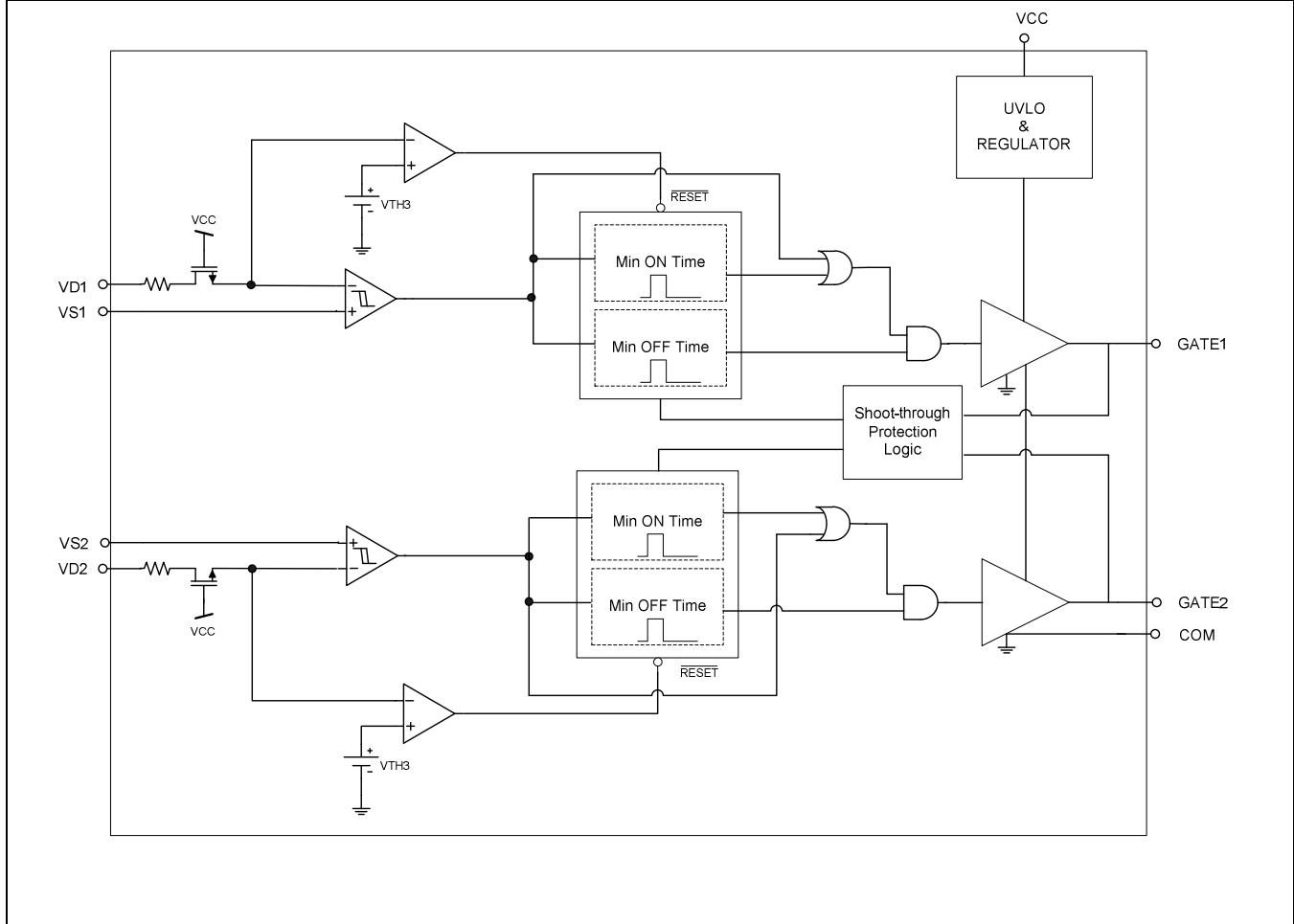
Electrical Characteristics

The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_J from -25°C to 125°C . Typical values represent the median values, which are related to 25°C . If not otherwise stated, a supply voltage of $V_{CC} = 15\text{ V}$ is assumed for test condition.

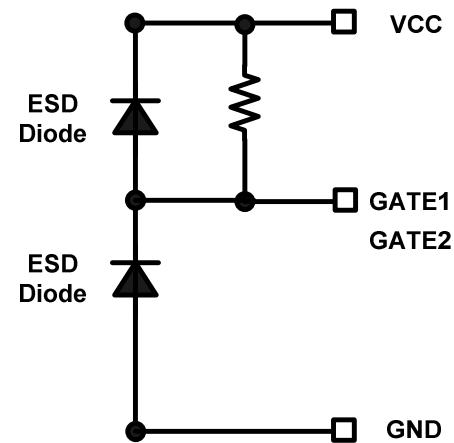
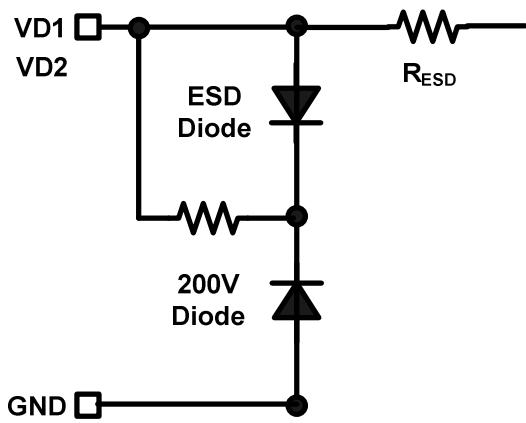
Gate Driver Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Gate Low Voltage	V_{GLO}		0.3	0.5	V	$I_{GATE} = 200\text{mA}$
Gate High Voltage	V_{GTH}	8.5	10.7	13.5	V	$V_{CC}=12\text{V-18V}$ (internally clamped)
Rise Time	t_{r1}		10		ns	$C_{LOAD} = 1\text{nF}$
	t_{r2}		80		ns	$C_{LOAD} = 4.7\text{nF}$
Fall Time	t_{f1}		5		ns	$C_{LOAD} = 1\text{nF}$
	t_{f2}		25		ns	$C_{LOAD} = 4.7\text{nF}$
Turn on Propagation Delay	t_{Don}		60	120	ns	$V_{DS} \text{ to } V_{GATE} - 100\text{mV}$ overdrive
Turn off Propagation Delay	t_{Doff}		70	120	ns	$V_{DS} \text{ to } V_{GATE} - 100\text{mV}$ overdrive
Pull up Resistance	r_{up}		5		Ω	$I_{GATE} = 15\text{mA} - \text{GBD}$
Pull down Resistance	r_{down}		1.2		Ω	$I_{GATE} = -200\text{mA}$
Output Peak Current (source)	I_{O_source}		1		A	$C_{LOAD} = 1\text{nF} - \text{GBD}$
Output Peak Current (sink)	I_{O_sink}		4		A	$C_{LOAD} = 1\text{nF} - \text{GBD}$

Functional Block Diagram



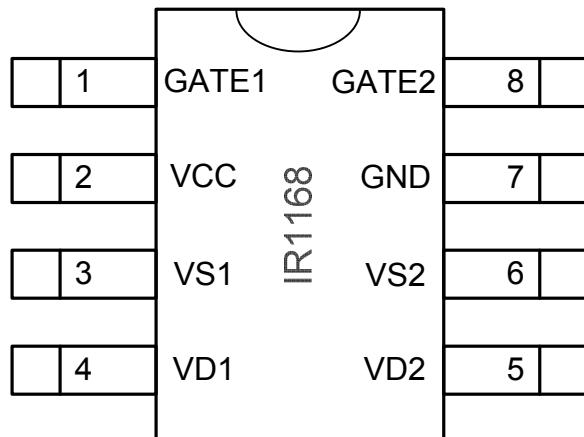
I/O Pin Equivalent Circuit Diagram



Lead Definitions

PIN#	Symbol	Description
1	GATE1	Gate Drive Output 1
2	VCC	Supply Voltage
3	VS1	Sync FET 1 Source Voltage Sense
4	VD1	Sync FET 1 Drain Voltage Sense
5	VD2	Sync FET 2 Drain Voltage Sense
6	VS2	Sync FET 2 Source Voltage Sense
7	GND	Analog and Power Ground
8	GATE2	Gate Drive Output 2

Lead Assignments



Detailed Pin Description

VCC: Power Supply

This is the supply voltage pin of the IC and it is monitored by the under voltage lockout circuit. It is possible to turn off the IC by pulling this pin below the minimum turn off threshold voltage, without damage to the IC.

To prevent noise problems, a bypass ceramic capacitor connected to Vcc and COM should be placed as close as possible to the IR1168. This pin is not internally clamped.

GND: Ground

This is ground potential pin of the integrated control circuit. The internal devices and gate driver are referenced to this point.

VD1 and VD2: Drain Voltage Sense

These are the two high-voltage pins used to sense the drain voltage of the two SR power MOSFETs. Routing between the drain of the MOSFET and the IC pin must be particularly optimized.

VS1 and VS2: Source Voltage Sense

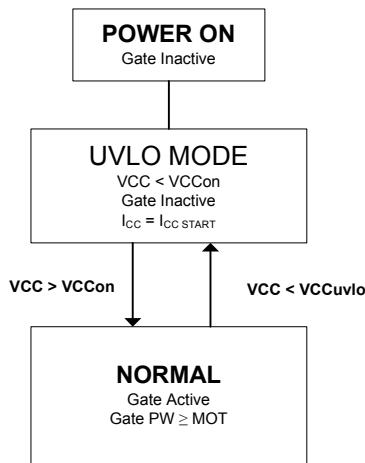
These are the two differential sense pins for the two source pins of the two SR power MOSFETs. This pin must not be connected directly to the GND pin (pin 7) but must be used to create a kelvin contact as close as possible to the power MOSFET source pin.

GATE1 and GATE2: Gate Drive Outputs

These are the two gate drive outputs of the IC. The gate voltage is internally clamped and has a +1A/-4A peak drive capability. Although this pin can be directly connected to the synchronous rectifier (SR) MOSFET gate, the use of gate resistor is recommended (specifically when putting multiple MOSFETs in parallel). Care must be taken in order to keep the gate loop as short and as small as possible in order to achieve optimal switching performance.

Application Information and Additional Details

State Diagram



UVLO Mode:

The IC is in the UVLO mode when the VCC pin voltage is below VCCUVLO. The UVLO mode is accessible from any other state of operation. In the UVLO state, most of the internal circuitry is unbiased and the IC draws a quiescent current of $I_{CC\ START}$.

The IC remains in the UVLO condition until the voltage on the VCC pin exceeds the VCC turn on threshold voltage, VCC ON.

Normal Mode:

The IC enters in normal operating mode once the UVLO voltage has been exceeded. At this point the gate driver are operating and the IC will draw a maximum of I_{CC} from the supply voltage source.

General Description

The IR1168 Dual Smart Rectifier controller IC is the industry first dedicated high-voltage controller IC for synchronous rectification in resonant converter applications. The IC can emulate the operation of the two secondary rectifier diodes by correctly driving the synchronous rectifier (SR) MOSFETs in the two secondary legs.

The core of this device are two high-voltage, high speed comparators which sense the drain to source voltage of the MOSFETs differentially. The device current is sensed using the R_{DSon} as a shunt resistance and the GATE pin of the MOSFET is driven accordingly. Dedicated internal logic then manages to turn the power device on and off in close proximity of the zero current transition.

IR1168 further simplifies synchronous rectifier control by offering the following power management features:

- Wide VCC operating range allows the IC to be directly powered from the converter output
- Shoot through protection logic that prevents both the GATE outputs from the IC to be high at the same time
- Device turn ON and OFF in close proximity of the zero current transition with low turn-on and turn-off propagation delays; eliminates reactive power flow between the output capacitors and power transformer
- Internally clamped gate driver outputs that significantly reduce gate losses.

The SmartRectifier™ control technique is based on sensing the voltage across the MOSFET and comparing it with two negative thresholds to determine the turn on and off transitions for the device. The rectifier current is sensed by the input comparators using the power MOSFET R_{DSon} as a shunt resistance and its GATE is driven depending on the level of the sensed voltage vs. the 3 thresholds shown below.

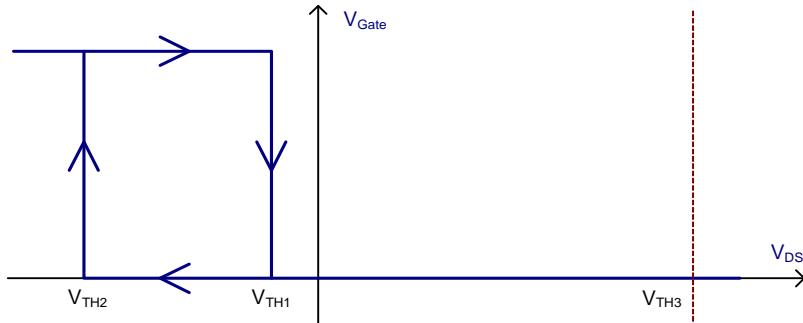


Figure 1: Input comparator thresholds

Turn-on phase

When the conduction phase of the SR FET is initiated, current will start flowing through its body diode, generating a negative V_{DS} voltage across it. The body diode has generally a much higher voltage drop than the one caused by the MOSFET on resistance and therefore will trigger the turn-on threshold V_{TH2} .

When V_{TH2} is triggered, IR1168 will drive the gate of MOSFET on which will in turn cause the conduction voltage V_{DS} to drop down to $I_D * R_{DSon}$. This drop is usually accompanied by some amount of ringing, that could trigger the input comparator to turn off; hence, a fixed Minimum On Time (MOT) blanking period is used that will maintain the power MOSFET on for a minimum amount of time.

The fixed MOT limits the minimum conduction time of the secondary rectifiers and hence, the maximum switching frequency of the converter.

Turn-off phase

Once the SR MOSFET has been turned on, it will remain on until the rectified current will decay to the level where V_{DS} will cross the turn-off threshold V_{TH1} .

Since the device currents are sinusoidal here, the device VDS will cross the V_{TH1} threshold with a relatively low dV/dt . Once the threshold is crossed, the current will start flowing again through the body diode, causing the VDS voltage to jump negative. Depending on the amount of residual current, VDS may once again trigger the turn-on threshold; hence, V_{TH2} is blanked for a time duration t_{BLANK} after V_{TH1} is triggered. When the device VDS crosses the positive reset threshold V_{TH3} , t_{BLANK} is terminated and the IC is ready for next conduction cycle as shown below.

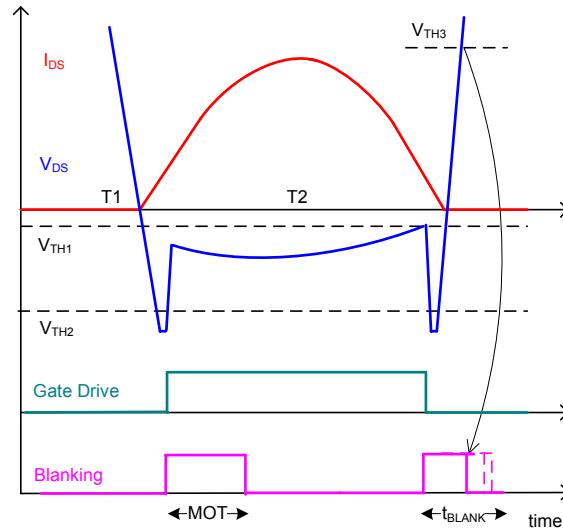


Figure 2: Secondary currents and voltages

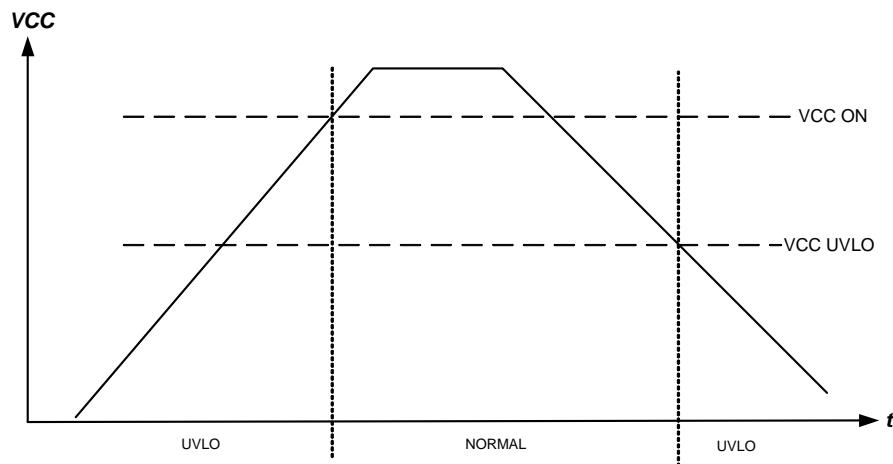


Figure 3: Vcc UVLO

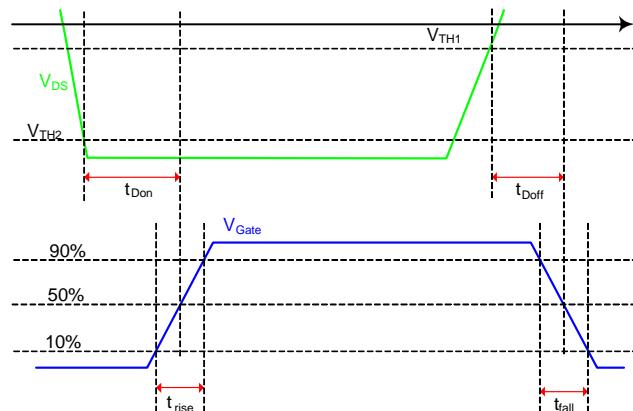


Figure 4: Timing waveform

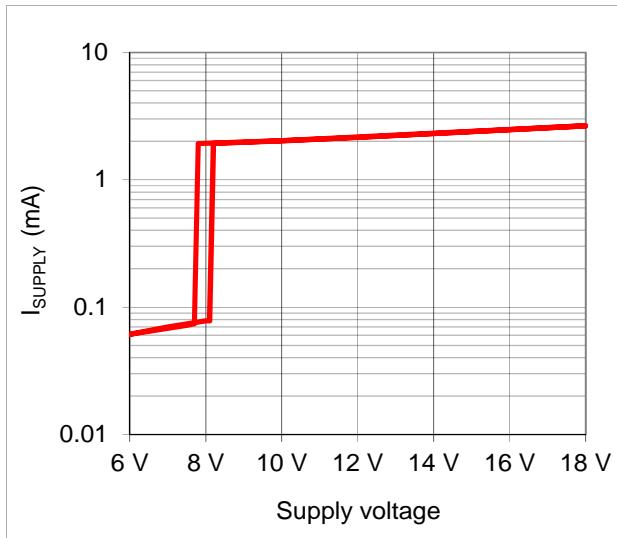


Figure 5: Supply Current vs. Supply Voltage

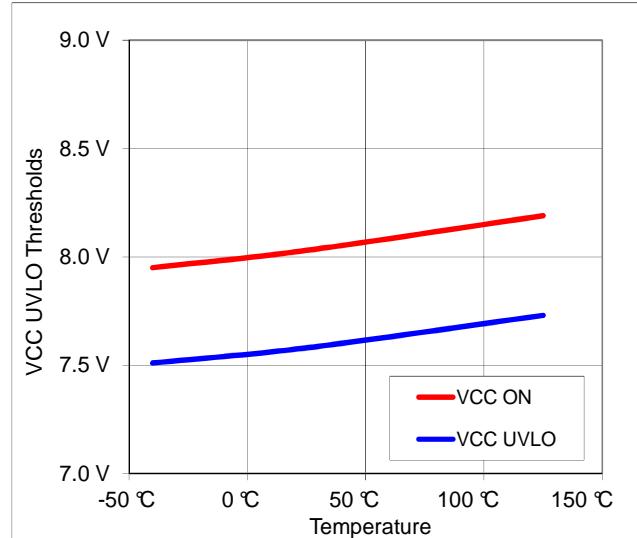


Figure 6: Undervoltage Lockout vs. Temperature

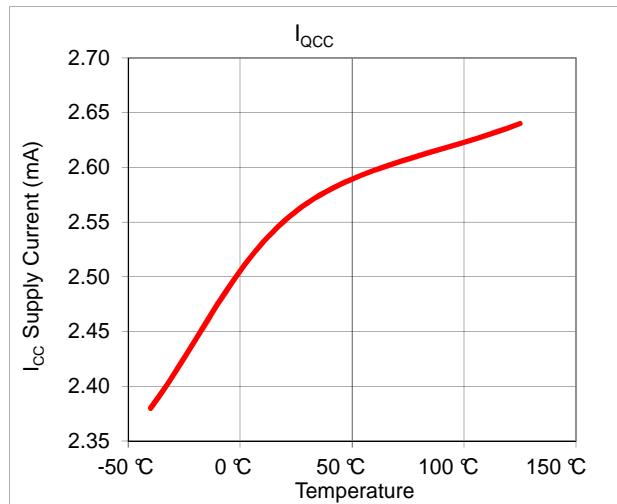


Figure 7: Icc Quiescent Current vs. Temperature

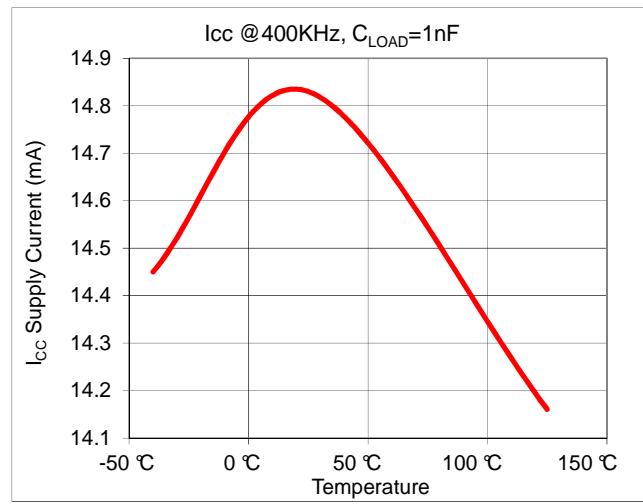


Figure 8: Icc Supply Current @1nF Load vs. Temperature

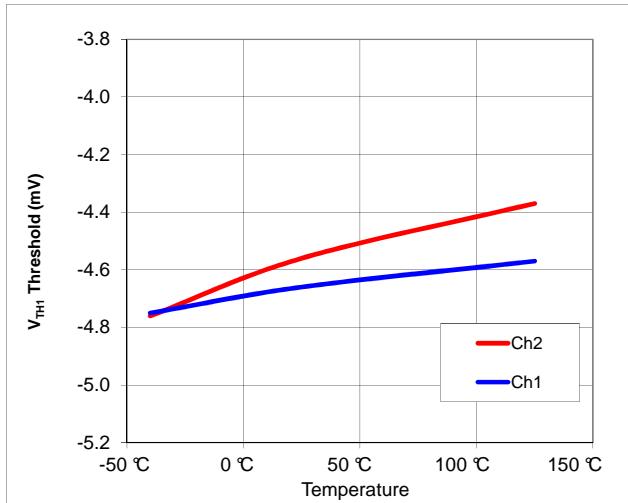


Figure 9: V_{TH1} vs. Temperature

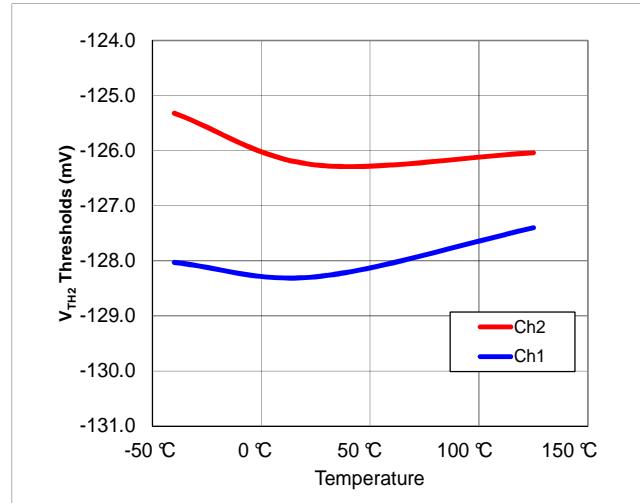


Figure 10: V_{TH2} vs. Temperature

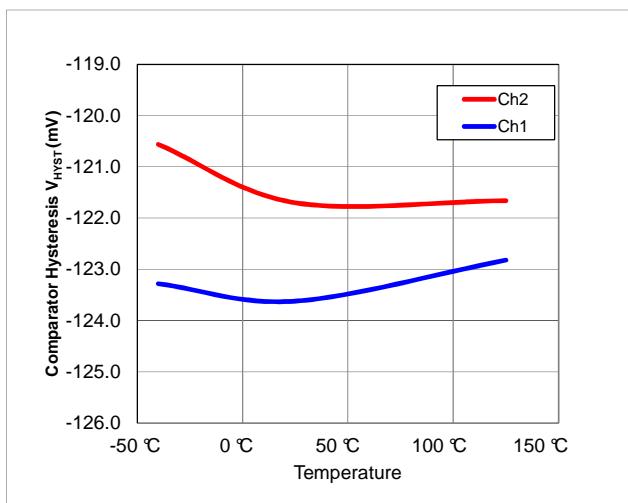
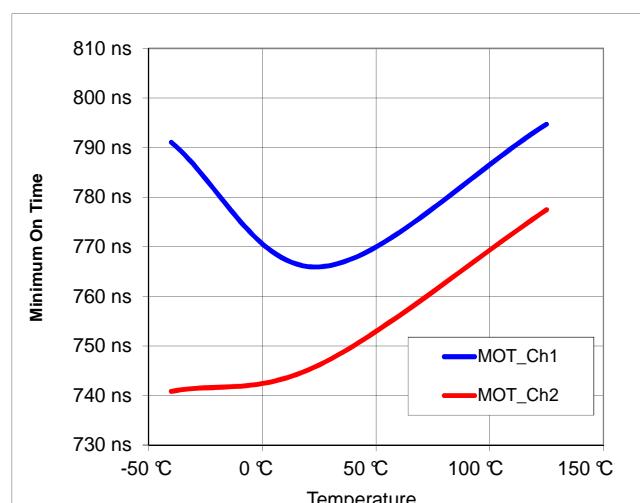


Figure 11: Comparator Hysteresis vs.
Temperature



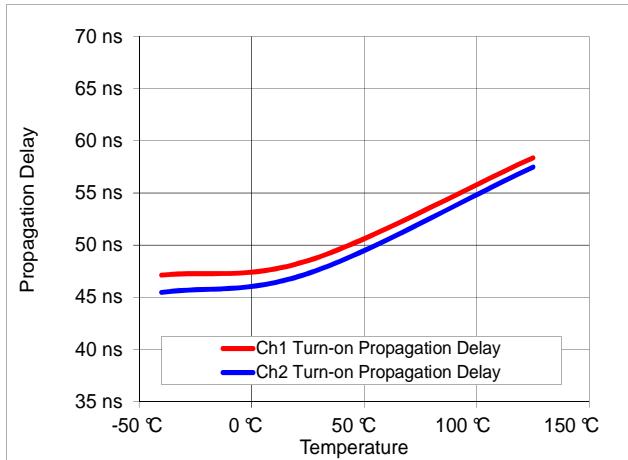


Figure 13: Turn-on Propagation Delay vs. Temperature

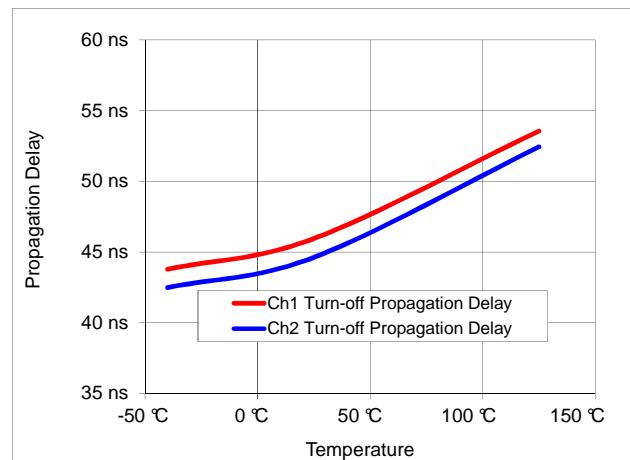


Figure 14: Turn-off Propagation Delay vs. Temperature

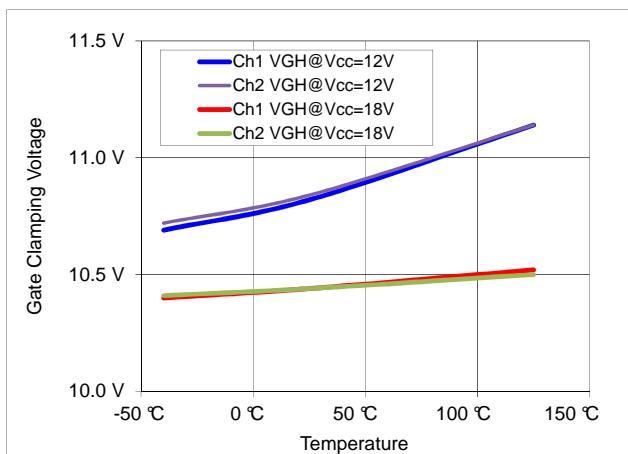


Figure 15: Gate Clamping Voltage vs. Temperature

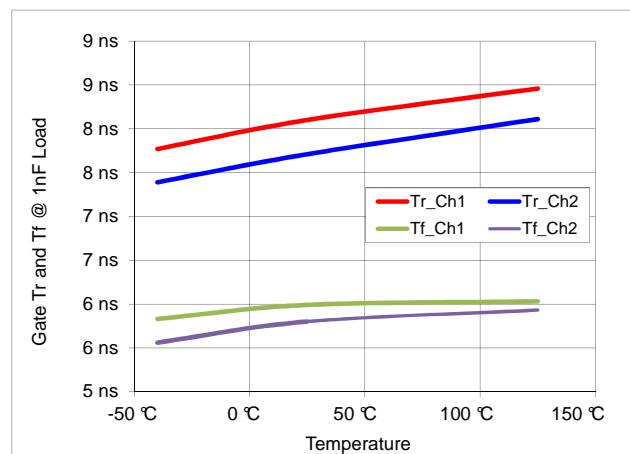
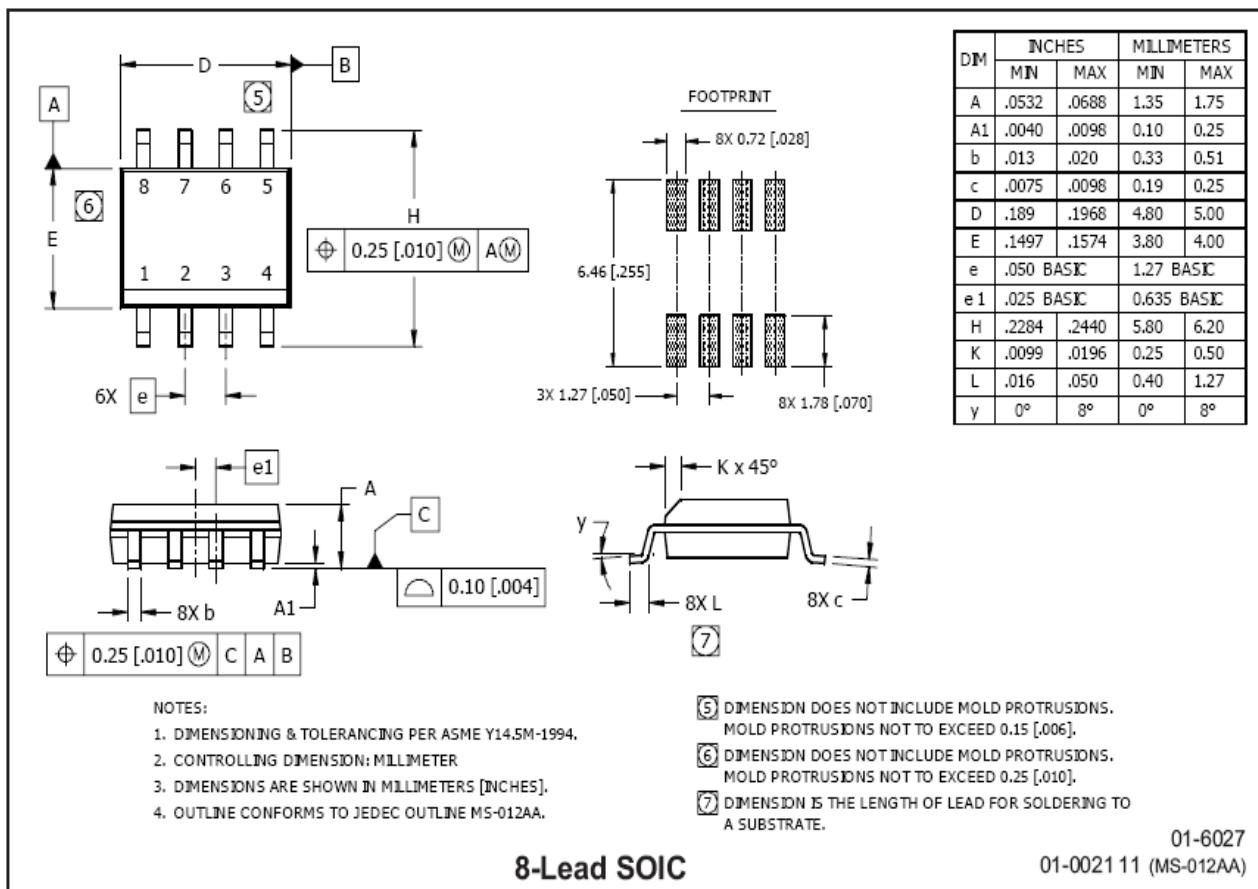
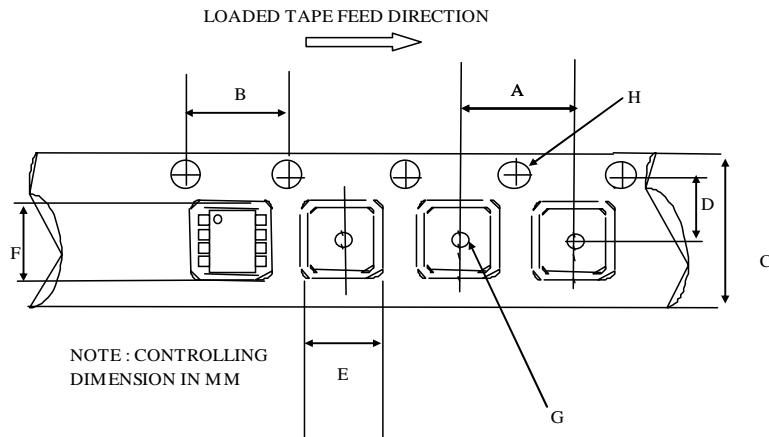


Figure 16: Gate Output Tr and Tf time @ 1nF Load vs. Temperature

Package Details: SOIC8N

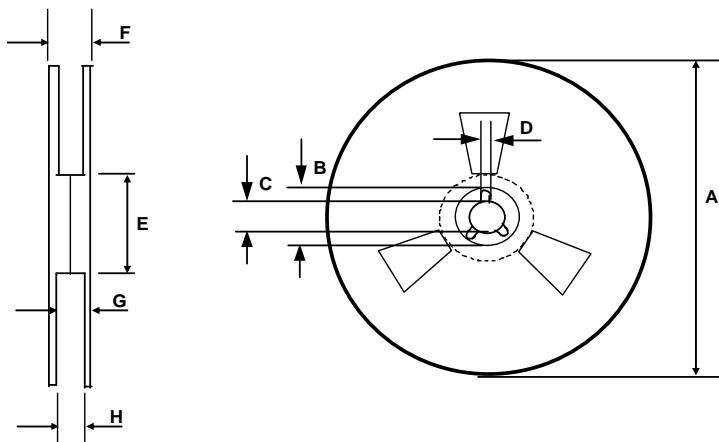


Tape and Reel Details: SOIC8N



CARRIER TAPE DIMENSION FOR 8SOIC8N

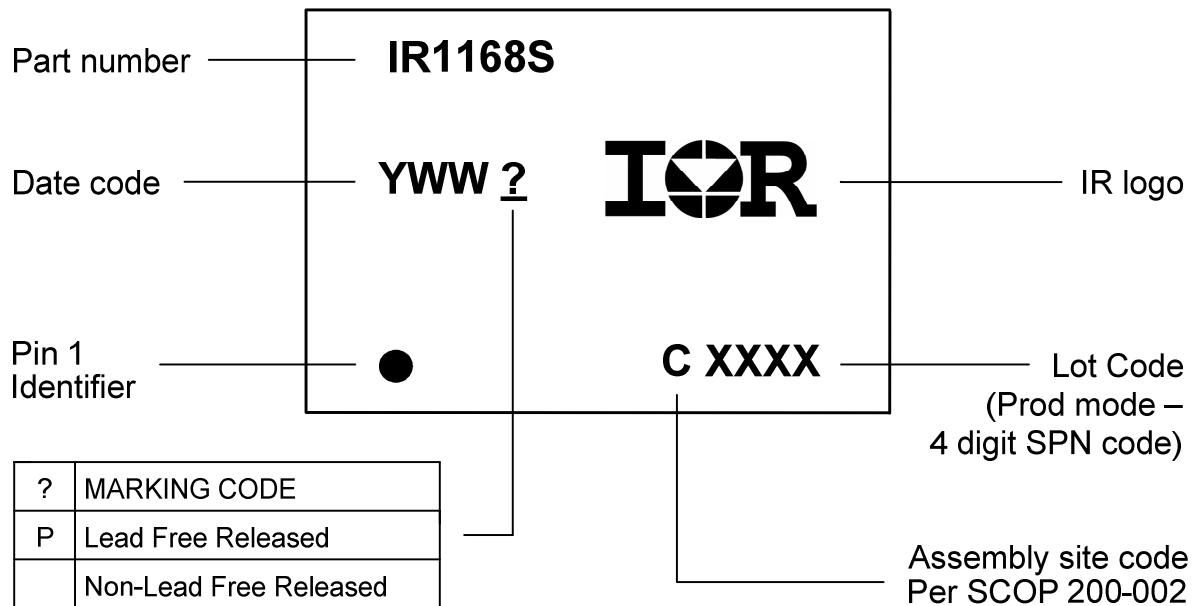
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOIC8N

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information



Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IR1168	SOIC8N	Tube/Bulk	95	IR1168SPBF
		Tape and Reel	2500	IR1168STRPBF

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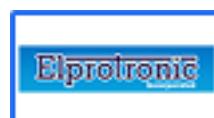
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