

SDP Biased Series - SOT23-6



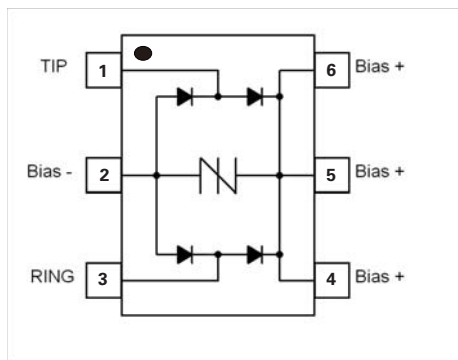
Description

This new SDP Biased series provides overvoltage protection for applications such as VDSL2, ADSL2, and ADSL2+ with minimal effect on data signals. This silicon design innovation results in a capacitive loading characteristic that is compatible with these high bandwidth applications. This surface mount SOT23-6 package provides a surge capability that exceeds most worldwide standards and recommendations for lightning surge withstand capability of tertiary protectors.

Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation & Schematic Symbol



Features & Benefits

- Compatible with VDSL2 (30MHz)
- Balanced overvoltage protection
- Low distortion
- Low insertion loss
- Low profile
- Response time under 500ns

Applicable Global Standards

- ANSI C62.41
- IEC 61000-4-12
- IEC 61000-4-5, 30A ($t_p=8/20\mu s$)
- IEC 61000-4-2 level 4 – 15kV (air discharge)
- IEC 61000-4-2 level 4 – 8kV (contact discharge)

Absolute Maximum Ratings between pin1 and pin 3, $T_a=25^\circ C$ (Unless otherwise noted)

Part Number	Marking	Maximum Junction Temperature	Storage Temperature Range	I_{PP} 8/20 μs
		$^\circ C$	$^\circ C$	A Max
SDP0240T023G6RP	P24	150	-65 to 150	30 ¹

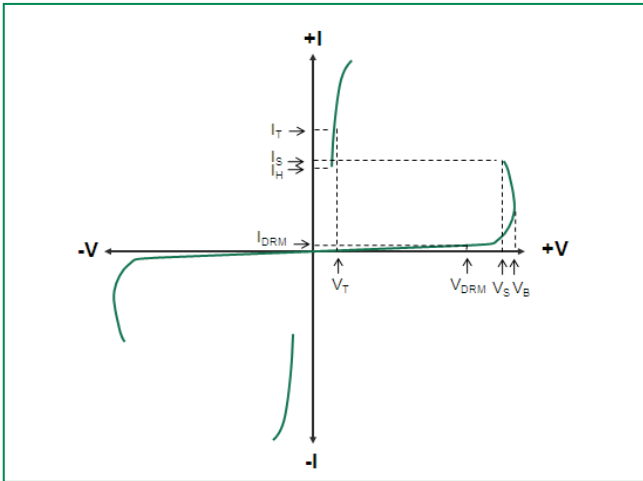
Notes:

1. The device must be in thermal equilibrium at 25 $^\circ C$

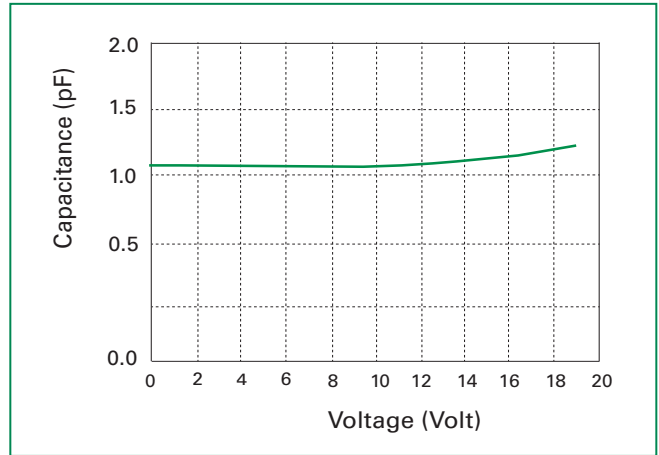
Electrical Characteristics between pin 1 and pin 3, $T_a = 25^\circ C$

Part Number	Marking	V_{DRM} @ $I_{DRM}=100nA$	V_{DRM} @ $I_{DRM}=19V$	$V_s @ 1V/us$	I_H	I_S	$Co @ f=1MHz, 2V$	Delta Co @ Line Bias = 1V to 19V
		V min	pA typ	V max	mA typ	mA min	pF max	pF max
SDP0240T023G6RP	P24	19	300	29	40	10	3.0	0.5

V-I: Characteristics



Typical capacitance against line voltage (without external bias)



Surge Ratings

Series	I_{PP}
	1.2/50 μ s ¹ / 8/20 μ s ²
	A min
G	30

Notes:

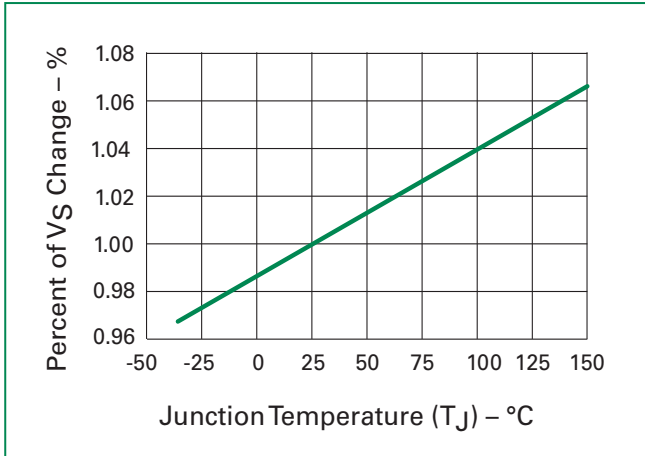
- 1 Voltage waveform in μ s
- 2 Current waveform in μ s

- Peak pulse current rating (I_{pp}) is repetitive and guaranteed for the life of the product.
- The device must be in thermal equilibrium at 25°C.

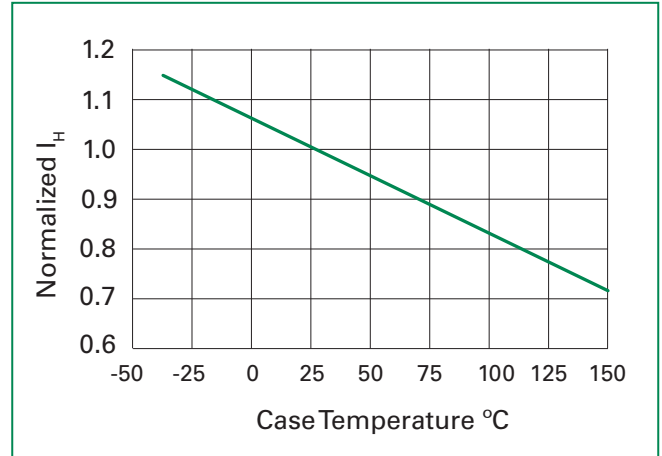
Thermal Information

Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 10s)	260	°C

Normalized V_s Change vs. Junction Temperature

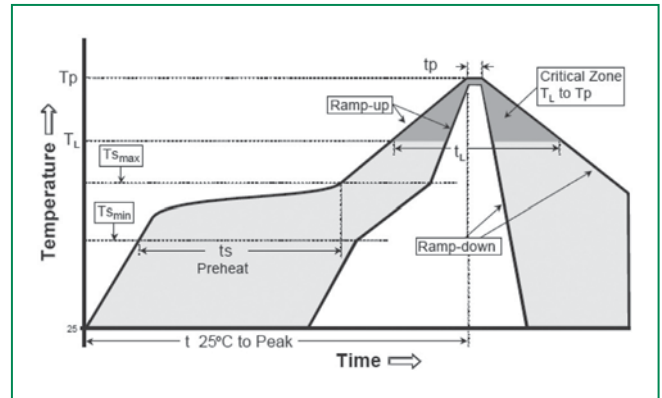


Normalized Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{s(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_p)		250(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		20-40 secs.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_p)		8 min. Max.
Do not exceed		260°C



Physical Specifications

Lead Plating	SOT23: Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Substrate Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

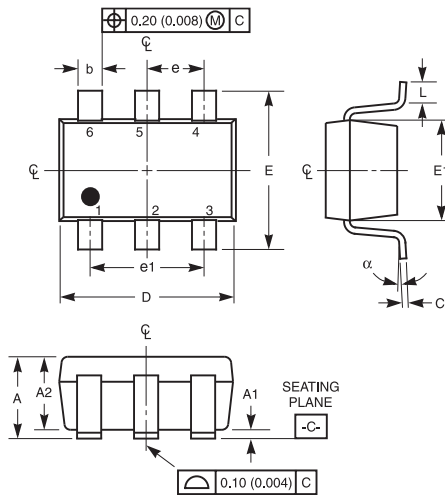
Notes:

1. All dimensions are in millimeters.
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC MO-178
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte tine

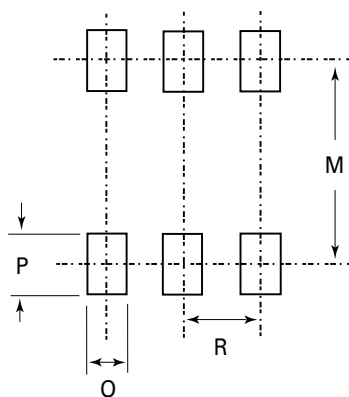
Environmental Specifications

Temp Cycling	Mil-STD-883F, Method 1010.8 Condition C, -65°C to +150°C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Bias Humidity	JESD 22-A101-B 85°C , 85°C CRH. 50V 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Pressure Cooker	JEDEC 22-A102C No Bias, 121°C, 100%RH 96Hrs/192Hrs. 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
High Temp Storage	JESD 22-A103C Con B. 150°C, no bias 1000Hrs
HTRB	JESD 22-108C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Thermal Shock	Mil-STD-883F, Method 1011.9 Condition A, 0°C to 100°C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
C-SAM	As per flow, JSTD-020C pre&post preconditioning test.
Wet Humidity (Tin only)	JESD 201A standard: 55°C/85%RH

Dimensions - SOT23-6



Recommended Solder Pad Layout

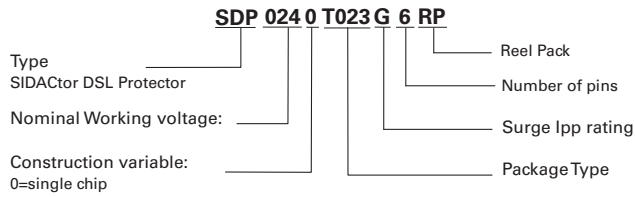


Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	-	0.057	-	1.450
A1	-	0.006	-	0.150
A2	-	0.051	-	1.300
b	0.014	0.020	0.350	0.508
C	0.004	0.008	0.090	0.200
D	0.110	0.118	2.800	3.000
E	0.102	0.118	2.600	3.000
E1	0.057	0.069	1.450	1.750
e	-	0.037	-	0.950
e1	-	0.075	-	1.900
L (note 4.5)	0.004	0.023	0.100	0.600
N (note 6)	6		6	
Ø	0°C	10°C	0°C	10°C
M	-	0.102	-	2.590
O	-	0.027	-	0.690
P	-	0.039	-	0.990
R	-	0.038	-	0.950

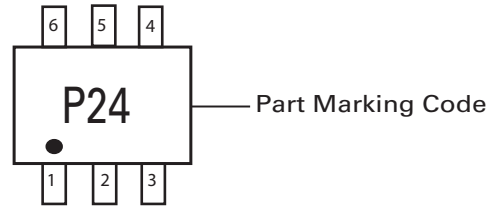
Notes:

1. Dimensioning and tolerances per ANSI 14.5M-1982.
2. Package conforms to EIAJ SC-74 (1992)
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Foot length L measured at reference to seating plane.
5. "L" is the length of flat foot surface for soldering to substrate.
6. "N" is the number of terminal positions.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Part Numbering



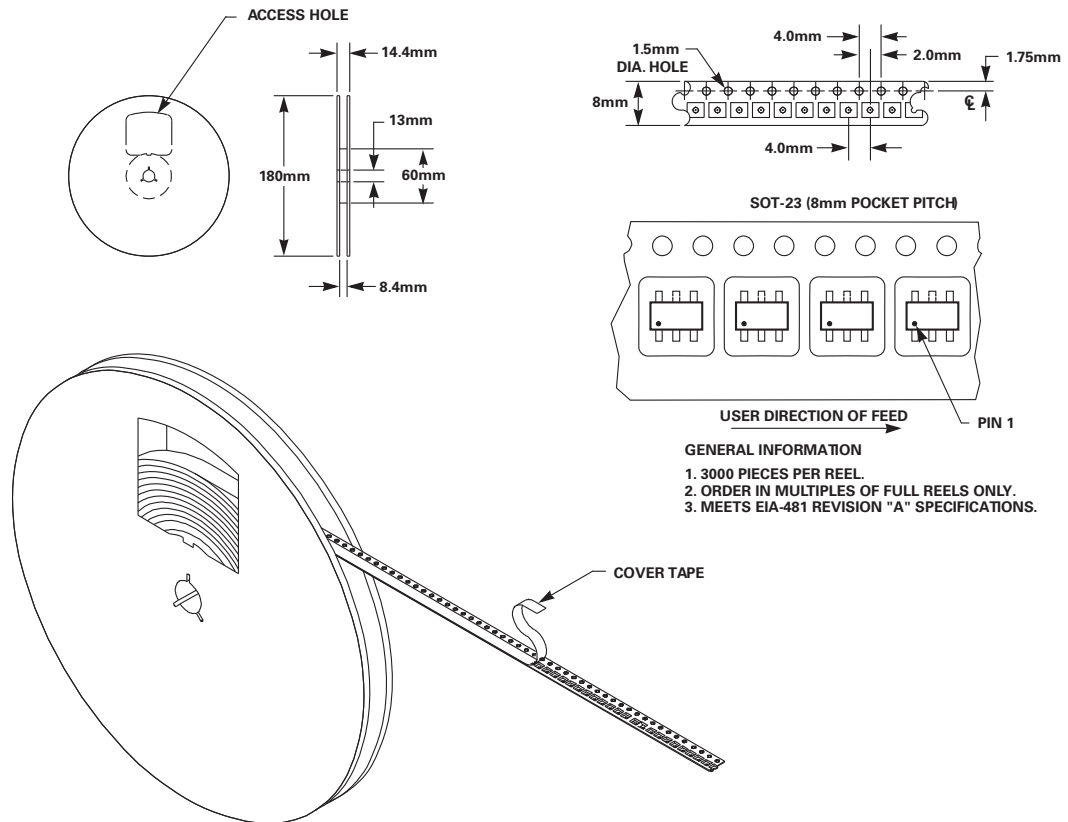
Part Marking



Packing Options

Package Type	Description	Quantity
SOT23-6	Tape and Reel	3000

Embossed Carrier Tape & Reel Specification - SOT23-6



AMEYA360

Components Supply Platform

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Website :

Welcome to visit www.ameya360.com

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype [ameyasales1](#) [ameyasales2](#)

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com