PCS3P25811, PCS3P25812, PCS3P25814

Spread Spectrum Clock Generator

ON Semiconductor®

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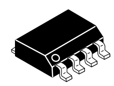
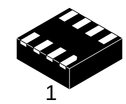

1

SOIC−8 NB
CASE 751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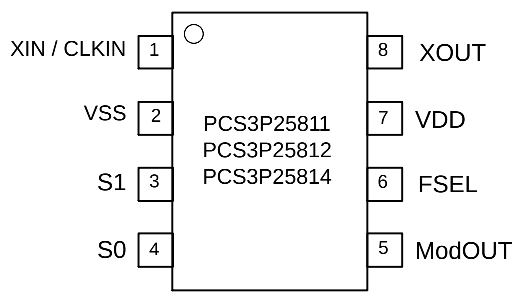
WDFN8 2x2, 0.5P
CASE 511AQ

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

Product Description

The PCS3P25811/12/14 devices are versatile spread spectrum frequency modulators designed specifically for a wide range of input clock frequencies from 4 MHz to 32 MHz.

The PCS3P25811/12/14 reduce electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. It allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding, and other passive components that are traditionally required to pass EMI regulations.

The PCS3P25811/12/14 can generate an EMI reduced clock from crystal, ceramic resonator, or system clock.

The PCS3P25811/12/14 modulate the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation’.

The PCS3P25811/12/14 use the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all−digital method.

The PCS3P25811/12/14 have 2 pins S0 and S1 to control the selection of Center Spread, Down Spread and No−Spread functions. Additionally there is a 3 level logic contol FSEL, for selecting one of the three different frequency ranges within the operating frequency range. Refer *Input/Output Frequency Range Selection Table*.

The PCS3P25811/12/14 operate from a 2.8 V to 3.6 V supply and are available in 8 pin SOIC, and 8L 2 mm x 2 mm WDFN packages.

Applications

The PCS3P25811/12/14 are targeted towards EMI management in applications such as LCD Panels, MFPs, Digital copiers, Networking, PC peripheral devices, consumer electronics, and embedded controller systems.

Features

- Generates a 1x (PCS3P25811), 2x (PCS3P25812) and 4x(PCS3P25814) Low EMI Spread Spectrum Clock of the Input Frequency
- Provides up to 15 dB of EMI Suppression
- Input Frequency: 4 MHz − 32 MHz
- Output Frequency: PCS3P25811: 4 MHz − 32 MHz
  PCS3P25812: 8 MHz − 64 MHz
  PCS3P25814: 16 MHz − 128 MHz
- Selectable Spread Options: Down Spread and Center Spread
- Low Power Dissipation: 3.3 V: 20 mW (typ) @ 6 MHz
  3.3 V: 24 mW (typ) @ 12 MHz
  3.3 V: 30 mW (typ) @ 24 MHz
- Low Inherent Cycle−to−Cycle Jitter
- Supply Voltage: 2.8 V to 3.6 V
- LVCMOS Input and Output
- Functional and Pinout Compatible to Cypress CY25811, CY25812 and CY25814
- 8−pin SOIC, and 8L 2 mm x 2 mm WDFN (TDFN) Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

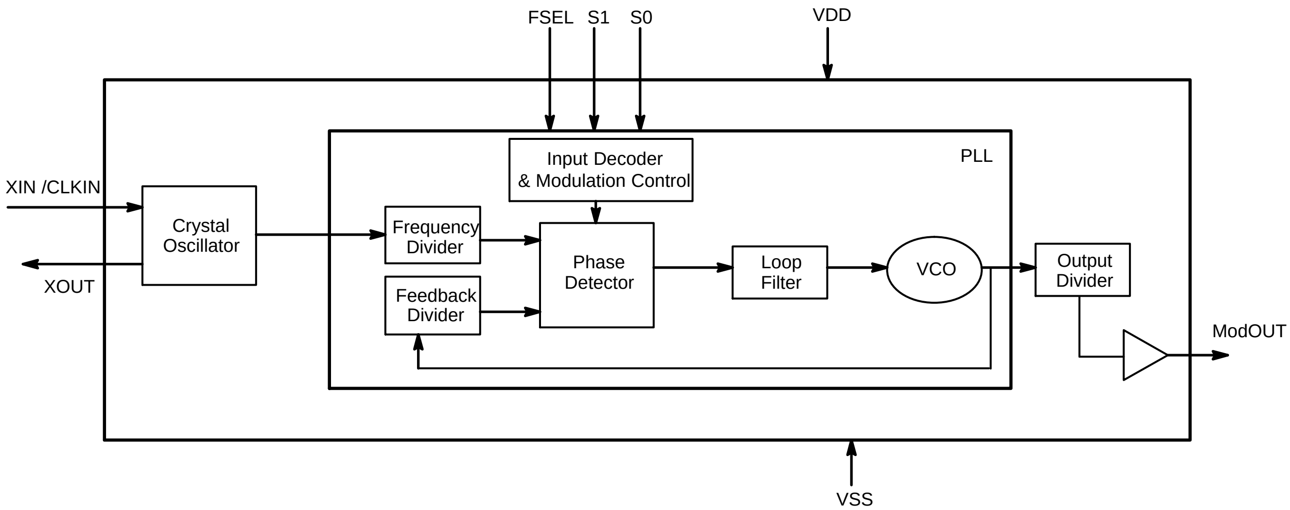


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	XIN / CLKIN	Input	Crystal connection or External Clock input.
2	VSS	Power	Ground to entire chip.
3	S1	Input	Digital 3 level logic input (1−M−0) used to select Center, Down and No spread options. (Refer to *Frequency Deviation Selection Table).* Default = M.
4	S0	Input	Digital 3 level logic input (1−M−0) used to select Center, Down and No spread options. (Refer to *Frequency Deviation Selection Table).* Default = M.
5	ModOUT	Output	Spread Spectrum Clock Output.
6	FSEL	Input	Frequency range select. Digital 3 level logic input (1−M−0) used to select Input Clock frequency range (Refer to *Input/Output Frequency Range Selection Table*). Default = M.
7	VDD	Power	Power supply for the entire chip (2.8 V to 3.6 V).
8	XOUT	Output	Crystal connection. If using an external reference, this pin must be left unconnected.

Table 2. OUTPUT FREQUENCY RANGE SELECTION

	Part Number						
	PCS3P25811 (1x)		PCS3P25812 (2x)		PCS3P25814 (4x)		
FSEL (pin 6)	Input (MHz)	Output (MHz)	Input (MHz)	Output (MHz)	Input (MHz)	Output (MHz)	Modulation Rate
0	4 − 8	4 − 8	4 − 8	8 − 16	4 − 8	16 − 32	Input Frequency / 128
1	8 − 16	8 − 16	8 − 16	16 − 32	8 − 16	32 − 64	Input Frequency / 256
M	16 − 32	16 − 32	16 − 32	32 − 64	16 − 32	64 − 128	Input Frequency / 512

Table 3. OUTPUT FREQUENCY DEVIATION SELECTION

CLKIN (MHz)	FSEL	S1 = 0 S0 = 0	S1 = 0 S0 = M	S1 = 0 S0 = 1	S1 = M S0 = 0	S1 = 1 S0 = 1	S1 = 1 S0 = 0	S1 = M S0 = 1	S1 = 1 S0 = M	S1 = M S0 = M
		Center	Center	Center	Center	Down	Down	Down	Down	No Spread
4 − 5	0	±1.4	±1.2	±0.6	±0.5	−3	−2.2	−1.9	−0.7	0
5 − 6	0	±1.3	±1.1	±0.5	±0.4	−2.7	−1.9	−1.7	−0.6	0
6 − 7	0	±1.2	±0.9	±0.5	±0.4	−2.5	−1.8	−1.5	−0.6	0
7 − 8	0	±1.1	±0.9	±0.4	±0.3	−2.3	−1.7	−1.4	−0.5	0
8 − 10	1	±1.4	±1.2	±0.6	±0.5	−3	−2.2	−1.9	−0.7	0
10 − 12	1	±1.3	±1.1	±0.5	±0.4	−2.7	−1.9	−1.7	−0.6	0
12 − 14	1	±1.2	±0.9	±0.5	±0.4	−2.5	−1.8	−1.5	−0.6	0
14 − 16	1	±1.1	±0.9	±0.4	±0.3	−2.3	−1.7	−1.4	−0.5	0
16 − 20	M	±1.4	±1.2	±0.6	±0.5	−3	−2.2	−1.9	−0.7	0
20 − 24	M	±1.3	±1.1	±0.5	±0.4	−2.7	−1.9	−1.7	−0.6	0
24 − 28	M	±1.2	±0.9	±0.5	±0.4	−2.5	−1.8	−1.5	−0.6	0
28 − 32	M	±1.1	±0.9	±0.4	±0.3	−2.3	−1.7	−1.4	−0.5	0

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3 Level Digital Logic

S0, S1, and FSEL digital inputs are designed to sense 3 different logic levels designated as High “1”, Low “0” and Middle “M”. With this 3−Level digital input logic 9 different logic states can be detected.

S0, S1 and FSEL pins include an on chip 100 K (50 K / 50 K) resistor divider. No external application resistors are needed to implement the 3−Level logic levels as shown in table on the right:

Logic	Control Pins
1	FSEL, S0, S1 to VDD
M	FSEL, S0, S1 UNCONNECTED
0	FSEL, S0, S1 to VSS

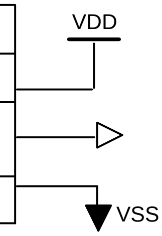


Table 4. OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to VSS	2.8	3.6	V
T_A	Operating temperature	0	+70	°C
C_L	Load Capacitance		15	pF
C_{IN}	Input Capacitance		7	pF

Table 5. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD 22− A114−B)	2	KV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 6. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter			Min	Typ	Max	Units
VDD	Supply Voltage			2.8	3.3	3.6	V
V_{IL}	Input low voltage (S0, S1, FSEL Inputs)	Commercial Temperature		0		0.15 V_{DD}	V
		Industrial Temperature		0		0.13 V_{DD}	
V_{IM}	Input middle voltage (S0, S1, FSEL Inputs)			0.4 VDD		0.60 V_{DD}	V
V_{IH}	Input high voltage (S0, S1, FSEL Inputs)			0.85 VDD		V_{DD}	V
V_{OL}	Output low voltage (ModOUT Output)	I_{OL} = 4 mA				0.4	V
		I_{OL} = 10 mA				1.2	
V_{OH}	Output high voltage (ModOUT Output)	I_{OH} = −4 mA		2.4			V
		I_{OH} = −6 mA		2			
C_{IN}	Input Capacitance (XIN and XOUT)			6		9	pF
I_{DD}	Dynamic supply current (Unloaded Output)	Commercial Temperature	XIN / CLKIN = 12 MHz			8	mA
			XIN / CLKIN = 24 MHz			10	
			XIN / CLKIN = 32 MHz			13	
		Industrial Temperature	XIN / CLKIN = 12 MHz			10	mA
			XIN / CLKIN = 24 MHz			12	
			XIN / CLKIN = 32 MHz			15	
I_{CC}	Static supply current (XIN / CLKIN pulled to VSS)					0.5	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Table 7. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Min	Typ	Max	Units
f_{IN}	Input Clock frequency for PCS3P25811/12/14		4		32	MHz
f_{OUT}	ModOUT Clock frequency for PCS3P25811		4		32	MHz
	ModOUT Clock frequency for PCS3P25812		8		64	
	ModOUT Clock frequency for PCS3P25814		16		128	
t_{LH} (Notes 1, 2)	ModOUT Rise time (Measured from 20% to 80%)	PCS3P25811/12/14	2		5	nS
		PCS3P25814 when FSEL = M	1		2.2	
t_{HL} (Notes 1, 2)	ModOUT Fall time (Measured from 80% to 20%)	PCS3P25811/12/14	2		4.4	nS
		PCS3P25814 when FSEL = M	1		2.2	
T_{DCIN}	Input Clock Duty Cycle (XIN / CLKIN)		40		60	%
T_{DCOUT} (Notes 1, 2)	Output Clock Duty Cycle (ModOUT)		40		60	%

1. Parameters are specified with 15 pF loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 7. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter			Min	Typ	Max	Units
T_{JC} (Note 2)	Cy−Cy Jitter, for ModOUT with Spread ON *(for Commercial temperature)*	PCS3P25811	4 MHz			600	pS
			8 MHz			450	
		PCS3P25812	16 MHz			400	
			32 MHz			380	
		PCS3P25814	64 MHz			380	
			128 MHz			380	
	Cy−Cy Jitter, for ModOUT with Spread ON *(for Industrial temperature)*	PCS3P25811 PCS3P25812 PCS3P25814	CLKIN = 6 MHz			500	pS
			CLKIN = 12 MHz			400	
			CLKIN = 24 MHz			380	
t_{ON} (Note 2)	PLL Lock Time (Stable power supply, valid input clock to valid Clock on ModOUT)	Commercial Temperature				2	mS
		Industrial Temperature				3	

1. Parameters are specified with 15 pF loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Application Schematic

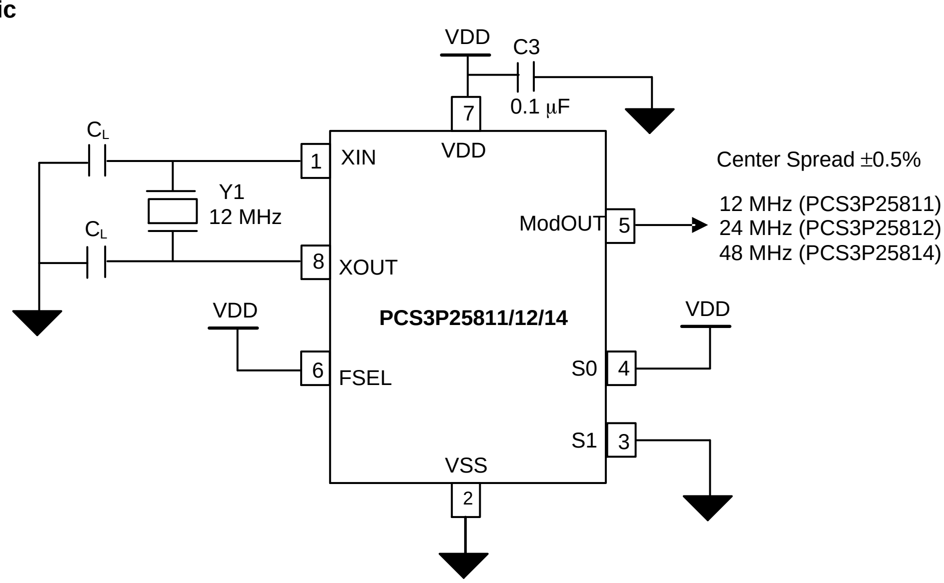
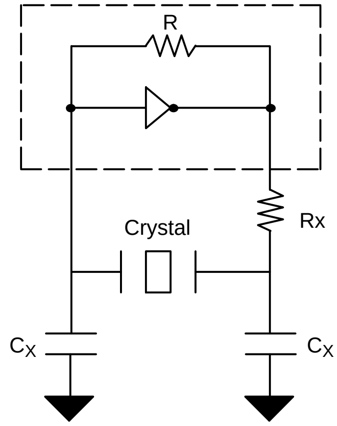


Figure 2. Application Schematic

Table 8. TYPICAL CRYSTAL SPECIFICATIONS

Fundamental AT Cut Parallel Resonant Crystal	
Nominal frequency	12 MHz
Frequency tolerance	±30 ppm or better at 25°C
Operating temperature range	−25°C to +85°C
Storage temperature	−40°C to +85°C
Load capacitance	18 pF
Shunt capacitance	7 pF maximum
ESR	25 Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

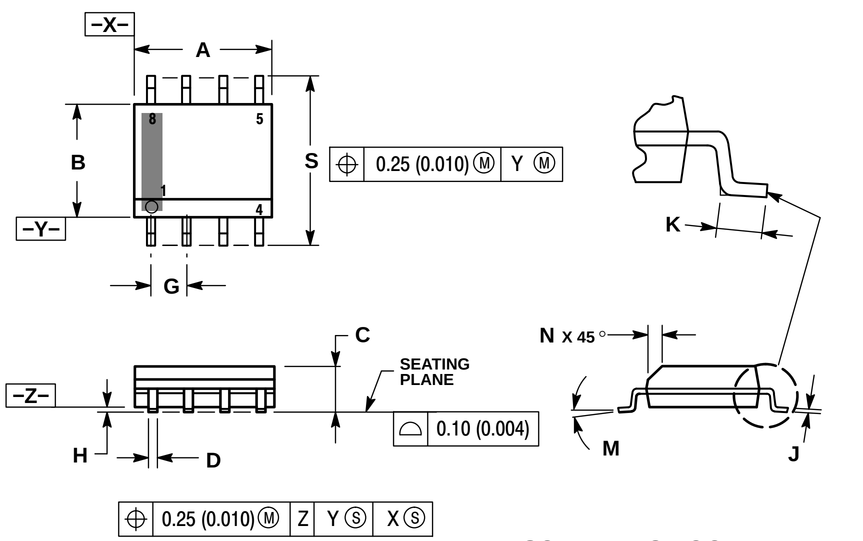


$C_X = 2*(C_P - C_S)$,
Where C_P = Load capacitance of crystal.
C_S = Stray capacitance due to C_{IN}, PCB, Trace, etc.

Figure 3. Typical Crystal Interface Circuit

PACKAGE DIMENSIONS

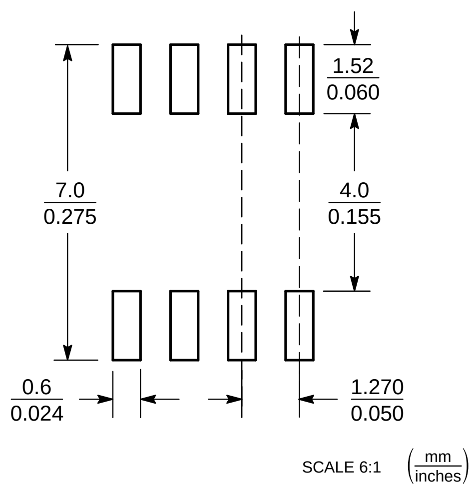
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

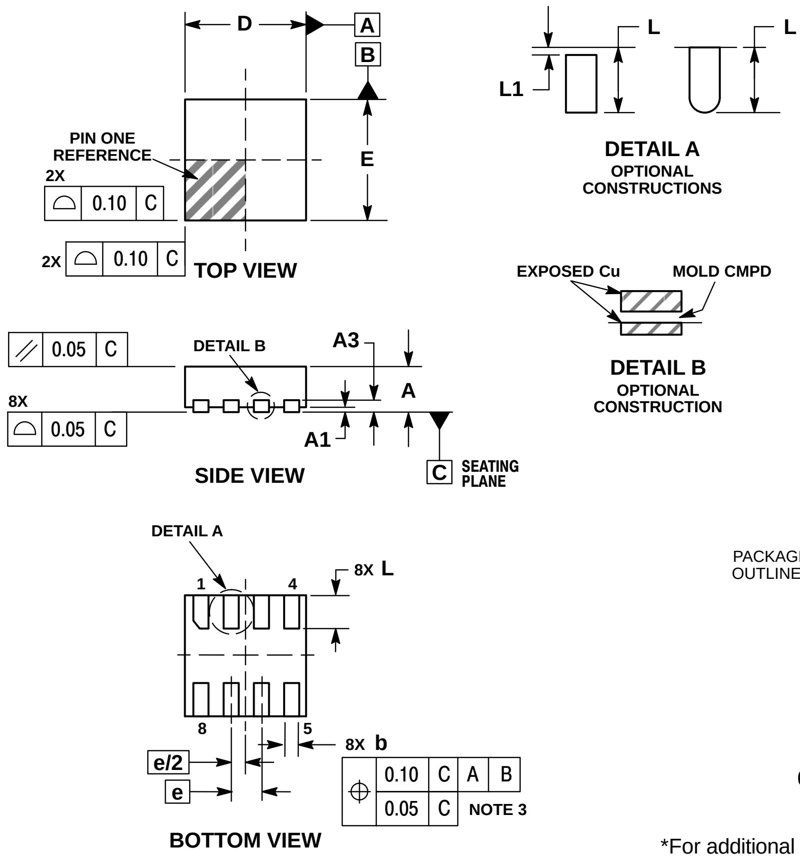
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

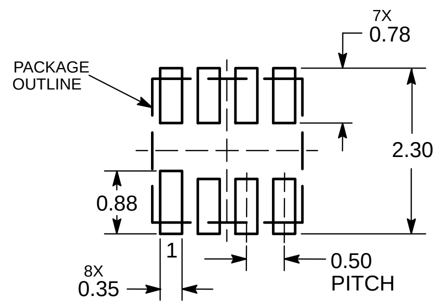
WDFN8 2x2, 0.5P
CASE 511AQ
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.50	0.60
L1	---	0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 9. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
PCS3P25811AG08SR	CGL	8−pin SOIC − Tape & Reel, Green	0°C to +70°C
P3P25812AG−08SR	CIL	8−pin SOIC − Tape & Reel, Green	0°C to +70°C
P3P25814AG−08SR	CKL	8−pin SOIC − Tape & Reel, Green	0°C to +70°C
P3P25811AG−08CR	CG	8L−WDFN (2 mm x 2 mm) − Tape & Reel, Green	0°C to +70°C
P3P25812AG−08CR	CI	8L−WDFN (2 mm x 2 mm) − Tape & Reel, Green	0°C to +70°C
P3P25814AG−08CR	CK	8L−WDFN (2 mm x 2 mm) − Tape & Reel, Green	0°C to +70°C

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

PUBLICATION ORDERING INFORMATION

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Email: orderlit@onsemi.com

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