CDB4351

Evaluation Board for CS4351

Features

- Demonstrates recommended layout and grounding arrangements.
- CS8416 receives S/PDIF, & EIAJ-340-compatible digital audio.
- Headers for External PCM Audio and Control Input
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog Converter system.

Description

The CDB4351 evaluation board is an excellent means for quickly evaluating the CS4351 24-bit, high performance stereo D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, a PC for controlling the CS4351 (stand alone operation is also available) and a power supply. Analog line-level outputs are provided via RCA phono jacks.

The CS8416 digital audio receiver IC. provides the system timing necessary to operate the Digital-to-Analog converter and will accept S/PDIF, and EIAJ-340-compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION

CDB4351	Evaluation Board

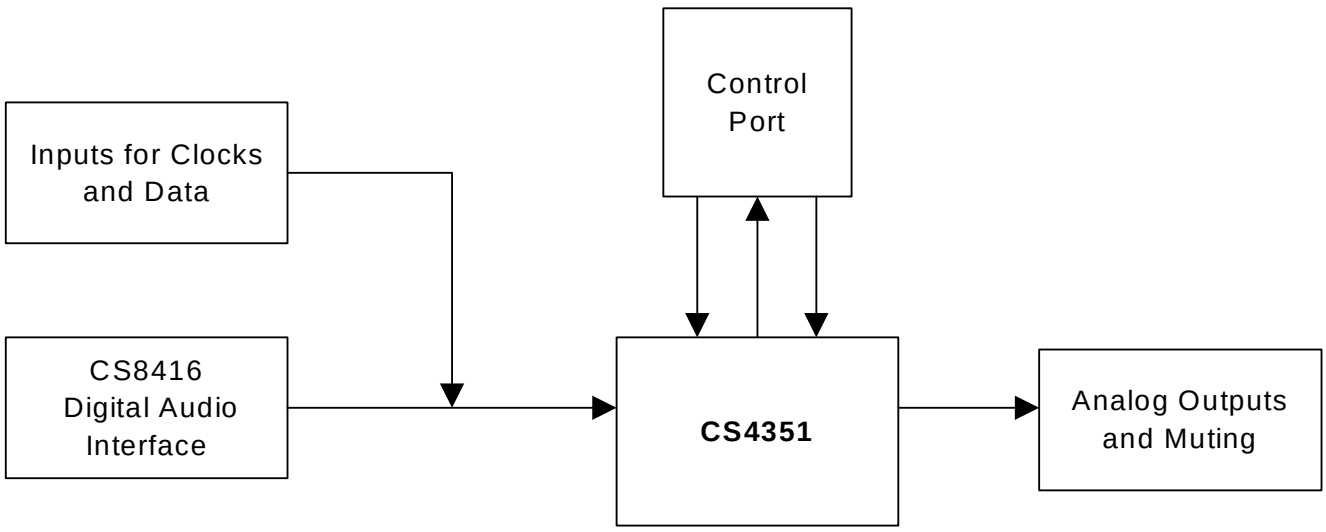

TABLE OF CONTENTS

1. CS4351 DIGITAL TO ANALOG CONVERTER 3
2. CS8416 DIGITAL AUDIO RECEIVER 3
3. INPUT FOR CLOCKS AND DATA 3
4. POWER SUPPLY CIRCUITRY 3
5. GROUNDING AND POWER SUPPLY DECOUPLING 4
6. CONTROL PORT SOFTWARE 4
7. ANALOG OUTPUT FILTERING 4
8. DESIGN NOTE 5

LIST OF FIGURES

Figure 1. System Block Diagram and Signal Flow 6
Figure 2. CS4351 7
Figure 3. Analog Outputs 8
Figure 4. PCM Input Headers 9
Figure 5. CS8416 S/PDIF Input 10
Figure 6. Control Port Interface 11
Figure 7. Power Supply Connections 12
Figure 8. Silkscreen Top 13
Figure 9. Top Side 14
Figure 10. Bottom Side 15

CDB4351 SYSTEM OVERVIEW

The CDB4351 evaluation board is an excellent means of quickly evaluating the CS4351. The CS8416 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply external PCM clocks and data through a header for system development.

The CDB4351 schematic has been partitioned into 6 schematics shown in Figures 2 through 7. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

1. CS4351 DIGITAL-to-ANALOG CONVERTER

A description of the CS4351 is included in the CS4351 datasheet.

2. CS8416 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8416 Digital Audio Receiver, Figure 5. The outputs of the CS8416 include a serial bit clock, serial data, left-right clock, and a 128/256 Fs master clock. The CS8416 data format is selected by switch S1. The operation of the CS8416 and a discussion of the digital audio interface is included in the CS8416 datasheet.

The evaluation board has been designed such that the input can be either optical or coaxial, see Figure 5. However, both inputs cannot be driven simultaneously.

Positions 1 and 2 of S1 set the serial format for the CS8416. These should match the settings of the CS4351 (default is both set to I^2S). Position 3 of S1 sets the output MCLK to LRCK ratio of the CS8416. This switch should be set to 256 (LO) for input Fs<=48 kHz and can be either 256 (LO) or 128 (HI) for Fs>48 kHz

3. INPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the header J9. Header J9 allows the evaluation board to accept externally generated PCM clocks and data. The schematic for the clock/data input is shown in Figure 4. Switch position 4 of S1 selects the source as either CS8416 or header J9.

Please see the CS4351 datasheet for more information.

4. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by six binding posts (GND, +5 V, VL, VD, VA, and VA_H), see Figure 7. The VD, VL, and VA supplies can be jumpered to a +3.3 V regulator and the +5 V binding post can be jumpered to a 5 V regulator thus requiring only VA_H and GND for ease of use. VD, VL, VA and VA_H should be set to the recommended values stated in the CS4351 datasheet.

WARNING: Refer to the CS4351 datasheet for maximum allowable voltages levels. Operation outside of this range can cause permanent damage to the device.

5. GROUNDING AND POWER SUPPLY DECOUPLING

As with any high-performance converter, the CS4351 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 2 details the connections to the CS4351 and Figures 8, 9, and 10 show the component placement and top and bottom layout. The decoupling capacitors are located as close to the CS4351 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

6. CONTROL PORT SOFTWARE

The CDB4351 is shipped with Windows 95/98/ME-based software as well as Windows NT/2000/XP drivers for interfacing with the CS4351 control port via the DB25 connector, J16. The software can be used to communicate with the CS4351 in either SPI® or I^2C mode. See the *readme.txt* file for more information.

7. ANALOG OUTPUT FILTERING

The analog output on the CDB4351 has been designed according to the CS4351 datasheet. This output circuit includes an AC coupling cap, the FET mute circuit, and a single-pole R and C. An additional load resistance of 5.1 kΩ can be jumpered in (J15 and J24) to test the CS4351's load driving capability. The FET muting circuit may be bypassed by placing a shunt on J13 and J21.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5V	Input	+ 5 V power
VD	Input	+ 3.3 V power for the CS4351 digital supply
VL	Input	+ 1.8 V to +3.3 V power for the CS4351 serial interface
VA	Input	+ 3.3 V power for the CS4351 low-voltage analog
VA_H	Input	+9 V to +12 V positive supply for the CS4351 high-voltage analog
GND	Input	Ground connection from power supply
SPDIF INPUT - J11	Input	Digital audio interface input via coaxial cable
SPDIF INPUT - OPT1	Input	Digital audio interface input via optical cable
PCM INPUT - J9	Input	Input for master, serial, left/right clocks and serial data
PC Port	Input/Output	Parallel connection to PC for SPI / I^2C control port signals
EXT CTRL I/O	Input/Output	I/O for SPI / I^2C control port signals
AOUTA and AOUTB	Output	RCA line-level analog outputs

Table 1. System Connections

JUMPER / SWITCH	PURPOSE	POSITION	S/C	FUNCTION SELECTED
J5	Selects source of voltage for the +5V supplies	+5 V *+5V_REG		Voltage source is +5 V binding post Voltage source is +5 V regulator
J6	Selects source of voltage for the VD supplies	VD *+3.3V REG		Voltage source is VD binding post Voltage source is +3.3 V regulator
J7	Selects source of voltage for the VL supply	VL *+3.3V REG		Voltage source is VL binding post Voltage source is +3.3 V regulator
J10	Selects source of voltage for the VA supply	VA *+3.3V REG		Voltage source is VA binding post Voltage source is +3.3 V regulator
S1	Sets Mode of CS8416 and clock source	*1 = open *2, 3, 4 = closed		Default setting is I^2S mode from CS8416 See CS8416 datasheet for details
J20	Stand-alone/Control Port Select	DIS *EN	S C	Stand-alone Mode (No PC required) Control Port Mode (PC required)
J17	DEM(AD0/CS)	HI *LO	- SC	See CS4351 datasheet for details
J18	DIF0(SDA/CDIN)	*HI LO	C S	See CS4351 datasheet for details
J19	DIF1(SCL/CCLK)	*HI LO	C S	See CS4351 datasheet for details
J15 J24	LOAD select	SHUNTED *OPEN		Adds resistor for max loading Normal output circuit
J13 J21	Mute Disable	*SHUNTED OPEN		Bypasses FET muting Normal output circuit

Table 2. CDB4351 Jumper Settings

*Default Factory Settings.

The S/C column denotes standard jumper settings for either stand-alone (S) or control port (C) operation.

8. DESIGN NOTE

CDB4351 Revision A.0

The FET muting circuit must be bypassed by placing a shunt on J13 and J21, otherwise unwanted noise will occur while muted.

CDB4351 Revision B.0

There are no known issues on this revision.

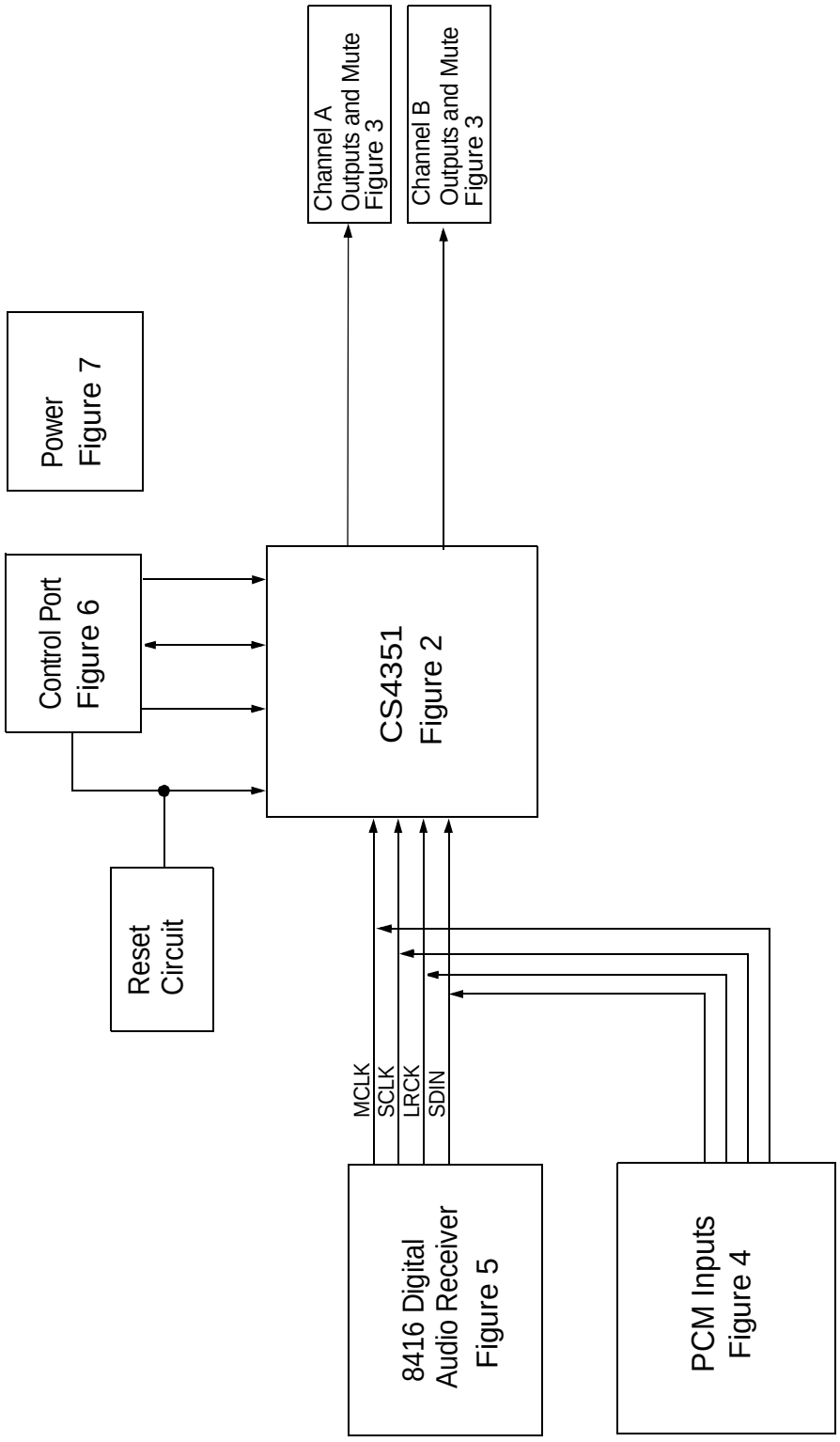

Figure 1. System Block Diagram and Signal Flow

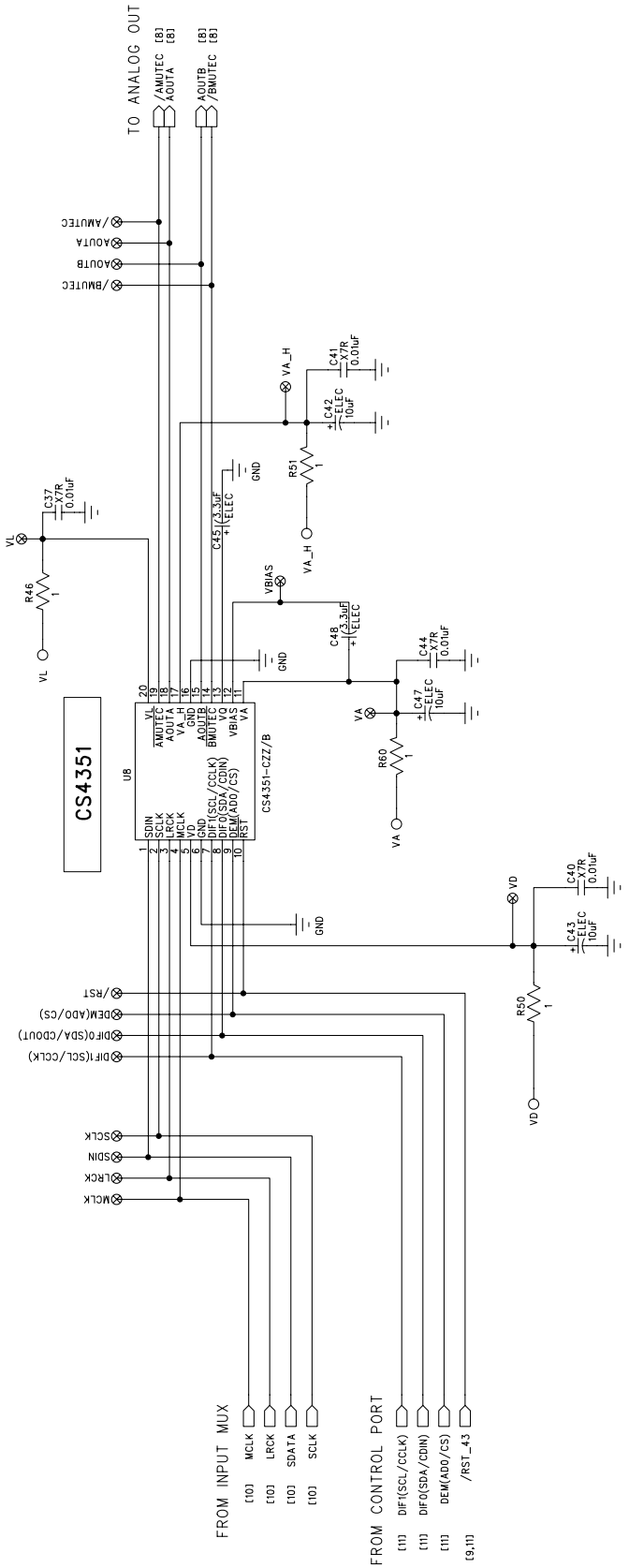

Figure 2. CS4351

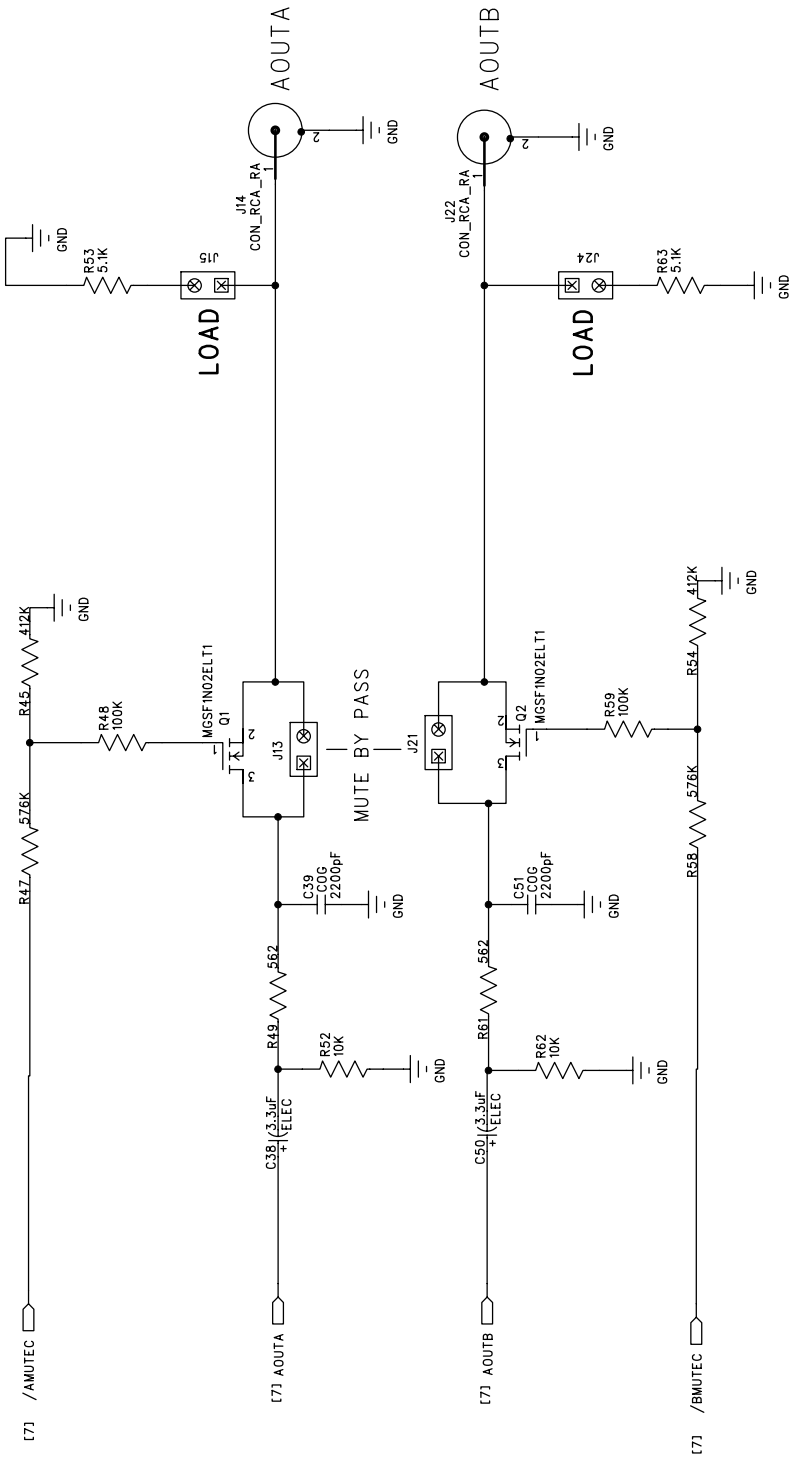

Figure 3. Analog Outputs

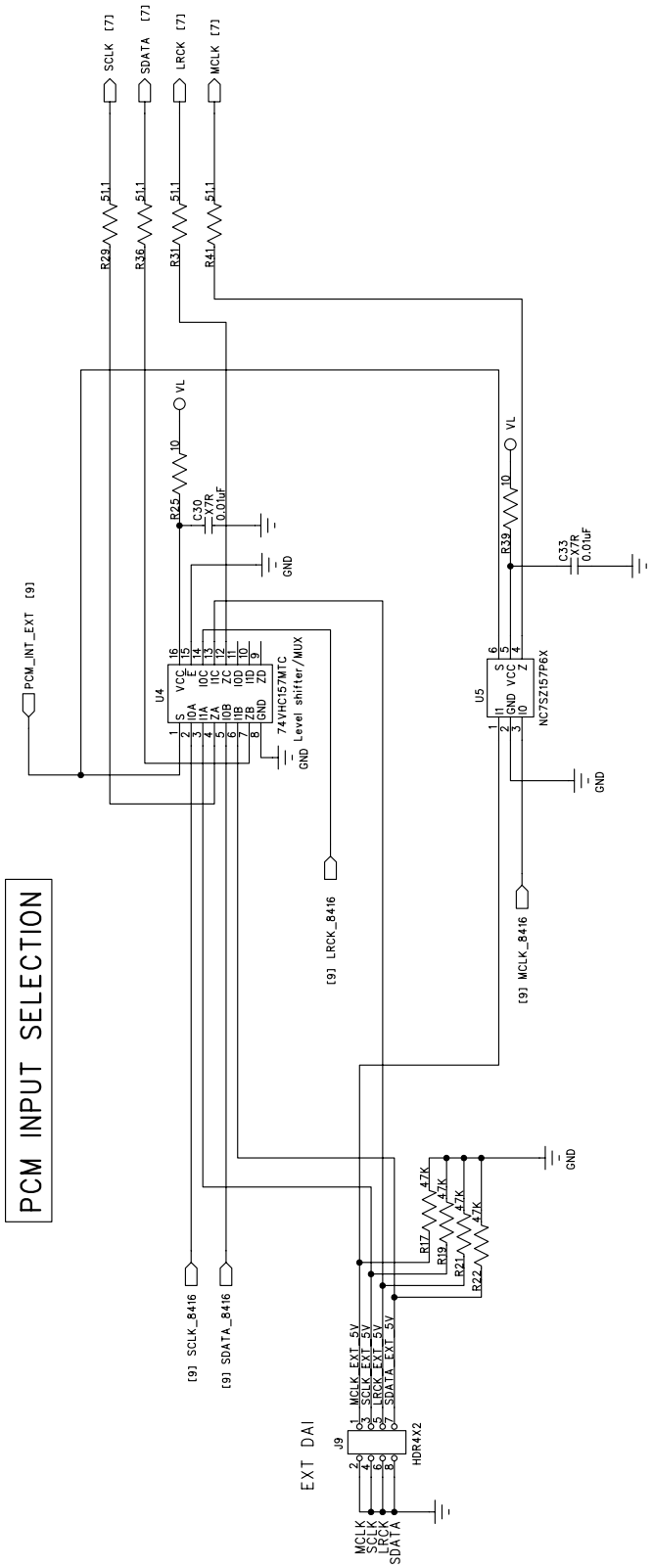

Figure 4. PCM Input Headers

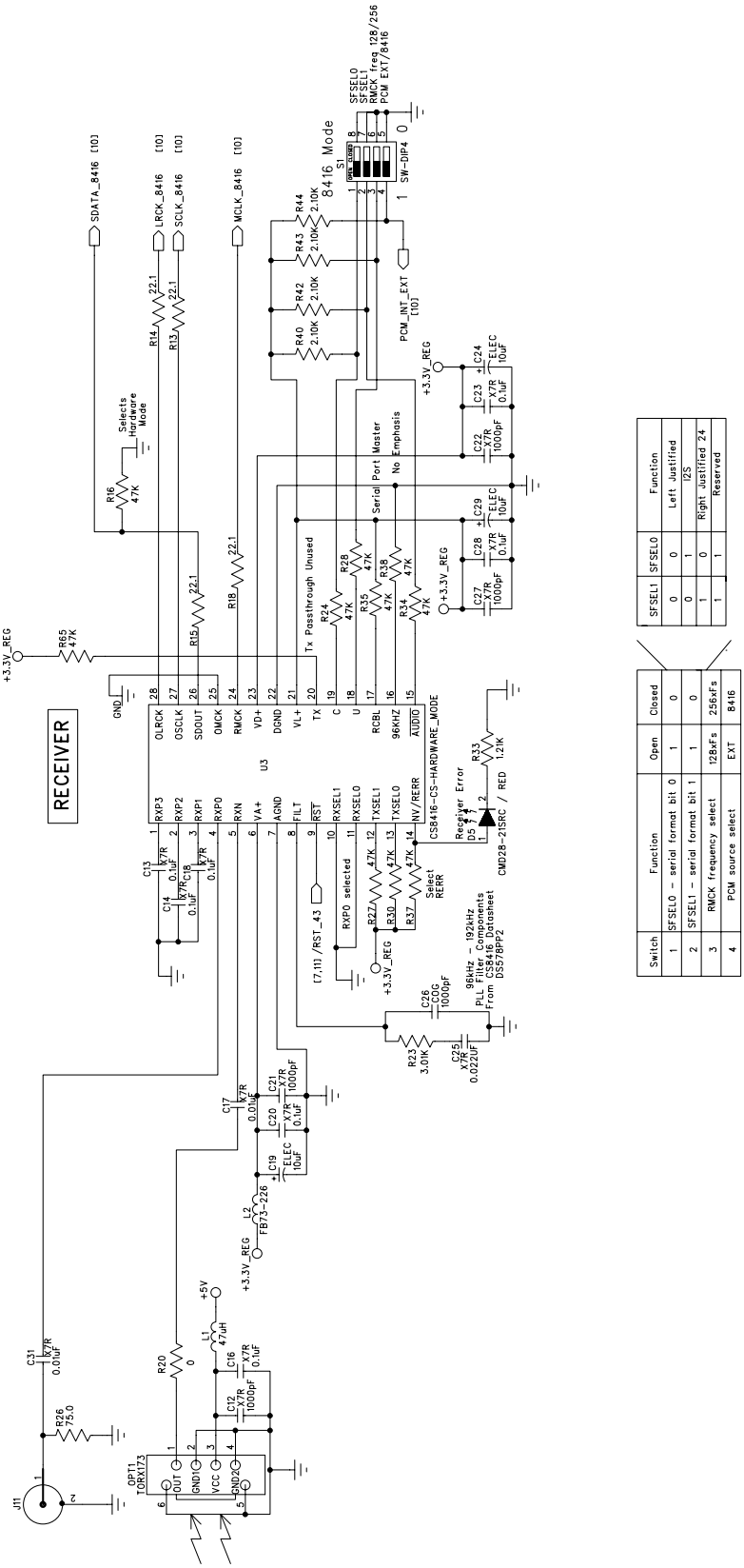

Figure 5. CS8416 S/PDIF Input

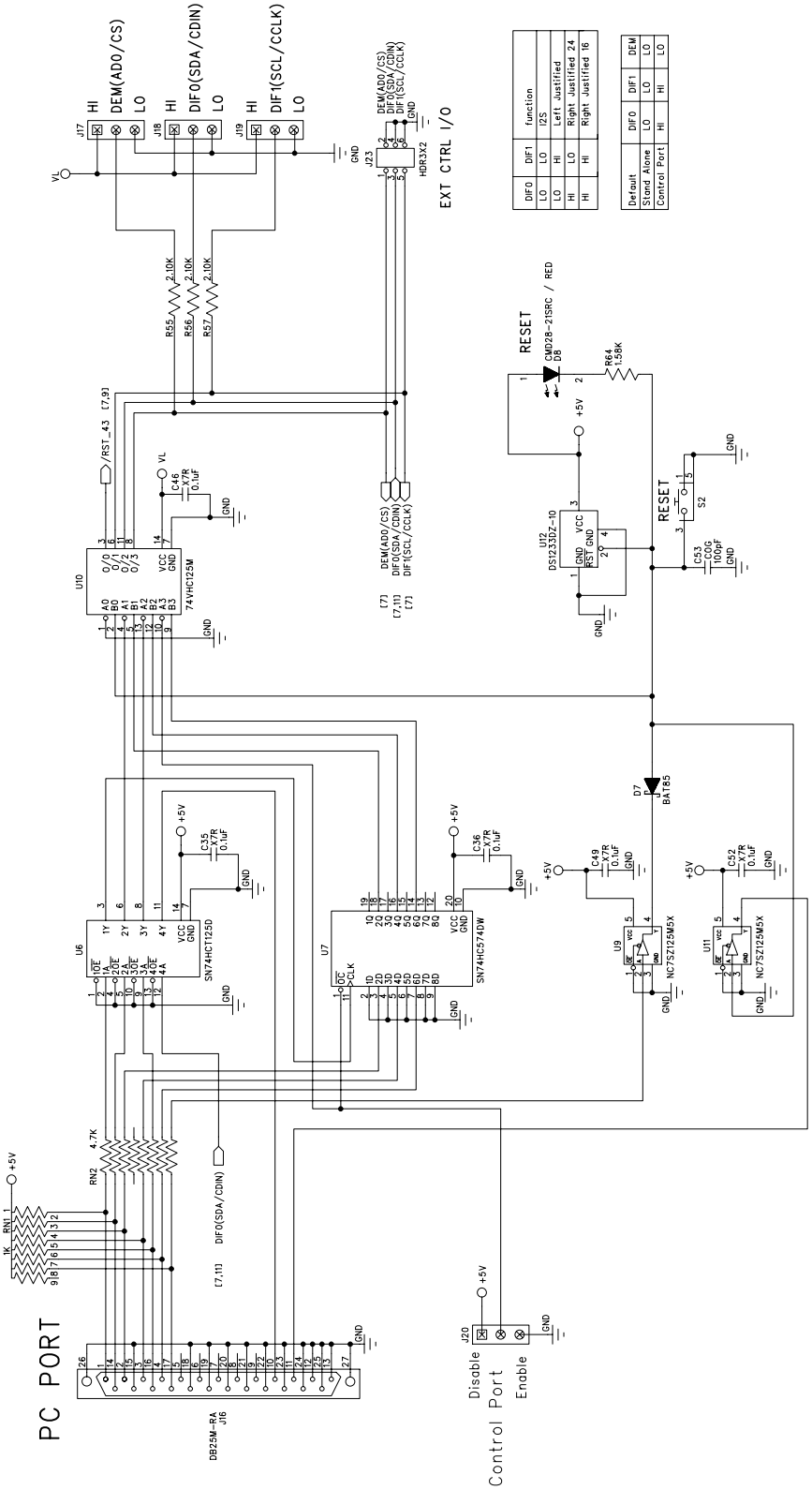

Figure 6. Control Port Interface

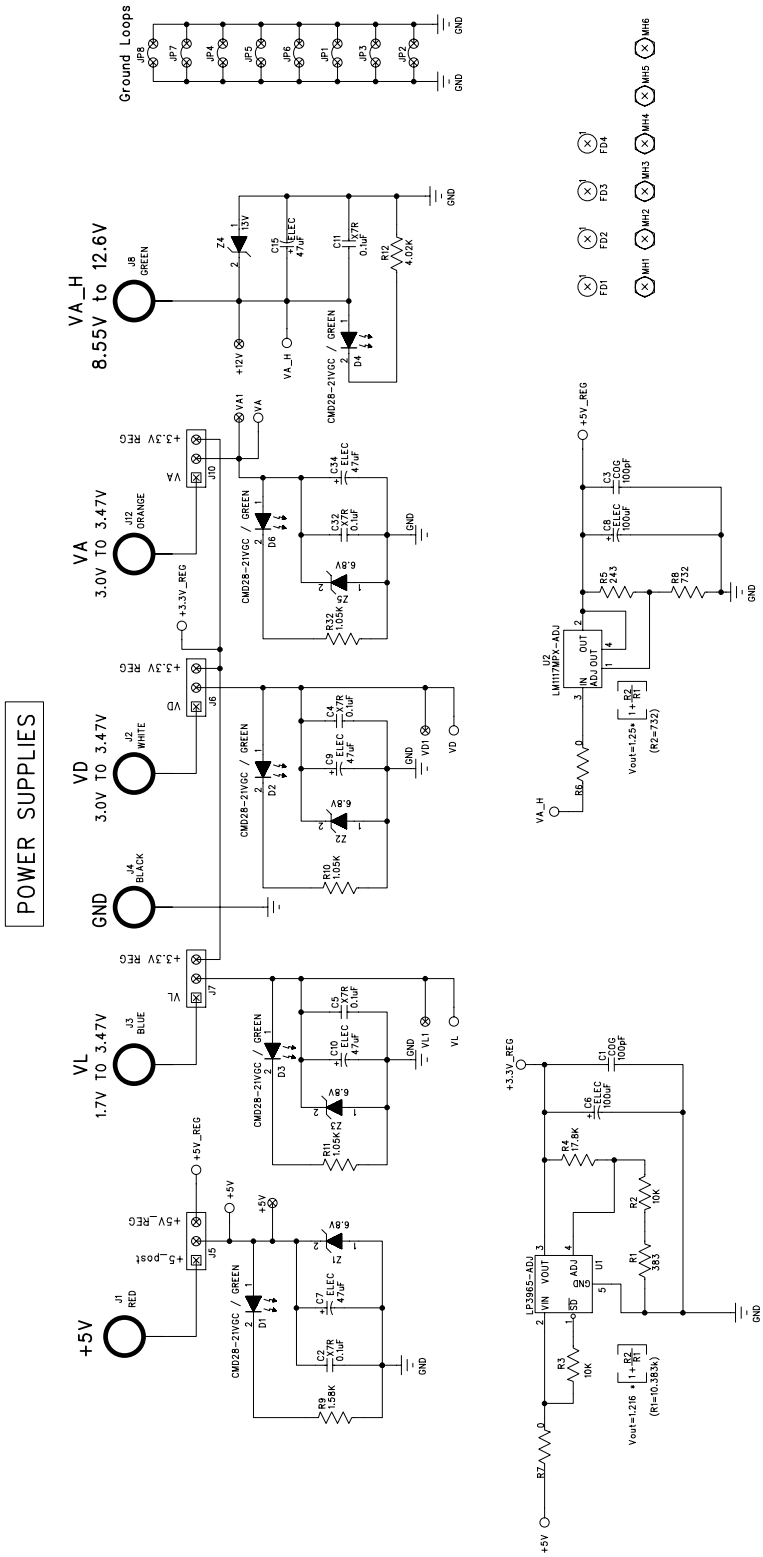

Figure 7. Power Supply Connections

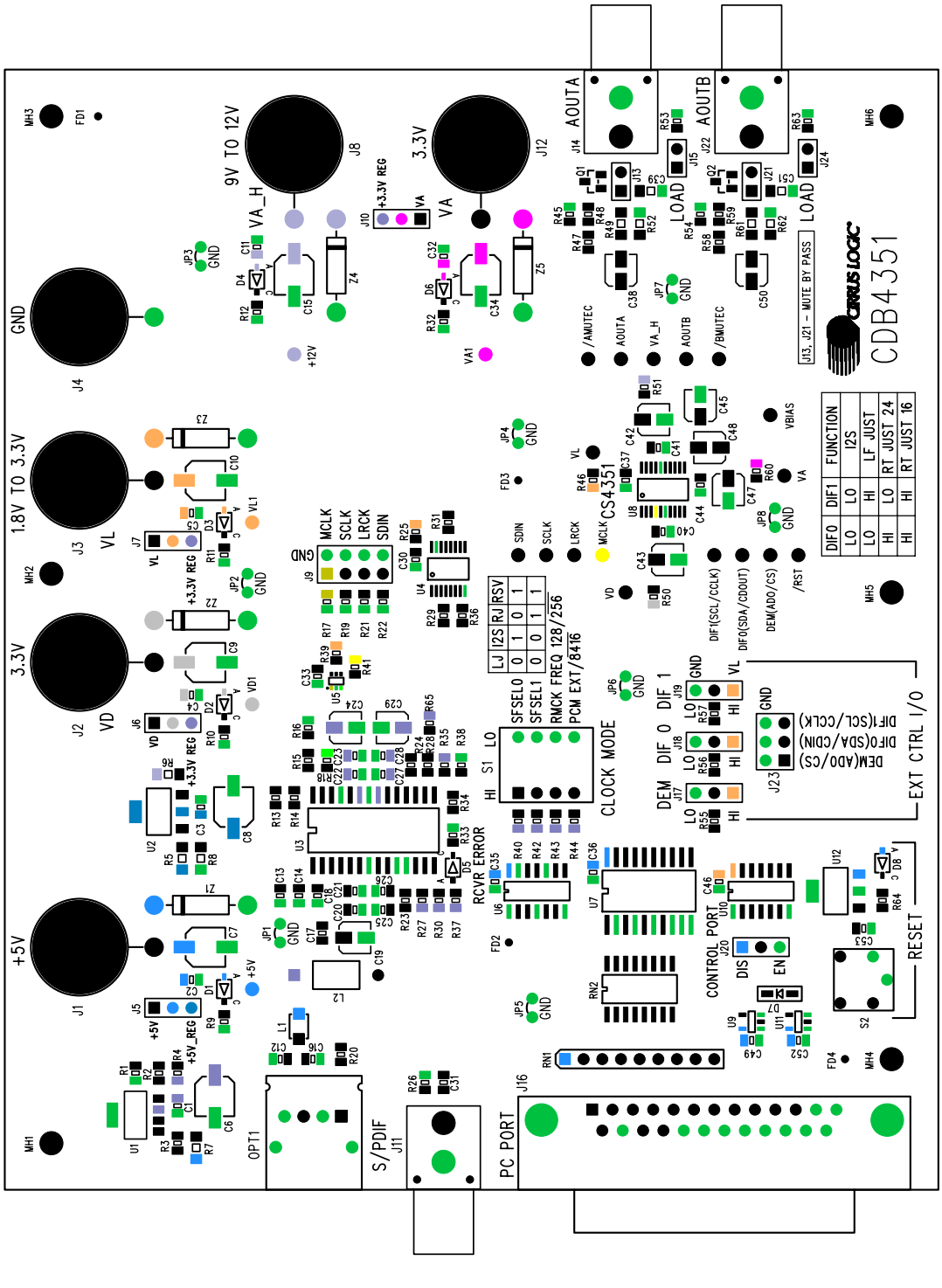

Figure 8. Silkscreen Top

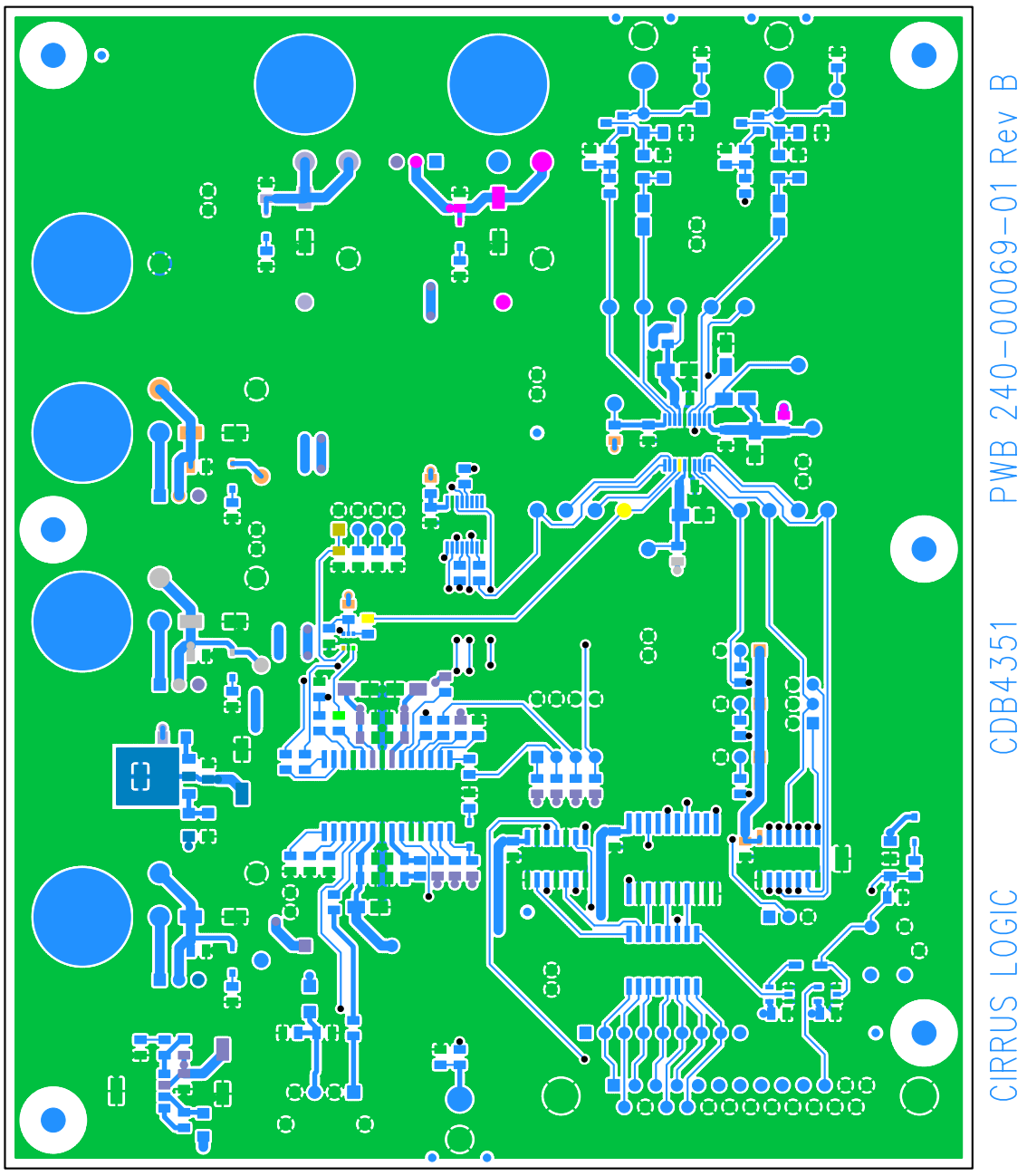

Figure 9. Top Side

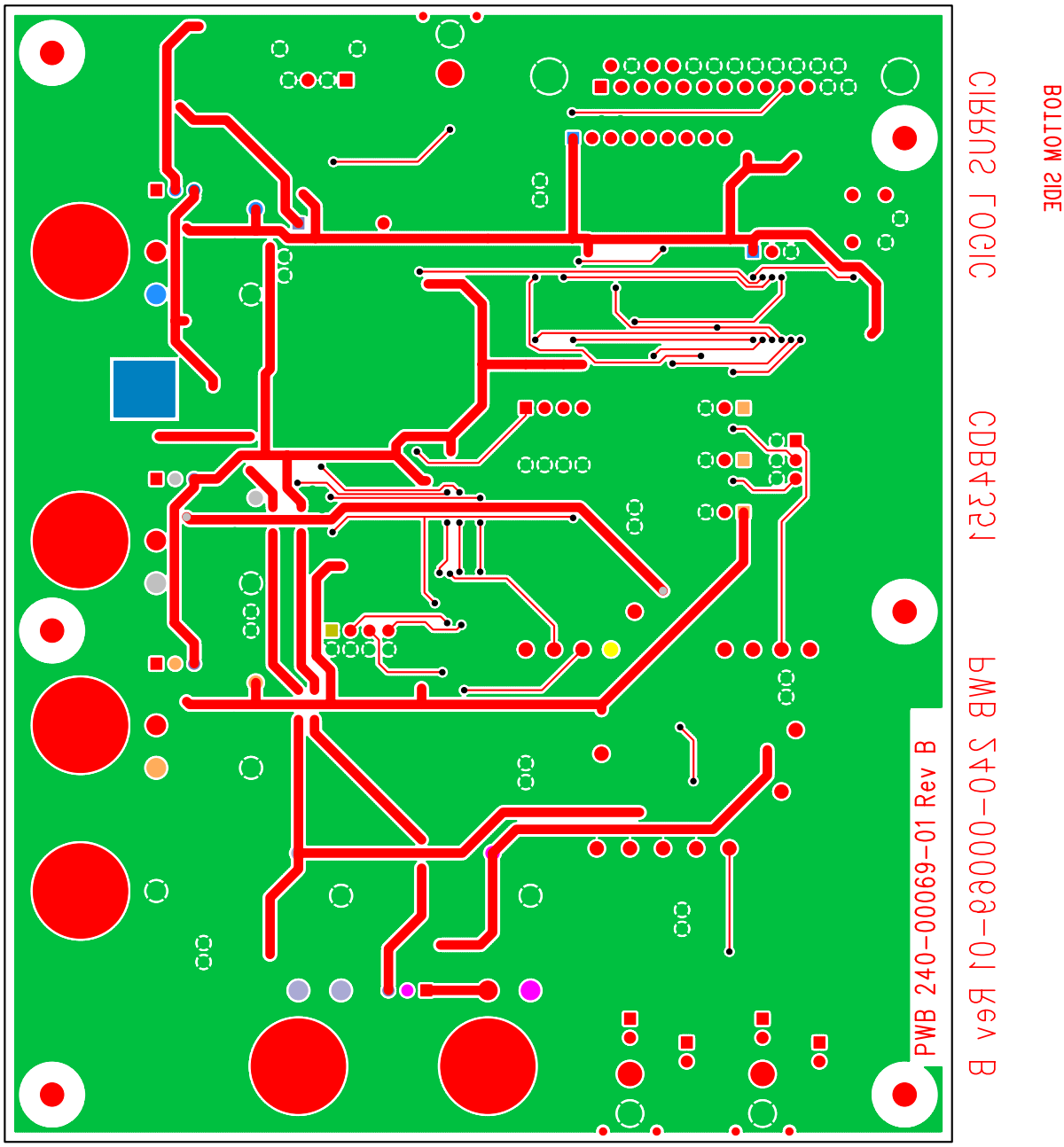

Figure 10. Bottom Side

REVISION HISTORY

Release	Date	Changes
DB1	November 2003	Initial Release
DB2	June 2004	Updated figures 2 and 5 (C48 and R65)
DB3	October 2004	Updated schematic and layout figures to match rev B of the PCB

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