GENERAL DESCRIPTION

The ST16C650A[1] (650A) is a 2.90 to 5.5 volt Universal Asynchronous Receiver and Transmitter (UART) with 5 volt tolerant inputs. This device supports Intel and PC ISA mode data bus interfaces and is software compatible to industry standard 16C450, 16C550, and ST16C580 UARTs.

The 650A has 32 bytes of TX and RX FIFOs and is capable of operating up to serial data rates of 3.125 Mbps at 5 volt supply voltage. The internal registers include the 16C550 register set plus Exar's enhanced registers for additional features to support today's highly demanding data communication needs. The enhanced features include automatic hardware and software flow control, selectable TX and RX trigger levels, and wireless infrared (IrDA) encoder/decoder.

The device provides a new capability to give user the ability to program the wireless infrared encoder output pulse width, hence reducing the power consumption of a handheld unit.

The ST16C650A device comes in the 44-pin PLCC and 48-pin TQFP packages in both the commercial and industrial temperature ranges.

NOTE: *1 Covered by US patents #5,649,122.*

FEATURES

Added features in devices with a top mark date code of "HC YYWW" and newer:

- 2.90 to 5.5 Volt Operation
- 5 Volt Tolerant Inputs
- Automatic RS485 Half-Duplex Control Output
- Programmable Infrared Encoder Pulse Width
- Sleep Mode with Wake-up Indicator
- Device ID & Revision
- Up to 3.125 Mbps Data Rate at 5 Volts

Added feature in devices with a top mark date code of "I2 YYWW" and newer:

- 0 ns address hold time

- Intel or PC Mode 8-bit Bus Interface
- 32-byte Transmit and Receive FIFOs
- Automatic Hardware (RTS/CTS) Flow Control
- Hardware Flow Control Hysteresis
- Automatic Software (Xon/Xoff) Flow Control

APPLICATIONS

- Battery Operated Electronics
- Handheld Terminal
- Personal Digital Assistants
- Cellular Phones DataPort
- Wireless Infrared Data Communications Systems

FIGURE 1. BLOCK DIAGRAM

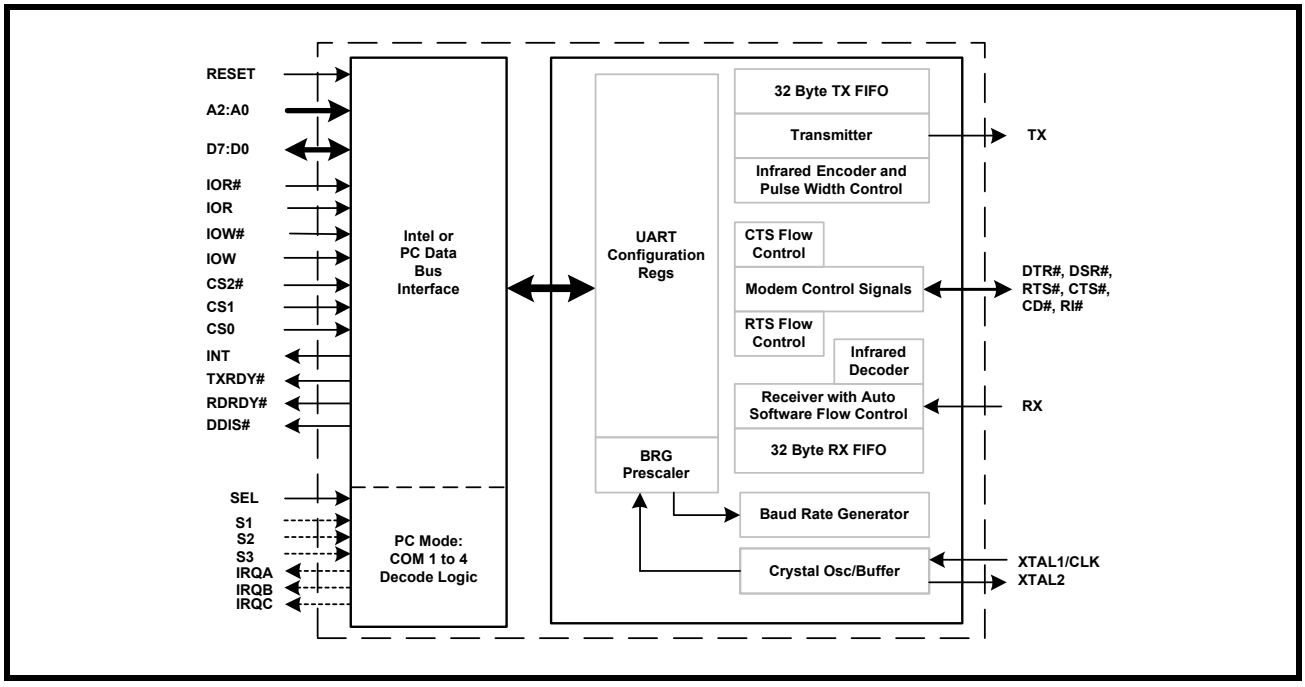
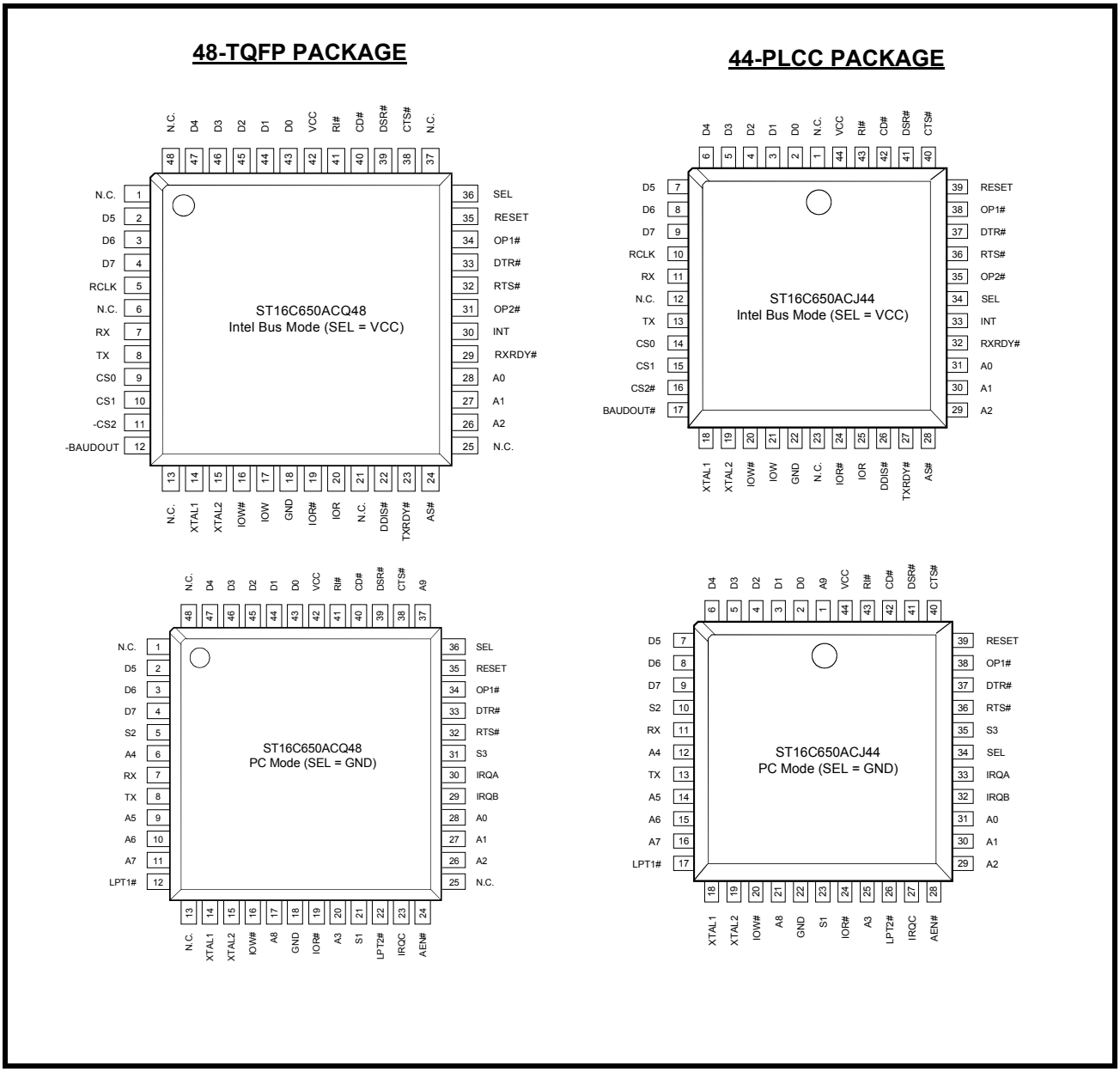


FIGURE 2. INTEL AND PC MODE PIN OUT



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
ST16C650ACJ44	44-Lead PLCC	0°C to +70°C	Active
ST16C650ACQ48	48-Lead TQFP	0°C to +70°C	Active
ST16C650AIJ44	44-Lead PLCC	-40°C to +85°C	Active
ST16C650AIQ48	48-Lead TQFP	-40°C to +85°C	Active

PIN DESCRIPTIONS

NAME	44-PLCC PIN #	48-TQFP PIN #	TYPE	DESCRIPTION
16 (Intel) MODE DATA BUS INTERFACE. The SEL pin is connected to VCC.				
A2 A1 A0	29 30 31	26 27 28	I	**Address bus lines [2:0]** A2:A0 selects internal UART's configuration registers.
D7 D6 D5 D4 D3 D2 D1 D0	9 8 7 6 5 4 3 2	4 3 2 47 46 45 44 43	IO	**Data bus lines [7:0] (bidirectional)**
IOR#	24	19	I	**Input/Output Read (active low)** The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], places it on the data bus to allow the host processor to read it on the leading edge. Its function is the same as IOR, except it is active low. Either an active IOR# or IOR is required to transfer data from 650A to CPU during a read operation. If this input is unused, it should be connected to VCC to minimize supply current.
IOR	25	20	I	**Input/Output Read (active high)** Same as IOR# but active high. If this input is unused, it should be connected to GND to minimize supply current.
IOW#	20	16	I	**Input/Output Write (active low)** The falling edge instigates the internal write cycle and the trailing edge transfers the data byte on the data bus to an internal register pointed by the address lines [A2:A0]. Its function is the same as IOW, except it is active low. Either an active IOW# or IOW is required to transfer data from 650A to the Intel type CPU during a write operation. If this input is unused, it should be connected to VCC to minimize supply current.
IOW	21	17	I	**Input/Output Write (active high)** Same as IOW# but active high. If this input is unused, it should be connected to GND to minimize supply current.
CS0	14	9	I	**Chip Select 0 input (active high)** This input selects the ST16C650A device. If CS1 or CS2# is used as the chip select then this pin must be connected to VCC. The 650A is selected when all three chip selects are active. See **Figure 3** and **Figure 4**.
CS1	15	10	I	**Chip Select 1 input (active high)** This input selects the ST16C650A device. If CS0 or CS2# is used as the chip select then this pin must be connected to VCC. The 650A is selected when all three chip selects are active. See **Figure 3** and **Figure 4**.
CS2#	16	11	I	**Chip Select 2 input (active low)** This input selects the ST16C650A device. If CS0 or CS1 is used as the chip select then this pin must be connected to GND. The 650A is selected when all three chip selects are active. See **Figure 3** and **Figure 4**.

NAME	44-PLCC PIN #	48-TQFP PIN #	TYPE	DESCRIPTION
INT	33	30	O	**Interrupt Output (active high)** This output becomes active whenever the transmitter, receiver, line and/or modem status register has an active condition. See interrupt section for more details. This interrupt output may be set to normal active high or active high open source (see MCR bit-5) to provide wire-OR capability by connecting a 1k to 10k ohms resistor between this pin and ground.
AS#	28	24	I	**Address Strobe input (active low)** In the Intel bus mode, the leading-edge transition of AS# latches the chip selects (CS0, CS1, CS2#) and the address lines A0, A1 and A2. This input is used when the address lines are not stable for the duration of a read or write operation. In devices with top mark date code of "I2 YYWW" and newer, the address bus is latched even if this input is not used. These devices feature a '0 ns' address hold time. See "AC Electrical Characteristics" . If not required, this input can be permanently tied to GND.
TXRDY#	27	23	O	**UART Transmitter Ready (active low)** The output provides the TX FIFO/THR status. See **Table 2**. If it is not used, leave it unconnected.
RXRDY#	32	29	O	**UART Receiver Ready (active low)** This output provides the RX FIFO/RHR status for receive channel A. See **Table 2**. If it is not used, leave it unconnected.
PC Mode Interface Signals. Connect SEL pin to GND to select PC Mode.				
A3 A4 A5 A6 A7 A8 A9	25 12 14 15 16 21 1	20 6 9 10 11 17 37	I	**PC mode additional Address Lines** In the PC mode, these are the additional address lines from the host address bus. They are inputs to the on-board chip select decode function for COM 1-4 and LPT ports. See **Table 1** for details. The pins A4 and A9 have internal 100kΩ pull-up resistors.
AEN#	28	24	I	**Address Enable input (active low)** When AEN# transition to logic 0, it decodes and validates COM 1-4 ports address per S1, S2 and S3 inputs.
S1 S2 S3	23 10 35	21 5 31	I	**Select 1 to 3** These are the standard PC COM 1-4 ports and IRQ selection inputs. See **Table 1** and **Table 3** for details. The S1 pin has an internal 100kΩ pull-up resistor.
IRQA IRQB IRQC	33 32 27	30 29 23	O	**Interrupt Request A, B and C Outputs (active high, tri-state)** These are the interrupt outputs associated with COM 1-4 to be connected to the host data bus. See interrupt section for details. The Interrupt Requests A, B or C functions as IRQx to the PC bus. IRQx is enabled by setting MCR bit-3 to logic 1 and the desired interrupt(s) in the interrupt enable register (IER).
LPT1#	17	12	O	**Line Printer Port-1 Decode Logic Output (active low)** This pin functions as the PC standard LPT-1 printer port address decode logic output, see **Table 1**. The baud rate generator clock output, BAUDOUT#, is internally connected to the RCLK input in the PC mode.

NAME	44-PLCC PIN #	48-TQFP PIN #	TYPE	DESCRIPTION
LPT2#	26	22	O	**Line Printer Port-2 Decode Logic Output (active low)** This pin functions as the PC standard LPT-2 printer port address decode logic output, see Table 1.
MODEM OR SERIAL I/O INTERFACE				
TX	13	8	O	**Transmit Data or wireless infrared transmit data** This output is active low in normal standard serial interface operation (RS-232, RS-422 or RS-485) and active high in the infrared mode.
RX	11	7	I	**Receive Data or wireless infrared receive data** Normal received data input idles at logic 1 condition and logic 0 in the infrared mode. The wireless infrared pulses are applied to the decoder. This input must be connected to its idle logic state in either normal, logic 1, or infrared mode, logic 0, else the receiver may report “receive break” and/or “error” condition(s).
RTS#	36	32	O	**Request to Send or general purpose output (active low)** This port may be used for one of two functions: 1) automatic hardware flow control, see EFR bit-6, MCR bit-1and IER bit-6. 2) RS485 half-duplex direction control, see XFR bits 2 and 5. RTS# output must be asserted before auto RTS flow control can start.
CTS#	40	38	I	**Clear to Send or general purpose input (active low)** If used for automatic hardware flow control, data transmission will be stopped when this pin is de-asserted and will resume when this pin is asserted again. See EFR bit-7 and IER bit-7.
DTR#	37	33	O	**Data Terminal Ready or general purpose output (active low)**
DSR#	41	39	I	**Data Set Ready input or general purpose input (active low)**
CD#	42	40	I	**Carrier Detect input or general purpose input (active low)**
RI#	43	41	I	**Ring Indicator input or general purpose input (active low)**
ANCILLARY SIGNALS				
XTAL1	18	14	I	**Crystal or external clock input. Caution: this input is not 5V tolerant.**
XTAL2	19	15	O	**Crystal or buffered clock output**
RCLK	10	5	I	**Receiver Clock** This input is used as external 16X clock input to the receiver section. Connect the BAUDOUT# pin to this input externally.
BAUDOUT#	17	12	O	**Baud Rate Generator Output (active low)** This pin provides the 16X clock of the selected data rate from the baud rate generator. The RCLK pin must be connected externally to BAUDOUT# when the receiver is operating at the same data rate. When the PC mode is selected, the baud rate generator clock output is internally connected to the RCLK input. This pin then functions as the LPT-1 printer port decode logic output, see Table 3.
SEL	34	36	I	**PC Mode Select (active low)** When this input is at logic 0, it enables the on-board chip select decode function according to PC ISA bus COM[4:1] and IRQ[4:3] port definitions. See Table 3 for details. This pin has an internal 100kΩ pull-up resistor.

NAME	44-PLCC PIN #	48-TQFP PIN #	TYPE	DESCRIPTION
DDIS#	26	22	O	**Drive Disable Output** This pin goes to a logic 0 whenever the host CPU is reading data from the 650A. It can control the direction of a data bus transceiver between the CPU and 650A or other logic functions.
RESET	39	35	I	**Reset Input (active high)** A 40 ns minimum active pulse on this pin will reset the internal registers and all outputs. The UART transmitter output will be held at logic 1, the receiver input will be ignored and outputs are reset. See UART Reset Conditions in **Table 13**.
OP1#	38	34	O	**Output Port 1** General purpose output.
OP2#	35	31	O	**Output Port 2** General purpose output.
VCC	44	42	Pwr	**2.90V to 5.5V supply voltage** All inputs are 5V tolerant except for XTAL for devices with date code top mark of "HC YYWW" and newer. Devices with date code top mark of "GC YYWW" and older do not have 5V tolerant inputs.
GND	22	18	Pwr	**Power supply common ground**
NC	-	1, 13, 25	-	**No Connect**

Pin type: I=Input, O=Output, IO= Input/output, OD=Output Open Drain.

1.0 PRODUCT DESCRIPTION

The ST16C650A (650A) is a low power UART that can operate from 2.90V to 5.5V power supplies. Its inputs are 5V tolerant to facilitate interconnection to transceiver devices of RS-232, RS-422 or RS-485. The 650A is software compatible to the industry standard 16C550 with some additional enhanced features.

The 650A provides serial asynchronous receive data synchronization, parallel-to-serial data conversion for the transmitter section and serial-to-parallel data conversions for receiver section. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmitted data to form a data character (character orientated protocol). Data integrity is ensured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The ST16C650A represents such an integration with greatly enhanced features. The 650A is fabricated with an advanced CMOS process.

The 650A supports standard 8-bit Intel or PC bus interfaces through an input selection pin (SEL input pin). The Intel bus uses the standard read and write signals for all bus transactions. The PC bus mode associates with the PC ISA bus and follow the industry standard PC definitions for COM 1-4 serial port addresses. The 650A includes on-board chip select decode logic and selection for the proper interrupt request. This eliminates the need for an external logic array device.

The 650A has 32-bytes each of transmit and receive FIFOs, automatic RTS/CTS hardware flow control with hysteresis, automatic Xon/Xoff and special character software flow control, selectable transmit and receive FIFO trigger levels, wireless infrared encoder and decoder (IrDA ver. 1.0), programmable baud rate generator with a prescaler of divide by 1 or 4, and data rates up to 3.125 Mbps with a 16X sampling clock rate.

The 650A is an upward solution that provides 32 bytes of transmit and receive FIFO memory, instead of 16 bytes provided in the 16C550, or none in the 16C450. The 650A is designed to work with high speed communication devices, that require fast data processing time. Increased performance is realized in the 650A by the larger transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. For example, the standard ST16C550 with a 16 byte FIFO, unloads 16 bytes of receive data in 1.53 ms (This example uses a character length of 11 bits, including start/stop bits at 115.2Kbps). This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However with the 32 byte FIFO in the 650A, the data buffer will not require unloading/loading for 3.05 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the 4 selectable levels of FIFO trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance especially when operating in a multi-channel environment. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The rich feature set of the 650A is available through internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, selectable TX and RX baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features. In the PC mode, two tri-state interrupt lines (IRQB and IRQC) and one selectable open source interrupt output (IRQA) are available. The open source interrupt scheme allows multiple interrupts to be combined in a “wire-OR” operation, thus reducing the number of interrupt lines in larger systems. Following a power on reset or an external reset, the 650A is software compatible with previous generation of UARTs, 16C450, 16C550 and ST16C580.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 Host Data Bus Interface

The host interface is 8 data bits wide with 3 address lines and control signals to execute bus read and write transactions. The 650A supports 2 type of host interfaces: Intel and PC mode. The Intel bus interface is selected by connecting SEL to a logic 1. The Intel bus interconnections are shown in **Figure 3**. The special PC mode is selected when SEL is connected to a logic 0. The PC mode interconnections are shown in **Figure 4**.

FIGURE 3. ST16C650A INTEL BUS INTERCONNECTIONS

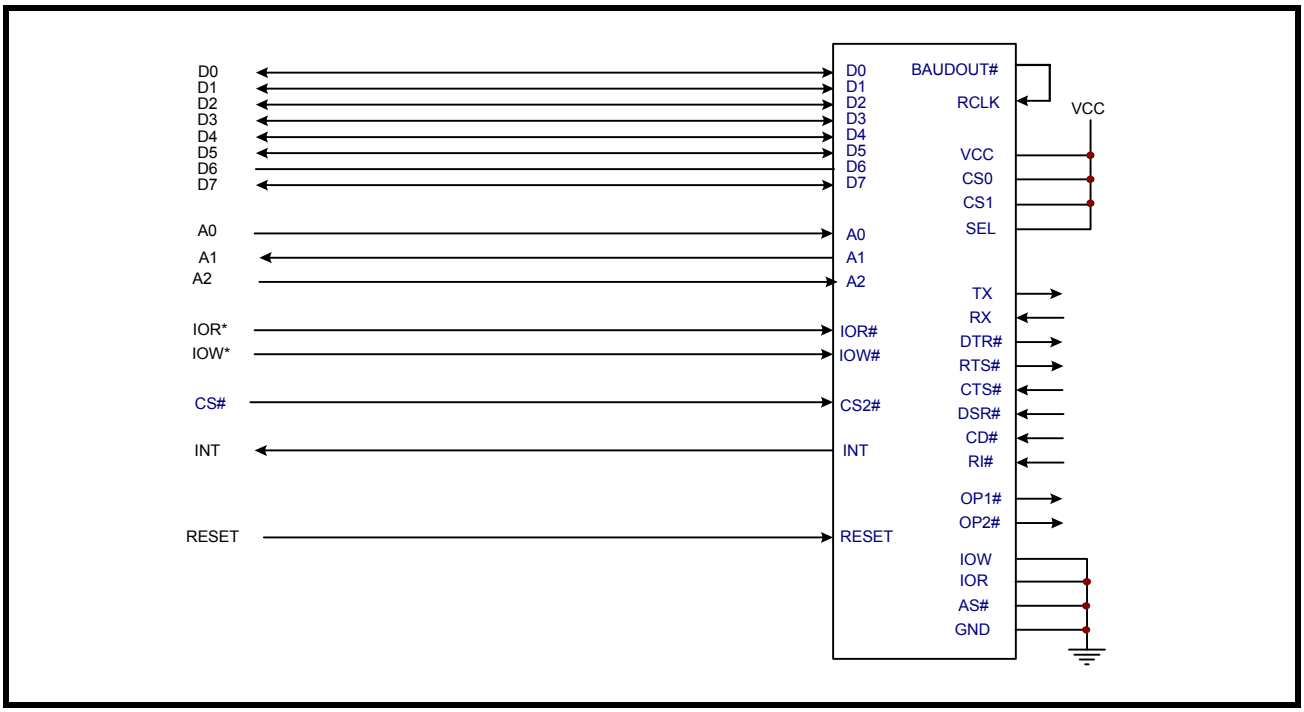
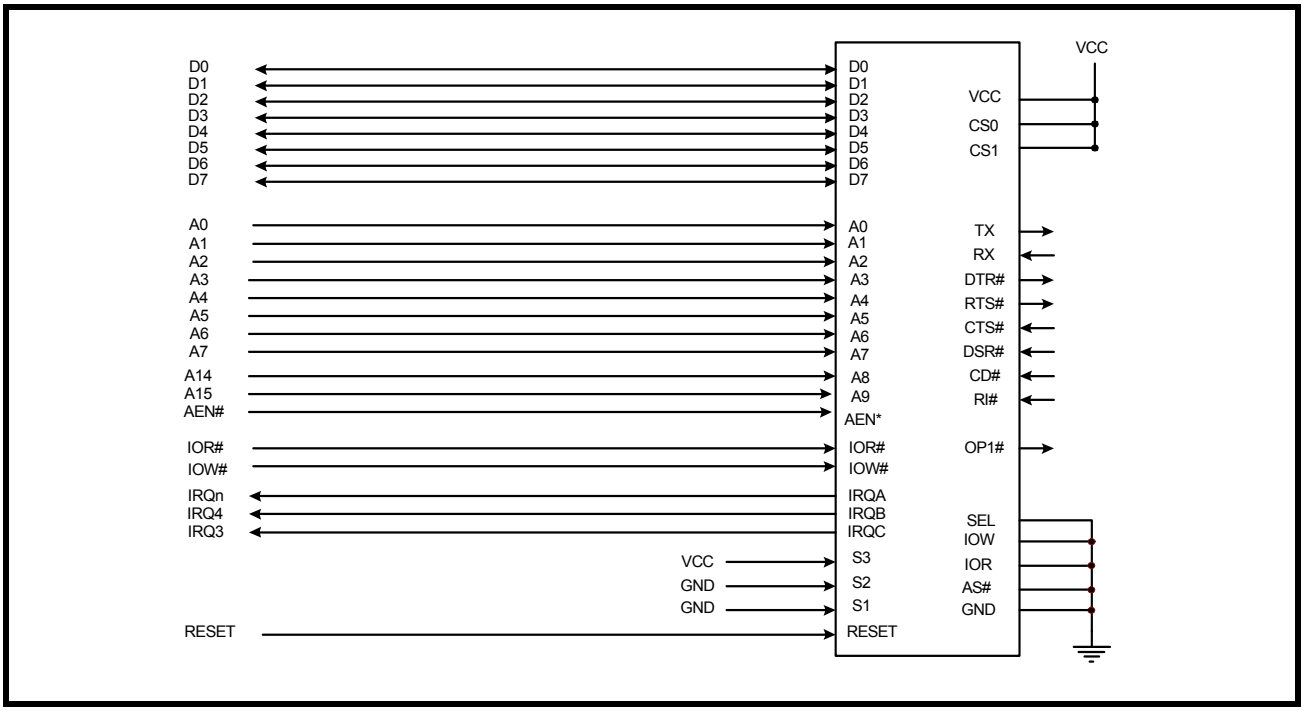


FIGURE 4. ST16C650A PC MODE INTERCONNECTIONS



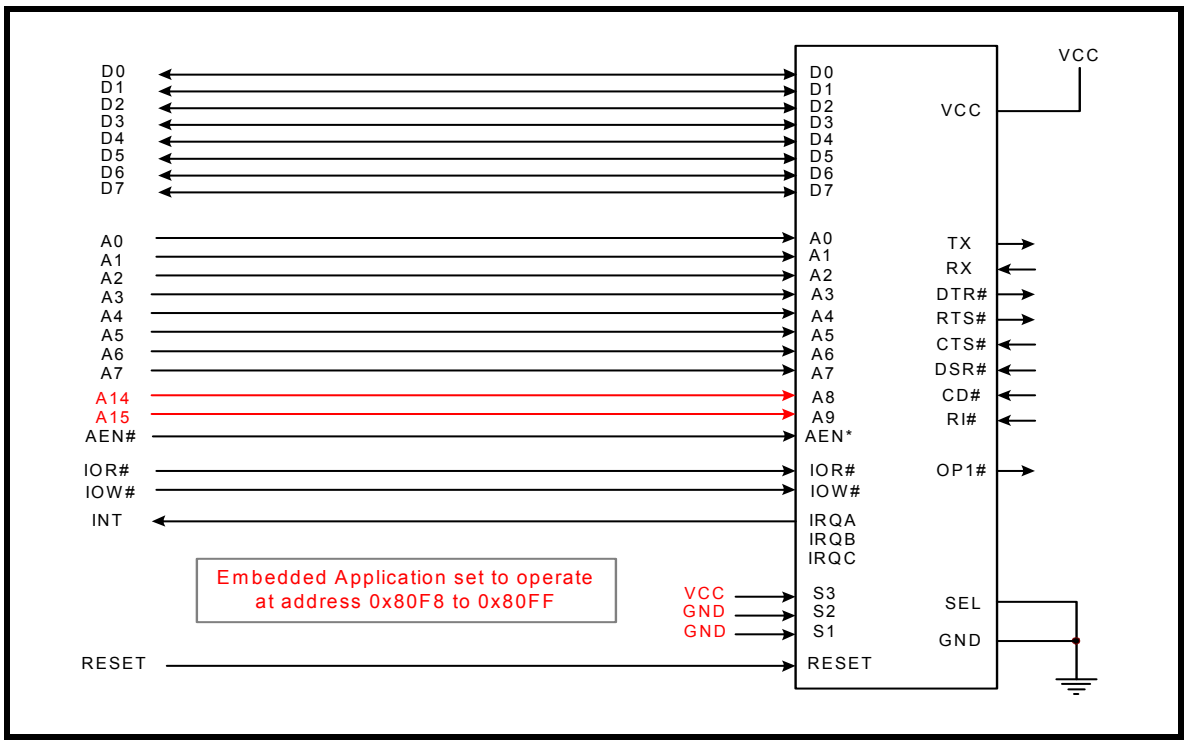
2.1.1 PC MODE

The PC mode interface includes an on-chip address decoder and interrupt selection function for the standard PC COM 1-4 port addresses. The selection is made through three input signals: S1, S2 and S3. The selection summary is shown in Table 1. Although the on-chip address decoder was designed for PC applications ranging from 0x278 to 0x3FF, it can fit into an embedded applications by offsetting the address lines to the 650A. An example is shown in Figure 5 where the UART is operating from 0x80F8 to 0x80FF address space. Operating in the PC mode eliminates external address decode components.

TABLE 1: PC MODE INTERFACE ON-CHIP ADDRESS DECODER AND INTERRUPT SELECTION.

SEL INPUT	S3, S2, S1 INPUTS	A9-A3 ADDRESS LINES TO ON-CHIP DECODER	COM/LPT PORT SELECTION	IRQ OUTPUT SELECTION
0	0 0 0	0x3F8 - 0x3FF	COM-1	IRQB (for PC's IRQ4)
0	0 0 1	0x2F8 - 0x2FF	COM-2	IRQC (for PC's IRQ3)
0	0 1 0	0x3E8 - 0x3EF	COM-3	IRQB (for PC's IRQ4)
0	0 1 1	0x2E8 - 0x2EF	COM-4	IRQC (for PC's IRQ3)
0	1 0 0	0x3F8 - 0x3FF	COM-1	IRQA (for PC's IRQn)
0	1 0 1	0x2F8 - 0x2FF	COM-2	IRQA (for PC's IRQn)
0	1 1 0	0x3E8 - 0x3EF	COM-3	IRQA (for PC's IRQn)
0	1 1 1	0x2E8 - 0x2EF	COM-4	IRQA (for PC's IRQn)
0	- - -	0x278 - 0x27F	LPT-2	N/A
0	- - -	0x378 - 0x37F	LPT-1	N/A

FIGURE 5. PC MODE INTERFACE IN AN EMBEDDED APPLICATION.



2.2 5-Volt Tolerant Inputs

The 650A can acccept up to 5V inputs even when operating at 3.3V. Caution: XTAL1 is not 5 volt tolerant.

2.3 Device Reset

The RESET input resets the internal registers and the serial interface outputs to their default state (see Figure 13). An active high pulse of longer than 40 ns duration will be required to activate the reset function in the device.

2.4 Device Identification and Revision

The ST16C650A provides a Device Identification code and a Device Revision code to distinguish the part from other devices and revisions. To read the identification code from the part, it is required to set the baud rate generator registers DLL and DLM both to 0x00. Now reading the content of the DLM will provide 0x04 for the ST16C650A and reading the content of DLL will provide the revision of the part; for example, a reading of 0x01 means revision A.

2.5 DMA Mode

The device does not support direct memory access. The DMA Mode (a legacy term) in this document does not mean “direct memory access” but refers to data block transfer operation. The DMA mode affects the state of the RXRDY# and TXRDY# output pins. The transmit and receive FIFO trigger levels provide additional flexibility to the user for block mode operation. The LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s) for more data. The user can optionally operate the transmit and receive FIFO in the DMA mode (FCR bit-3=1). When the transmit and receive FIFO are enabled and the DMA mode is disabled (FCR bit-3 = 0), the 650A is placed in single-character mode for data transmit or receive operation. When DMA mode is enabled (FCR bit-3 = 1), the user takes advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the programmed trigger level. In this mode, the 650A sets the TXRDY# pin when the transmit FIFO becomes full, and sets the RXRDY# pin when the receive FIFO becomes empty. The following table shows their behavior. Also see Figures 23 through 28.

TABLE 2: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE

PINS	FCR BIT-0=0 (FIFO DISABLED)	FCR BIT-0=1 (FIFO ENABLED)	
		FCR BIT-3 = 0 (DMA MODE DISABLED)	FCR BIT-3 = 1 (DMA MODE ENABLED)
RXRDY#	0 = 1 byte. 1 = no data.	0 = at least 1 byte in FIFO 1 = FIFO empty.	1 to 0 transition when FIFO reaches the trigger level, or timeout occurs. 0 to 1 transition when FIFO empties.
TXRDY#	0 = THR empty. 1 = byte in THR.	0 = FIFO empty. 1 = at least 1 byte in FIFO.	0 = FIFO has at least 1 empty location. 1 = FIFO is full.

2.6 Interrupt

The output function of interrupt, INT, output changes according to the operating bus type and various factors. Table 3 summarizes its behavior in Intel and PC mode of operation. Multiple interrupts can be wire-OR'ed. This is accomplished by setting MCR bit-5 to a logic 1 and connecting a 1KΩ to 10KΩ resistor between this pin and ground to provide an acceptable logic 0 level.

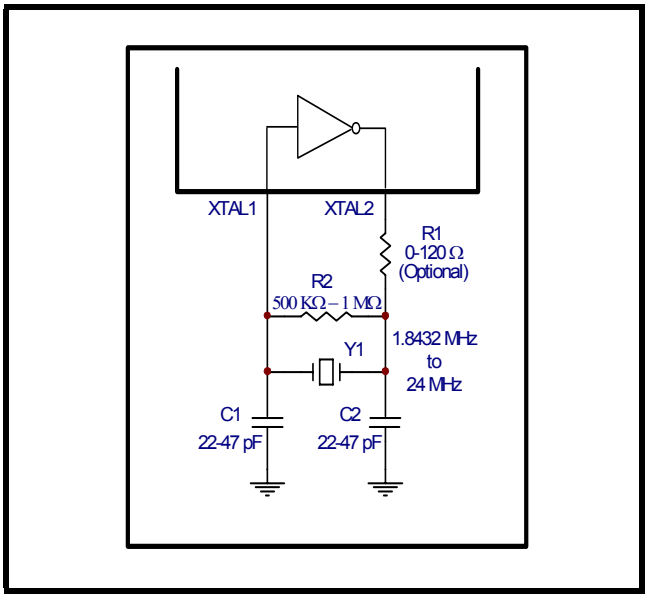
TABLE 3: INTERRUPT OUTPUT (INT AND IRQA) FUNCTIONS

SEL INPUT	S3 INPUT	MCR BIT-5 (INT TYPE SELECT)	MCR BIT-3 (IRQN ENABLE)	INTERRUPT OUTPUT (INT OR IRQA)
Intel Bus Mode				
1	don't care	0	don't care	INT is logic 0 for inactive interrupt. INT is logic 1 for active interrupt (active high)
1	don't care	1	don't care	INT is three-state for inactive interrupt INT is logic 1 for active interrupt (open source). Requires a 1K-10KΩ resistor to GND.
PC Mode				
0	0	don't care	don't care	IRQA is three-state. Either IRQB or IRQC is used, see Table 1.
0	1	don't care	0	IRQA is three-state.
0	1	0	1	IRQA is logic 0 for inactive interrupt. IRQA is logic 1 for active interrupt (active high).
0	1	1	1	IRQA is three-state for no interrupt. IRQA is logic 1 for active interrupt (active high, open source).

2.7 Crystal Oscillator or External Clock

The 650A includes an on-chip oscillator (XTAL1 and XTAL2). The crystal oscillator provides the system clock to the Baud Rate Generators (BRG) in the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. Caution if external clock is used: XTAL1 input is not 5 Volt tolerant. For programming details, see "Programmable Baud Rate Generator."

FIGURE 6. TYPICAL OSCILLATOR CONNECTIONS

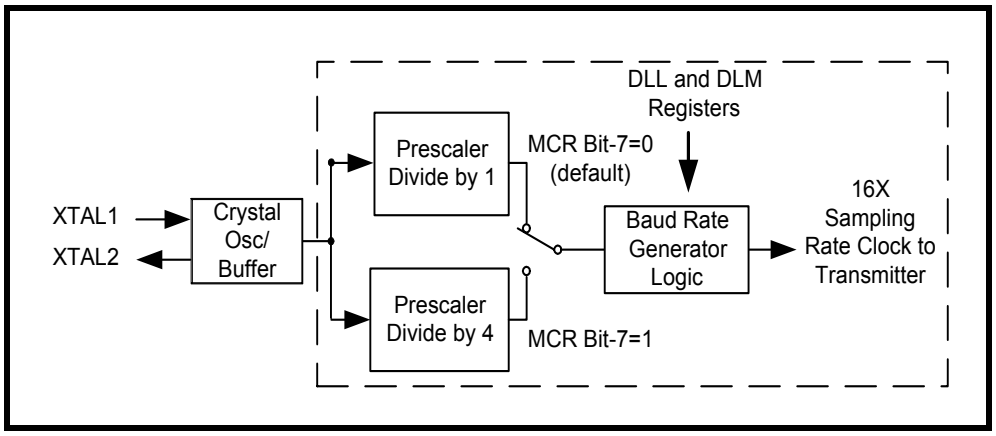


The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100 ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see **Figure 6**). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. Typically, the oscillator connections are shown in **Figure 6**. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

2.8 Programmable Baud Rate Generator

The UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The clock output of the prescaler goes to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (2^{16} -1) to obtain a 16X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL and DLM registers) defaults to a random value upon power up or a reset. Therefore, the BRG must be programmed during initialization to the operating data rate.

FIGURE 7. BAUD RATE GENERATOR



Programming the Baud Rate Generator Registers DLM and DLL provides the capability of selecting the operating data rate. Table 4 shows the standard data rates available with a 14.7456 MHz crystal or external clock at 16X clock rate. When using a non-standard data rate crystal or external clock, the divisor value can be calculated for DLL/DLM with the following equation.

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16)

TABLE 4: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK

OUTPUT Data Rate MCR Bit-7=1	OUTPUT Data Rate MCR Bit-7=0	DIVISOR FOR 16x Clock (Decimal)	DIVISOR FOR 16x Clock (HEX)	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DATA RATE ERROR (%)
100	400	2304	900	09	00	0
600	2400	384	180	01	80	0
1200	4800	192	C0	00	C0	0
2400	9600	96	60	00	60	0
4800	19.2k	48	30	00	30	0
9600	38.4k	24	18	00	18	0
19.2k	76.8k	12	0C	00	0C	0
38.4k	153.6k	6	06	00	06	0
57.6k	230.4k	4	04	00	04	0
115.2k	460.8k	2	02	00	02	0
230.4k	921.6k	1	01	00	01	0

2.9 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 32 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X internal clock. A bit time is 16 clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

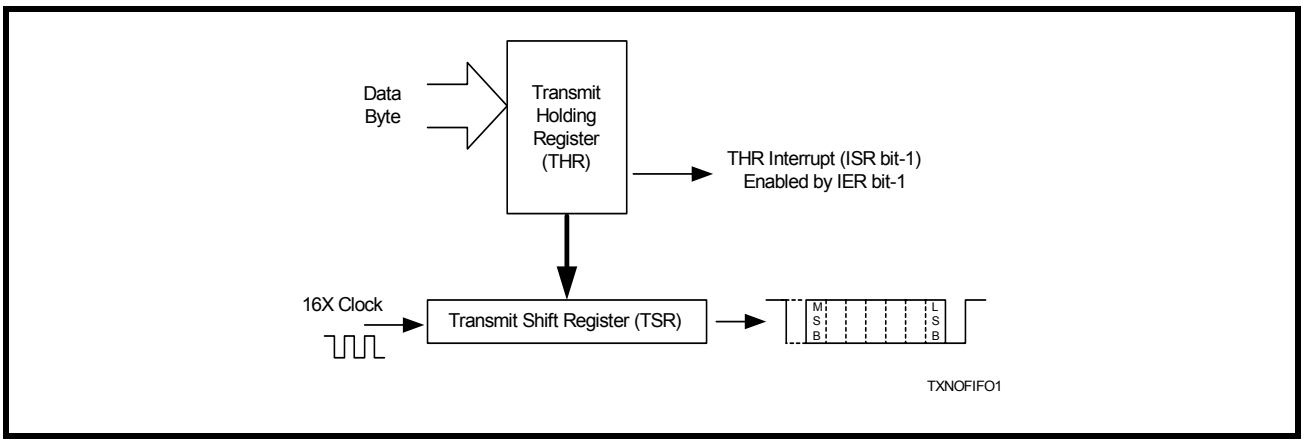
2.9.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including a start bit, data bits, parity bit and stop bit(s). The least-significant-bit (Bit-0) is the first data bit to go out. The THR is the input register to the transmit FIFO of 32 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.9.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

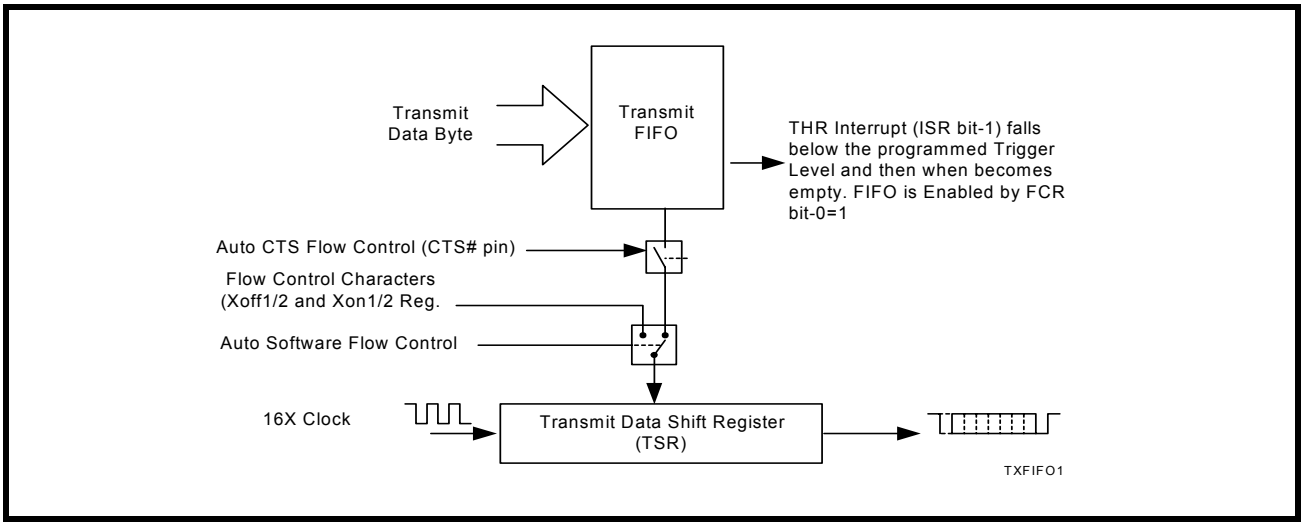
FIGURE 8. TRANSMITTER OPERATION IN NON-FIFO MODE



2.9.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 32 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 9. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



2.10 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 32 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X clock for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X clock rate. After 8 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in the RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level (XFR bit-3). Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.10.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 32 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 10. RECEIVER OPERATION IN NON-FIFO MODE

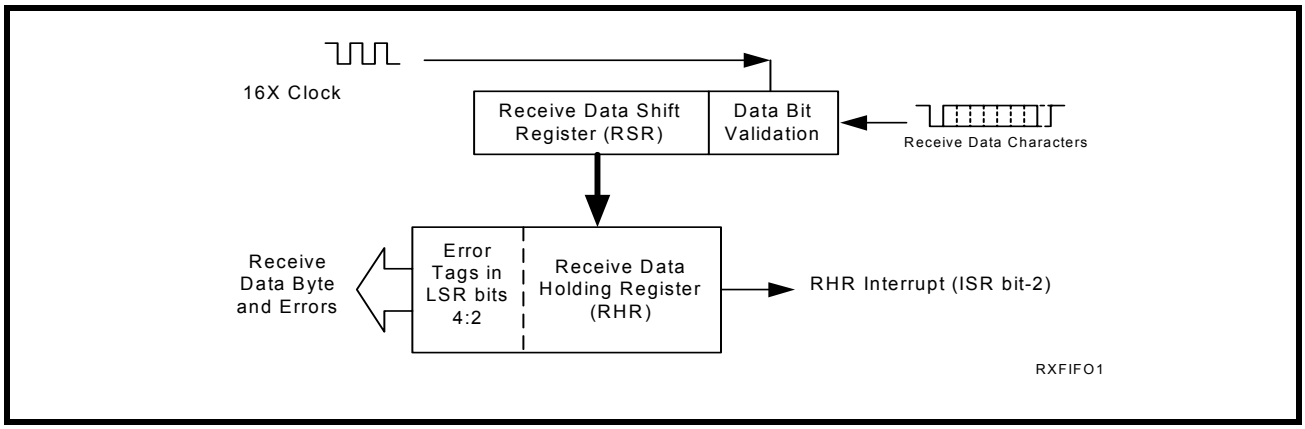
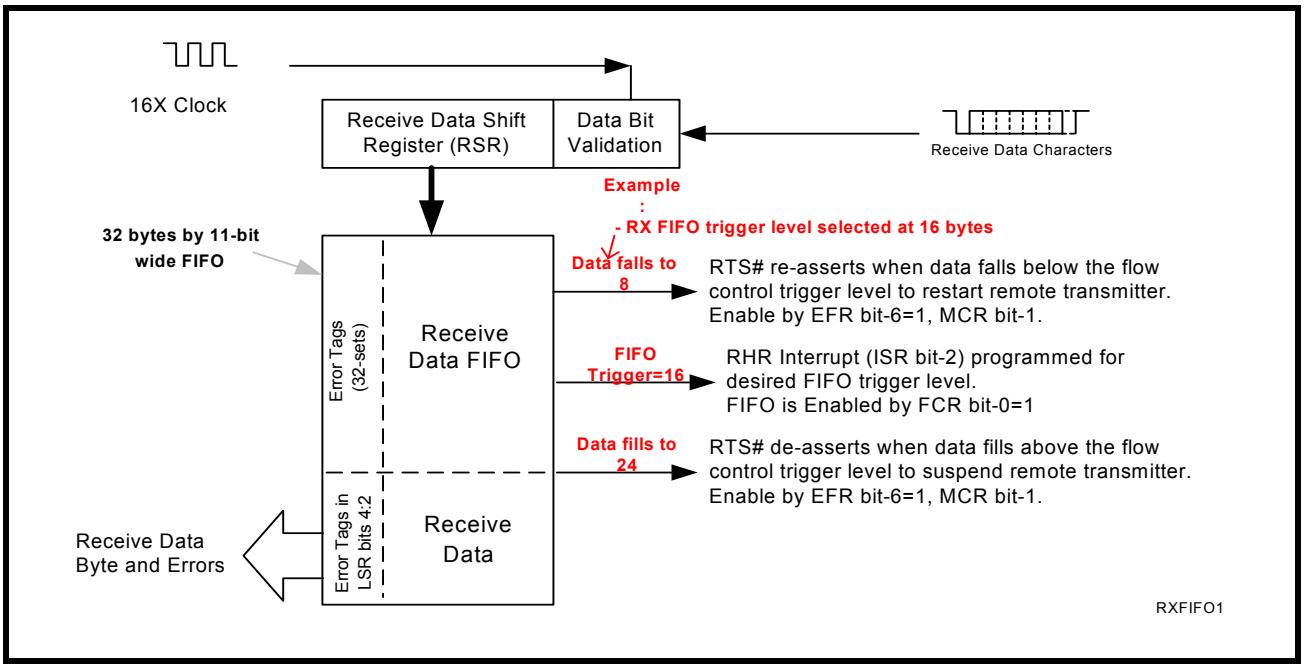


FIGURE 11. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



2.11 Automatic RTS (Hardware) Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see **Figure 12**):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS output pin (MCR bit-1 to logic 1 after it is enabled).

With the Auto RTS function enabled, the RTS# output pin will not be de-asserted (logic 1) when the receive FIFO reaches the programmed trigger level, but will be de-asserted when the FIFO reaches the next trigger level (**See Table 10**). The RTS# output pin will be asserted again after the FIFO is unloaded to the next trigger level below the programmed trigger level. However, even under these conditions, the 650A will continue to accept data until the receive FIFO is full if the remote UART transmitter continues to send data.

- Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS# pin is de-asserted (logic 1) during Auto RTS flow control mode: ISR bit-5 will be set to logic 1.

2.12 Auto CTS Flow Control

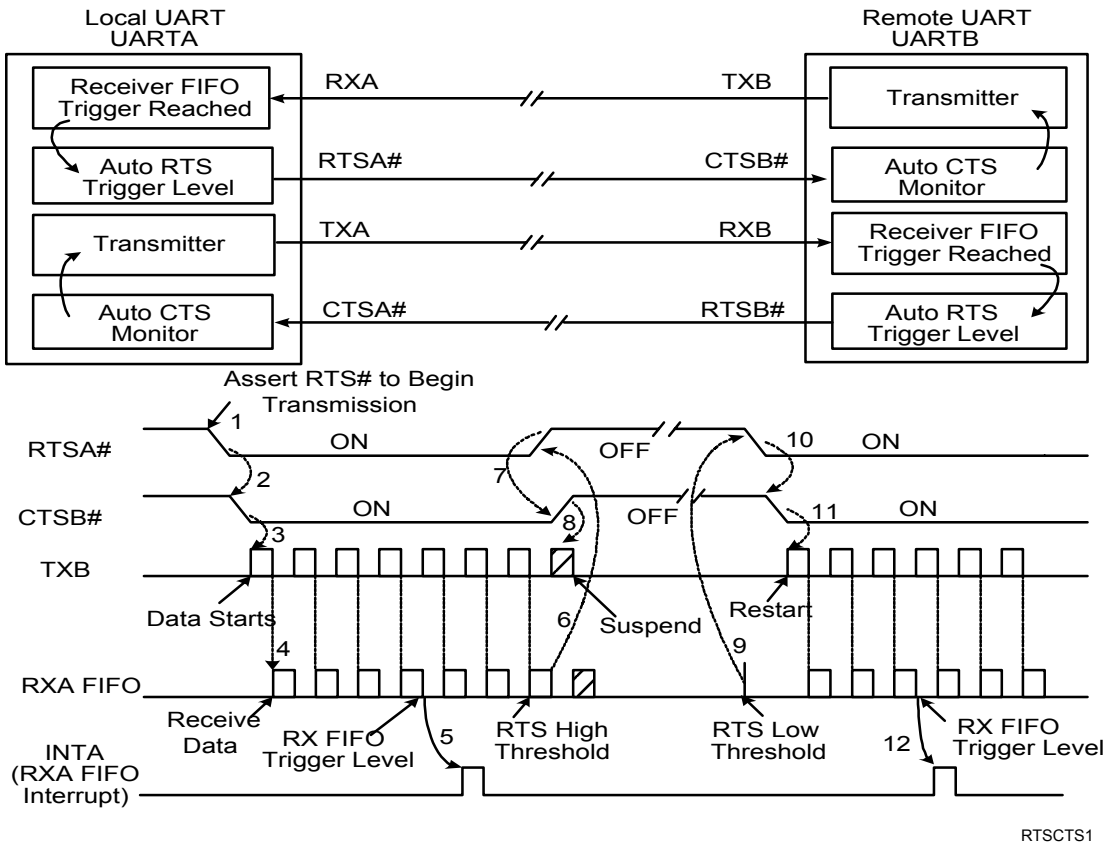
Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see **Figure 12**):

- Enable auto CTS flow control using EFR bit-7.

With the Auto CTS function enabled, the UART will suspend transmission as soon as the stop bit of the character in the Transmit Shift Register has been shifted out. Transmission is resumed after the CTS# input is re-asserted (logic 0), indicating more data may be sent.

- Enable CTS interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (logic 1) during Auto CTS flow control mode: ISR bit-5 will be set to 1.

FIGURE 12. AUTO RTS AND CTS FLOW CONTROL OPERATION



The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

2.13 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (**See Table 12**), the 650A compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If received character(s) (RX) match the programmed values, the 650A will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character values, the 650A will monitor the receive data stream for a match to the Xon-1,2 character value(s). If a match is found, the 650A will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (**See Table 12**) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the 650A compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow

control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the 650A automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The 650A sends the Xoff-1,2 characters two-character-times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level. To clear this condition, the 650A will transmit the programmed Xon-1,2 characters as soon as receive FIFO drops to one trigger level below the programmed trigger level. Table 5 below explains this:

TABLE 5: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO)	XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO)
8	8	8*	0
16	16	16*	8
24	24	24*	16
28	28	28*	24

** After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2 characters); for example, after 2.083ms has elapsed for 9600 baud and 10-bit word length setting.*

2.14 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The 650A compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to the RX FIFO and ISR bit-4 will be set to indicate detection of a special character.

Although the Internal Register Table shows each X-Register with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the X-registers corresponds with the LSB bit for the receive character.

2.15 Auto RS485 Half-duplex Control

The auto RS485 half-duplex direction control changes the behavior of the transmitter when enabled by XFR bit-3. By default, it asserts RTS# (logic 0) output following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote station's response. When the host is ready to transmit next polling data packet again, it only has to load data bytes to the transmit FIFO. The transmitter automatically re-asserts RTS# (logic 1) output prior to sending the data. The RS485 half-duplex direction control output polarity can be inverted by enabling XFR bit-5.

TABLE 6: RS485 HALF-DUPLEX CONTROL

XFR BIT-2	XFR BIT-5	RTS# PIN
0	X	RS485 Half-Duplex control disabled
1	0	Logic 1 = TX Logic 0 = RX
1	1	Logic 1 = RX Logic 0 = TX

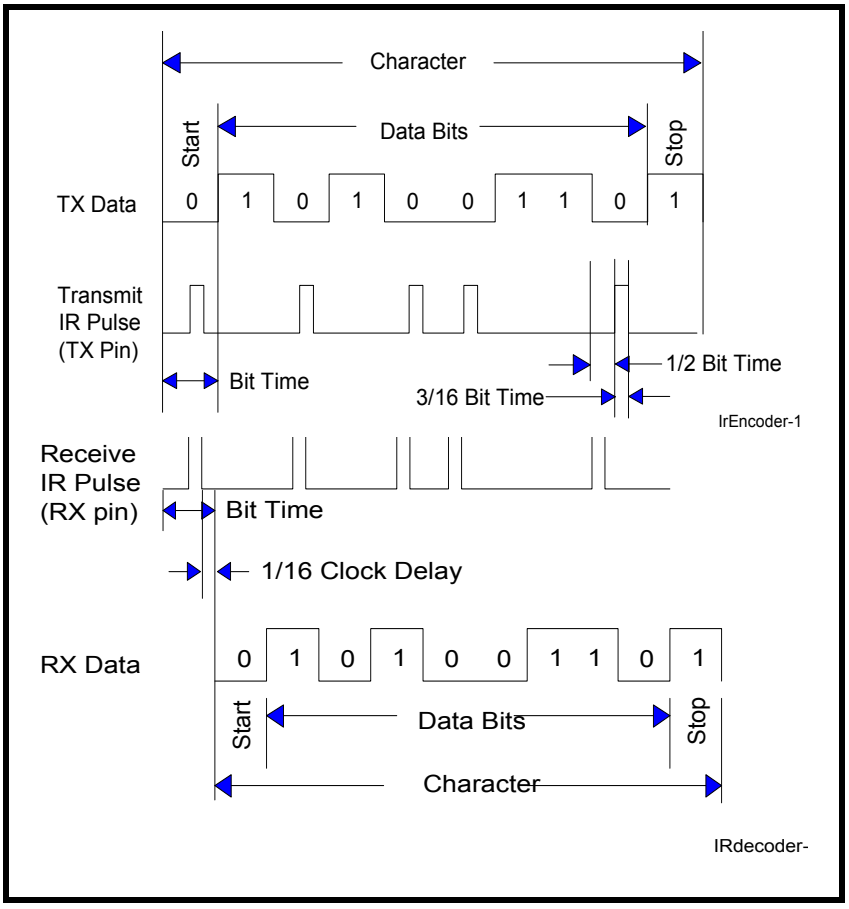
2.16 Infrared Mode

The 650A UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The infrared mode can be enabled by setting MCR bit-6 to a '1'. In the infrared mode, the user can choose to send/receive data either half-duplex or full-duplex. The half-duplex mode is chosen by setting bit-0 of XFR register to a '1'. This prevents echoed data from reaching the receiver. When the infrared feature is enabled, the transmit data outputs, TX, idles at logic zero level. Likewise, the RX input assumes an idle level of logic zero, see **Figure 13**.

The IrDA standard defines the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each "0" bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See **Figure 13** below. The 650A has an additional feature to allow user to vary the transmit pulse width further reducing power consumption of the system where application permits (see IRPW register for details).

The wireless infrared decoder receives the input pulse from the infrared sensing diode on RX pin. Each time it senses a light pulse, it returns a logic 0 to the data bit stream. The 650A also includes another feature - inversion of the IR pulse (XFR register bit-1), where a LOW IR pulse in the receive data stream is recognized as a '0' bit.

FIGURE 13. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



2.17 Sleep Mode & Wake-up Indicator

The 650A is designed to operate with low power consumption. A special sleep mode is included to further reduce power consumption when the chip is not being used. All of these conditions must be satisfied for the 650A to enter sleep mode:

- no interrupts pending 650A (ISR bit-0 = 1)
- sleep mode is enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RX input pin is idling at a logic 1

The 650A stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The 650A resumes normal operation by any of the following:

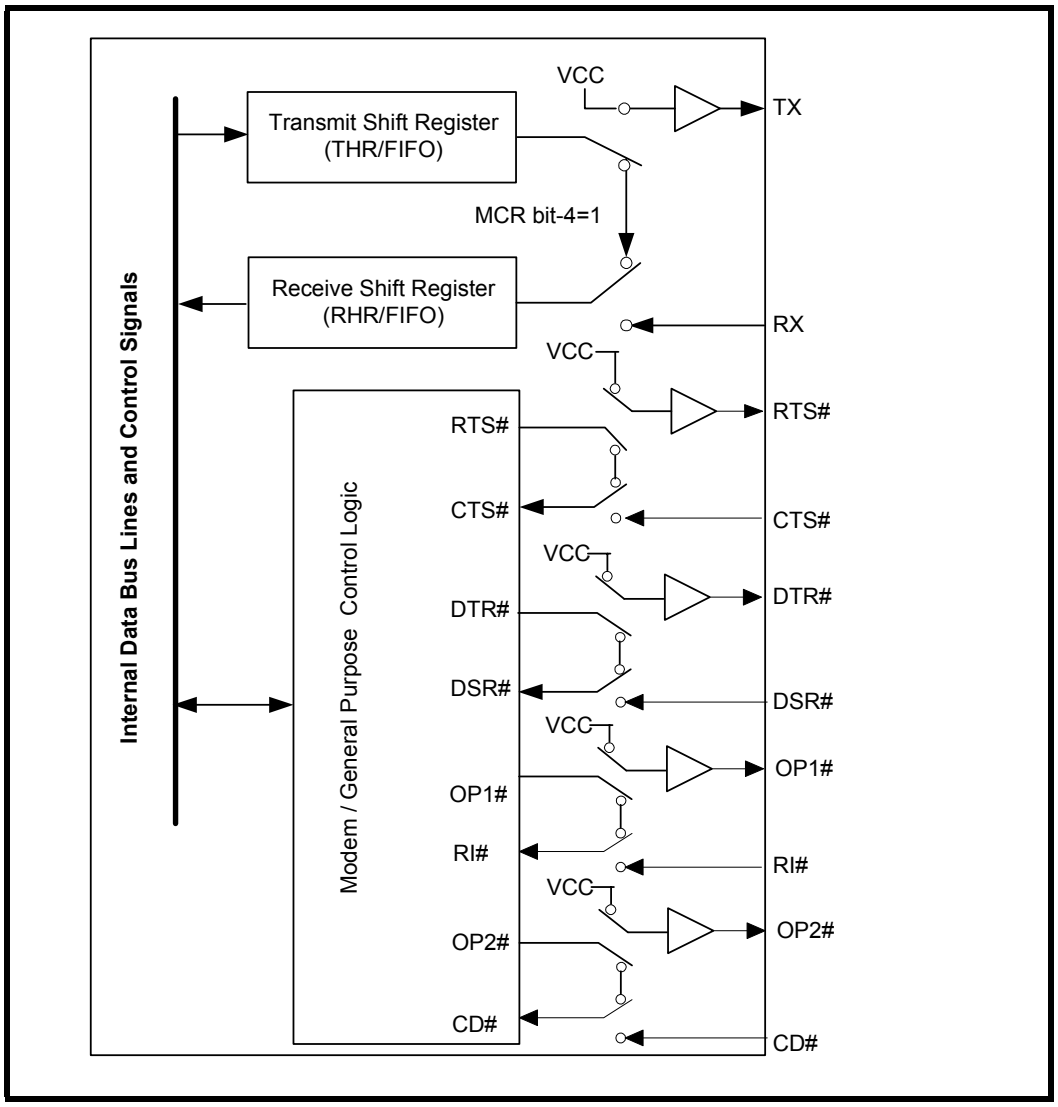
- a receive data start bit transition (logic 1 to 0)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the sleep mode is enabled and the 650A is awakened by one of the conditions described above, an interrupt is issued by the 650A to signal to the CPU that it is awake. The lower nibble of the interrupt source register (ISR) will read a value of 0x1 for this interrupt and reading the ISR clears this interrupt. Since the same value (0x1) is also used to indicate no pending interrupt, users should exercise caution while using the sleep mode. Once awakened, the 650A will return to the sleep mode automatically after any other interrupting condition (the true cause of waking up the 650A) has been serviced. If the 650A is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending. The 650A will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

2.18 Internal Loopback

The 650A UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 14 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX pin is held at logic 1 or mark condition while RTS# and DTR# are de-asserted, and CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input must be held to a logic 1 during loopback test else upon exiting the loopback test the UART may detect and report a false "break" signal. Also, Auto RTS/CTS is not supported during internal loopback.

FIGURE 14. INTERNAL LOOP BACK



3.0 UART CONFIGURATION REGISTERS

The 650A has a set of configuration registers selected by address lines A0 to A2. The based page registers are 16C550 compatible with EXAR enhanced feature registers located on the second page (mirror) addresses. The second page registers are only accessible by setting LCR register to a value of 0xBF. The register set is shown on Table 7 and Table 8. .

TABLE 7: ST16C650A UART CONFIGURATION REGISTERS

ADDRESS	REGISTER	READ/WRITE	COMMENTS
A2 A1 A0			
16550 COMPATIBLE REGISTERS			
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Divisor Latch Low	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DLM - Divisor Latch High	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 0	DREV - Device Revision Code	Read-only	LCR[7] = 1, LCR ≠ 0xBF, DLL, DLM = 0x00
0 0 1	DVID - Device Identification Code	Read-only	LCR[7] = 1, LCR ≠ 0xBF, DLL, DLM = 0x00
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	LCR[7] = 0
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR[7] = 0
1 0 1	LSR - Line Status Register	Read-only	LCR[7] = 0
	XFR - Extra Feature Register	Write-only	LCR[7] = 0, EFR[4] = 1
1 1 0	MSR - Modem Status Register	Read-only	LCR[7] = 0
	IRPW - Infrared Pulse Width Register	Write-only	LCR[7] = 0, EFR[4] = 1
1 1 1	SPR - Scratch Pad Register	Read/Write	LCR[7] = 0
ENHANCED REGISTERS			
0 1 0	EFR - Enhanced Function Register	Read/Write	LCR = 0xBF
1 0 0	Xon-1 - Xon Character 1	Read/Write	LCR = 0xBF
1 0 1	Xon-2 - Xon Character 2	Read/Write	LCR = 0xBF
1 1 0	Xoff-1 - Xoff Character 1	Read/Write	LCR = 0xBF
1 1 1	Xoff-2 - Xoff Character 2	Read/Write	LCR = 0xBF

TABLE 8: UART CONFIGURATION REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1.

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 0
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0/ CTS Int. Enable	0/ RTS Int. Enable	0/ Xoff Int. Enable	0/ Sleep Mode Enable	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ INT Source Bit-5	0/ INT Source Bit-4	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	
0 1 0	FCR	WR	RXFIFO Trigger	RXFIFO Trigger	0/ TXFIFO Trigger	0/ TXFIFO Trigger	DMA Mode Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Par-ity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0/ BRG Pres-caler	0/ IR Mode ENable	0/ INT Type Select	Internal Loop-back Enable	OP2#/ IRQn Output Enable	OP1#	RTS# Output Control	DTR# Output Control	LCR[7]=0
1 0 1	LSR	RD	RX FIFO Error	TSR Empty	THR Empty	RX Break	RX Fram-ing Error	RX Parity Error	RX Data Over-run Error	RX Data Ready	
	XFR	WR	Rsrvd	Rsrvd	Invert RS485 Control Output	Enable XonAny	LSR INT Mode	Auto RS485 Enable	Invert IR RX Input	Enable Half-duplex IR	
1 1 0	MSR	RD	CD	RI	DSR	CTS	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
	IRPW	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

TABLE 8: UART CONFIGURATION REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1.

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
Baud Rate Generator Divisor											
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR ≠ 0xBF
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 0	DREV	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 1 LCR ≠ 0xBF DLL=0x00 DLM=0x00
0 0 1	DVID	RD	0	0	0	0	0	1	0	0	
Enhanced Registers											
0 1 0	EFR	R/W	Auto CTS Enable	Auto RTS Enable	Special Char Select	Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5] MSR[7:4] IRPW[7:0] XFR[7:0]	Soft-ware Flow Cntl Bit-3	Soft-ware Flow Cntl Bit-2	Soft-ware Flow Cntl Bit-1	Soft-ware Flow Cntl Bit-0	LCR=0xBF
1 0 0	XON1	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 1	XON2	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 0	XOFF1	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1	XOFF2	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

4.0 INTERNAL REGISTER DESCRIPTIONS

4.1 Receive Holding Register (RHR) - Read-Only

SEE"RECEIVER" ON PAGE 15.

4.2 Transmit Holding Register (THR) - Write-Only

SEE"TRANSMITTER" ON PAGE 13.

4.3 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR) register.

4.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR bit-0 = a logic 1) and receive interrupts (IER bit-0 = logic 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR bit-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

4.3.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR bit-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the ST16C650A in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR bit-0 indicates there is data in RHR or RX FIFO.

B. LSR bit-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR bits 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR bit-5 indicates THR is empty.

E. LSR bit-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR bit-7 indicates a data error in at least one character in the RX FIFO.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the THR becomes empty in the non-FIFO mode or when data in the FIFO falls below the programmed trigger level in the FIFO mode. If the THR is empty when this bit is enabled, an interrupt will be generated.

- Logic 0 = Disable Transmit Holding Register empty interrupt (default).
- Logic 1 = Enable Transmit Holding Register empty interrupt.

IER[2]: Receive Line Status Interrupt Enable

Any change of state of the LSR register bits 1, 2, 3 or 4 will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bit-1 generates an interrupt immediately when the character has been received. LSR bits 2-4 generate an interrupt either when the character with errors is next to be read out of the FIFO (XFR[3] = 0) or when the received chracter is received (XFR[3] = 1).

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

IER[4]: Sleep Mode Enable (requires EFR bit-4 = 1)

- Logic 0 = Disable Sleep Mode (default).
- Logic 1 = Enable Sleep Mode. **SEE"SLEEP MODE & WAKE-UP INDICATOR" ON PAGE 20.**

IER[5]: Xoff Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the software flow control, receive Xoff interrupt (default).
- Logic 1 = Enable the software flow control, receive Xoff interrupt. **SEE"AUTO XON/XOFF (SOFTWARE) FLOW CONTROL" ON PAGE 17.**

IER[6]: RTS# Output Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the RTS# interrupt (default).
- Logic 1 = Enable the RTS# interrupt. The UART issues an interrupt when the RTS# pin makes a transition from LOW to HIGH.

IER[7]: CTS# Input Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the CTS# interrupt (default).
- Logic 1 = Enable the CTS# interrupt. The UART issues an interrupt when CTS# pin makes a transition from LOW to HIGH.

4.4 Interrupt Status Register (ISR) - Read-Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others queue up for next service. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, Table 9, shows the data values (bit 0-5) for the six prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

4.4.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level and TX FIFO empty (or transmitter empty in auto RS485 control).
- MSR is by any of the MSR bits, 0, 1, 2 and 3.
- Receive Xoff/Special character is by detection of an Xoff or Special character.
- CTS# is when its transmitter toggles the input pin (from low to high) during auto CTS flow control.
- RTS# is when its receiver toggles the output pin (from low to high) during auto RTS flow control.
- Wake-up Indicator: when the UART comes out of sleep mode.

4.4.2 Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.
- Xoff interrupt is cleared by a read to ISR or when Xon character(s) is received.
- Special character interrupt is cleared by a read to ISR or after the next character is received.
- RTS# and CTS# status change interrupts are cleared by a read to the MSR register.
- Wake-up Indicator is cleared by a read to the ISR register.

TABLE 9: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS						SOURCE OF INTERRUPT
	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	1	1	0	0	RXRDY (Receive Data Time-out)
3	0	0	0	1	0	0	RXRDY (Received Data Ready)
4	0	0	0	0	1	0	TXRDY (Transmit Ready)
5	0	0	0	0	0	0	MSR (Modem Status Register)
6	0	1	0	0	0	0	RXRDY (Received Xoff or Special character)
7	1	0	0	0	0	0	CTS#, RTS# change of state
-	0	0	0	0	0	1	None (default) or wake-up indicator

ISR[0]: Interrupt Status

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending (default condition) or the device has come out of sleep mode.

ISR[3:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, 3 and 4 (See Interrupt Source Table 9).

ISR[5:4]: Interrupt Status

These bits are enabled when EFR bit-4 is set to a logic 1. ISR bit-4 indicates that the receiver detected a data match of the Xoff character(s). Note that once set to a logic 1, the ISR bit-4 will stay a logic 1 until a Xon character is received. ISR bit-5 indicates that CTS# or RTS# has changed state.

ISR[7:6]: FIFO Enable Status

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

4.5 FIFO Control Register (FCR) - Write-Only

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

FCR[0]: TX and RX FIFO Enable

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

FCR[1]: RX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No receive FIFO reset (default).
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[2]: TX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No transmit FIFO reset (default).
- Logic 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[3]: DMA Mode Select

Controls the behavior of the TXRDY# and RXRDY# pins. SEE"DMA MODE" ON PAGE 10.

- Logic 0 = DMA Mode disabled (default).
- Logic 1 = DMA Mode enabled.

FCR[5:4]: Transmit FIFO Trigger Select

(logic 0 = default, TX trigger level = one)

These 2 bits set the trigger level for the transmit FIFO interrupt. The UART will issue a transmit interrupt when the number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. Table 10 below shows the selections. EFR bit-4 must be set to '1' before these bits can be accessed.

FCR[7:6]: Receive FIFO Trigger Select

(logic 0 = default, RX trigger level =1).

These 2 bits are used to set the trigger level for the receiver FIFO interrupt. Table 10 shows the complete selections..

TABLE 10: TRANSMIT AND RECEIVE FIFO TRIGGER LEVEL SELECTION WITH AUTO RTS HYSTERESIS

FCR BIT-7	FCR BIT-6	FCR BIT-5	FCR BIT-4	TRANSMIT INT TRIGGER LEVEL	RECEIVE INT TRIGGER LEVEL	AUTO RTS DE-ASSERT	AUTO RTS RE-ASSERT
		0	0	16			
		0	1	8			
		1	0	24			
		1	1	30			
0	0				8	16	0
0	1				16	24	8
1	0				24	28	16
1	1				28	28	24

4.6 Line Control Register (LCR) - Read/Write

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR[1:0]: TX and RX Word Length Select

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	WORD LENGTH
0	0	5 (default)
0	1	6
1	0	7
1	1	8

LCR[2]: TX and RX Stop-bit Length Select

The length of the stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	WORD LENGTH	STOP BIT LENGTH (BIT TIME(S))
0	5,6,7,8	1 (default)
1	5	1-1/2
1	6,7,8	2

LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See Table 11 for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even the number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR BIT-5 = logic 0, parity is not forced (default).
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

TABLE 11: PARITY SELECTION

LCR BIT-5	LCR BIT-4	LCR BIT-3	PARITY SELECTION
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity to mark, "1"
1	1	1	Forced parity to space, "0"

LCR[6]: Transmit Break Enable

When enabled the Break control bit causes a break condition to be transmitted (the TX output is forced to a "space', logic 0, state). This condition remains until disabled by setting LCR bit-6 to a logic 0.

- Logic 0 = No TX break condition (default).
- Logic 1 = Forces the transmitter output (TX) to a "space", logic 0, for alerting the remote receiver of a line break condition.

LCR[7]: Baud Rate Divisors Enable

Baud rate generator divisor (DLL/DLM) enable.

- Logic 0 = Data registers are selected (default).
- Logic 1 = Divisor latch registers are selected if LCR ≠ 0xBF.

4.7 Modem Control Register (MCR) or General Purpose Outputs Control - Read/Write

The MCR register is used for controlling the serial/modem interface signals or general purpose inputs/outputs.

MCR[0]: DTR# Pins

The DTR# pin is a modem control output. If the modem interface is not used, this output may be used for general purpose.

- Logic 0 = Force DTR# output to a logic 1 (default).
- Logic 1 = Force DTR# output to a logic 0.

MCR[1]: RTS# Pins

The RTS# pin is a modem control output and may be used for automatic hardware flow control enabled by EFR bit-6. If the modem interface is not used, this output may be used for general purpose.

- Logic 0 = Force RTS# output to a logic 1 (default).
- Logic 1 = Force RTS# output to a logic 0.

MCR[2]: OP1# Output

OP1# is a general purpose output.

- Logic 0 = OP1# output is at logic 1 (default).
- Logic 1 = OP1# output is at logic 0

MCR[3]: OP2# or IRQn Enable during PC Mode

OP2# is a general purpose output available during the Intel bus interface mode of operation. In the PC bus mode, it enables the IRQn operation. See PC Mode section.

During Intel Bus Mode Operation:

- Logic 0 = OP2# output is at logic 1 (default).
- Logic 1 = OP2# output is at logic 0.

During PC Mode Operation:

- Logic 0 = Disable IRQn operation (default).
- Logic 1 = Enable IRQn operation.

MCR[4]: Internal Loopback Enable

- Logic 0 = Disable loopback mode (default).
- Logic 1 = Enable local loopback mode, see loopback section and **Figure 14**.

MCR[5]: Active/Three-state Interrupt Output Enable

- Logic 0 = Enable active or three-state interrupt output (default).
- Logic 1 = Enable open source interrupt output mode. See **Table 3** for detailed information.

MCR[6]: Infrared Encoder/Decoder Enable

- Logic 0 = Enable the standard modem receive and transmit input/output interface (default).
- Logic 1 = Enable infrared IrDA receive and transmit inputs/outputs. The TX/RX output/input are routed to the infrared encoder/decoder. The data input and output levels conform to the IrDA infrared interface requirement. The infrared TX output is at logic 0 during idle condition. The infrared receive data input polarity is also logic 0, however, it may be inverted when using an infrared module that provides inverted signal output. Use register XFR bit-1 to invert the receive input signal level going to the infrared decoder. Also see XFR bit-0 for half-duplex operation where the receiver can be disabled while transmitting.

MCR[7]: Clock Prescaler Select

- Logic 0 = Divide by one. The input clock from the crystal or external clock is fed directly to the Programmable Baud Rate Generator without further modification, i.e., divide by one (default).
- Logic 1 = Divide by four. The prescaler divides the input clock from the crystal or external clock by four and feeds it to the Programmable Baud Rate Generator, hence, data rates become one forth.

4.8 Line Status Register (LSR) - Read Only

This register provides the status of data transfers between the UART and the host.

LSR[0]: Receive Data Ready Indicator

- Logic 0 = No data in receive holding register or RX FIFO (default).
- Logic 1 = Data has been received and is saved in the receive holding register or RX FIFO.

LSR[1]: Receiver Overrun Flag

- Logic 0 = No overrun error (default).
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error. If IER bit-2 is enabled, an interrupt is generated immediately.

LSR[2]: Receive Data Parity Error Flag

- Logic 0 = No parity error (default).
- Logic 1 = Parity error. The receive character in RHR does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR. If IER bit-2 is enabled, an interrupt is generated when the character is available in the RHR (XFR[3] = 0) or when the character is received (XFR[3] = 1).

LSR[3]: Receive Data Framing Error Flag

- Logic 0 = No framing error (default).
- Logic 1 = Framing error. The receive character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR. If IER bit-2 is enabled, an interrupt is generated when the character is available in the RHR (XFR[3] = 0) or when the character is received (XFR[3] = 1).

LSR[4]: Receive Break Flag

- Logic 0 = No break condition (default).
- Logic 1 = The receiver received a break signal (RX was a logic 0 for at least one character frame time). In the FIFO mode, only one break character is loaded into the FIFO. The break indication is cleared when LSR is read, but the RX input may still be a logic 0. If IER bit-2 is enabled, an interrupt is generated when the character is available in the RHR (XFR[3] = 0) or when the character is received (XFR[3] = 1).

LSR[5]: Transmit Holding Register Empty Flag

This bit is the Transmit Holding Register Empty indicator. The THR bit is set to a logic 1 when the last data byte is transferred from the transmit holding register to the transmit shift register. The bit is reset to logic 0 concurrently with the data loading to the transmit holding register by the host. In the FIFO mode this bit is set when the transmit FIFO is empty, it is cleared when the transmit FIFO contains at least 1 byte.

LSR[6]: Transmit Shift Register Empty Flag

This bit is the Transmit Shift Register Empty indicator. This bit is set to a logic 1 whenever the transmitter goes idle. It is set to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmit FIFO and transmit shift register are both empty.

LSR[7]: Receive FIFO Data Error Flag

- Logic 0 = No FIFO error (default).
- Logic 1 = A global indicator for the sum of all error bits in the RX FIFO. At least one parity error, framing error or break indication is in the FIFO data. This bit clears when there is no more error(s) in the FIFO.

4.9 Extra Feature Register (XFR) - Write Only

This register provides additional features and controls to the ST16C650A UART.

XFR [0]: Half-duplex Infrared Mode Enable

When infrared mode is enabled, MCR bit-6=1, this bit selects the infrared mode to operate in normal full-duplex or half-duplex mode. This half-duplex mode feature is very desirable when the UART does not want to “see” its own data that may be reflected.

- Logic 0 = Disable. The receiver is active during data transmission.
- Logic 1 = Enable half-duplex operation. The infrared receiver is disabled during data transmission.

XFR [1]: Invert Received Infrared Input Signal

This bit controls the input polarity of the infrared data.

- Logic 0 = Infrared data input idles at logic 0 (default).
- Logic 1 = Infrared data idles at logic 1, pulses low.

XFR [2]: Auto RS485 Enable

This bit enables the auto RS485 direction control feature for half-duplex operation with RS-485 transceiver. The feature should only be enabled when normal RTS# output and auto RTS flow control are not used.

- Logic 0 = Disable the auto RS485 direction control function. This allows normal RTS# output or auto RTS flow control operation.
- Logic 1 = Enable the auto RS485 direction function. The RTS# output will automatically change its logic state to control the RS-485 transceiver from sending and receiving. **SEE”AUTO RS485 HALF-DUPLEX CONTROL” ON PAGE 18.**

XFR [3]: LSR Bad Data Interrupt Operation

When the LSR interrupt is enabled, IER bit-2=1, this bit selects when the interrupt pin (INT) will report received character error: parity, framing or break. Use this feature only if application needs immediate knowledge when a bad character is received.

- Logic 0 = Received data error interrupt (LSR interrupt) will be generated when the bad character is available for reading from the FIFO. This is compatible to industry standard 16C550 operation.
- Logic 1 = Received data error interrupt (LSR interrupt) is generated immediately upon receipt of the bad character. It will be reset when LSR is read. If user does not read the bad character out, another bad character interrupt is generated when it’s available for reading from the FIFO.

XFR [4]: Xon-Any Enable

This bit enables and disables the Xon-Any function when Xon/Xoff software flow control is enabled.

- Logic 0 = Disable the Xon-Any function.
- Logic 1 = Enable the Xon-Any function. The receiver will use any received character as an Xon character and resume data transmission.

XFR [5]: Invert Auto RS-485 Control Output

When Auto RS485 feature is enabled, XFR[2]=1, RTS# output automatically changes its logic state to control the RS-485 transceiver.

- Logic 0 = During auto RS-485, RTS# control output signal to the transceiver is logic 1 for transmit and logic 0 for receive.
- Logic 1 = The RTS# output control signal to the transceiver is logic 0 for transmit and logic 1 for receive. User must assert RTS# for operation to take effect.

XFR [7:6]: Reserved

4.10 Modem Status Register (MSR) - Read Only

This register provides the current state of the modem interface signals, or other peripheral device that the UART is connected. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used as general purpose inputs/outputs when they are not used with modem signals.

MSR[0]: Delta CTS# Input Flag

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[1]: Delta DSR# Input Flag

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[2]: Delta RI# Input Flag

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from a logic 0 to a logic 1, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[3]: Delta CD# Input Flag

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[4]: CTS Input Status

CTS# pin may function as automatic hardware flow control signal input if it is enabled and selected by Auto CTS (EFR bit-7). Auto CTS flow control allows starting and stopping of local data transmissions based on the modem CTS# signal. A logic 1 on the CTS# pin will stop UART transmitter as soon as the current character has finished transmission, and a logic 0 will resume data transmission. Normally MSR bit-4 bit is the compliment of the CTS# input. However in the loopback mode, this bit is equivalent to the RTS# bit in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.

MSR[5]: DSR Input Status

DSR# (active high, logical 1). Normally this bit is the compliment of the DSR# input. In the loopback mode, this bit is equivalent to the DTR# bit in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.

MSR[6]: RI Input Status

RI# (active high, logical 1). Normally this bit is the compliment of the RI# input. In the loopback mode this bit is equivalent to bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.

MSR[7]: CD Input Status

CD# (active high, logical 1). Normally this bit is the compliment of the CD# input. In the loopback mode this bit is equivalent to bit-3 in the MCR register. The CD# input may be used as a general purpose input when the modem interface is not used.

4.11 Infrared Transmit Pulse Width Control Register (IRPW) - Write Only

The IRPW register allows the user to program the encoder's pulse width. This cuts the LED on-time, hence, reducing power consumption.

IRPW [7:0]: Pulse width control

A 0x00 value (default) will set the pulse width to normal width of 3/16 of the data bit rate. The programmable infrared pulse width can be calculated using the following equation:

- Infrared pulse width (PW) = Crystal clock period x 'N', where 'N' is the value in IRPW from 1 to 255.

Examples:

Crystal frequency = 14.7456MHz (clock period of 67.82ns)

PW = 67.82 x 'N' or ranges from 67.82ns to 17.29ms

Caution: Never allow PW to exceed the operating data rate bit period, else the encoder stops.

4.12 Scratch Pad Register (SPR)

This is an 8-bit general purpose register for the user to store temporary data. The content of this register is preserved during sleep mode but becomes 0xFF (default) after a reset or a power off-on cycle.

4.13 Baud Rate Generator Divisors (DLL and DLM) - Read/Write

The Baud Rate Generator (BRG) is a 16-bit counter that generates the data rate for the transmitter. The rate is programmed through registers DLL and DLM which are only accessible when LCR bit-7 is set to '1'. See Programmable Baud Rate Generator section for more details. The concatenation of the contents of DLM and DLL gives the 16-bit divisor value which is used to calculate the baud rate:

- Baud Rate = (Clock Frequency / 16) / Divisor

Also see MCR bit-7 and Table 4.

4.14 Device Identification Register (DVID) - Read Only

This register contains the device ID (0x04 for ST16C650A). Prior to reading this register, DLL and DLM should be set to 0x00.

4.15 Device Revision Register (DREV) - Read Only

This register contains the device revision information. For example, 0x01 means revision A. Prior to reading this register, DLL and DLM should be set to 0x00.

4.16 Enhanced Feature Register (EFR)

Enhanced features are enabled or disabled using this register. Bit 0-3 provide single or dual consecutive character software flow control selection (see Table 12). When the Xon1 and Xon2 and Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential characters. Caution: note that whenever changing the TX or RX flow control bits, always reset all bits back to logic 0 (disable) before programming a new setting.

EFR[3:0]: Software Flow Control Select

Combinations of software flow control can be selected by programming these bits.

TABLE 12: SOFTWARE FLOW CONTROL FUNCTIONS

EFR BIT-3	EFR BIT-2	EFR BIT-1	EFR BIT-0	TRANSMIT AND RECEIVE SOFTWARE FLOW CONTROL
0	0	0	0	No TX and RX flow control (default and reset)
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1/Xoff1
0	1	X	X	Transmit Xon2/Xoff2
1	1	X	X	Transmit Xon1 and Xon2/Xoff1 and Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1/Xoff1
X	X	0	1	Receiver compares Xon2/Xoff2
1	0	1	1	Transmit Xon1/ Xoff1, Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Transmit Xon2/Xoff2, Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmit Xon1 and Xon2/Xoff1 and Xoff2, Receiver compares Xon1 and Xon2/Xoff1 and Xoff2
0	0	1	1	No transmit flow control, Receiver compares Xon1 and Xon2/Xoff1 and Xoff2

EFR[4]: Enhanced Function Bits Enable

Enhanced function control bit. This bit enables IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7, XFR bits 0-7 and IRPW bits 0-7 to be modified. After modifying any enhanced bits, EFR bit-4 can be set to a logic 0 to latch the new values. This feature prevents legacy software from altering or overwriting the enhanced functions once set. Normally, it is recommended to leave it enabled, logic 1.

- Logic 0 = modification disable/latch enhanced features. IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7, XFR bits 0-7 and IRPW bits 0-7 are saved to retain the user settings. After a reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7, XFR bits 0-7 and IRPW bits 0-7 are set to a logic 0 to be compatible with ST16C550 mode. (default).
- Logic 1 = Enables the above-mentioned register bits to be modified by the user.

EFR[5]: Special Character Detect Enable

- Logic 0 = Special Character Detect Disabled. (default)
- Logic 1 = Special Character Detect Enabled. The UART compares each incoming receive character with data in Xoff-2 register. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of the special character. Bit-0 corresponds with the LSB bit for the receive character. If flow control is set for comparing Xon1, Xoff1 (EFR [1:0]=10) then flow control and special character work normally. However, if flow control is set for comparing Xon2, Xoff2 (EFR[1:0]=01) then flow control works normally, but Xoff2 will not go to the FIFO, and will generate an Xoff interrupt and a special character interrupt.

EFR[6]: Auto RTS Flow Control Enable

RTS# output may be used for hardware flow control by setting EFR bit-6 to logic 1. When Auto RTS is selected, an interrupt will be generated (if IER bit-6 = 1) when the receive FIFO is filled to the programmed trigger level and RTS de-asserts to a logic 1 at the next upper trigger level. RTS# will return to a logic 0 when FIFO data falls below the next lower trigger level. The RTS# output must be asserted (logic 0) before the auto RTS can take effect. RTS# pin will function as a general purpose output when hardware flow control is disabled.

- Logic 0 = Automatic RTS flow control is disabled. (default)
- Logic 1 = Enable Automatic RTS flow control.

EFR[7]: Auto CTS Flow Control Enable

Automatic CTS Flow Control.

- Logic 0 = Automatic CTS flow control is disabled. (default)
- Logic 1 = Enable Automatic CTS flow control. Data transmission stops when CTS# input de-asserts to logic 1. Data transmission resumes when CTS# input returns to a logic 0.

4.17 Software Flow Control Registers (XOFF1, XOFF2, XON1, XON2) - Read/Write

These registers are used as the programmable software flow control characters xoff1, xoff2, xon1, and xon2. For more details, see **Table 5**.

TABLE 13: UART RESET CONDITIONS

REGISTERS	RESET STATE
DLL	Bits 7-0 = 0xXX
DLM	Bits 7-0 = 0xXX
RHR	Bits 7-0 = 0xXX
THR	Bits 7-0 = 0xXX
IER	Bits 7-0 = 0x00
FCR	Bits 7-0 = 0x00
ISR	Bits 7-0 = 0x01
LCR	Bits 7-0 = 0x00
MCR	Bits 7-0 = 0x00
LSR	Bits 7-0 = 0x60
XFR	Bits 7-0 = 0x00
MSR	Bits 3-0 = logic 0 Bits 7-4 = logic levels of the inputs
IRPW	Bits 7-0 = 0x00
SPR	Bits 7-0 = 0xFF
EFR	Bits 7-0 = 0x00
XON1	Bits 7-0 = 0x00
XON2	Bits 7-0 = 0x00
XOFF1	Bits 7-0 = 0x00
XOFF2	Bits 7-0 = 0x00
I/O SIGNALS	**RESET STATE**
TX	Normal = logic 1 Infrared = logic 0
RTS#	Logic 1
DTR#	Logic 1
OP1#	Logic 1
OP2#	Logic 1
TXRDY#	Logic 0
RXRDY#	Logic 1
INT (Intel Mode) IRQA, IRQB, IRQC (PC Mode)	Logic 0 Three-State Condition

ABSOLUTE MAXIMUM RATINGS

Power Supply Range	7 Volts
Voltage at Any Pin	-0.5 to 7V
Operating Temperature	-40° to +85°C
Storage Temperature	-65° to +150°C
Package Dissipation	500 mW
Thermal Resistance (48-TQFP)	theta-ja = 59°C/W, theta-jc = 16°C/W
Thermal Resistance (44-PLCC)	theta-ja = 53°C/W, theta-jc = 21°C/W

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA=0° TO 70°C (-40° TO +85°C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.90V TO 5.5V

SYMBOL	PARAMETER	LIMITS 3.3V MIN	LIMITS 3.3V MAX	LIMITS 5.0V MIN	LIMITS 5.0V MAX	UNITS	CONDITION
V_{ILCK}	Clock Input Low Level	-0.3	0.6	-0.5	0.6	V	
V_{IHCK}	Clock Input High Level	2.4	VCC	3.0	VCC	V	
V_{IL}	Input Low Voltage	-0.3	0.8	-0.5	0.8	V	
V_{IH}	Input High Voltage (top mark date code of "GC YYWW" and older)	2.0	VCC	2.0	VCC	V	
V_{IH}	Input High Voltage (top mark date code of "HC YYWW" and newer)	2.0	5.5	2.0	5.5	V	
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 5 mA
V_{OL}	Output Low Voltage		0.4			V	I_{OL} = 4 mA
V_{OH}	Output High Voltage			2.4		V	I_{OH} = -5 mA
V_{OH}	Output High Voltage	2.0				V	**I_{OH} = -1 mA**
I_{IL}	Input Low Leakage Current		+/-10		+/-10	uA	
I_{IH}	Input High Leakage Current		+/-10		+/-10	uA	
C_{IN}	Input Pin Capacitance		5		5	pF	
I_{CC}	Power Supply Current		1.3		3.0	mA	
I_{SLEEP}	Sleep Current		30		100	uA	See Test1

Test 1: The following inputs should remain steady at VCC or GND state to minimize sleep current: A0-A2, D0-D7, IOR#, IOW#, CS# and modem inputs. Also, RX input must idle at logic 1 state while in sleep mode. In mixed voltage environments, where the voltage at any of the inputs of the 650A is lower than its VCC supply voltage, the sleep current will be higher than the maximum values given here.

AC ELECTRICAL CHARACTERISTICS

TA=0^{O} TO 70^{O}C (-40^{O} TO +85^{O}C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.90V TO 5.5V, 70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 3.3V MIN	LIMITS 3.3V MAX	LIMITS 5.0V MIN	LIMITS 5.0V MAX	UNIT
CLK	Clock Pulse Duration	30		20		ns
OSC	Crystal Frequency		20		24	MHz
OSC	External Clock Frequency		33		50	MHz
T_{AS}	Address Setup Time (AS# tied to GND)	5		5		ns
T_{AH}	Address Hold Time (AS# tied to GND) (top mark date code of "HC YYWW" and older)	10		10		ns
T_{AH}	Address Hold Time (AS# tied to GND) (top mark date code of "I2 YYWW" and newer)	0		0		ns
T_{CS}	Chip Select Width	50		40		ns
T_{RD}	IOR# Strobe Width	50		40		ns
T_{DY}	Read/Write Cycle Delay	40		30		ns
T_{RDV}	Data Access Time		40		30	ns
T_{DD}	Data Disable Time	0	15	0	10	ns
T_{WR}	IOW# Strobe Width	50		40		ns
T_{DS1}	Data Setup Time (AS# tied to GND)	20		10		ns
T_{DH1}	Data Hold Time (AS# tied to GND)	5		5		ns
T_{ASW}	Address Strobe Width	35		25		ns
T_{AS1}	Address Setup Time (AS# used)	5		5		ns
T_{AH1}	Address Hold Time (AS# used)	10		10		ns
T_{AS2}	Address Setup Time (AS# used)	5		5		ns
T_{AH2}	Address Hold Time (AS# used)	10		10		ns
T_{CS1}	Delay from Chip Select to AS#	5		5		ns
T_{CSH}	Delay from AS# to Chip Select	0		0		ns
T_{CS2}	Delay from AS# to Chip Select	5		5		ns
T_{RD1}	Delay from AS# to Read	10		10		ns
T_{RD2}	Delay from Chip Select to IOR#	10		10		ns
T_{DIS}	Delay from IOR# to DDIS#	15		10		ns
T_{WR1}	Delay from AS# to IOW#	10		10		ns

AC ELECTRICAL CHARACTERISTICS

TA=0° TO 70°C (-40° TO +85°C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.90V TO 5.5V, 70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 3.3V		LIMITS 5.0V		UNIT
		MIN	MAX	MIN	MAX	
T_{DS2}	Data Setup Time (AS# used)	20		10		ns
T_{DH2}	Data Hold Time (AS# used)	5		5		ns
T_{AS3}	Address Setup Time (PC Mode)	5		5		ns
T_{RD3}	Delay from AEN# to IOR#	10		10		ns
T_{RD4}	Delay from IOR# to AEN#	10		10		ns
T_{WR2}	Delay from AEN# to IOW#	10		10		ns
T_{WR3}	Delay from IOW# to AEN#	10		10		ns
T_{DS3}	Data Setup Time (PC Mode)	20		10		ns
T_{DH3}	Data Hold Time (PC Mode)	5		5		ns
T_{WDO}	Delay From IOW# To Output		50		40	ns
T_{MOD}	Delay To Set Interrupt From MODEM Input		40		35	ns
T_{RSI}	Delay To Reset Interrupt From IOR#		40		35	ns
T_{SSI}	Delay From Stop To Set Interrupt		1		1	Bclk
T_{RRI}	Delay From IOR# To Reset Interrupt		45		40	ns
T_{SI}	Delay From Stop To Interrupt		45		40	ns
T_{INT}	Delay From Initial INT Reset To Transmit Start	8	24	8	24	Bclk
T_{WRI}	Delay From IOW# To Reset Interrupt		45		40	ns
T_{SSR}	Delay From Stop To Set RXRDY#		1		1	Bclk
T_{RR}	Delay From IOR# To Reset RXRDY#		45		40	ns
T_{WT}	Delay From IOW# To Set TXRDY#		45		40	ns
T_{SRT}	Delay From Center of Start To Reset TXRDY#		8		8	Bclk
T_{RST}	Reset Pulse Width	40		40		ns
N	Baud Rate Divisor	1	2^{16}-1	1	2^{16}-1	-
Bclk	Baud Clock	16X of data rate				Hz

FIGURE 15. CLOCK TIMING

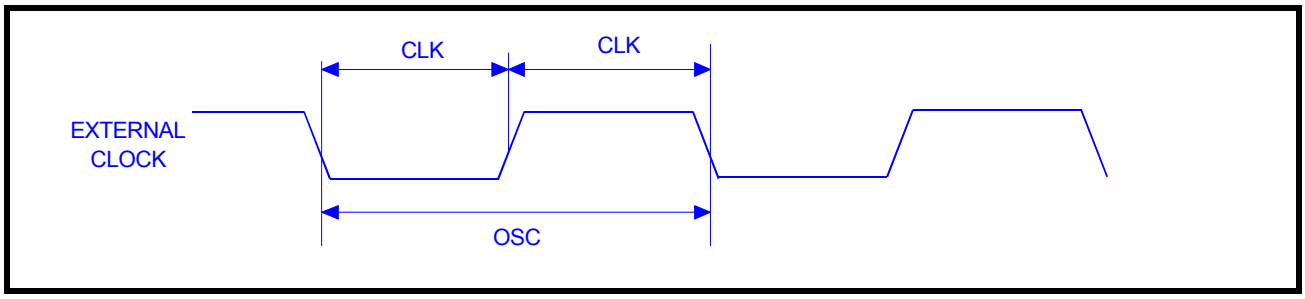


FIGURE 16. MODEM INPUT/OUTPUT TIMING

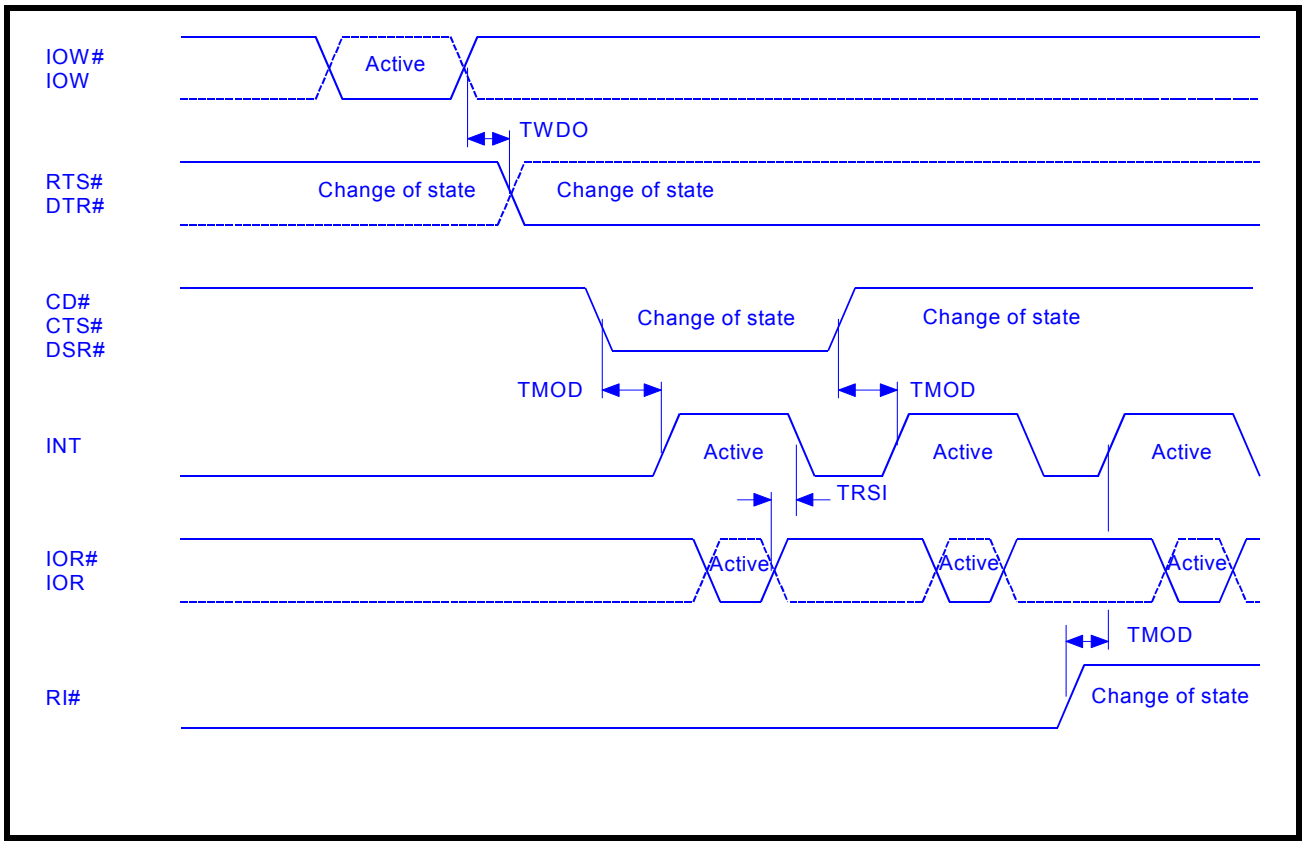
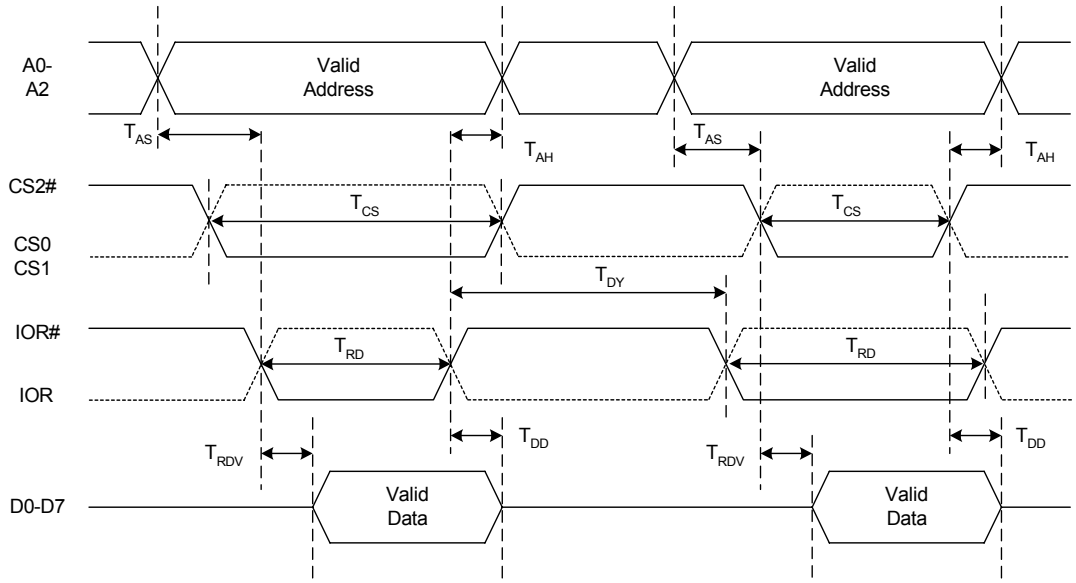
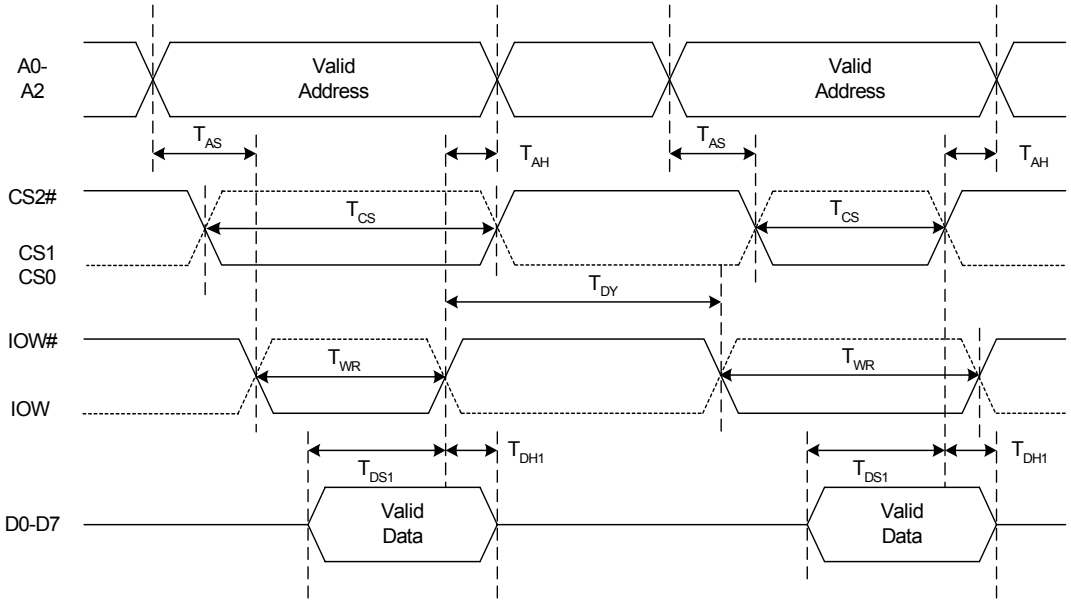


FIGURE 17. DATA BUS READ TIMING IN INTEL BUS MODE WITH AS# TIED TO GND



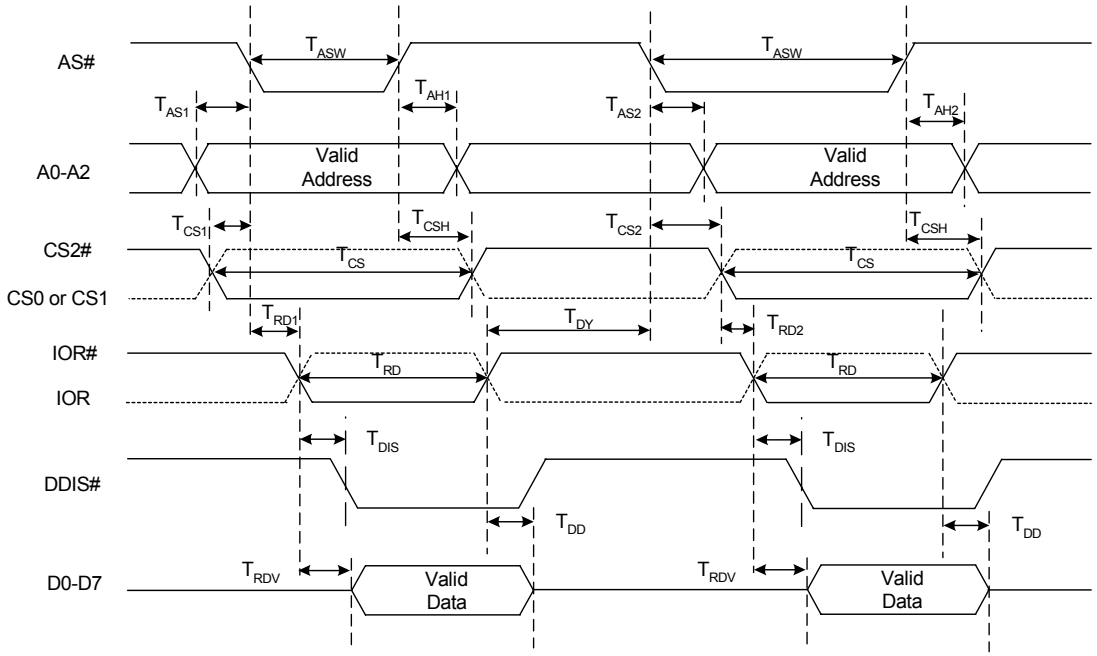
Note: Only one chipselect and one read strobe should be used.

FIGURE 18. DATA BUS WRITE TIMING IN INTEL BUS MODE WITH AS# TIED TO GND



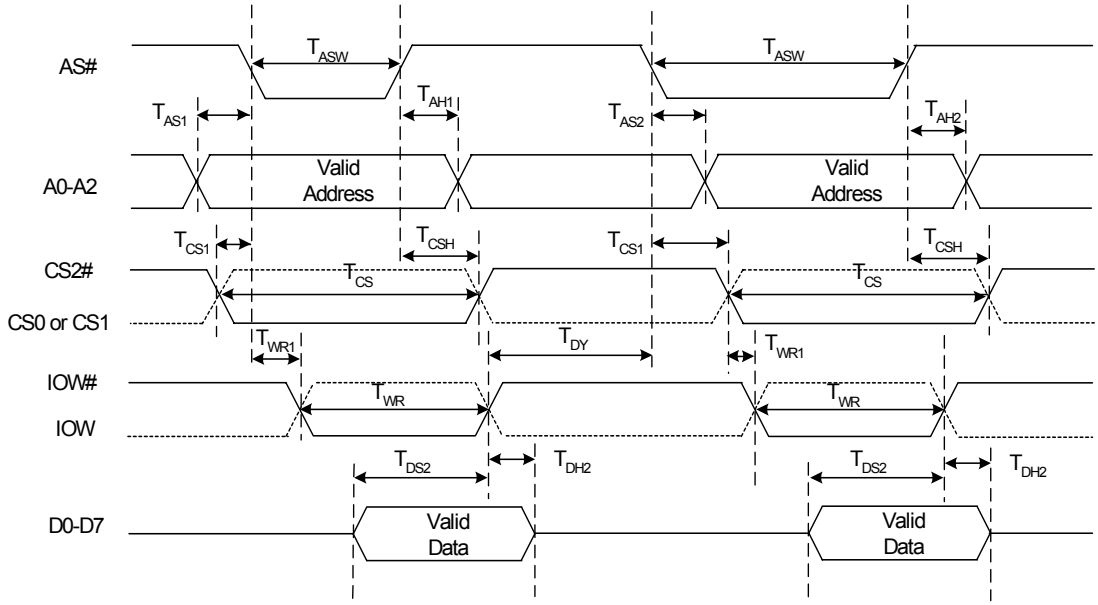
Note: Only one chipselect and one write strobe should be used.

FIGURE 19. DATA BUS READ TIMING IN INTEL BUS MODE USING AS#



Note: Only one chipselect and one read strobe should be used.

FIGURE 20. DATA BUS WRITE TIMING IN INTEL BUS MODE USING AS#



Note: Only one chipselect and one write strobe should be used.

FIGURE 21. DATA BUS READ TIMING IN PC MODE

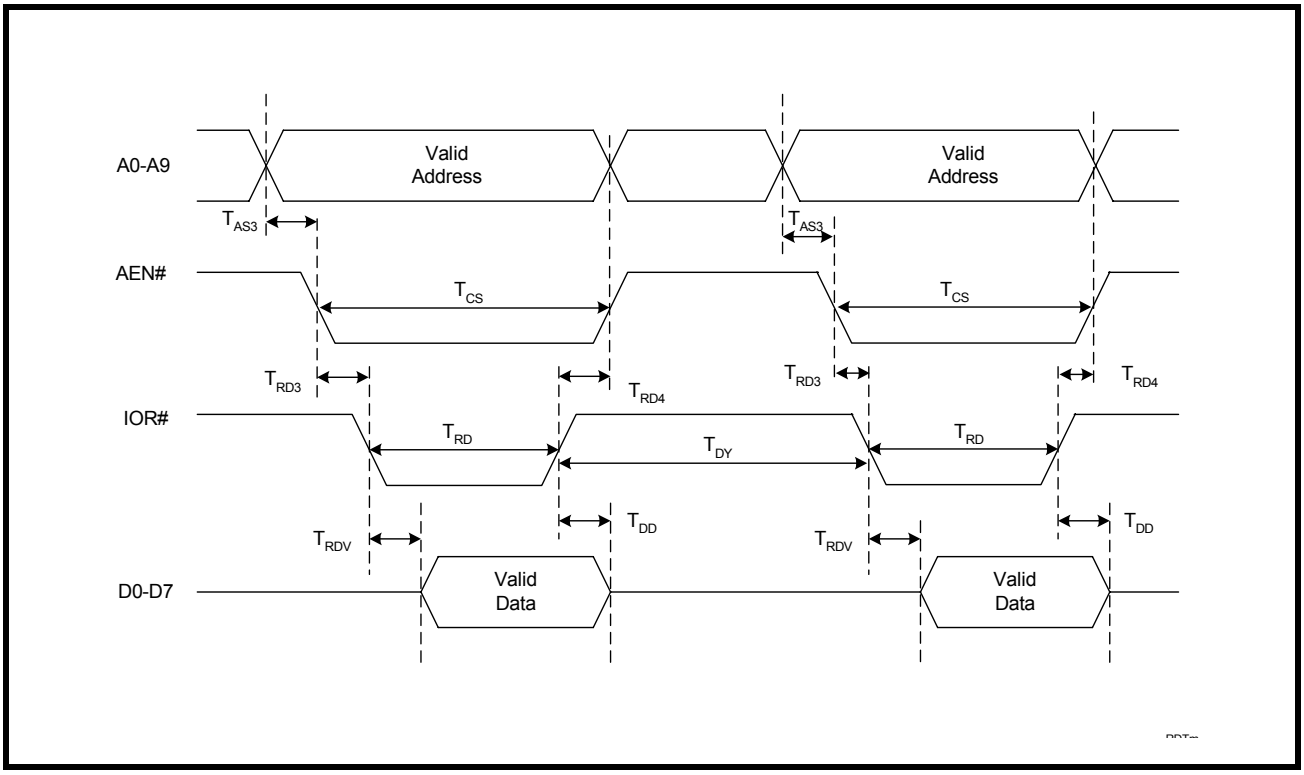


FIGURE 22. DATA BUS WRITE TIMING IN PC MODE

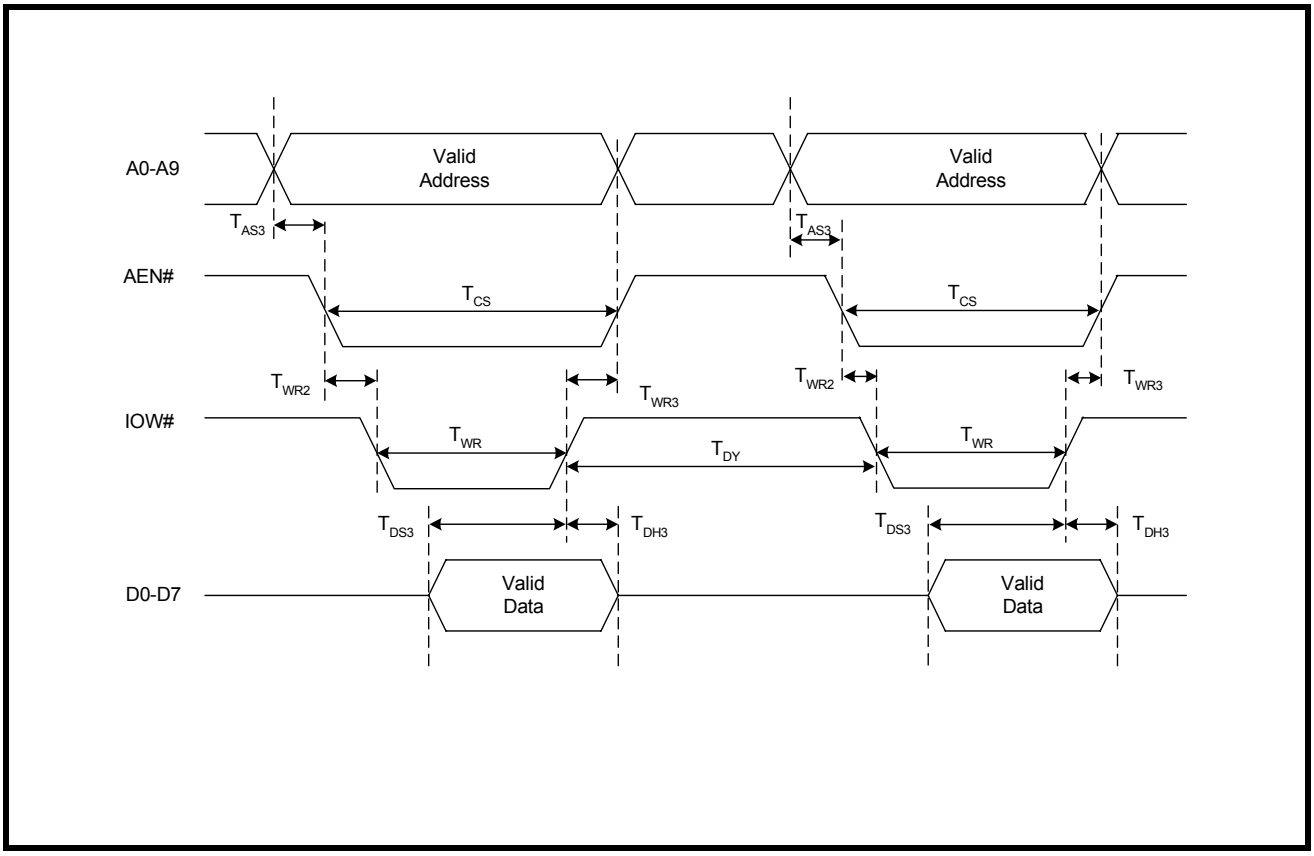


FIGURE 23. RECEIVE READY & INTERRUPT TIMING [NON-FIFO MODE]

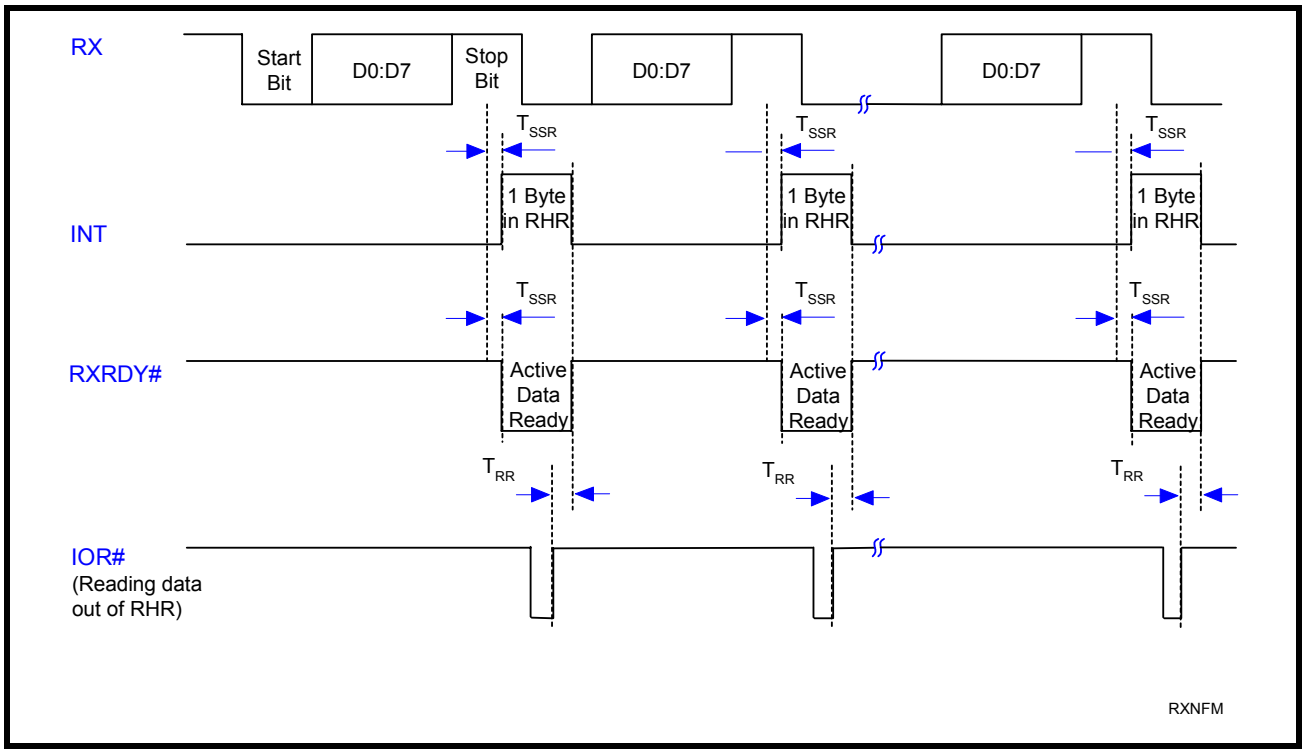


FIGURE 24. TRANSMIT READY & INTERRUPT TIMING [NON-FIFO MODE]

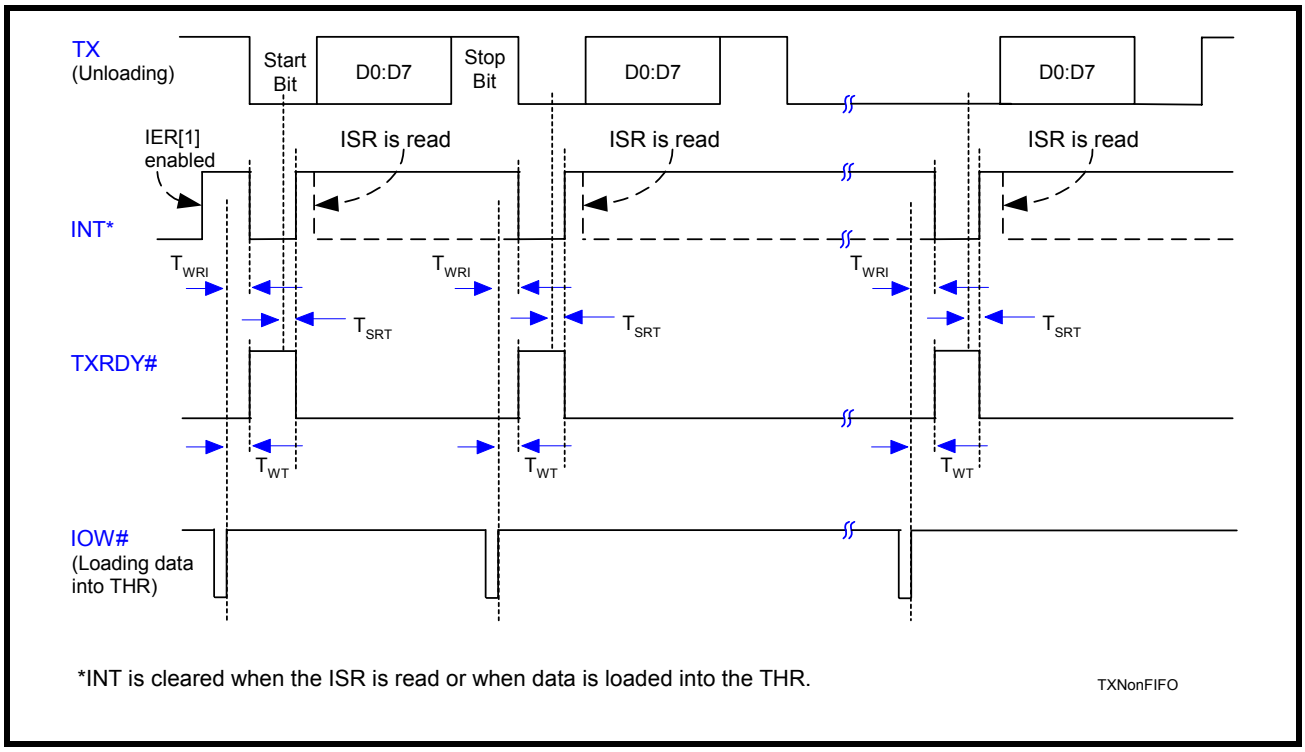


FIGURE 25. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA DISABLED]

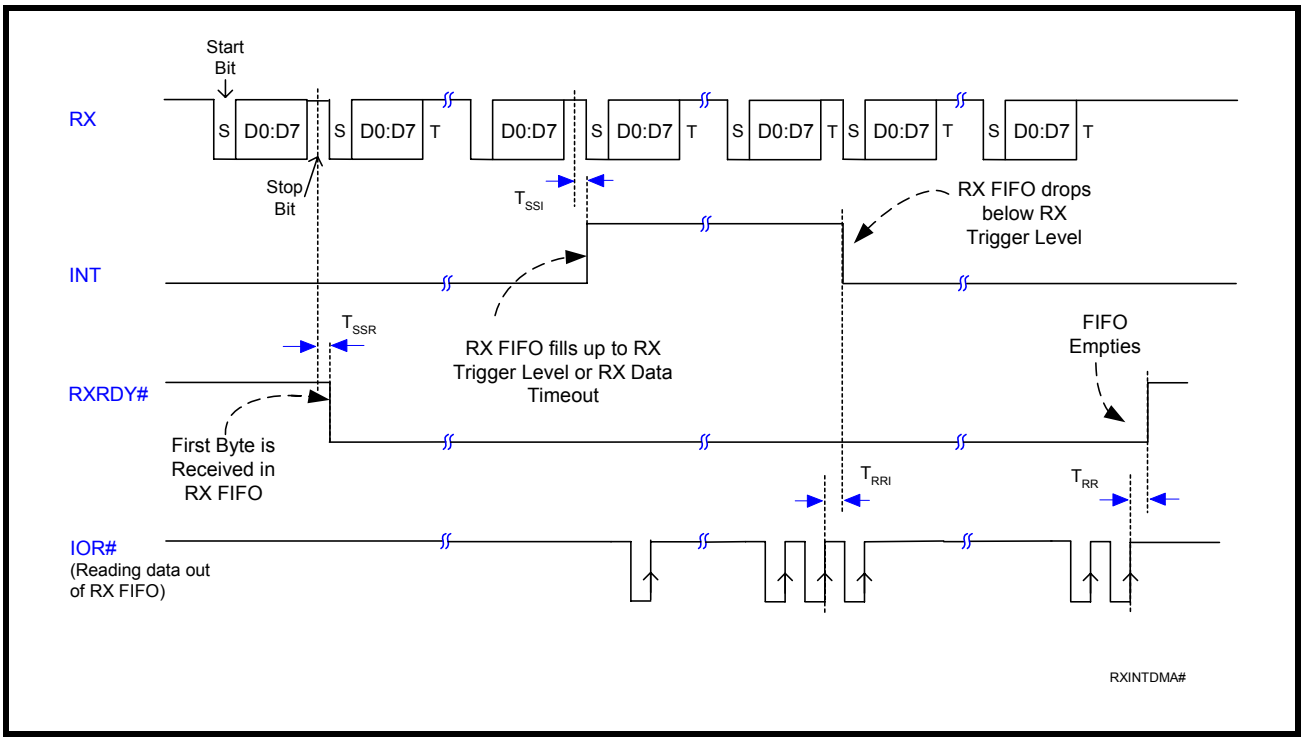


FIGURE 26. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA ENABLED]

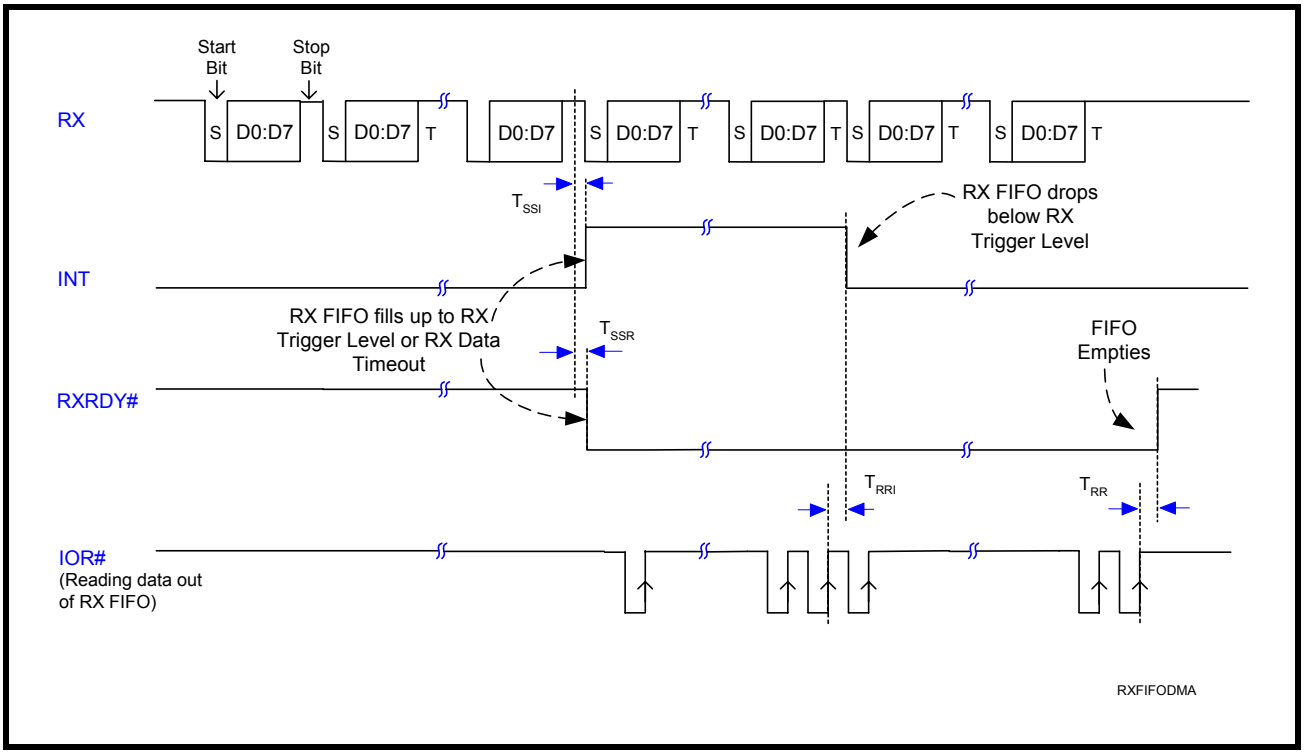


FIGURE 27. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE DISABLED]

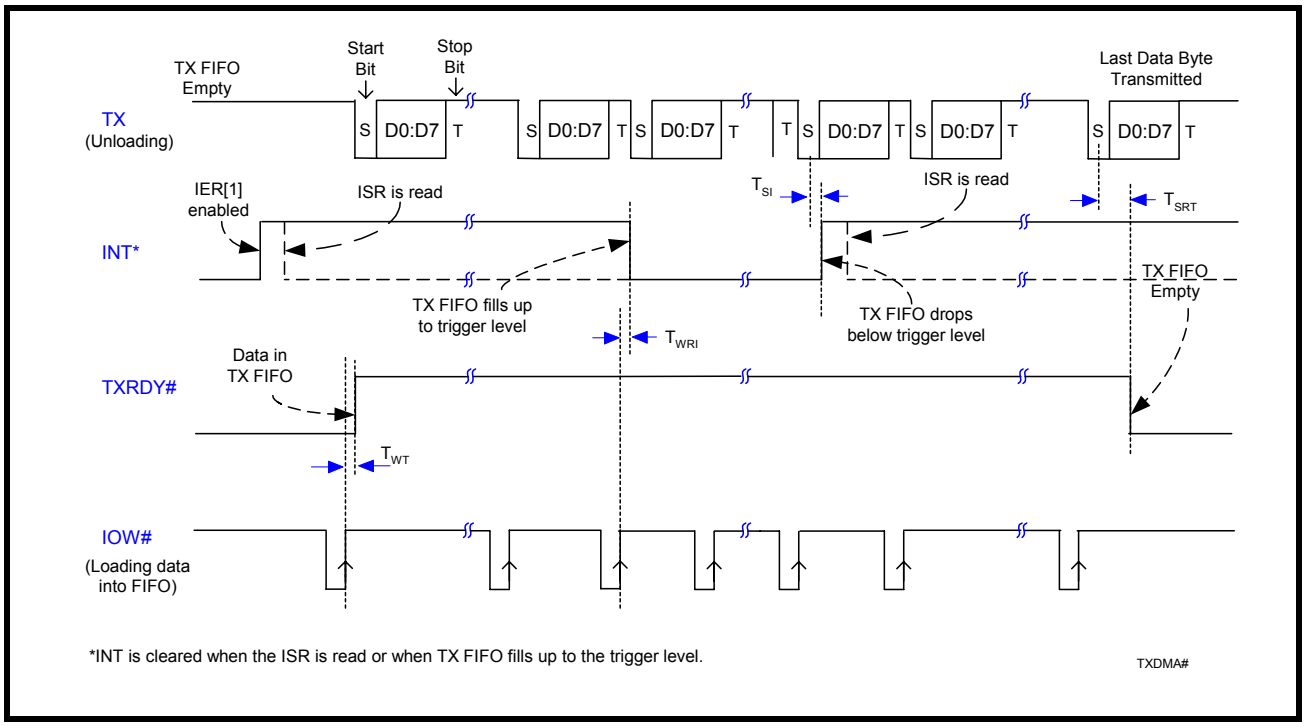
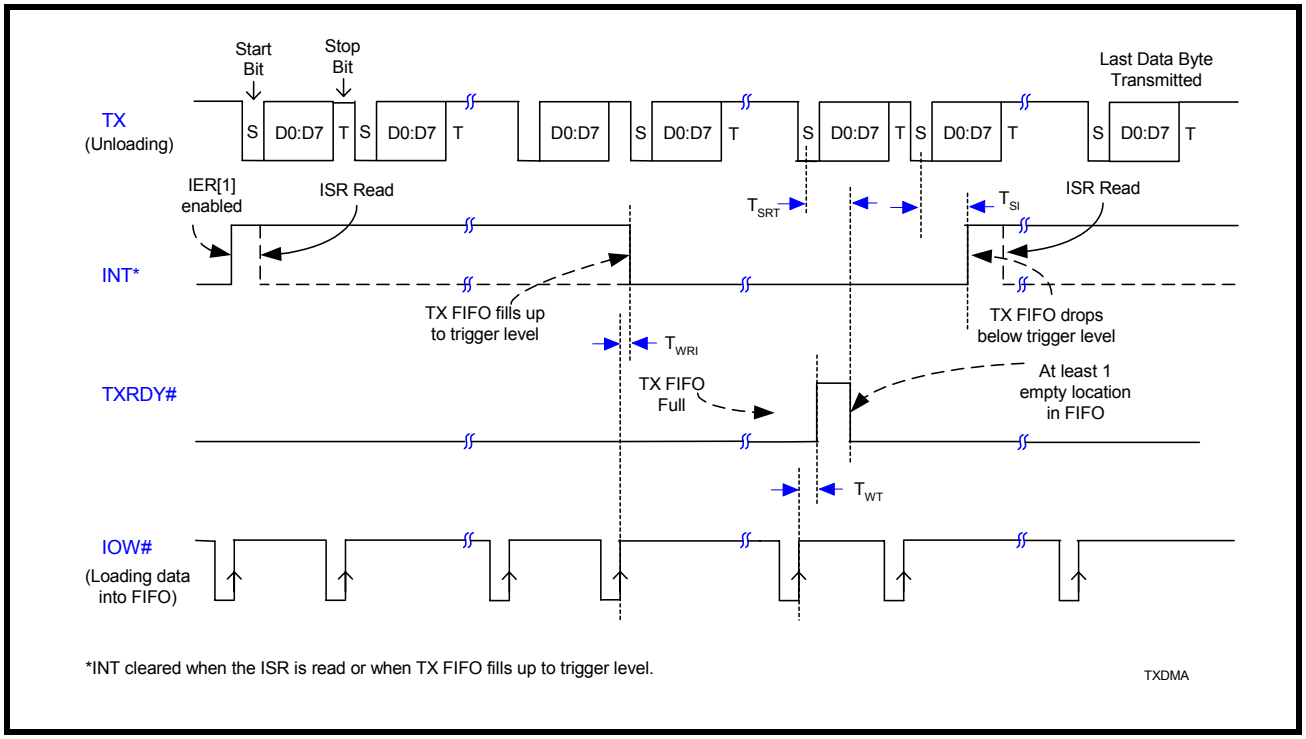
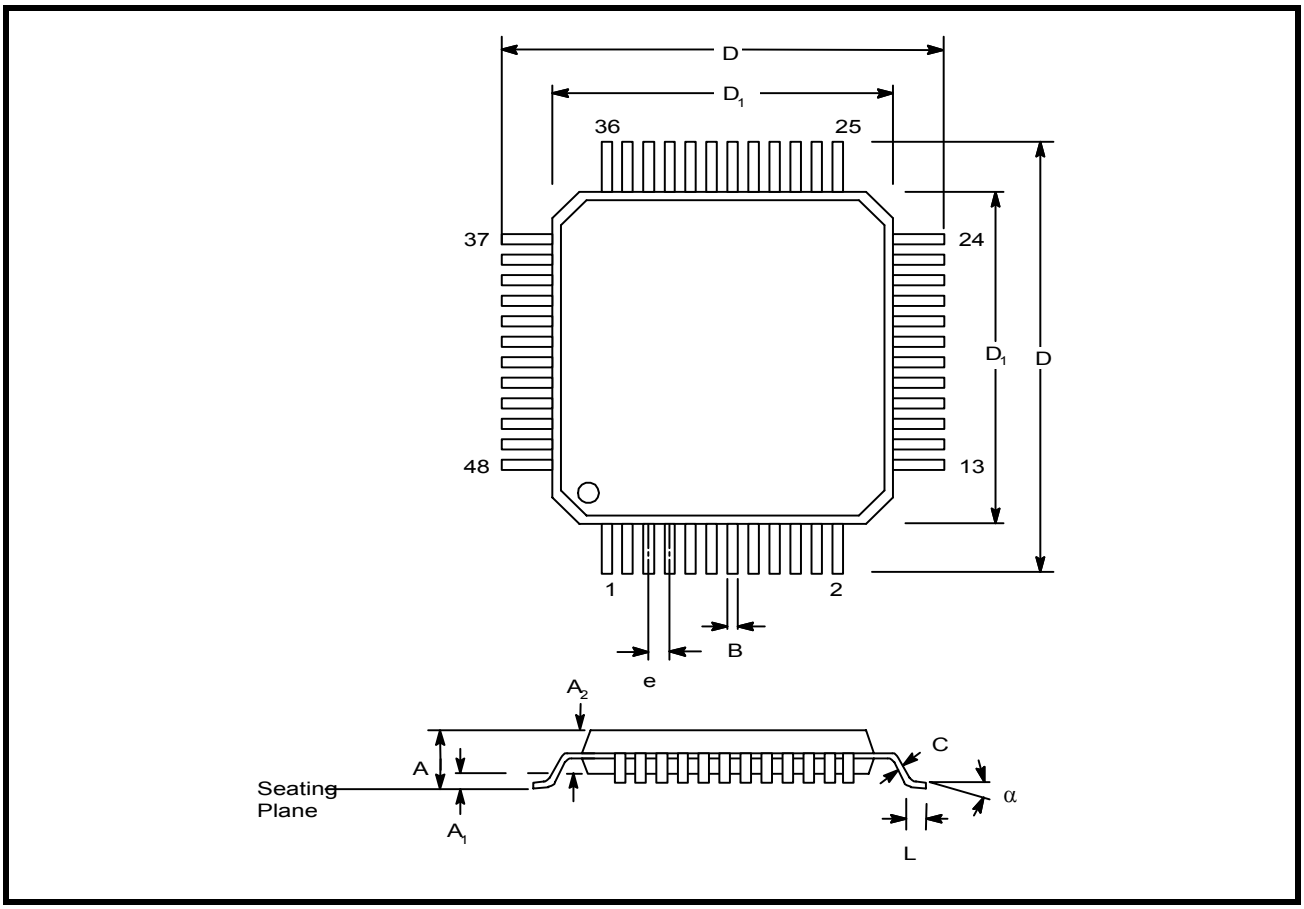


FIGURE 28. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE ENABLED]



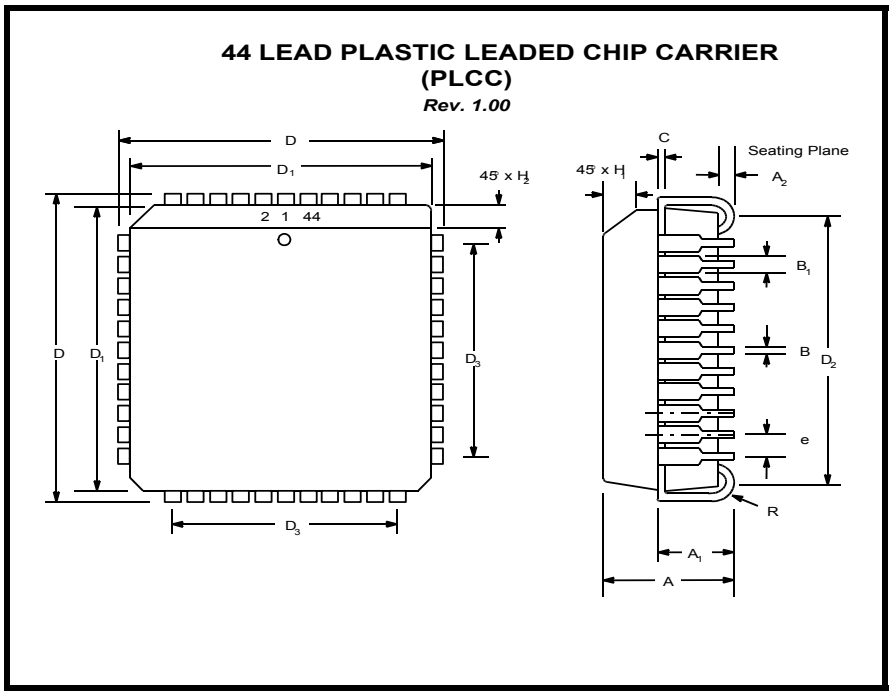
PACKAGE DIMENSIONS (48 PIN TQFP - 7 X 7 X 1 mm)



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.039	0.047	1.00	1.20
A_1	0.002	0.006	0.05	0.15
A_2	0.037	0.041	0.95	1.05
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

PACKAGE DIMENSIONS (44 PIN PLCC)



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.090	0.120	2.29	3.05
A_2	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.685	0.695	17.40	17.65
D_1	0.650	0.656	16.51	16.66
D_2	0.590	0.630	14.99	16.00
D_3	0.500 typ.		12.70 typ.	
e	0.050 BSC		1.27 BSC	
H_1	0.042	0.056	1.07	1.42
H_2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

REVISION HISTORY

DATE	REVISION	DESCRIPTION
January 2001	4.20	Updated information specific to Device Revision "FC" and newer: ■ 2.90V to 5.5V Operation with 5V tolerant inputs ■ 3.125 Mbps dta rate at 5V and 2 Mbps at 3.3V ■ Auto RS485 Half-duplex control output ■ Wireless Infrared (IrDA) encoder with programmable pulse width capability and decoder interface ■ Description of Device ID & Revision, IRPW and XFR registers
December 2001	4.30	Updated values in AC Electrical Characteristics Table.
January 2004	5.0.0	Changed to standard style format. Clarified timing diagrams. Added Device Status to Ordering Information. Devices with top mark date code of "I2 YYWW" and newer have 0 ns address hold time. Devices with top mark date code of "HC YYWW" and older do not have this feature.
August 2005	5.0.1	Removed discontinued 40-pin PDIP from Ordering Information.
June 2009	5.0.2	Corrected table 1.
June 2010	5.0.3	Corrected pin 13 name of TQFP-48 package Intel mode in **Figure 2**.

Datasheet June 2010.

Send your UART technical inquiry with technical details to hotline: uarttechsupport@exar.com.

AMEYA360
Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com