AS62V256A-70SIN

Low Voltage 32K x 8 SRAM

Features

- 32768 x 8 bit static CMOS RAM
- 70 ns Access Time
- Common data inputs and data outputs
- Three-state outputs
- Typ. operating supply current
  70ns: 30 mA
- Standby current < 40 µA at 125 °C
- TTL/CMOS-compatible
- Power supply voltage 2.5 - 3.6 V
- Operating temperature range
  -40 °C to 85 °C
- ESD protection > 2000 V
  (MIL STD 883C M3015.7)
- Latch-up immunity >100 mA
- Package: SOP28 (300/330 mil)

Description

The AS62V256A-70SIN is a static RAM manufactured using a CMOS pro-cess technology with the following operating modes:

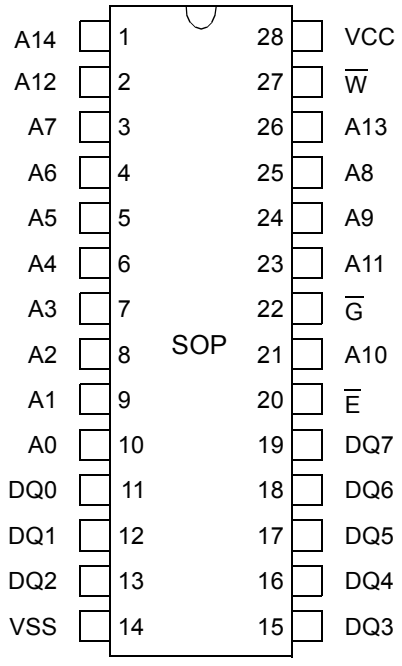
- Read - Standby
- Write - Data Retention

The memory array is based on a 6-Transistor cell.

The circuit is activated by the falling edge of $\overline{E}$. The address and control inputs open simultaneously. According to the information of $\overline{W}$ and $\overline{G}$, the data inputs, or outputs, are active. In a Read cycle, the data outputs are activated by the falling edge of $\overline{G}$, afterwards the data word will be available at the outputs DQ0-DQ7. After the address change, the data outputs go High-Z until the new information is available. The data outputs have no preferred state. The Read cycle is finished by the falling edge of $\overline{W}$, or by the rising edge of $\overline{E}$, respectively.

Data retention is guaranteed down to 2 V. With the exception of $\overline{E}$, all inputs consist of NOR gates, so that no pull-up/pull-down resistors are required.

Pin Configuration

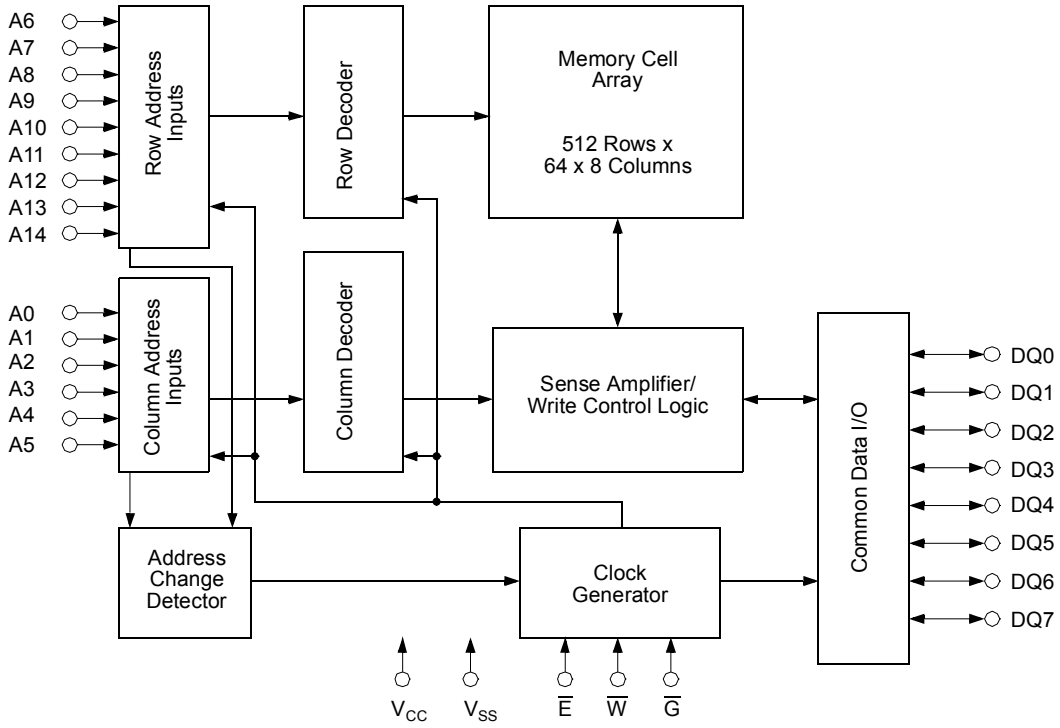


Top View

Pin Description

Signal Name	Signal Description
A0 - A14	Address Inputs
DQ0 - DQ7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
VCC	Power Supply Voltage
VSS	Ground

Block Diagram



Truth Table

Operating Mode	$\overline{E}$	$\overline{W}$	$\overline{G}$	DQ0 - DQ7
Standby/not selected	H	*	*	High-Z
Internal Read	L	H	H	High-Z
Read	L	H	L	Data Outputs Low-Z
Write	L	L	*	Data Inputs High-Z

* H or L

Characteristics

All voltages are referenced to V_{SS} = 0 V (ground).
All characteristics are valid in the power supply voltage range and in the operating temperature range specified.
Dynamic measurements are based on a rise and fall time of ≤ 5 ns, measured between 10 % and 90 % of V_I, as well as input levels of V_{IL} = 0.2 V and V_{IH} = 2.8 V. The timing reference level of all input and output signals is 1.5 V, with the exception of the t_{dis}-times and t_{en}-times, in which cases transition is measured ±200 mV from steady-state voltage.

Absolute Maximum Ratings [a]	Symbol	Min.	Max.	Unit
Power Supply Voltage	V_{CC}	-0.3	4.6	V
Input Voltage	V_I	-0.5	V_{CC} + 0.5 [b]	V
Output Voltage	V_O	-0.5	V_{CC} + 0.5 [b]	V
Power Dissipation	P_D	-	1	W
Operating Temperature	T_a	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C
Output Short-Circuit Current at V_{CC} = 3.3 V and V_O = 0 V [c]	$\lvert I_{OS} \rvert$		100	mA

[a] Stresses greater than those listed under „Absolute Maximum Ratings“ may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
[b] Maximum voltage is 4.6 V
[c] Not more than 1 output should be shorted at the same time. Duration of the short circuit should not exceed 30 s.

Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	V_{CC}		2.5	3.6	V
Input Low Voltage [d]	V_{IL}		-0.3	0.5	V
Input High Voltage	V_{IH}		2.0	V_{CC} + 0.3	V

[d] -2 V at Pulse Width 30 ns

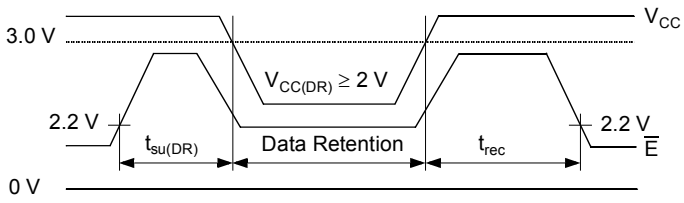
Electrical Characteristics	Symbol	Conditions	Min.	Max.	Unit
Supply Current - Operating Mode	$I_{CC(OP)}$	V_{CC} = 3.6 V V_{IL} = 0.5 V V_{IH} = 2.0 V t_{cW} = 70 ns t_{cW} = 70 ns		 90 70	 mA mA
Supply Current - Standby Mode (CMOS level)	$I_{CC(SB)}$	V_{CC} = 3.6 V $V_{\overline{E}}$ = V_{CC} - 0.2 V I-Type		 10	 µA
Supply Current - Standby Mode (TTL level)	$I_{CC(SB)1}$	V_{CC} = 3.6 V $V_{\overline{E}}$ = 2.0 V I-Type		 10	 mA
Output High Voltage	V_{OH}	V_{CC} = 2.5 V I_{OH} = -1.0 mA	2.2		V
Output Low Voltage	V_{OL}	V_{CC} = 2.5 V I_{OL} = 2.1 mA		0.4	V
Input High Leakage Current	I_{IH}	V_{CC} = 3.6 V V_{IH} = 3.6 V		2	µA
Input Low Leakage Current	I_{IL}	V_{CC} = 3.6 V V_{IL} = 0 V	-2		µA
Output High Current	I_{OH}	V_{CC} = 2.5 V V_{OH} = 2.2 V		-1.0	mA
Output Low Current	I_{OL}	V_{CC} = 2.5 V V_{OL} = 0.4 V	2.1		mA
Output Leakage Current High at Three-State Outputs	I_{OHZ}	V_{CC} = 3.6 V V_{OH} = 3.6 V		2	µA
Low at Three-State Outputs	I_{OLZ}	V_{CC} = 3.6 V V_{OL} = 0 V	-2		µA

Switching Characteristics Read Cycle	Symbol		70		Unit
	Alt.	IEC	Min.	Max.	
Read Cycle Time	t_{RC}	t_{cR}	70		ns
Address Access Time to Data Valid	t_{AA}	$t_{a(A)}$		70	ns
Chip Enable Access Time to Data Valid	t_{ACE}	$t_{a(E)}$		70	ns
$\overline{G}$ LOW to Data Valid	t_{OE}	$t_{a(G)}$		25	ns
$\overline{E}$ HIGH to Output in High-Z	t_{HZCE}	$t_{dis(E)}$		15	ns
$\overline{G}$ HIGH to Output in High-Z	t_{HZOE}	$t_{dis(G)}$		15	ns
$\overline{E}$ LOW to Output in Low-Z	t_{LZCE}	$t_{en(E)}$	3		ns
$\overline{G}$ LOW to Output in Low-Z	t_{LZOE}	$t_{en(G)}$	0		ns
Output Hold Time from Address Change	t_{OH}	$t_{v(A)}$	3		ns
$\overline{E}$ LOW to Power-Up Time	t_{PU}		0		ns
$\overline{E}$ HIGH to Power-Down Time	t_{PD}			70	ns

Switching Characteristics Write Cycle	Symbol		70		Unit
	Alt.	IEC	Min.	Max.	
Write Cycle Time	t_{WC}	t_{cW}	70		ns
Write Pulse Width	t_{WP}	$t_{w(W)}$	35		ns
Write Setup Time	t_{WP}	$t_{su(W)}$	35		ns
Address Setup Time	t_{AS}	$t_{su(A)}$	0		ns
Address Valid to End of Write	t_{AW}	$t_{su(A-WH)}$	40		ns
Chip Enable Setup Time	t_{CW}	$t_{su(E)}$	40		ns
Pulse Width Chip Enable to End of Write	t_{CW}	$t_{w(E)}$	40		ns
Data Setup Time	t_{DS}	$t_{su(D)}$	25		ns
Data Hold Time	t_{DH}	$t_{h(D)}$	0		ns
Address Hold from End of Write	t_{AH}	$t_{h(A)}$	0		ns
$\overline{W}$ LOW to Output in High-Z	t_{HZWE}	$t_{dis(W)}$		20	ns
$\overline{G}$ HIGH to Output in High-Z	t_{HZOE}	$t_{dis(G)}$		15	ns
$\overline{W}$ HIGH to Output in Low-Z	t_{LZWE}	$t_{en(W)}$	0		ns
$\overline{G}$ LOW to Output in Low-Z	t_{LZOE}	$t_{en(G)}$	0		ns

Data Retention Mode

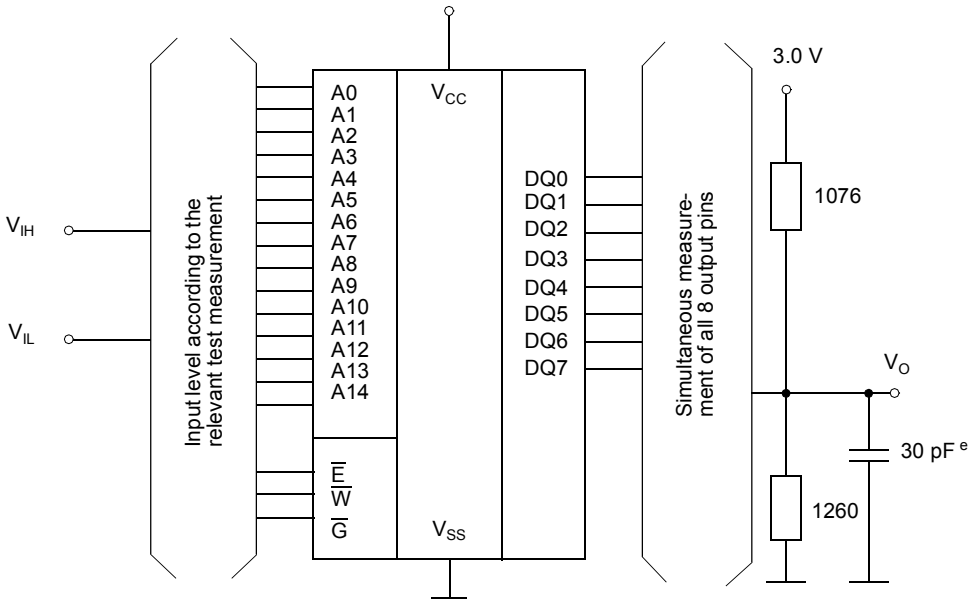
$\overline{E}$ - controlled



$V_{CC(DR)} - 0.2\ V \leq V_{\overline{E}(DR)} \leq V_{CC(DR)} + 0.3\ V$

Data Retention Characteristics	Symbol		Conditions	Min.	Typ.	Max.	Unit
	Alt.	IEC					
Data Retention Supply Voltage		$V_{CC(DR)}$		2			V
Data Retention Supply Current		$I_{CC(DR)}$	$V_{CC(DR)}$ = 2V $V_{\overline{E}}$ = $V_{CC(DR)}$ - 0.2 V			5 20	µA µA
Data Retention Setup Time	t_{CDR}	$t_{su(DR)}$	See Data Retention Waveforms (above)	0			ns
Operating Recovery Time	t_R	t_{rec}		t_{cR}			ns

Test Configuration for Functional Check



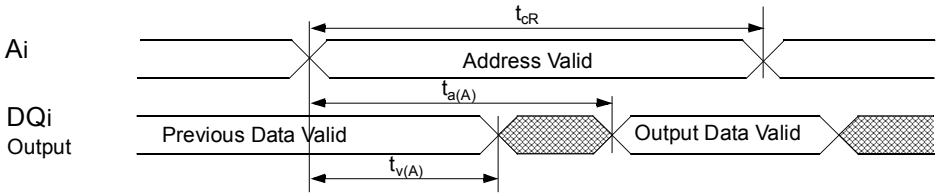
[e] In measurement of $t_{dis(E)}$,$t_{dis(W)}$, $t_{en(E)}$, $t_{en(W)}$, $t_{en(G)}$ the capacitance is 5 pF.

Capacitance	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	V_{CC} = 3.3V V_I = V_{SS} t = 1 MHz T_a = 25 °C	C_I		7	pF
Output Capacitance		C_o		7	pF

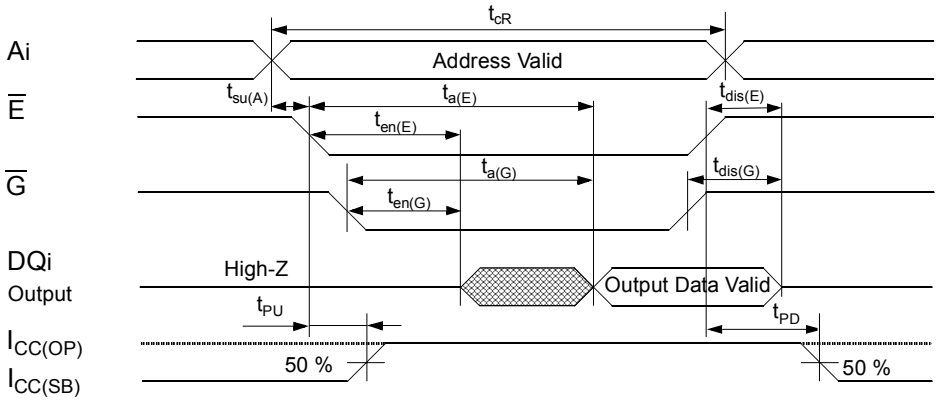
All pins not under test must be connected with ground by capacitors.

Alliance	Organization	VCC Range	Package	Operating Temp	Speed ns
AS62V256A-70SIN	32K x 8	2.7V – 3.6V	SOP28 (330 mil)	Industrial ~ -40°C - 85°C	70

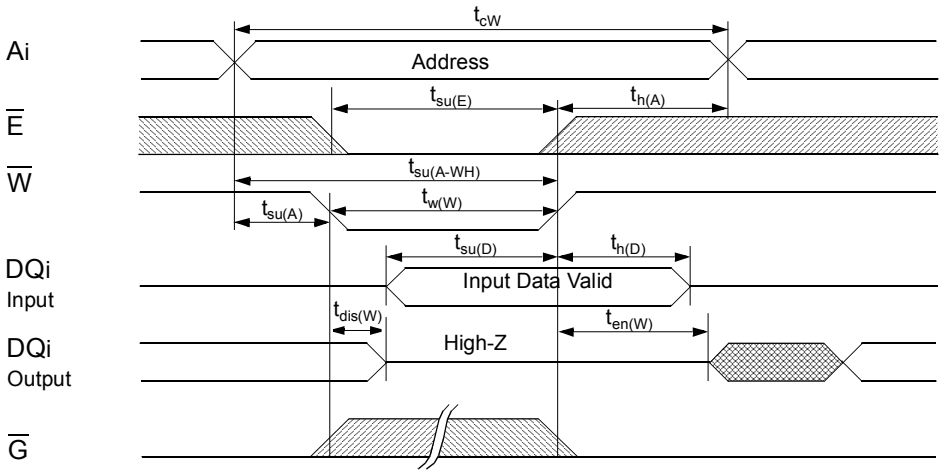
Read Cycle 1: A_i-controlled (during Read Cycle : $\overline{E}$ = $\overline{G}$ = V_{IL}, $\overline{W}$ = V_{IH})



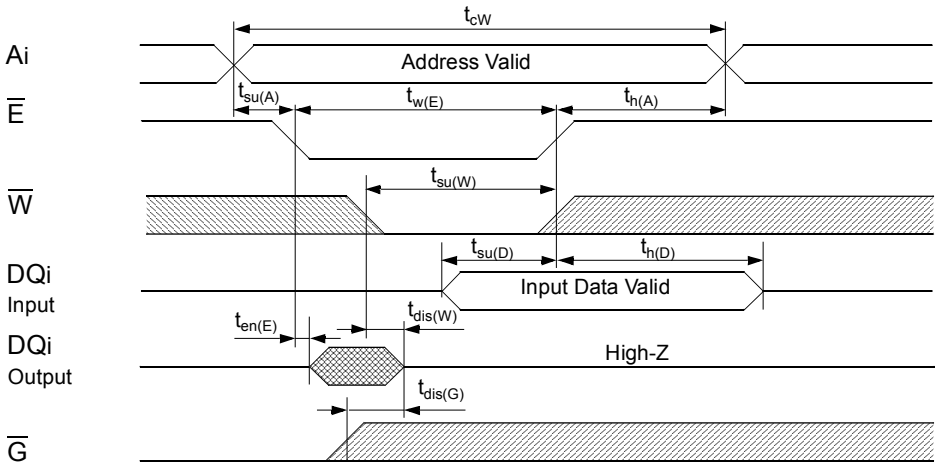
Read Cycle 2: $\overline{G}$-, $\overline{E}$-controlled (during Read Cycle: $\overline{W}$ = V_{IH})

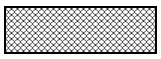


Write Cycle1: $\overline{W}$-controlled



Write Cycle 2: $\overline{E}$-controlled



undefined  L- to H-level  H- to L-level 

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