# Quad, 16-/12-Bit nanoDAC+ with I²C Interface

Data Sheet

# AD5696/AD5694

## FEATURES

**High relative accuracy (INL): ±2 LSB maximum at 16 bits**
**Tiny package: 3 mm × 3 mm, 16-lead LFCSP**
**Total unadjusted error (TUE): ±0.1% of FSR maximum**

**Offset error: ±1.5 mV maximum**
**Gain error: ±0.1% of FSR maximum**
**High drive capability: 20 mA, 0.5 V from supply rails**
**User-selectable gain of 1 or 2 (GAIN pin)**
**Reset to zero scale or midscale (RSTSEL pin)**
**1.8 V logic compatibility**
**400 kHz I²C-compatible serial interface**
**4 I²C addresses available**
**Low glitch: 0.5 nV-sec**
**Robust 3.5 kV HBM and 1.5 kV FICDM ESD rating**
**Low power: 1.8 mW at 3 V**
**2.7 V to 5.5 V power supply**
**−40°C to +105°C temperature range**

## APPLICATIONS

**Digital gain and offset adjustment**
**Programmable attenuators**
**Process control (PLC I/O cards)**
**Industrial automation**
**Data acquisition systems**

## GENERAL DESCRIPTION

The AD5696 and AD5694, members of the *nano*DAC+™ family, are low power, quad, 16-/12-bit buffered voltage output DACs. The devices include a gain select pin giving a full-scale output of 2.5 V (gain = 1) or 5 V (gain = 2). The devices operate from a single 2.7 V to 5.5 V supply, are guaranteed monotonic by design, and exhibit less than 0.1% FSR gain error and 1.5 mV offset error performance. The devices are available in a 3 mm × 3 mm LFCSP package and in a TSSOP package.

The AD5696/AD5694 incorporate a power-on reset circuit and a RSTSEL pin; the RSTSEL pin ensures that the DAC outputs power up to zero scale or midscale and remain at that level until a valid write takes place. The parts contain a per-channel power-down feature that reduces the current consumption of the device in power-down mode to 4 µA at 3 V.

The AD5696/AD5694 use a versatile 2-wire serial interface that operates at clock rates up to 400 kHz and include a $V_{LOGIC}$ pin intended for 1.8 V/3 V/5 V logic.

## FUNCTIONAL BLOCK DIAGRAM

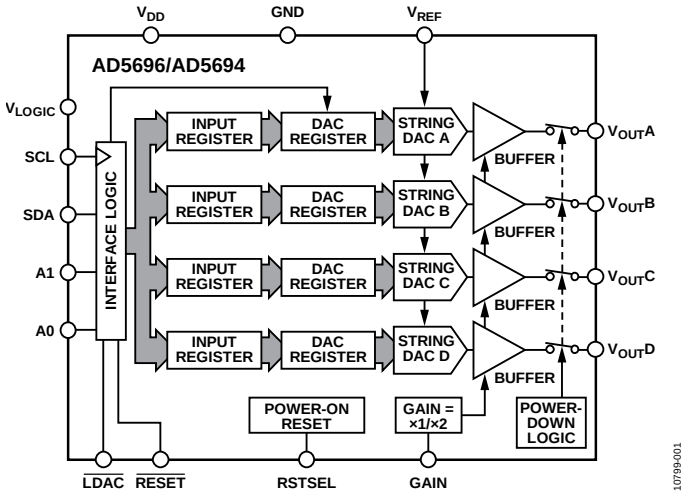



*Figure 1.*

**Table 1. Quad *nano*DAC+ Devices**

| Interface | Reference | 16-Bit | 14-Bit | 12-Bit |
|---|---|---|---|---|
| SPI | Internal | AD5686R | AD5685R | AD5684R |
| | External | AD5686 | | AD5684 |
| I²C | Internal | AD5696R | AD5695R | AD5694R |
| | External | AD5696 | | AD5694 |

## PRODUCT HIGHLIGHTS

1. High Relative Accuracy (INL).
   AD5696 (16-bit): ±2 LSB maximum
   AD5694 (12-bit): ±1 LSB maximum
2. Excellent DC Performance.
   Total unadjusted error: ±0.1% of FSR maximum
   Offset error: ±1.5 mV maximum
   Gain error: ±0.1% of FSR maximum
3. Two Package Options.
   3 mm × 3 mm, 16-lead LFCSP
   16-lead TSSOP

**Rev. A** Document Feedback


One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 
Technical Support www.analog.com

# TABLE OF CONTENTS



## REVISION HISTORY

**6/13—Rev. 0 to Rev. A**

Changes to Pin GAIN and Pin RSTSEL Descriptions; Table 7 ... 8

**7/12—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{DD}$ = 2.7 V to 5.5 V; $V_{REF}$ = 2.5 V; 1.8 V ≤ $V_{LOGIC}$ ≤ 5.5 V; $R_L$ = 2 kΩ; $C_L$ = 200 pF; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 2.**

| Parameter | A Grade | | | B Grade | | | Unit | Test Conditions/Comments[1] |
|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | | |
| STATIC PERFORMANCE[2] | | | | | | | | |
| AD5696 | | | | | | | | |
| Resolution | 16 | | | 16 | | | Bits | |
| Relative Accuracy | | ±2 | ±8 | | ±1 | ±2 | LSB | Gain = 2 |
| | | ±2 | ±8 | | ±1 | ±3 | LSB | Gain = 1 |
| Differential Nonlinearity | | | ±1 | | | ±1 | LSB | Guaranteed monotonic by design |
| AD5694 | | | | | | | | |
| Resolution | 12 | | | 12 | | | Bits | |
| Relative Accuracy | | ±0.12 | ±2 | | ±0.12 | ±1 | LSB | |
| Differential Nonlinearity | | | ±1 | | | ±1 | LSB | Guaranteed monotonic by design |
| Zero-Code Error | | 0.4 | 4 | | 0.4 | 1.5 | mV | All 0s loaded to DAC register |
| Offset Error | | +0.1 | ±4 | | +0.1 | ±1.5 | mV | |
| Full-Scale Error | | +0.01 | ±0.2 | | +0.01 | ±0.1 | % of FSR | All 1s loaded to DAC register |
| Gain Error | | ±0.02 | ±0.2 | | ±0.02 | ±0.1 | % of FSR | |
| Total Unadjusted Error | | ±0.01 | ±0.25 | | ±0.01 | ±0.1 | % of FSR | Gain = 2 |
| | | | ±0.25 | | | ±0.2 | % of FSR | Gain = 1 |
| Offset Error Drift[3] | | ±1 | | | ±1 | | µV/°C | |
| Gain Temperature Coefficient[3] | | ±1 | | | ±1 | | ppm | Of FSR/°C |
| DC Power Supply Rejection Ratio[3] | | 0.15 | | | 0.15 | | mV/V | DAC code = midscale; $V_{DD}$ = 5 V ± 10% |
| DC Crosstalk[3] | | ±2 | | | ±2 | | µV | Due to single channel, full-scale output change |
| | | ±3 | | | ±3 | | µV/mA | Due to load current change |
| | | ±2 | | | ±2 | | µV | Due to power-down (per channel) |
| OUTPUT CHARACTERISTICS[3] | | | | | | | | |
| Output Voltage Range | 0 | | $V_{REF}$ | 0 | | $V_{REF}$ | V | Gain = 1 |
| | 0 | | 2 × $V_{REF}$ | 0 | | 2 × $V_{REF}$ | V | Gain = 2 (see Figure 20) |
| Capacitive Load Stability | | 2 | | | 2 | | nF | $R_L$ = ∞ |
| | | 10 | | | 10 | | nF | $R_L$ = 1 kΩ |
| Resistive Load[4] | 1 | | | 1 | | | kΩ | |
| Load Regulation | | | | | | | | DAC code = midscale |
| | | 80 | | | 80 | | µV/mA | 5 V ± 10%; −30 mA ≤ $I_{OUT}$ ≤ +30 mA |
| | | 80 | | | 80 | | µV/mA | 3 V ± 10%; −20 mA ≤ $I_{OUT}$ ≤ +20 mA |
| Short-Circuit Current[5] | | 40 | | | 40 | | mA | |
| Load Impedance at Rails[6] | | 25 | | | 25 | | Ω | See Figure 20 |
| Power-Up Time | | 2.5 | | | 2.5 | | µs | Coming out of power-down mode; $V_{DD}$ = 5 V |
| REFERENCE INPUT | | | | | | | | |
| Reference Current | | 90 | | | 90 | | µA | $V_{REF}$ = $V_{DD}$ = 5.5 V, gain = 1 |
| | | 180 | | | 180 | | µA | $V_{REF}$ = $V_{DD}$ = 5.5 V, gain = 2 |
| Reference Input Range | 1 | | $V_{DD}$ | 1 | | $V_{DD}$ | V | Gain = 1 |
| | 1 | | $V_{DD}$/2 | 1 | | $V_{DD}$/2 | V | Gain = 2 |
| Reference Input Impedance | | 16 | | | 16 | | kΩ | Gain = 2 |
| | | 32 | | | 32 | | kΩ | Gain = 1 |

| Parameter | A Grade | | | B Grade | | | Unit | Test Conditions/Comments[1] |
|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | | |
| LOGIC INPUTS[3] | | | | | | | | |
| Input Current | | | ±2 | | | ±2 | μA | Per pin |
| Input Low Voltage, $V_{INL}$ | | | $0.3 \times V_{LOGIC}$ | | | $0.3 \times V_{LOGIC}$ | V | |
| Input High Voltage, $V_{INH}$ | $0.7 \times V_{LOGIC}$ | | | $0.7 \times V_{LOGIC}$ | | | V | |
| Pin Capacitance | | 2 | | | 2 | | pF | |
| LOGIC OUTPUTS (SDA)[3] | | | | | | | | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | | | 0.4 | V | $I_{SINK}$ = 3 mA |
| Output High Voltage, $V_{OH}$ | $V_{LOGIC} - 0.4$ | | | $V_{LOGIC} - 0.4$ | | | V | $I_{SOURCE}$ = 3 mA |
| Floating State Output Capacitance | | 4 | | | 4 | | pF | |
| POWER REQUIREMENTS | | | | | | | | |
| $V_{LOGIC}$ | 1.8 | | 5.5 | 1.8 | | 5.5 | V | |
| $I_{LOGIC}$ | | | 3 | | | 3 | μA | |
| $V_{DD}$ | 2.7 | | 5.5 | 2.7 | | 5.5 | V | Gain = 1 |
| | $V_{REF} + 1.5$ | | 5.5 | $V_{REF} + 1.5$ | | 5.5 | V | Gain = 2 |
| $I_{DD}$ | | | | | | | | $V_{IH} = V_{DD}$, $V_{IL}$ = GND, $V_{DD}$ = 2.7 V to 5.5 V |
| Normal Mode[7] | | 0.59 | 0.7 | | 0.59 | 0.7 | mA | |
| All Power-Down Modes[8] | | 1 | 4 | | 1 | 4 | μA | −40°C to +85°C |
| | | | 6 | | | 6 | μA | −40°C to +105°C |

[1] Temperature range is −40°C to +105°C.
[2] DC specifications are tested with the outputs unloaded, unless otherwise noted. Upper dead band (10 mV) exists only when $V_{REF} = V_{DD}$ with gain = 1 or when $V_{REF}/2 = V_{DD}$ with gain = 2. Linearity calculated using a reduced code range of 256 to 65,280 (AD5696) or 12 to 4080 (AD5694).
[3] Guaranteed by design and characterization; not production tested.
[4] Channel A and Channel B can have a combined output current of up to 30 mA. Similarly, Channel C and Channel D can have a combined output current of up to 30 mA up to a junction temperature of 110°C.
[5] $V_{DD}$ = 5 V. The device includes current limiting that is intended to protect the device during temporary overload conditions. Junction temperature can be exceeded during current limit. Operation above the specified maximum junction temperature may impair device reliability.
[6] When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV (see Figure 20).
[7] Interface inactive. All DACs active. DAC outputs unloaded.
[8] All DACs powered down.

## AC CHARACTERISTICS

$V_{DD}$ = 2.7 V to 5.5 V; $V_{REF}$ = 2.5 V; 1.8 V ≤ $V_{LOGIC}$ ≤ 5.5 V; $R_L$ = 2 kΩ; $C_L$ = 200 pF; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 3.**

| Parameter[1, 2] | Min | Typ | Max | Unit | Test Conditions/Comments[3] |
|---|---|---|---|---|---|
| Output Voltage Settling Time | | | | | ¼ to ¾ scale settling to ±2 LSB |
| AD5696 | | 5 | 8 | µs | |
| AD5694 | | 5 | 7 | µs | |
| Slew Rate | | 0.8 | | V/µs | |
| Digital-to-Analog Glitch Impulse | | 0.5 | | nV-sec | 1 LSB change around major carry transition |
| Digital Feedthrough | | 0.13 | | nV-sec | |
| Multiplying Bandwidth | | 500 | | kHz | |
| Digital Crosstalk | | 0.1 | | nV-sec | |
| Analog Crosstalk | | 0.2 | | nV-sec | |
| DAC-to-DAC Crosstalk | | 0.3 | | nV-sec | |
| Total Harmonic Distortion[4] | | −80 | | dB | At $T_A$, BW = 20 kHz, $V_{DD}$ = 5 V, $f_{OUT}$ = 1 kHz |
| Output Noise Spectral Density | | 100 | | nV/√Hz | DAC code = midscale, 10 kHz, gain = 2 |
| Output Noise | | 6 | | µV p-p | 0.1 Hz to 10 Hz |
| Signal-to-Noise Ratio (SNR) | | 90 | | dB | At $T_A$, BW = 20 kHz, $V_{DD}$ = 5 V, $f_{OUT}$ = 1 kHz |
| Spurious-Free Dynamic Range (SFDR) | | 83 | | dB | At $T_A$, BW = 20 kHz, $V_{DD}$ = 5 V, $f_{OUT}$ = 1 kHz |
| Signal-to-Noise-and-Distortion Ratio (SINAD) | | 80 | | dB | At $T_A$, BW = 20 kHz, $V_{DD}$ = 5 V, $f_{OUT}$ = 1 kHz |

[1] Guaranteed by design and characterization; not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to +105°C; typical at 25°C.
[4] Digitally generated sine wave at 1 kHz.

## TIMING CHARACTERISTICS

$V_{DD}$ = 2.7 V to 5.5 V; 1.8 V ≤ $V_{LOGIC}$ ≤ 5.5 V; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 4.**

| Parameter[1, 2] | Min | Max | Unit | Description |
|---|---|---|---|---|
| $t_1$ | 2.5 | | µs | SCL cycle time |
| $t_2$ | 0.6 | | µs | $t_{HIGH}$, SCL high time |
| $t_3$ | 1.3 | | µs | $t_{LOW}$, SCL low time |
| $t_4$ | 0.6 | | µs | $t_{HD,STA}$, start/repeated start hold time |
| $t_5$ | 100 | | ns | $t_{SU,DAT}$, data setup time |
| $t_6$[3] | 0 | 0.9 | µs | $t_{HD,DAT}$, data hold time |
| $t_7$ | 0.6 | | µs | $t_{SU,STA}$, repeated start setup time |
| $t_8$ | 0.6 | | µs | $t_{SU,STO}$, stop condition setup time |
| $t_9$ | 1.3 | | µs | $t_{BUF}$, bus free time between a stop condition and a start condition |
| $t_{10}$[4] | 0 | 300 | ns | $t_R$, rise time of SCL and SDA when receiving |
| $t_{11}$[4, 5] | 20 + 0.1$C_B$ | 300 | ns | $t_F$, fall time of SCL and SDA when transmitting/receiving |
| $t_{12}$ | 20 | | ns | $\overline{LDAC}$ pulse width |
| $t_{13}$ | 400 | | ns | SCL rising edge to $\overline{LDAC}$ rising edge |
| $t_{SP}$[6] | 0 | 50 | ns | Pulse width of suppressed spike |
| $C_B$[5] | | 400 | pF | Capacitive load for each bus line |

[1] See Figure 2.
[2] Guaranteed by design and characterization; not production tested.
[3] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH}$ min of the SCL signal) to bridge the undefined region of the SCL falling edge.
[4] $t_R$ and $t_F$ are measured from 0.3 × $V_{DD}$ to 0.7 × $V_{DD}$.
[5] $C_B$ is the total capacitance of one bus line in pF.
[6] Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns.

### *Timing Diagram*

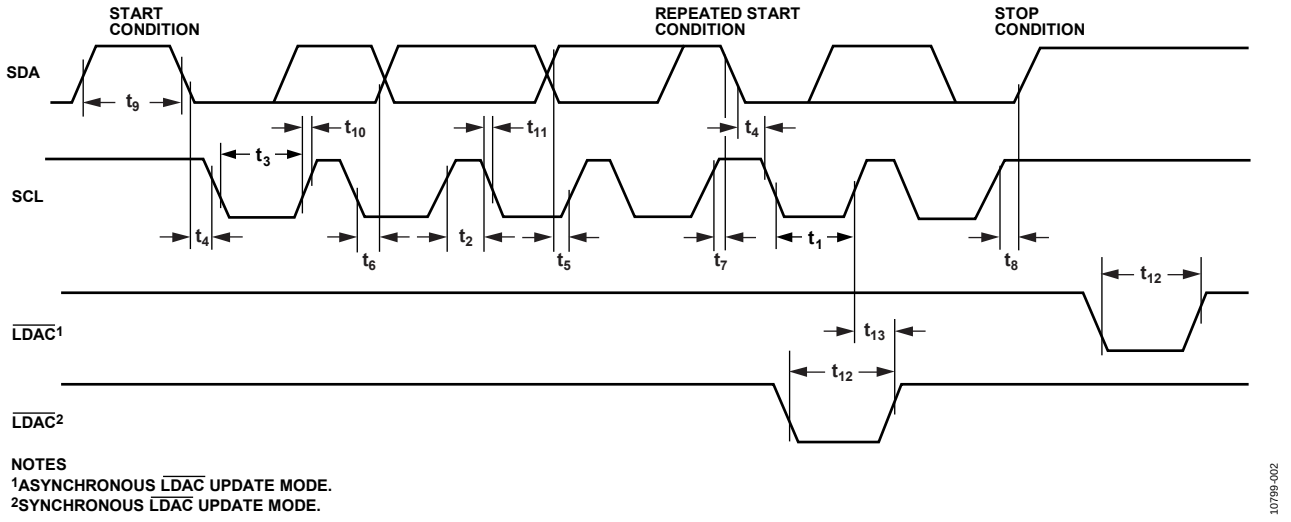



*Figure 2. 2-Wire Serial Interface Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 5.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +7 V |
| $V_{LOGIC}$ to GND | −0.3 V to +7 V |
| $V_{OUT}$ to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| $V_{REF}$ to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Digital Input Voltage to GND[1] | −0.3 V to $V_{LOGIC}$ + 0.3 V |
| SDA and SCL to GND | −0.3 V to +7 V |
| Operating Temperature Range | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 125°C |
| Reflow Soldering Peak Temperature, Pb Free (J-STD-020) | 260°C |
| ESD | |
| Human Body Model (HBM) | 3.5 kV |
| Field-Induced Charged Device Model (FICDM) | 1.5 kV |

[1] Excluding SDA and SCL.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. This value was measured using a JEDEC standard 4-layer board with zero airflow. For the LFCSP package, the exposed pad must be tied to GND.

**Table 6. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| 16-Lead LFCSP | 70 | °C/W |
| 16-Lead TSSOP | 112.6 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

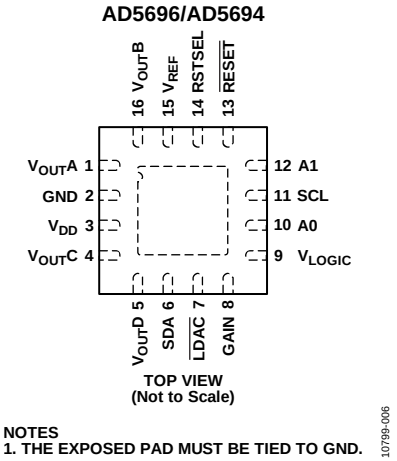



*Figure 3. Pin Configuration, 16-Lead LFCSP*

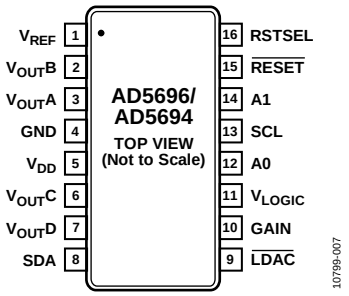



*Figure 4. Pin Configuration, 16-Lead TSSOP*

**Table 7. Pin Function Descriptions**

| Pin No. | | | |
|---|---|---|---|
| **LFCSP** | **TSSOP** | **Mnemonic** | **Description** |
| 1 | 3 | $V_{OUT}A$ | Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation. |
| 2 | 4 | GND | Ground Reference Point for All Circuitry on the Part. |
| 3 | 5 | $V_{DD}$ | Power Supply Input. The parts can be operated from 2.7 V to 5.5 V. The supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND. |
| 4 | 6 | $V_{OUT}C$ | Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation. |
| 5 | 7 | $V_{OUT}D$ | Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation. |
| 6 | 8 | SDA | Serial Data Input. This pin is used in conjunction with the SCL line to clock data into or out of the 24-bit input shift register. SDA is a bidirectional, open-drain data line that should be pulled to the supply with an external pull-up resistor. |
| 7 | 9 | $\overline{LDAC}$ | $\overline{LDAC}$ can be operated in two modes, asynchronous update mode and synchronous update mode. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data; all DAC outputs are simultaneously updated. This pin can also be tied permanently low. |
| 8 | 10 | GAIN | Gain Select Pin. When this pin is tied to GND, all four DAC outputs have a span of 0 V to $V_{REF}$. When this pin is tied to $V_{LOGIC}$, all four DAC outputs have a span of 0 V to 2 × $V_{REF}$. |
| 9 | 11 | $V_{LOGIC}$ | Digital Power Supply. Voltage ranges from 1.8 V to 5.5 V. |
| 10 | 12 | A0 | Address Input. Sets the first LSB of the 7-bit slave address. |
| 11 | 13 | SCL | Serial Clock Line. This pin is used in conjunction with the SDA line to clock data into or out of the 24-bit input shift register. |
| 12 | 14 | A1 | Address Input. Sets the second LSB of the 7-bit slave address. |
| 13 | 15 | $\overline{RESET}$ | Asynchronous Reset Input. The $\overline{RESET}$ input is falling edge sensitive. When $\overline{RESET}$ is activated (low), the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin. When $\overline{RESET}$ is low, all $\overline{LDAC}$ pulses are ignored. |
| 14 | 16 | RSTSEL | Power-On Reset Pin. When this pin is tied to GND, all four DACs are powered up to zero scale. When this pin is tied to $V_{LOGIC}$, all four DACs are powered up to midscale. |
| 15 | 1 | $V_{REF}$ | Reference Input Voltage. |
| 16 | 2 | $V_{OUT}B$ | Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation. |
| 17 | N/A | EPAD | Exposed Pad. The exposed pad must be tied to GND. |

# TYPICAL PERFORMANCE CHARACTERISTICS

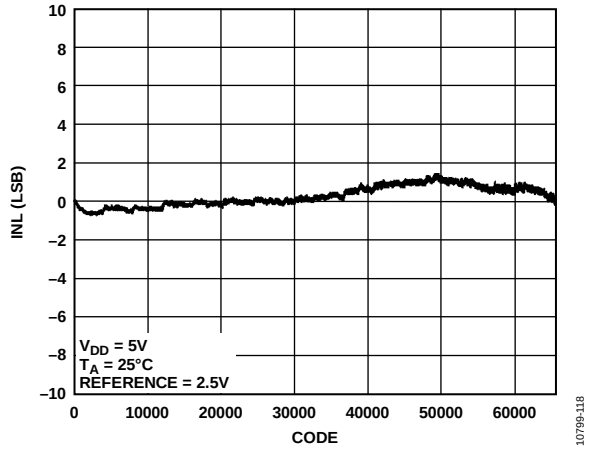



Figure 5. AD5696 INL

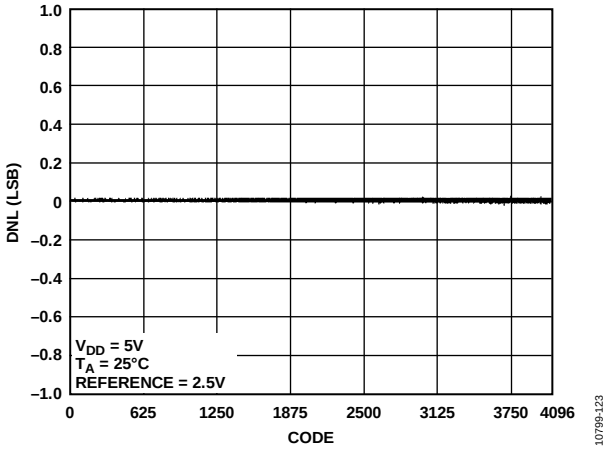



Figure 8. AD5694 DNL

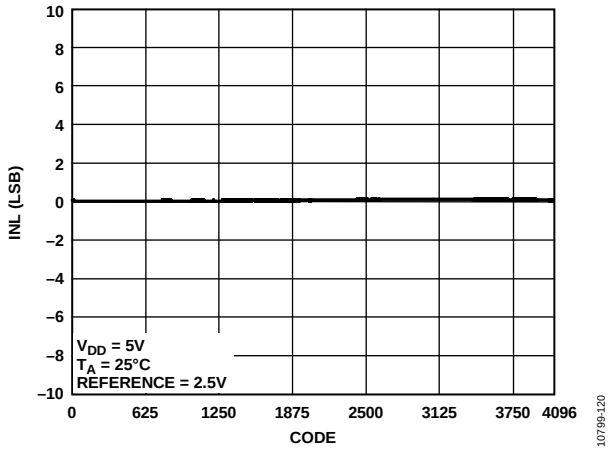



Figure 6. AD5694 INL

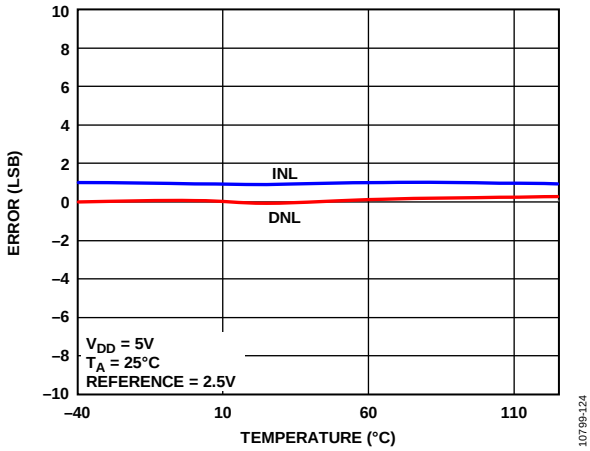



Figure 9. INL Error and DNL Error vs. Temperature

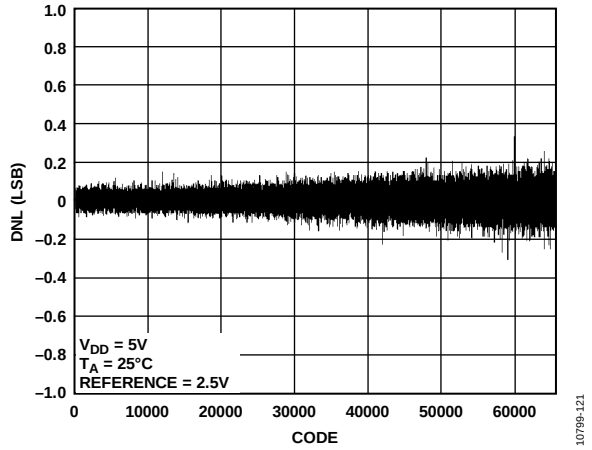



Figure 7. AD5696 DNL

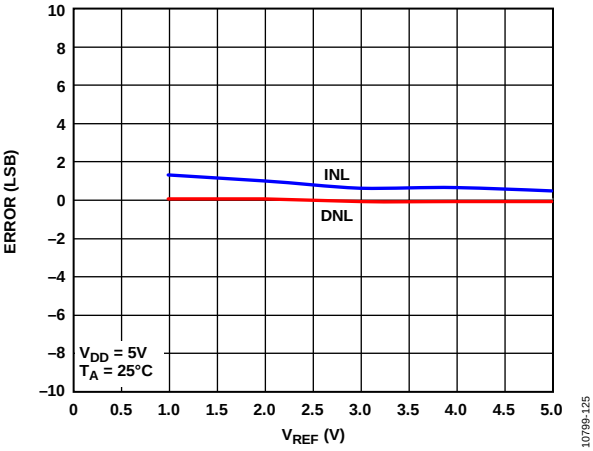



Figure 10. INL Error and DNL Error vs. $V_{REF}$

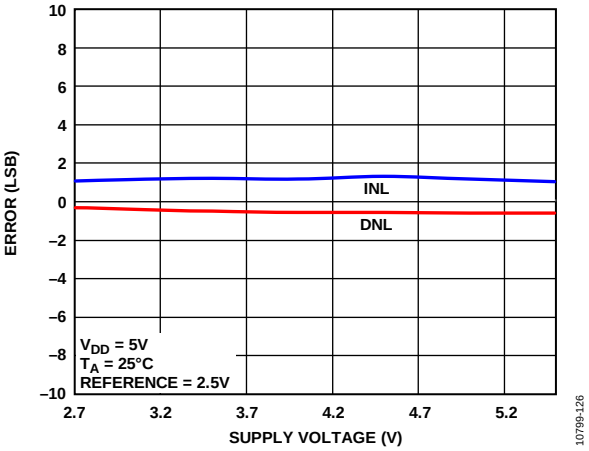



Figure 11. INL Error and DNL Error vs. Supply Voltage

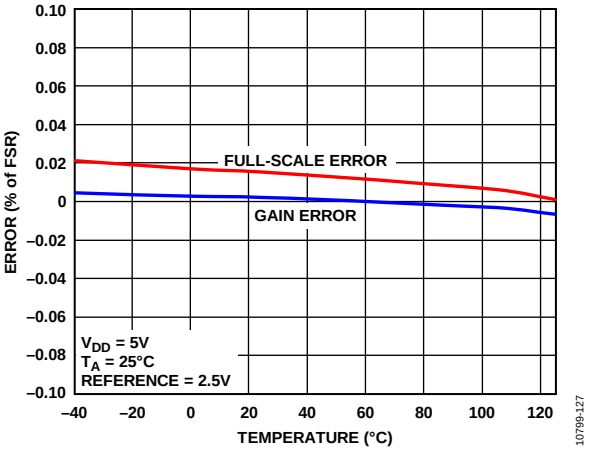



Figure 12. Gain Error and Full-Scale Error vs. Temperature

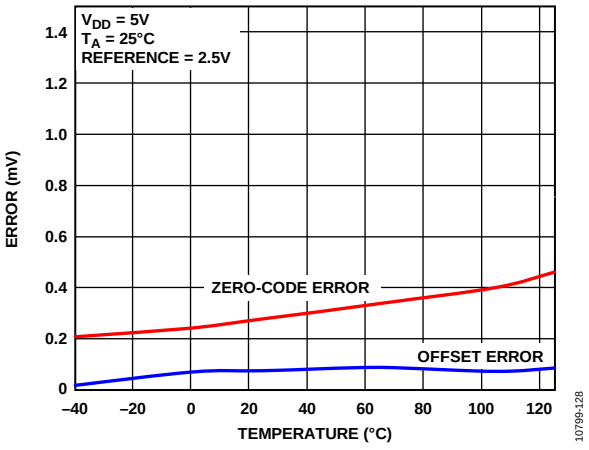



Figure 13. Zero-Code Error and Offset Error vs. Temperature

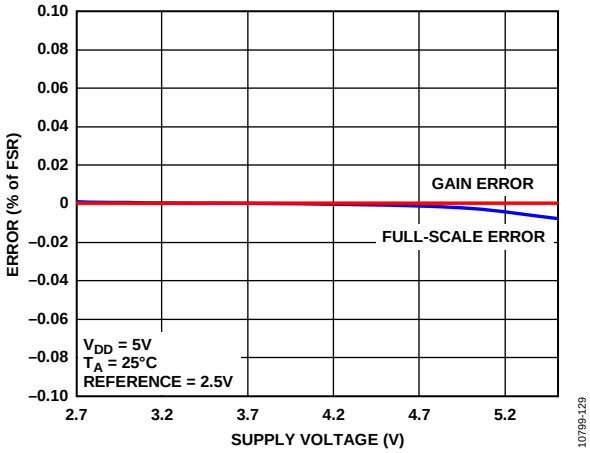



Figure 14. Gain Error and Full-Scale Error vs. Supply Voltage

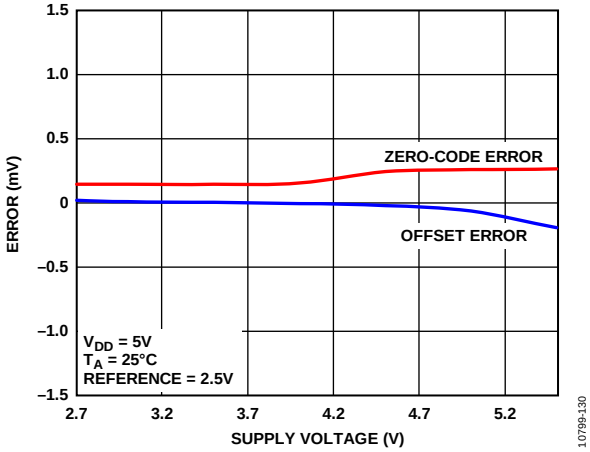



Figure 15. Zero-Code Error and Offset Error vs. Supply Voltage

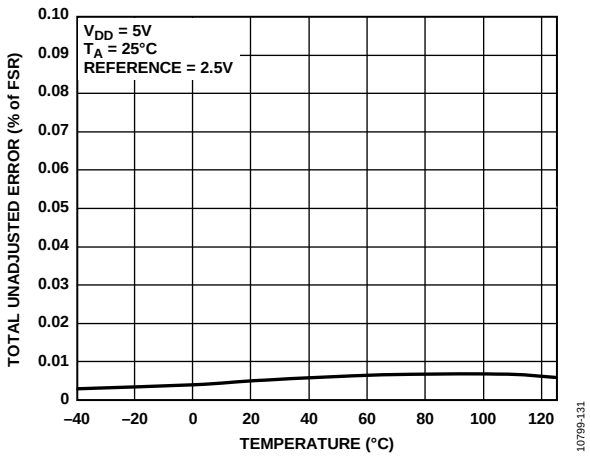



Figure 16. TUE vs. Temperature

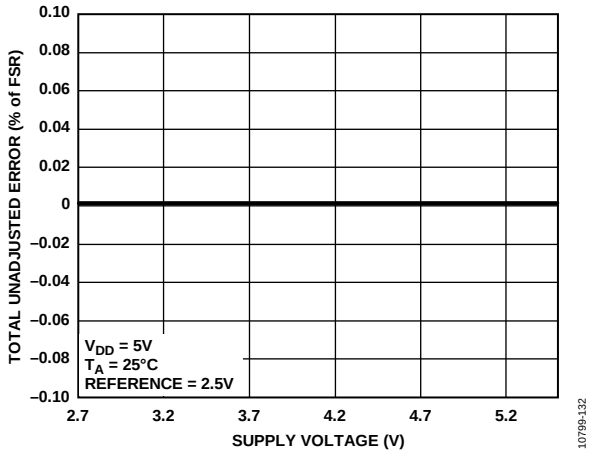



Figure 17. TUE vs. Supply Voltage, Gain = 1

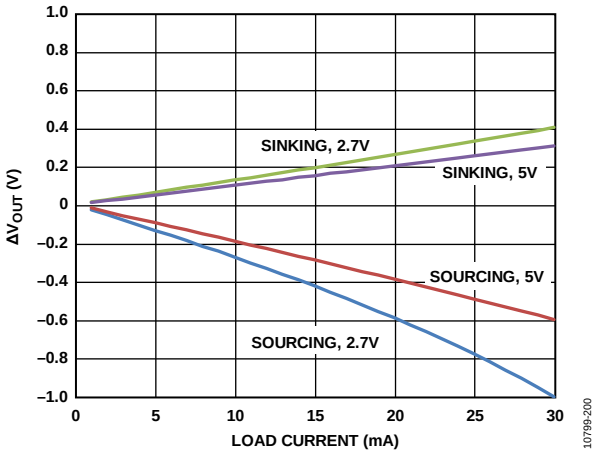



Figure 20. Headroom/Footroom vs. Load Current

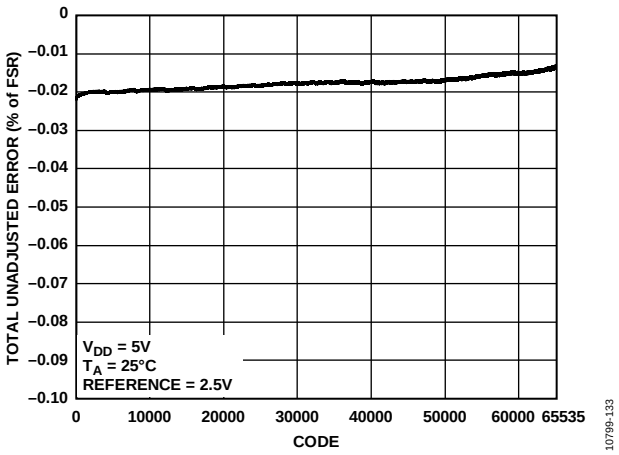



Figure 18. TUE vs. Code, AD5696

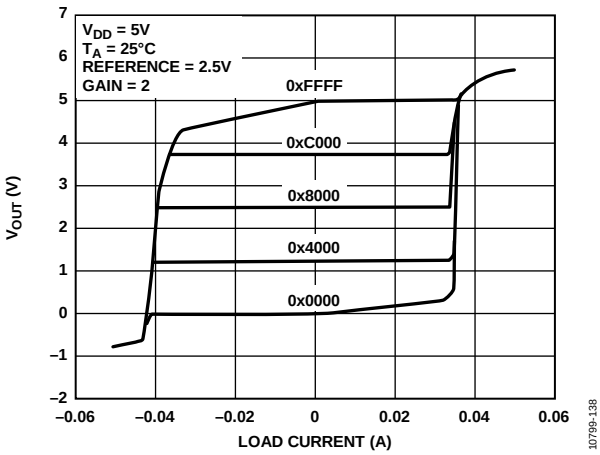



Figure 21. Source and Sink Capability at 5 V

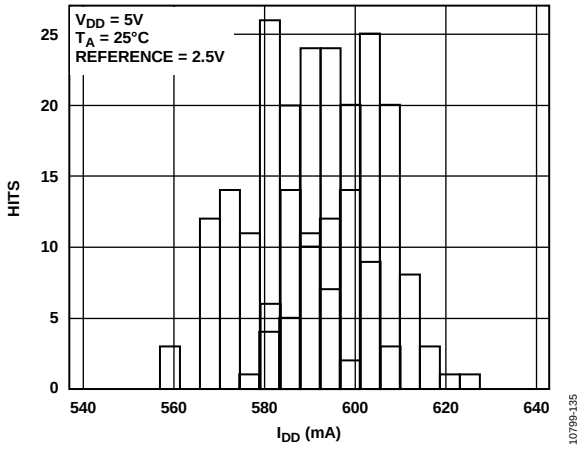



Figure 19. $I_{DD}$ Histogram at 5 V

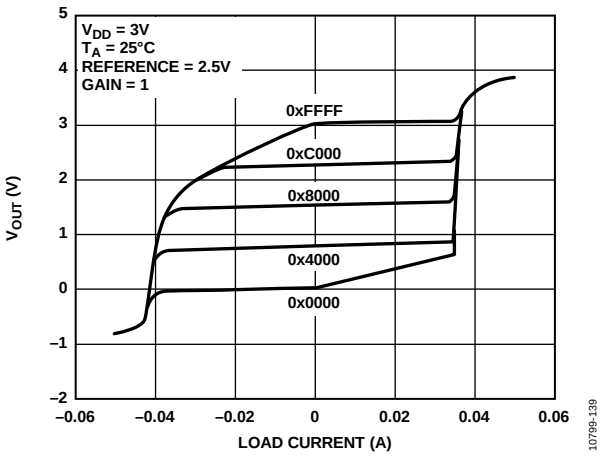



Figure 22. Source and Sink Capability at 3 V

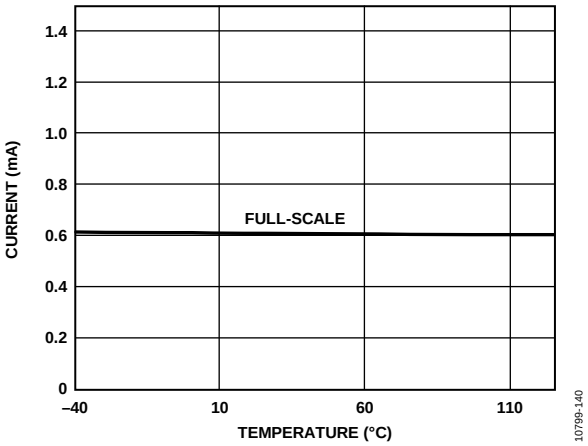



Figure 23. Supply Current vs. Temperature

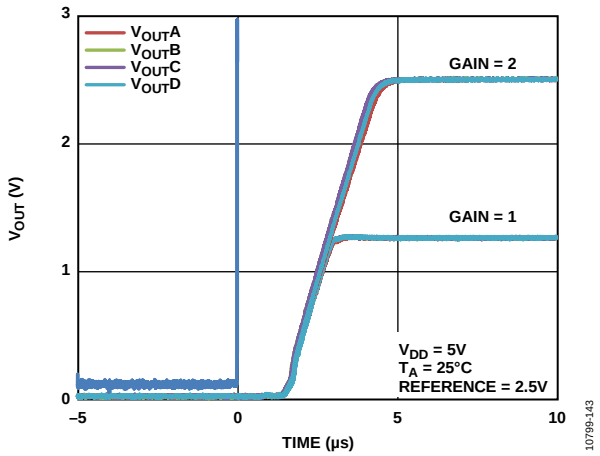



Figure 26. Exiting Power-Down to Midscale

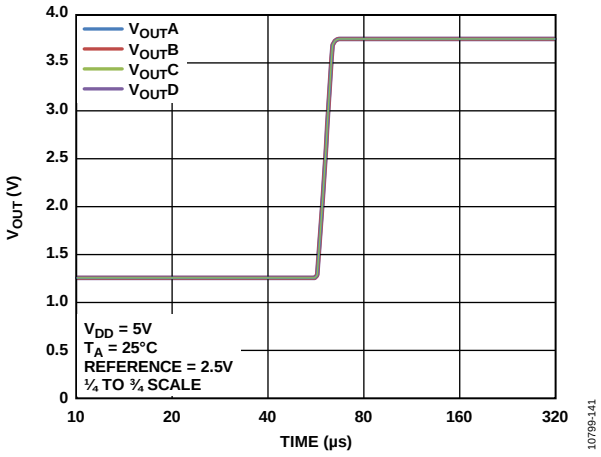



Figure 24. Settling Time

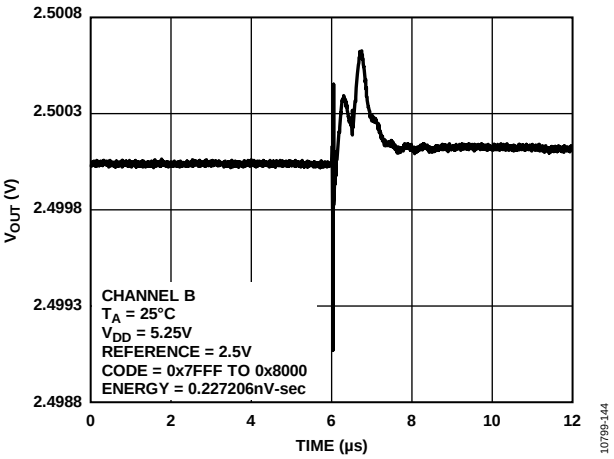



Figure 27. Digital-to-Analog Glitch Impulse

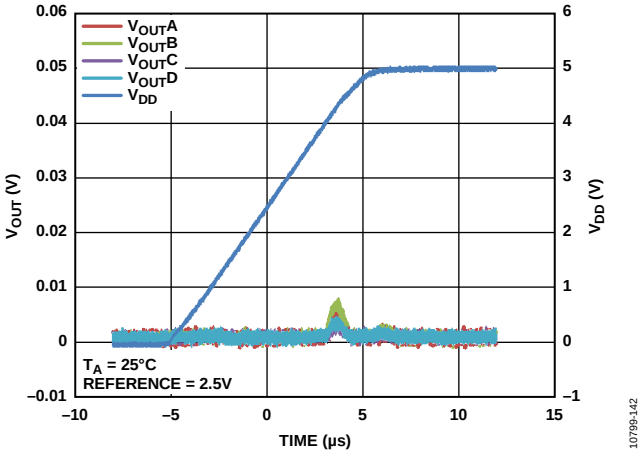



Figure 25. Power-On Reset to 0 V

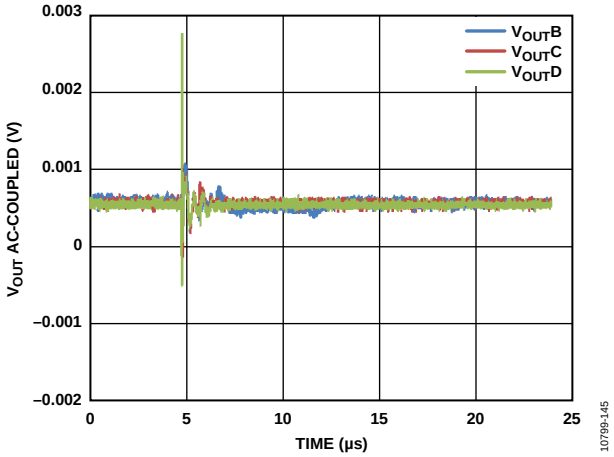



Figure 28. Analog Crosstalk, $V_{OUT}A$

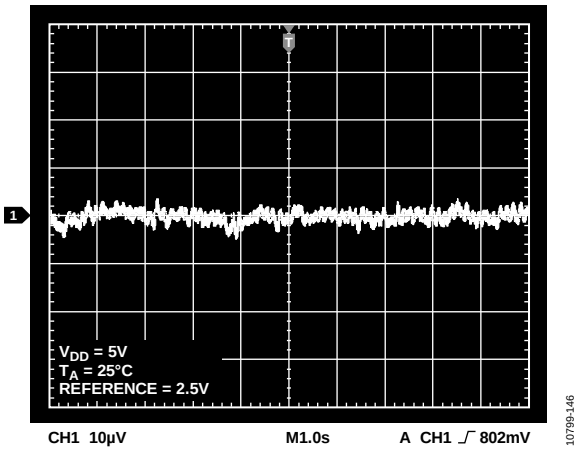



Figure 29. 0.1 Hz to 10 Hz Output Noise Plot

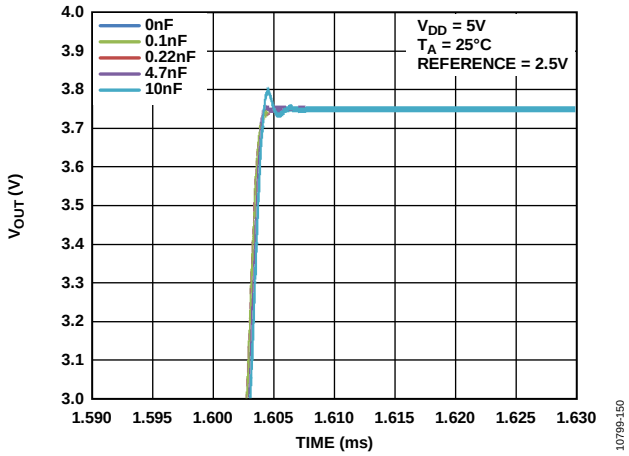



Figure 31. Settling Time vs. Capacitive Load

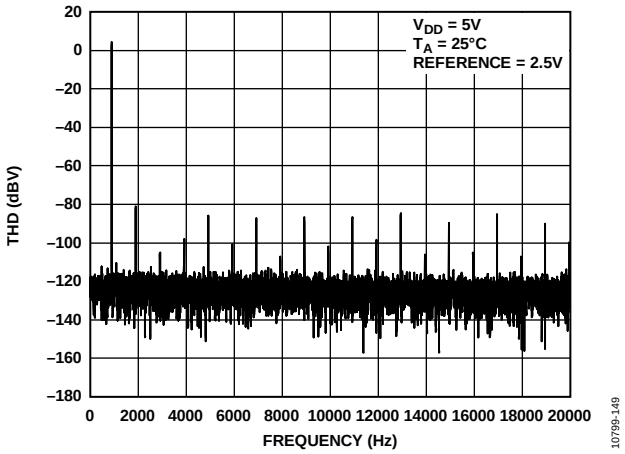



Figure 30. Total Harmonic Distortion at 1 kHz

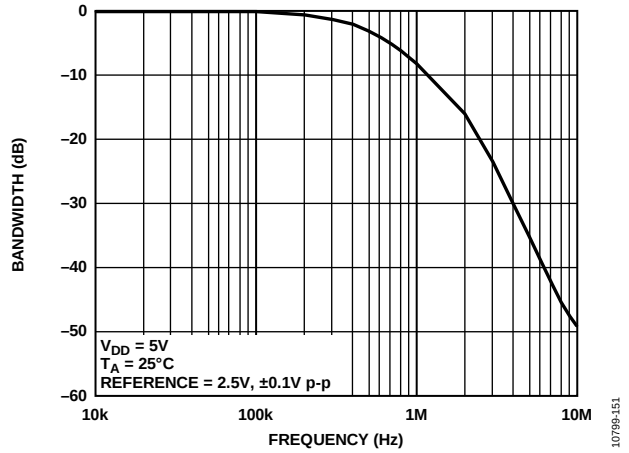



Figure 32. Multiplying Bandwidth

# TERMINOLOGY

**Relative Accuracy or Integral Nonlinearity (INL)**
Relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. Figure 5 and Figure 6 show typical INL vs. code plots.

**Differential Nonlinearity (DNL)**
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. The AD5696/AD5694 are guaranteed monotonic by design. Figure 7 and Figure 8 show typical DNL vs. code plots.

**Zero-Code Error**
Zero-code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5696/AD5694 because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero-code error is expressed in mV. Figure 13 shows a plot of zero-code error vs. temperature.

**Full-Scale Error**
Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be $V_{DD}$ − 1 LSB. Full-scale error is expressed as a percentage of the full-scale range (% of FSR). Figure 12 shows a plot of full-scale error vs. temperature.

**Gain Error**
Gain error is a measurement of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed in % of FSR.

**Gain Temperature Coefficient**
Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/°C.

**Offset Error**
Offset error is a measurement of the difference between $V_{OUT}$ (actual) and $V_{OUT}$ (ideal) expressed in mV in the linear region of the transfer function. It can be negative or positive.

**Offset Error Drift**
Offset error drift is a measurement of the change in offset error with changes in temperature. It is expressed in µV/°C.

**DC Power Supply Rejection Ratio (PSRR)**
DC PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in $V_{OUT}$ to a change in $V_{DD}$ for midscale output of the DAC. It is measured in mV/V. $V_{REF}$ is held at 2.5 V, and $V_{DD}$ is varied by ±10%.

**Output Voltage Settling Time**
The output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change.

**Digital-to-Analog Glitch Impulse**
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000) (see Figure 27).

**Digital Feedthrough**
Digital feedthrough is a measurement of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

**Noise Spectral Density (NSD)**
Noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz) and is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz.

**DC Crosstalk**
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in µV.

DC crosstalk due to load current change is a measurement of the impact that a change in load current on one DAC has on another DAC kept at midscale. It is expressed in µV/mA.

**Digital Crosstalk**
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is expressed in nV-sec.

**Analog Crosstalk**
Analog crosstalk is the glitch impulse transferred to the output of one DAC in response to a change in the output of another DAC. To measure analog crosstalk, load one of the input registers with a full-scale code change (all 0s to all 1s and vice versa), and then execute a software LDAC and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-sec.

**DAC-to-DAC Crosstalk**
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC in response to a digital code change and subsequent analog output change of another DAC. It is measured by loading one channel with a full-scale code change (all 0s to all 1s and vice versa) using the write to and update commands while monitoring the output of another channel that is at mid-scale. The energy of the glitch is expressed in nV-sec.

**Multiplying Bandwidth**
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

**Total Harmonic Distortion (THD)**
THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC; THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

# THEORY OF OPERATION

## DIGITAL-TO-ANALOG CONVERTER

The AD5696/AD5694 are quad, 16-/12-bit, serial input, voltage output DACs that operate from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5696/AD5694 in a 24-bit word format via a 2-wire serial interface. The AD5696/AD5694 incorporate a power-on reset circuit to ensure that the DAC output powers up to a known output state. The devices also have a software power-down mode that reduces the current consumption to 4 µA.

## TRANSFER FUNCTION

Because the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = V_{REF} \times Gain \left[ \frac{D}{2^N} \right]$$

where:

$V_{REF}$ is the value of the external reference.

*Gain* is the gain of the output amplifier and is set to 1 by default. The gain can be set to 1 or 2 using the gain select pin. When the GAIN pin is tied to GND, all four DAC outputs have a span of 0 V to $V_{REF}$. When this pin is tied to $V_{DD}$, all four DAC outputs have a span of 0 V to 2 × $V_{REF}$.

*D* is the decimal equivalent of the binary code that is loaded to the DAC register as follows: 0 to 4095 for the 12-bit AD5694, and 0 to 65,535 for the 16-bit AD5696.

*N* is the DAC resolution (12 bits or 16 bits).

## DAC ARCHITECTURE

The DAC architecture consists of a string DAC followed by an output amplifier. Figure 33 shows a block diagram of the DAC architecture.

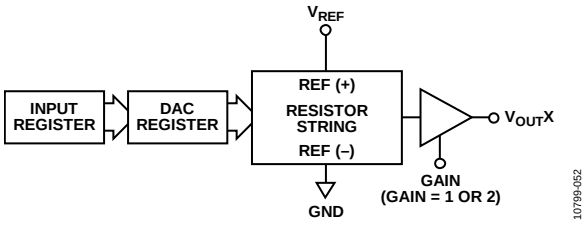



*Figure 33. Single DAC Channel Architecture Block Diagram*

The resistor string structure is shown in Figure 34. Each resistor in the string has a value R. The code loaded to the DAC register determines the node on the string from which the voltage is tapped off and fed into the output amplifier. The voltage is tapped off by closing one of the switches that connect the string to the amplifier. Because the AD5696/AD5694 are a string of resistors, they are guaranteed monotonic.

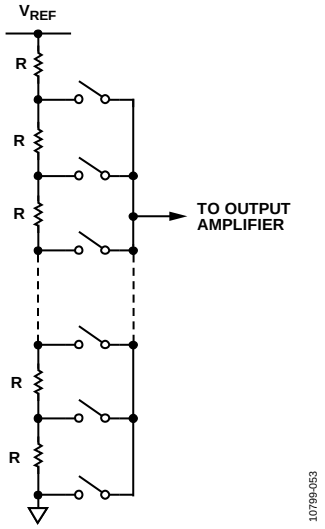



*Figure 34. Resistor String Structure*

### *Output Amplifiers*

The output buffer amplifier can generate rail-to-rail voltages on its output for an output range of 0 V to $V_{DD}$. The actual range depends on the value of $V_{REF}$, the GAIN pin, the offset error, and the gain error. The GAIN pin selects the gain of the output.

- When this pin is tied to GND, all four outputs have a gain of 1, and the output range is from 0 V to $V_{REF}$.
- When this pin is tied to $V_{DD}$, all four outputs have a gain of 2, and the output range is from 0 V to 2 × $V_{REF}$.

The output amplifiers are capable of driving a load of 1 kΩ in parallel with 2 nF to GND. The slew rate is 0.8 V/µs with a ¼ to ¾ scale settling time of 5 µs.

## SERIAL INTERFACE

The AD5696/AD5694 have a 2-wire, I²C-compatible serial interface (see the *I²C-Bus Specification*, Version 2.1, January 2000, available from Philips Semiconductor). See Figure 2 for a timing diagram of a typical write sequence. The AD5696/AD5694 can be connected to an I²C bus as slave devices, under the control of a master device. The AD5696/AD5694 support standard (100 kHz) and fast (400 kHz) data transfer modes. Support is not provided for 10-bit addressing or general call addressing.

### *Input Shift Register*

The input shift register of the AD5696/AD5694 is 24 bits wide. Data is loaded into the device, MSB first, as a 24-bit word under the control of the serial clock input, SCL. The first eight MSBs make up the command byte (see Figure 35 and Figure 36).

- The first four bits of the command byte are the command bits (C3, C2, C1, and C0), which control the mode of operation of the device (see Table 8).
- The last four bits of the command byte are the address bits (DAC D, DAC C, DAC B, and DAC A), which select the DAC that is operated on by the command (see Table 9).

The 8-bit command byte is followed by two data bytes, which contain the data-word. For the AD5696, the data-word comprises the 16-bit input code (see Figure 35); for the AD5694, the data-word comprises the 12-bit input code followed by four don't care bits (see Figure 36). The data bits are transferred to the input shift register on the 24 falling edges of SCL.

Commands can be executed on one DAC channel, any two or three DAC channels, or on all four DAC channels, depending on the address bits selected (see Table 9).

**Table 8. Command Definitions**

| Command Bits | | | | |
|---|---|---|---|---|
| C3 | C2 | C1 | C0 | Command |
| 0 | 0 | 0 | 0 | No operation |
| 0 | 0 | 0 | 1 | Write to Input Register n (dependent on $\overline{\text{LDAC}}$) |
| 0 | 0 | 1 | 0 | Update DAC Register n with contents of Input Register n |
| 0 | 0 | 1 | 1 | Write to and update DAC Channel n |
| 0 | 1 | 0 | 0 | Power down/power up DAC |
| 0 | 1 | 0 | 1 | Hardware $\overline{\text{LDAC}}$ mask register |
| 0 | 1 | 1 | 0 | Software reset (power-on reset) |
| 0 | 1 | 1 | 1 | Reserved |
| 1 | X[1] | X[1] | X[1] | Reserved |

[1] X = don't care.

**Table 9. Address Bits and Selected DACs**

| Address Bits | | | | |
|---|---|---|---|---|
| DAC D | DAC C | DAC B | DAC A | Selected DAC Channels[1] |
| 0 | 0 | 0 | 1 | DAC A |
| 0 | 0 | 1 | 0 | DAC B |
| 0 | 0 | 1 | 1 | DAC A and DAC B |
| 0 | 1 | 0 | 0 | DAC C |
| 0 | 1 | 0 | 1 | DAC A and DAC C |
| 0 | 1 | 1 | 0 | DAC B and DAC C |
| 0 | 1 | 1 | 1 | DAC A, DAC B, and DAC C |
| 1 | 0 | 0 | 0 | DAC D |
| 1 | 0 | 0 | 1 | DAC A and DAC D |
| … | … | … | … | … |
| 1 | 1 | 1 | 1 | All DACs |

[1] Any combination of DAC channels can be selected using the address bits.

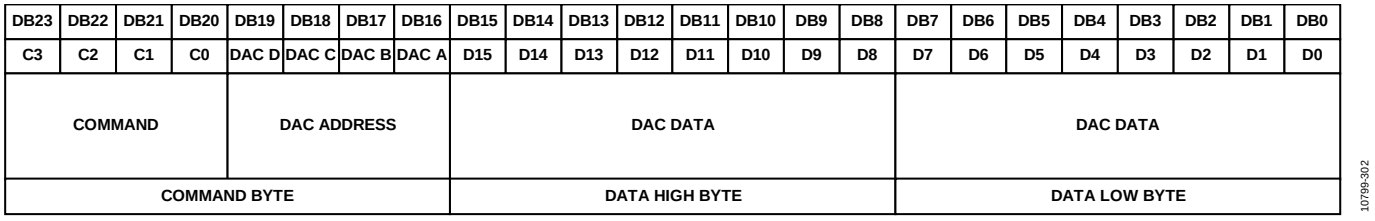



*Figure 35. Input Shift Register Contents, AD5696*

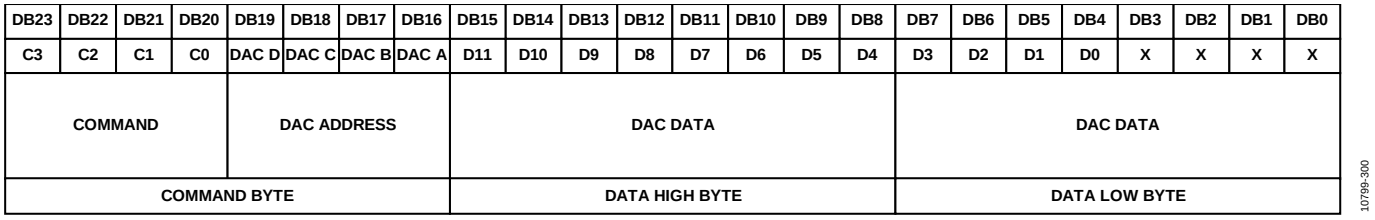



*Figure 36. Input Shift Register Contents, AD5694*

## WRITE AND UPDATE COMMANDS

For more information about the $\overline{\text{LDAC}}$ function, see the Load DAC (Hardware $\overline{\text{LDAC}}$ Pin) section.

### *Write to Input Register n (Dependent on $\overline{\text{LDAC}}$)*

Command 0001 allows the user to write to each DAC's dedicated input register individually. When $\overline{\text{LDAC}}$ is low, the input register is transparent (if not controlled by the $\overline{\text{LDAC}}$ mask register).

### *Update DAC Register n with Contents of Input Register n*

Command 0010 loads the DAC registers/outputs with the contents of the input registers selected by the address bits (see Table 9) and updates the DAC outputs directly.

### *Write to and Update DAC Channel n (Independent of $\overline{\text{LDAC}}$)*

Command 0011 allows the user to write to the DAC registers and update the DAC outputs directly, independent of the state of the $\overline{\text{LDAC}}$ pin.

## I²C SLAVE ADDRESS

The AD5696/AD5694 have a 7-bit I²C slave address. The five MSBs are 00011, and the two LSBs (A1 and A0) are set by the state of the A1 and A0 address pins. The ability to make hard-wired changes to A1 and A0 allows the user to incorporate up to four AD5696/AD5694 devices on one bus (see Table 10).

**Table 10. Device Address Selection**

| A1 Pin Connection | A0 Pin Connection | A1 Bit | A0 Bit |
|---|---|---|---|
| GND | GND | 0 | 0 |
| GND | $V_{LOGIC}$ | 0 | 1 |
| $V_{LOGIC}$ | GND | 1 | 0 |
| $V_{LOGIC}$ | $V_{LOGIC}$ | 1 | 1 |

## SERIAL OPERATION

The 2-wire I²C serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address.
2. The slave device with the transmitted address responds by pulling SDA low during the 9th clock pulse (this is called the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its input shift register.
3. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). Transitions on the SDA line must occur during the low period of SCL; SDA must remain stable during the high period of SCL.
4. After all data bits are read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the 9th clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse and then high again during the 10th clock pulse to establish a stop condition.

## WRITE OPERATION

When writing to the AD5696/AD5694, the user must begin with a start command followed by an address byte (R/$\overline{\text{W}}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The AD5696/AD5694 require two bytes of data for the DAC and a command byte that controls various DAC functions. Three bytes of data must, therefore, be written to the DAC with the command byte followed by the most significant data byte and the least significant data byte, as shown in Figure 37. All these data bytes are acknowledged by the AD5696/AD5694. A stop condition follows.

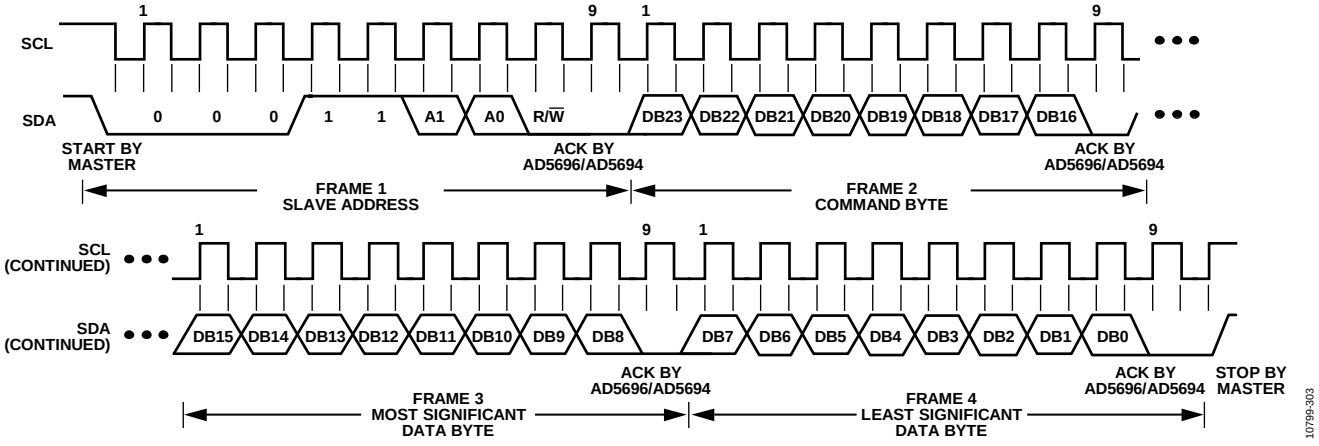



*Figure 37. I²C Write Operation*

## READ OPERATION

When reading data back from the AD5696/AD5694, the user must begin with a start command followed by an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte must be followed by the command byte, which determines both the read command that is to follow and the pointer address to read from; the command byte is also acknowledged by the DAC. The user configures the channel to read back the contents of one or more DAC registers and sets the readback command to active using the command byte.

Following this, the master establishes a repeated start condition, and the address is resent with R/$\overline{W}$ = 1. This byte is acknowledged by the DAC, indicating that it is prepared to transmit data. Two bytes of data are then read from the DAC, as shown in Figure 38. A NACK condition from the master, followed by a stop condition, completes the read sequence. If more than one DAC is selected, Channel A is read back by default.

## MULTIPLE DAC READBACK SEQUENCE

When reading data back from multiple AD5696/AD5694 DACs, the user begins with an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte must be followed by the command byte, which is also acknowledged by the DAC. The user selects the first channel to read back using the command byte.

Following this, the master establishes a repeated start condition, and the address is resent with R/$\overline{W}$ = 1. This byte is acknowledged by the DAC, indicating that it is prepared to transmit data. The first two bytes of data are then read from DAC Input Register n (selected using the command byte), most significant byte first, as shown in Figure 38. The next two bytes read back are the contents of DAC Input Register n + 1, and the next bytes read back are the contents of DAC Input Register n + 2. Data is read from the DAC input registers in this auto-incremented fashion until a NACK followed by a stop condition follows. If the contents of DAC Input Register D are read out, the next two bytes of data that are read are the contents of DAC Input Register A.

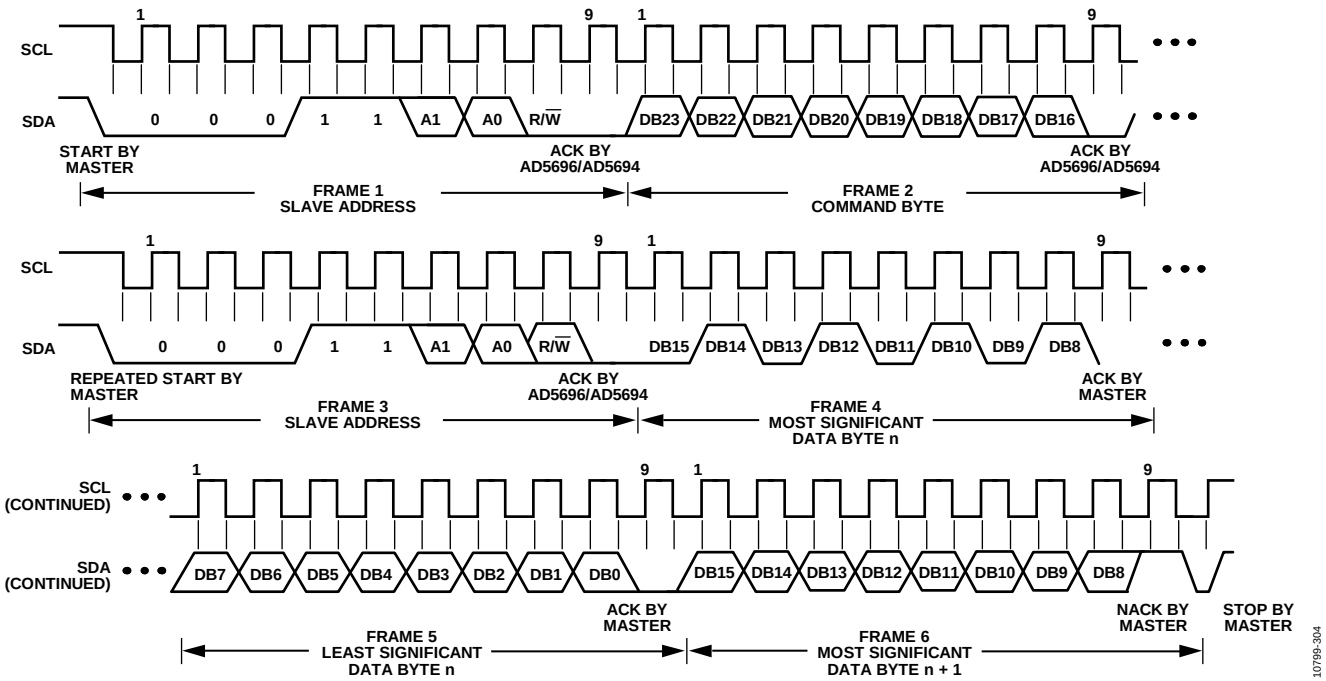



*Figure 38. I²C Read Operation*

## POWER-DOWN OPERATION

Command 0100 is designated for the power-down function. The AD5696/AD5694 provide three separate power-down modes (see Table 11). These power-down modes are software programmable by setting Bit DB7 to Bit DB0 in the input shift register (see Table 12). Two bits are associated with each DAC channel. Table 11 shows how the state of these two bits corresponds to the mode of operation of the device.

**Table 11. Modes of Operation**

| Operating Mode | PDx1 | PDx0 |
|---|---|---|
| Normal Operation | 0 | 0 |
| Power-Down Modes | | |
| 1 kΩ to GND | 0 | 1 |
| 100 kΩ to GND | 1 | 0 |
| Three-State | 1 | 1 |

Any or all DACs (DAC A to DAC D) can be powered down to the selected mode by setting the corresponding bits in the input shift register. See Table 12 for the contents of the input shift register during the power-down/power-up operation.

When both Bit PDx1 and Bit PDx0 (where x is the DAC selected) in the input shift register are set to 0, the parts work normally with their normal power consumption of 0.59 mA at 5 V. When Bit PDx1, Bit PDx0, or both Bit PDx1 and Bit PDx0 are set to 1, the part is in power-down mode. In power-down mode, the supply current falls to 4 μA at 5 V.

In power-down mode, the output stage is internally switched from the output of the amplifier to a resistor network of known values. In this way, the output impedance of the part is known when the part is in power-down mode.

Table 11 lists the three power-down options. The output is connected internally to GND through either a 1 kΩ or a 100 kΩ resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 39.

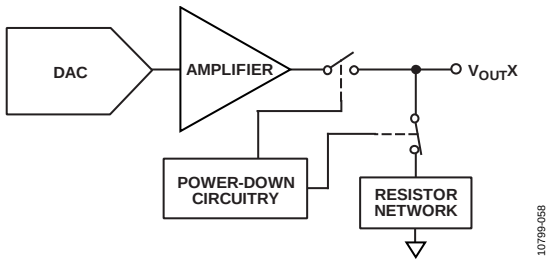



*Figure 39. Output Stage During Power-Down*

The bias generator, output amplifier, resistor string, and other associated linear circuitry are shut down when power-down mode is activated. However, the contents of the DAC registers are unaffected in power-down mode, and the DAC registers can be updated while the device is in power-down mode. The time required to exit power-down is typically 2.5 μs for $V_{DD}$ = 5 V.

## LOAD DAC (HARDWARE $\overline{\text{LDAC}}$ PIN)

The AD5696/AD5694 DACs have double buffered interfaces consisting of two banks of registers: input registers and DAC registers. The user can write to any combination of the input registers (see Table 9). Updates to the DAC registers are controlled by the $\overline{\text{LDAC}}$ pin.

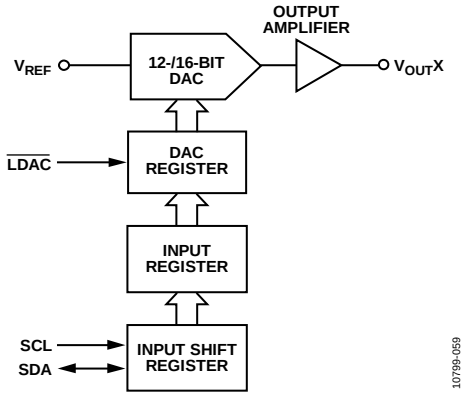



*Figure 40. Simplified Diagram of Input Loading Circuitry for a Single DAC*

**Table 12. 24-Bit Input Shift Register Contents for Power-Down/Power-Up Operation[1]**

| DB23 (MSB) | DB22 | DB21 | DB20 | DB19 to DB16 | DB15 to DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 (LSB) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | X | X | PDD1 | PDD0 | PDC1 | PDC0 | PDB1 | PDB0 | PDA1 | PDA0 |
| Command bits (C3 to C0) | | | | Address bits (don't care) | Don't care | Power-down select, DAC D | | Power-down select, DAC C | | Power-down select, DAC B | | Power-down select, DAC A | |

[1] X = don't care.

### *Instantaneous DAC Updating ($\overline{\text{LDAC}}$ Held Low)*

For instantaneous updating of the DACs, $\overline{\text{LDAC}}$ is held low while data is clocked into the input register using Command 0001. Both the addressed input register and the DAC register are updated on the 24th clock, and the output begins to change (see Table 14).

### *Deferred DAC Updating ($\overline{\text{LDAC}}$ Pulsed Low)*

For deferred updating of the DACs, $\overline{\text{LDAC}}$ is held high while data is clocked into the input register using Command 0001. All DAC outputs are asynchronously updated by pulling $\overline{\text{LDAC}}$ low after the 24th clock. The update occurs on the falling edge of $\overline{\text{LDAC}}$.

## $\overline{\text{LDAC}}$ MASK REGISTER

Command 0101 is reserved for the software $\overline{\text{LDAC}}$ function. When this command is executed, the address bits are ignored. When writing to the DAC using Command 0101, the 4-bit $\overline{\text{LDAC}}$ mask register (DB3 to DB0) is loaded. Bit DB3 of the $\overline{\text{LDAC}}$ mask register corresponds to DAC D; Bit DB2 corresponds to DAC C; Bit DB1 corresponds to DAC B; and Bit DB0 corresponds to DAC A.

The default value of these bits is 0; that is, the $\overline{\text{LDAC}}$ pin works normally. Setting any of these bits to 1 forces the selected DAC channel to ignore transitions on the $\overline{\text{LDAC}}$ pin, regardless of the state of the hardware $\overline{\text{LDAC}}$ pin. This flexibility is useful in applications where the user wishes to select which channels respond to the $\overline{\text{LDAC}}$ pin.

The $\overline{\text{LDAC}}$ mask register allows the user extra flexibility and control over the hardware $\overline{\text{LDAC}}$ pin (see Table 13). Setting the $\overline{\text{LDAC}}$ bit (DB3 to DB0) to 0 for a DAC channel allows the hard-ware $\overline{\text{LDAC}}$ pin to control the updating of that channel.

**Table 13. $\overline{\text{LDAC}}$ Overwrite Definition**

| Load $\overline{\text{LDAC}}$ Register | | |
|---|---|---|
| $\overline{\text{LDAC}}$ Bit (DB3 to DB0) | $\overline{\text{LDAC}}$ Pin | $\overline{\text{LDAC}}$ Operation |
| 0 | 1 or 0 | Determined by the $\overline{\text{LDAC}}$ pin. |
| 1 | X[1] | DAC channels are updated. (DAC channels see $\overline{\text{LDAC}}$ pin as 1.) |

[1] X = don't care.

## HARDWARE RESET PIN ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ is an active low reset that allows the outputs to be cleared to either zero scale or midscale. The clear code value is user selectable via the reset select pin (RSTSEL). It is necessary to keep $\overline{\text{RESET}}$ low for a minimum of 30 ns to complete the operation.

When the $\overline{\text{RESET}}$ signal is returned high, the output remains at the cleared value until a new value is programmed. The outputs cannot be updated with a new value while the $\overline{\text{RESET}}$ pin is low.

There is also a software executable reset function that resets the DAC to the power-on reset code. Command 0110 is designated for this software reset function (see Table 8). Any events on $\overline{\text{LDAC}}$ or $\overline{\text{RESET}}$ during power-on reset are ignored.

## RESET SELECT PIN (RSTSEL)

The AD5696/AD5694 contain a power-on reset circuit that controls the output voltage during power-up. When the RSTSEL pin is tied to GND, the outputs power up to zero scale (note that this is outside the linear region of the DAC). When the RSTSEL pin is tied to $V_{DD}$, the outputs power up to midscale. The outputs remain powered up at the level set by the RSTSEL pin until a valid write sequence is made to the DAC.

**Table 14. Write Commands and $\overline{\text{LDAC}}$ Pin Truth Table[1]**

| Command | Description | Hardware $\overline{\text{LDAC}}$ Pin State | Input Register Contents | DAC Register Contents |
|---|---|---|---|---|
| 0001 | Write to Input Register n (dependent on $\overline{\text{LDAC}}$) | $V_{LOGIC}$ | Data update | No change (no update) |
| | | GND[2] | Data update | Data update |
| 0010 | Update DAC Register n with contents of Input Register n | $V_{LOGIC}$ | No change | Updated with input register contents |
| | | GND | No change | Updated with input register contents |
| 0011 | Write to and update DAC Channel n | $V_{LOGIC}$ | Data update | Data update |
| | | GND | Data update | Data update |

[1] A high to low transition on the hardware $\overline{\text{LDAC}}$ pin always updates the contents of the DAC register with the contents of the input register on channels that are not masked (blocked) by the $\overline{\text{LDAC}}$ mask register.
[2] When the $\overline{\text{LDAC}}$ pin is permanently tied low, the $\overline{\text{LDAC}}$ mask bits are ignored.

# APPLICATIONS INFORMATION

## MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5696/AD5694 is via a serial bus that uses a standard protocol that is compatible with DSP processors and microcontrollers. The communications channel requires a 2-wire interface consisting of a clock signal and a data signal.

## AD5696/AD5694 TO ADSP-BF531 INTERFACE

The I²C interface of the AD5696/AD5694 is designed for easy connection to industry-standard DSPs and microcontrollers. Figure 41 shows the AD5696/AD5694 connected to the Analog Devices, Inc., Blackfin® processor. The Blackfin processor has an integrated I²C port that can be connected directly to the I²C pins of the AD5696/AD5694.

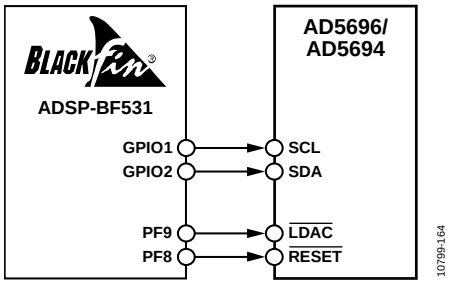



*Figure 41. AD5696/AD5694 to ADSP-BF531 Interface*

## LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The PCB on which the AD5696/AD5694 are mounted should be designed so that the AD5696/AD5694 lie on the analog plane.

The AD5696/AD5694 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitor is the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types; these capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

In systems where many devices are on one board, it is often useful to provide some heat sinking capability to allow the power to dissipate easily.

The AD5696/AD5694 LFCSP models have an exposed pad beneath the device. Connect this pad to the GND supply for the part. For optimum performance, use special considerations to design the motherboard and to mount the package.

For enhanced thermal, electrical, and board level performance, solder the exposed pad on the bottom of the LFCSP package to the corresponding thermal land paddle on the PCB. Design thermal vias into the PCB land paddle area to further improve heat dissipation.

The GND plane on the device can be increased (as shown in Figure 42) to provide a natural heat sinking effect.

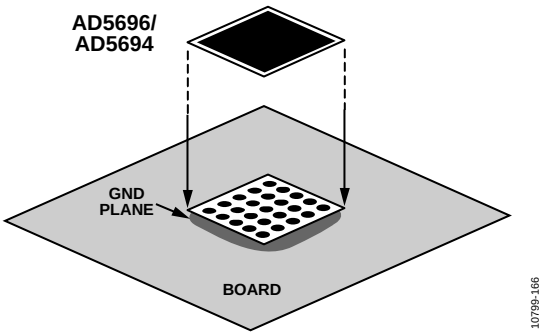



*Figure 42. Paddle Connection to Board*

## GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur.

The Analog Devices *i*Coupler® products provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5696/AD5694 makes the part ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 43 shows a 4-channel isolated interface to the AD5696/AD5694 using the ADuM1400. For more information, visit http://www.analog.com/icouplers.

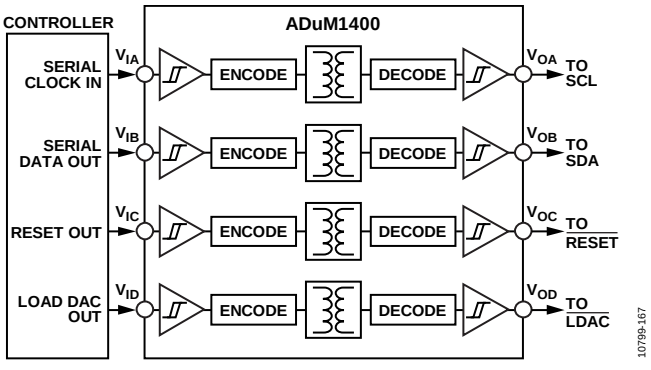
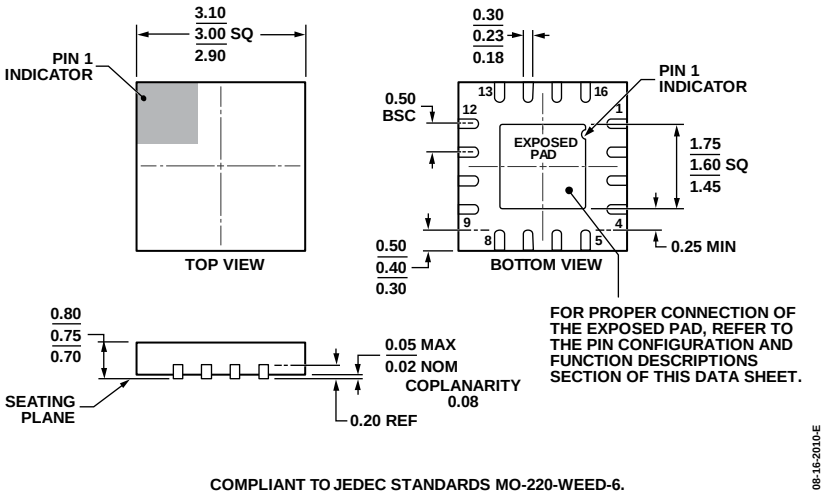


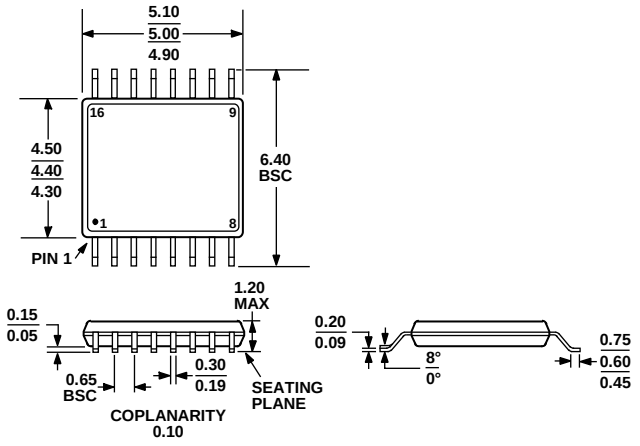

*Figure 43. Isolated Interface*

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

*Figure 44. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]*
*3 mm × 3 mm Body, Very Very Thin Quad*
*(CP-16-22)*
*Dimensions shown in millimeters*




COMPLIANT TO JEDEC STANDARDS MO-153-AB

*Figure 45. 16-Lead Thin Shrink Small Outline Package [TSSOP]*
*(RU-16)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Resolution | Temperature Range | Accuracy (INL) | Package Description | Package Option | Branding |
|---|---|---|---|---|---|---|
| AD5696ACPZ-RL7 | 16 Bits | −40°C to +105°C | ±8 LSB | 16-Lead LFCSP_WQ | CP-16-22 | DJ8 |
| AD5696BCPZ-RL7 | 16 Bits | −40°C to +105°C | ±2 LSB | 16-Lead LFCSP_WQ | CP-16-22 | DJ9 |
| AD5696ARUZ | 16 Bits | −40°C to +105°C | ±8 LSB | 16-Lead TSSOP | RU-16 | |
| AD5696ARUZ-RL7 | 16 Bits | −40°C to +105°C | ±8 LSB | 16-Lead TSSOP | RU-16 | |
| AD5696BRUZ | 16 Bits | −40°C to +105°C | ±2 LSB | 16-Lead TSSOP | RU-16 | |
| AD5696BRUZ-RL7 | 16 Bits | −40°C to +105°C | ±2 LSB | 16-Lead TSSOP | RU-16 | |
| AD5694BCPZ-RL7 | 12 Bits | −40°C to +105°C | ±1 LSB | 16-Lead LFCSP_WQ | CP-16-22 | DJQ |
| AD5694ARUZ | 12 Bits | −40°C to +105°C | ±2 LSB | 16-Lead TSSOP | RU-16 | |
| AD5694ARUZ-RL7 | 12 Bits | −40°C to +105°C | ±2 LSB | 16-Lead TSSOP | RU-16 | |
| AD5694BRUZ | 12 Bits | −40°C to +105°C | ±1 LSB | 16-Lead TSSOP | RU-16 | |
| AD5694BRUZ-RL7 | 12 Bits | −40°C to +105°C | ±1 LSB | 16-Lead TSSOP | RU-16 | |
| EVAL-AD5696RSDZ | | | | AD5696 TSSOP Evaluation Board | | |
| EVAL-AD5694RSDZ | | | | AD5694 TSSOP Evaluation Board | | |

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).


D10799-0-6/13(A)

# AMEYA360
Components Supply Platform

## Authorized Distribution Brand :

## Website :

Welcome to visit www.ameya360.com

## Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com