

TMS320DM357 ***Evaluation Module***

***Technical
Reference***

TMS320DM357 Evaluation Module Technical Reference

**511455-0001 Rev. A
December 2008**

**SPECTRUM DIGITAL, INC.
12502 Exchange Drive, Suite 440 Stafford, TX. 77477
Tel: 281.494.4505 Fax: 281.494.5310
sales@spectrumdigital.com www.spectrumdigital.com**

IMPORTANT NOTICE

Spectrum Digital, Inc. reserves the right to make changes to its products or to discontinue any product or service without notice. Customers are advised to obtain the latest version of relevant information to verify that the data being relied on is current before placing orders.

Spectrum Digital, Inc. warrants performance of its products and related software to current specifications in accordance with Spectrum Digital's standard warranty. Testing and other quality control techniques are utilized to the extent deemed necessary to support this warranty.

Please be aware that the products described herein are not intended for use in life-support appliances, devices, or systems. Spectrum Digital does not warrant nor is Spectrum Digital liable for the product described herein to be used in other than a development environment.

Spectrum Digital, Inc. assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does Spectrum Digital warrant or represent any license, either express or implied, is granted under any patent right, copyright, or other intellectual property right of Spectrum Digital, Inc. covering or relating to any combination, machine, or process in which such Digital Signal Processing development products or services might be or are used.

WARNING

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures necessary to correct this interference.

Contents

1	Introduction to the DM357 Evaluation Module	1-1
	<i>Provides you with a description of the DM357 Evaluation Module, key features, and block diagram.</i>	
1.1	Key Features	1-2
1.2	Functional Overview	1-3
1.3	Basic Operation	1-4
1.4	Memory Map	1-5
1.5	Configuration Switch Settings	1-6
1.6	Power Supply	1-7
2	Board Components	2-1
	<i>Describes the operation of the major board components on the DM357 Evaluation Module.</i>	
2.1	EMIF Interfaces	2-2
2.1.1	DDR2 Memory Interface	2-2
2.1.2	Flash, NAND Flash, SRAM Memory Interface	2-2
2.1.3	Memory Card Interface	2-2
2.1.4	UART Interface	2-3
2.1.5	EMIF Buffer/Decoder Control CPLD	2-3
2.2	Input Video Port Interfaces	2-4
2.2.1	On Chip Video Output DACs	2-4
2.2.2	AIC33 Interface	2-5
2.2.3	Audio PLL/VCXO Circuit/PLL1705 Clock Generator	2-6
2.3	Ethernet Interface	2-7
2.4	I ² C Interface	2-7
2.4.1	I/O Expanders	2-8
2.4.2	MSP430	2-9
2.5	Daughter Card Interface	2-10
2.6	DM357 Core CPU Clock	2-10
2.7	USB Clock	2-10
2.8	Battery	2-11

3	Physical Specifications	3-1
	<i>Describes the physical layout of the DM357 Evaluation Module and its connectors.</i>	
3.1	Board Layout	3-3
3.2	Connectors	3-4
3.2.1	J2, MSP430 JTAG Header	3-5
3.2.2	J3, SD/MMC Connector	3-5
3.2.3	J4, EM_CS2 Routing Connector	3-6
3.2.4	J6, External RESET Interface	3-6
3.2.5	J7, USB Host/Gadget Termination	3-7
3.2.6	J8, Video Out	3-7
3.2.7	J9, USB Capacitance Select	3-8
3.2.8	J10, MiniAB USB Connector	3-9
3.2.9	J11, Composite Video In	3-10
3.2.10	J12, RCA Jack, Video In	3-11
3.2.11	J13, 14 Pin TI JTAG Emulation Header	3-12
3.2.12	J14, +5 Volt Input	3-13
3.2.13	J15, 20 Pin ARM JTAG Emulation Header	3-13
3.2.14	J17, CPLD Programming Header	3-14
3.2.15	J18, MSP430 I/O	3-14
3.2.16	J19, I ² C Bus Expander	3-15
3.2.17	P2, Ethernet Interface	3-15
3.2.18	P3, Stereo Line In	3-16
3.2.19	P4, Headphone Out	3-17
3.2.20	P5, Stereo Line Out	3-17
3.2.21	P6, RS-232 UART	3-18
3.2.22	U3, Infrared Interface	3-19
3.3	Daughter Card Connectors	3-19
3.3.1	DC1, EMIF Expansion Connector	3-20
3.3.2	DC2, GIOV33/Ethernet Connector	3-21
3.3.3	DC3, SPI, McBSP, I ² C Connector	3-22
3.3.4	DC4, Video Input Connector	3-23
3.3.5	DC5, Video Output Connector	3-24
3.3.6	DC6, SD Interface Connector	3-25
3.3.7	DC7, Power Connector	3-25
3.4	LEDs	3-26
3.5	Switches	3-26
3.6.1	S1, EMU0/1 Select Switch	3-27
3.6.2	S3, Processor Configuration/Boot Load Options	3-28
3.6.3	S4, RESET	3-29
3.6.4	S5, User CPLD Option Switch	3-29
3.6.5	SW1, Power On/Off	3-29
3.6	Test Point Connector, JP1	3-30
3.7	Test Points	3-31
A	Schematics	A-1
	<i>Contains the schematics for the DM357 Evaluation Module</i>	
B	Mechanical Information	B-1
	<i>Contains the mechanical information about the DM357 Evaluation Module</i>	

About This Manual

This document describes the board level operations of the DM357 Evaluation Module (EVM). The EVM is based on the Texas Instruments DM357 Processor.

The DM357 Evaluation Module is a table top card that allows engineers and software developers to evaluate certain characteristics of the DM357 processor to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The DM357 Evaluation Module will sometimes be referred to as the DM357 EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

```
equations  
!rd = !strobe&rw;
```

Information About Cautions

This book may contain cautions.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes and User Guides

Information regarding TMS320DM357 technology can be found at the following Texas Instruments website:

<http://www.ti.com>

Table 1: Manual History

Revision	History
A	Alpha Release

Table 2: Board History

PWB Revision	History
A	Alpha Release

Chapter 1

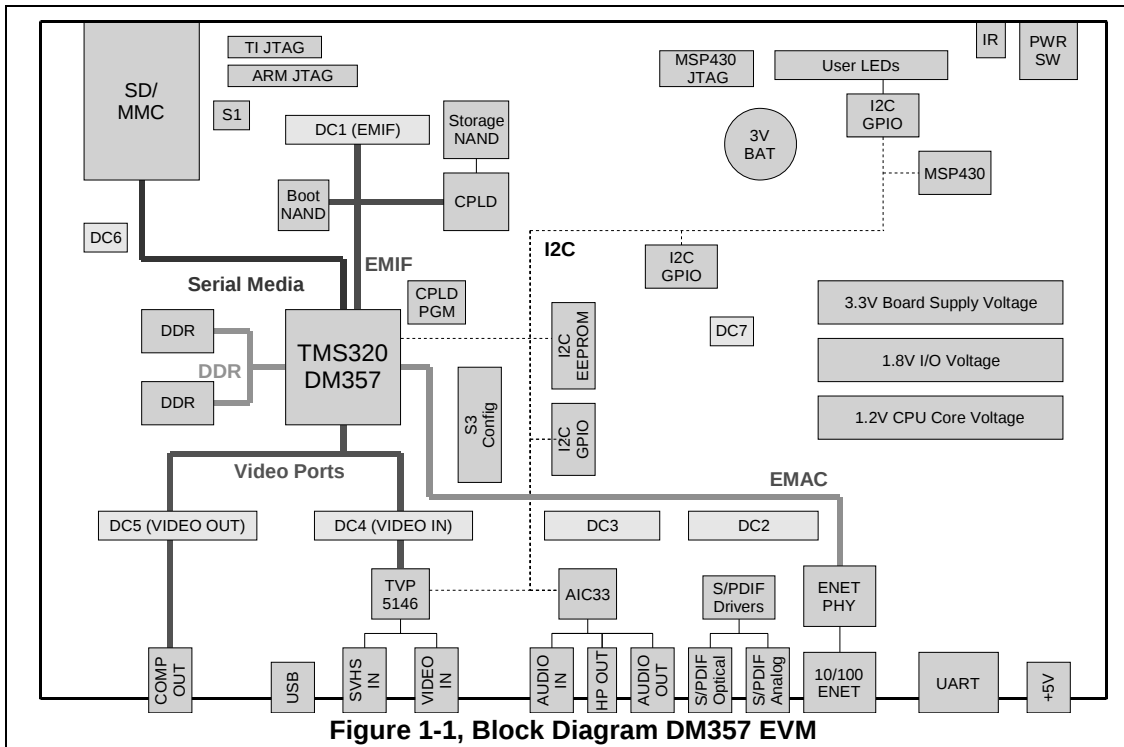
Introduction to the DM357 EVM

Chapter One provides a description of the DM357 EVM along with the key features and a block diagram of the circuit board.

Topic		Page
1.1	Key Features	1-2
1.2	Functional Overview	1-3
1.3	Basic Operation	1-4
1.4	Memory Map	1-5
1.5	Configuration Switch Settings	1-6
1.6	Power Supply	1-7

1.1 Key Features

The DM357 EVM is a standalone development platform that enables users to evaluate and develop applications for the TI DM357 processor. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.



The EVM comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments DM357 processor with an ARM processor operating up to 270 Mhz. and H.264/MPEG4/JPEG coprocessor
- 1 video input port, supports composite or S video
- 1 video DAC outputs - composite
- 256 Mbytes of DDR2 DRAM
- UART, Media interface (SD card, MMC)
- 64 Mbytes NAND Flash for BOOT, 2 gigabyte NAND storage NAND
- AIC33 stereo codec
- USB2 Interface

- 10/100 MBS Ethernet Interface
- IR Remote Interface, real time clock, via MSP430
- Configurable boot load options
- JTAG emulation interface with 1.8 volt to 3.3 volt translators
- 8 user LEDs
- Single voltage power supply (+5V)
- Expansion connectors for daughter card use

1.2 Functional Overview of the DM357 EVM

The DM357 on the EVM interfaces to on-board peripherals through the 16-bit wide EMIF peripheral interface pins. The DDR2 memory is connected to its own dedicated 32 bit wide bus. The EMIF bus is also connected to the boot NAND, storage NAND, and daughter card expansion connectors which are used for add-in boards.

On board video decoder for composite or s-video and on chip encoders interface video streams to the DM357 processor. One decoder and 1 on chip DAC channel for composite out are standard on the EVM. On screen display functions are implemented in software on the DM357 processor.

An on-board AIC33 codec allows the CPU to transmit and receive analog audio signals. The I²C bus is used for the codec control interface, while the McBSP controls the audio stream. Signal interfacing is done through 3.5mm audio jacks that correspond to microphone input, line input, and line output. The codec can select the line input as the active input.

The EVM includes 8 LEDs, IR interface, and Real time clock which can be used to provide the user with interactive feedback. These interfaces are implemented via software on a MSP430 and are accessed by reading and writing to the I²C registers.

SD/MMC Media card and ethernet MAC interfaces are integrated peripheral on the DM357 processor exploiting its system on a chip architecture.

An included 5V external power supply is used to power the board. On-board switching voltage regulators provide the +1.2V CPU core voltage and +3.3V for peripherals and +1.8V memory and DM357 I/O. The board is held in reset until these supplies are within operating specifications.

Code Composer Studio communicates with the EVM through an external emulator via the 14 TI or 20 pin ARM external JTAG connector.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio IDE™, or standard GDB tool environments. Code Composer communicates with the board through an external JTAG emulator.

Detailed information about the EVM including examples and reference material is available on the EVM's CD-ROM.

1.4 Memory Map

The DM357 processor has a large byte addressable address space. However, some limitations to byte addressing may be present depending on the board to device peripheral interconnection. Program code and data can be placed anywhere in the unified address space. Addresses are multiple sizes depending on hardware implementation. Refer to the appropriate device data sheets for more details.

The memory map shows the address space of a DM357 processor on the left with specific details of how each region is used on the right.

The part incorporates a dual EMIF interface. One dedicated EMIF directly interfaces to the DDR2 memory. The other EMIF has 4 separate addressable regions called chip enable spaces (CE2-CE5). The boot NAND Flash, or daughter card are mapped into CE2 space and selectable via J4. Daughter cards use CE2 and CE3. When CE2 is used for daughter card interfacing J4 must be set appropriately. CE4 is used to interface to storage NAND.

Address	Generic DaVinci Address Space	DM357 EVM
0x00000000	ARM Instruction RAM	ARM Instruction RAM
0x00040000	ARM Data RAM	ARM Data RAM
0x02000000	AEMIF CE2	BootNAND
0x04000000	AEMIF CE3	DC
0x06000000	AEMIF CE4	Storage NAND
0x08000000	AEMIF CE5	Reserved
0x80000000	DDR	DDR

Figure 1-2, Memory Map, DM357 EVM

1.5 Configuration Switch Settings

The EVM has a single 10 position configuration switch that allow users to control the operational state of the processor when it is released from reset. The configuration switch is labeled S3 on the EVM board.

Switch S3 configures the boot mode that will be used when the processor starts executing. By default the switches are configured to EMIF boot (out of 8-bit NAND Flash) in little endian mode. The settings for switch S3 in chapter 3.

1.6 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J14), a 2.5 MM. barrel-type plug. Internally, the +5V input is converted into +1.2V, +1.8V and +3.3V using Texas Instruments swift voltage regulators. The +1.2V supply is used for the CPU core while the +3.3V supply is used for the CPU's I/O buffers and other chips on the board. The +1.8 volt supply is used for DM357 I/O, low voltage memory, and peripherals, and DDR2 memory.

There are four power test points on the EVM; TP14, TP25, TP26, and TP43. These test points provide a convenient mechanism to check the EVM's multiple power supplies. The table below shows the voltages for each test point and what the supply is used for.

Table 1: Power Test Points

Test Point	Voltage	Voltage Use
TP43	+1.2 V	DM357 Core
TP25	+1.2 V	DM357 Core/Power Down
TP26	+1.8 V	DDR2 Memory, CPU I/O, and logic
TP14	+3.3V	CPU I/O and logic

Chapter 2

Board Components

This chapter describes the operation of the major board components on the DM357 EVM.

Topic	Page
2.1 EMIF Interfaces	2-2
2.1.1 DDR2 Memory Interface	2-2
2.1.2 NAND Flash Interface	2-2
2.1.3 Storage NAND Interface	2-2
2.1.4 Memory Card Interface	2-2
2.1.5 UART Interface	2-3
2.1.6 EMIF Buffer/Decoder Control CPLD	2-3
2.2 Input Video Port Interfaces	2-4
2.2.1 On Chip Video Output DACs	2-4
2.2.2 AIC33 Interface	2-5
2.2.3 Audio PLL/VCXO Circuit/PLL1705 Clock Generator	2-6
2.3 Ethernet Interface	2-7
2.4 I ² C Interface	2-7
2.4.1 I/O Expanders	2-8
2.4.2 MSP430	2-9
2.5 Daughter Card Interface	2-10
2.6 DM357 Core CPU Clock	2-10
2.7 USB Clock	2-10
2.8 Battery	2-11

2.1 EMIF Interfaces

A separate 16 bit EMIF with four chip enables divide up the address space and allow for asynchronous accesses on the EVM. The EVM has a dedicated chip enables. CE2 is used for the boot NAND Flash. Both CE2 and/or CE3 can be routed to the daughter card interface connectors. CE4 is used for storage NAND flash.

Table 1: EMIF Interfaces

Chip Select	Function
CE2	Boot NAND Flash (see JP4 definition)
CE2	Daughter Card Interface (see JP4 definition)
CE3	Daughter Card Interface
CE4	Storage NAND Flash
CE5	Reserved

2.1.1 DDR2 Memory Interface

The DM357 device incorporates a dedicated 32 bit wide DDR2 memory bus. The EVM uses two gigabit 16 bit wide memories on this bus, for a total of 256 megabytes of memory for program, data, and video storage. The internal DDR controller uses a PLL to control the DDR memory timing. The interface supports rates up to 166 Mhz., and is clocked on differential edges for optimal performance. Memory refresh for DDR2 is handled automatically by the DM357 internal DDR controller.

2.1.2 Boot NAND Flash Interface

The DM357 has 64 megabytes of Boot NAND Flash mapped into the CE2 space. This NAND Flash memory is used for boot loading. The CE2 space is configured as 8 bit wide for NAND flash usage.

2.1.3 Storage NAND Interface

The EVM interfaces to 2 gigabytes of storage NAND flash mapped to CE4 space. CE4 is configured to 8 bit wide access for storage NAND. The CPLD incorporates 1.8 to 3.3 volt level translators to interface to the NAND.

2.1.4 Memory Card Interface

The EVM supports MMC/SD media cards via the on chip controller.

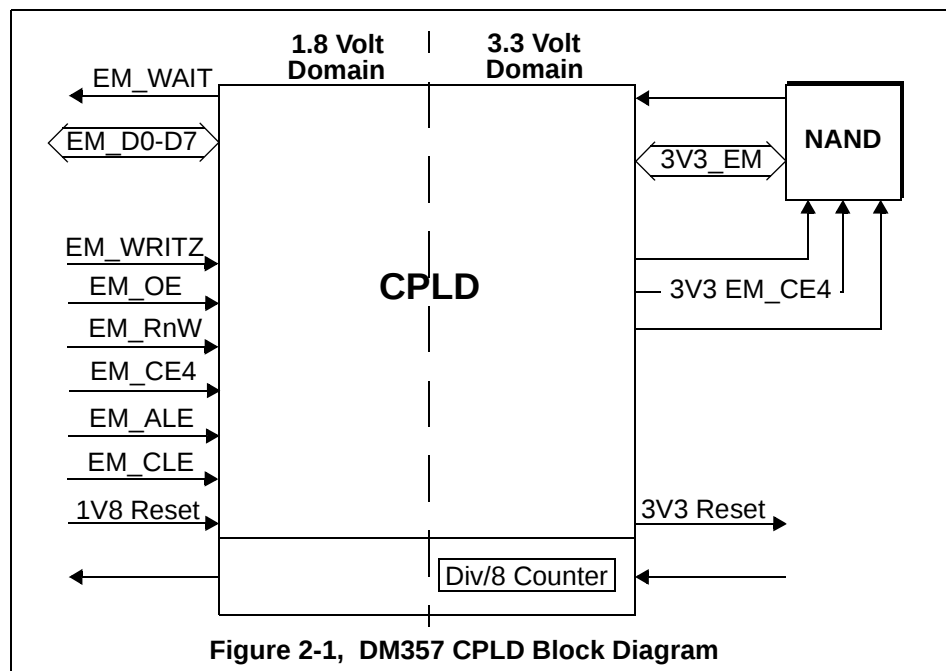
2.1.5 UART Interface

The internal UART0 on the DM357 device is driven to connector J6. The UART's interface is level shifted and routed to the RS-232 line drivers prior to being brought out to a DB-9 connector, J6.

2.1.6 EMIF Buffer/Decoder Control CPLD

The EMIF buffer and decode functions are implemented with a CPLD. The EVM board incorporates an Altera MAX II EPM240TCG100 device. The device has 2 banks of I/O. One bank is used for +1.8 volt signals. The other bank is for +3.3 volt signals. This allows the device to do level shifting.

The CPLD incorporates the storage NAND level translators and decode interface along with a divide by 8 counter for video synchronization. The CPLD also incorporates various glue logic for the EVM.



2.2 Input Video Port Interfaces

The DM357 EVM supports video capture via the devices internal video ports. A Texas Instruments TVP5146 is used to decode composite video or S-video inputs into the device after being level shifted. J11 is used for the S-video inputs and J12 for the composite inputs on the EVM.

User inputs can be driven via daughter card connector DC4 when the on board level translator is tristate via driving control Capture Enable signal high on DC4.

2.2.1 On Chip Video Output DACs

The DM357 incorporates 1 output DAC to interface to composite video. The DAC is buffered via opamps and driven to connector, J8.

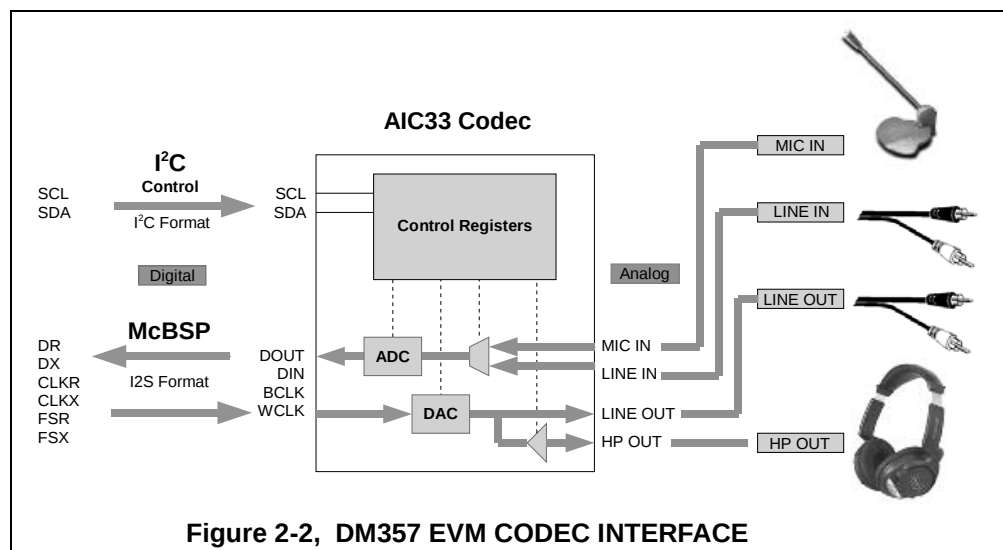
2.2.2 AIC33 Interface

The EVM uses a Texas Instruments TLV320AIC33 stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the CPU. When the processor is finished with the data it uses the codec to convert the samples back into analog signals on the line output so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I²C bus is used as the unidirectional control channel. The control channel is generally only used when configuring the codec, it is typically idle when audio data is being transmitted,

The McBSP is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the processor side.

The codec has a programmable clock from a PLL1705 PLL device. The internal sample rate generator subdivides the default system clock to generate common audio frequencies. The sample rate is set by a codec register. The figure below shows the codec interface on the DM357 EVM.



2.2.3 Audio PLL/VCXO Circuit/PLL1705 Clock Generator

The DM357 EVM implements a multiple PLL clock generator for creating the Audio clocks for the board.

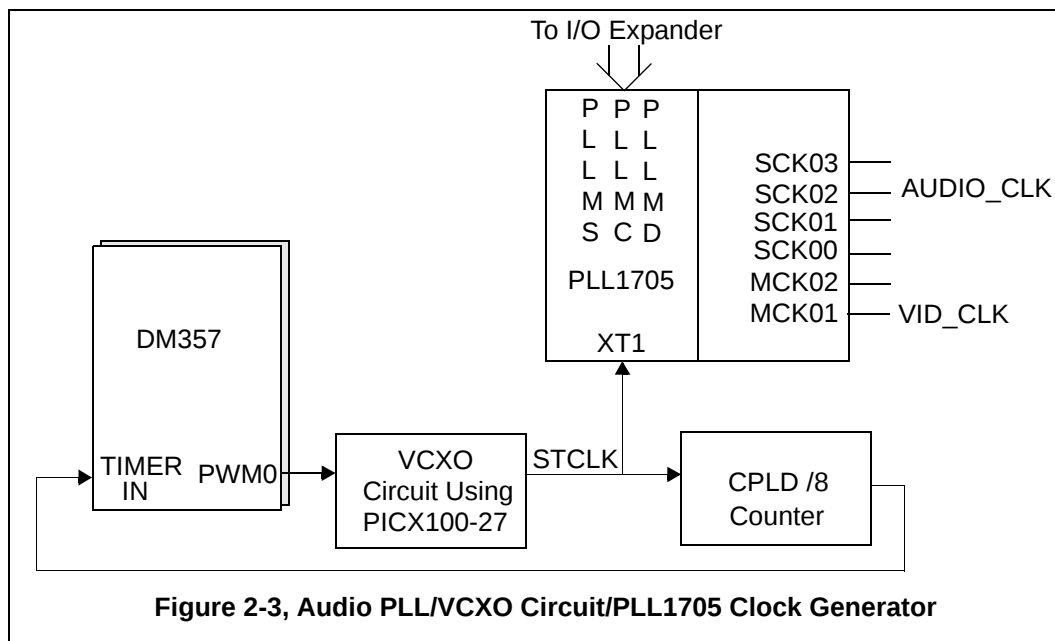
In streaming video applications the audio and video sequences can lose synchronization. The DM357 uses a VCXO interpolation circuit to incrementally speed up or slow down the STCLK input to allow for this synchronization to remain locked.

The PWM0 and timer inputs on DM357 are used to control this feature. The PWM0 pin drives a PICX100-27W Voltage Controlled Oscillator which is divided by 8 in the CPLD and fed back into the timer input pin.

The STCLK is also a source clock for the PLL1705 programmable PLL device. This device creates the clocks for the AIC33 Codec, daughter card VIDCLK an AUDIOCLK.

The PLL1705 is programmable via an I²C and Expander U18. Software sequencing on the I/O expander is required to interface correctly to the PLL1705's programmable inputs.

The diagram below is a simplified diagram of this clocking scheme.



2.3 Ethernet Interface

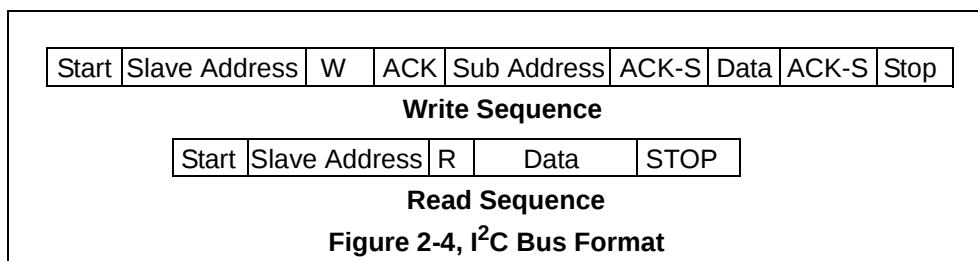
The DM357 integrates an ethernet MAC on chip. This interface is routed to the PHY via CBT switches. The EVM uses an Intel LXT971 PHY. The 10/100 Mbit interface is isolated and brought out to a RJ-45 standard ethernet connector, P2. The PHY directly interfaces to the DM357. The ethernet address is stored in the I²C serial ROM during manufacturing.

The RJ-45 has 2 LEDs integrated into its connector. The LEDs are green and yellow and indicate the status of the ethernet link. The green LED, when on, indicates link and when blinking indicates link activity. The yellow LED, when illuminated, indicates full duplex mode.

When configuring the PHY use the high drive option in the PHY register 26 to compensate for the routing length and extra capacitance of the CBT switches.

2.4 I²C Interface

The I²C bus on the DM357 is ideal for interfacing to the control registers of many devices. On the DM357 EVM the I²C bus is used to configure the video decoder, stereo Codec, I/O expanders, and communicate with the MSP430. An I²C ROM is also interfaced via the serial bus. The format of the bus is shown in the figure below.



The addresses of the on board peripherals are shown in the table below.

Table 2: I²C Memory Map

Device	Address	R/W	Function
TVP5146	0x5D	R/W	Capture 1 Decoder
PCF 8574A	0x38	R/W	LEDs
PCF 8574A	0x39	R/W	PLL/User Switch
PCF 8574A	0x3A	R/W	Peripheral Selects
TLV320AIC33	0x1B	R/W	CODEC
24WC256	0x50	R/W	I ² C EEPROM
MSP430	0x23	R/W	LEDs, IR, RTC

2.4.1 I/O Expanders

The DM357 EVM uses three I²C expanders to handle various bit I/O functions. Each of these is an bit I/O expander, a PCF8574A. At Power Up Reset the expanders are initialized to 0xFF, all ones. The functions for each of the I/O expanders are shown in the tables below.

Table 3: U2, I/O Expander

Pin Number	Function	States
P0	User LED DS8	0 = Turns LED On, 1 = Turns LED Off
P1	User LED DS7	0 = Turns LED On, 1 = Turns LED Off
P2	User LED DS6	0 = Turns LED On, 1 = Turns LED Off
P3	User LED DS5	0 = Turns LED On, 1 = Turns LED Off
P4	User LED DS4	0 = Turns LED On, 1 = Turns LED Off
P5	User LED DS3	0 = Turns LED On, 1 = Turns LED Off
P6	User LED DS2	0 = Turns LED On, 1 = Turns LED Off
P7	User LED DS1	0 = Turns LED On, 1 = Turns LED Off

Table 4: U18, I/O Expander

Pin Number	Function
P0	PLL Program Interface, PLL CSEL Pin
P1	PLL Program Interface, PLL SR Pin
P2	PLL Program Interface, PLL FS1 Pin
P3	PLL Program Interface, PLL FS2 Pin
P4	Spare IO1
P5	Spare IO2
P6	Spare IO3
P7	User DIP Switch *

* - useful as input only

High Input - Switch in "ON" Position

Low Input - Switch in "OFF" Position

Table 5: U35, I/O Expander

Pin Number	Function	State
P0	Reserved	
P1	VDD IMX Enable	0 = Disables VDDIMX supply
P2	Reserved	
P3	Reserved	
P4	Reserved	
P5	Reserved	
P6	Reserved	
P7	Reserved	

2.4.2 MSP430

The DM357 EVM incorporates infrared remote, real time clock, and some bit I/O in a MSP430 microcontroller. The I²C interface is used on the DM357 processor to communicate to the MSP430. The MSP430 acts as a slave device on the I²C bus.

2.5 Daughter Card Interfaces

The EVM provides expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for all major interfaces including memory, peripherals, and video expansion.

Spectrum Digital produces the THS8200 daughter card (part # 7xxxxx) which plugs onto the connector.

The pin outs for this interface are documented in Section 3.

The memory connector provides access to the CPU's EMIF signals to interface with memories and memory mapped devices.

The video capture port is brought out to the daughter card interface. Four signals are used to disable the on board video peripherals so that they can be used by the expansion connector. The table below indicates the operation of these signals.

Table 6: Daughter Card Video Enable

Signal	State To Enable Daughter Card Use	DM357 Signals Enables
CAPTURE_EN	1	DC4 YI0-YI7 PCLK,VD,HD
McBSP_EN	1	DC3 McBSP
ENET_ENABLE	1	DC2 GIOV33 pins

Other than the buffering, most daughter card signals are not modified on the board.

2.6 DM357 Core CPU Clock

The DM357 EVM uses a 27 Megahertz crystal to generate the input clock. The DM357 has an internal PLL which can multiply the input clock to generate the internal clock. The PLL multiplier is set via software on the DM357 device.

2.7 USB Clock

The DM357 EVM uses a 24 Mhz crystal for the USB II clock generator. The USB controller is completely integrated in the DM357 device.

2.8 Battery

The DM357 EVM incorporates a battery holder to provide backup power to the MSP430's real time clock when the power is not applied to the board. The optional battery should be +3 volt 20 millimeter coin type Lithium single cell.

Some common part numbers for batteries which should operate in the EVM are shown in the table below.

Table 7: Battery Part Numbers

Part Numbers
CR2032
DL2032
BR2032
CR2025
BR2025
CR2016
BR2016
DL2016

These batteries are available from Duracell, Eveready, Panasonic, Ray-O-Vac, Sanyo, Sony, Sieko, Toshiba, Varta, and other battery manufacturers.

Chapter 3

Physical Description

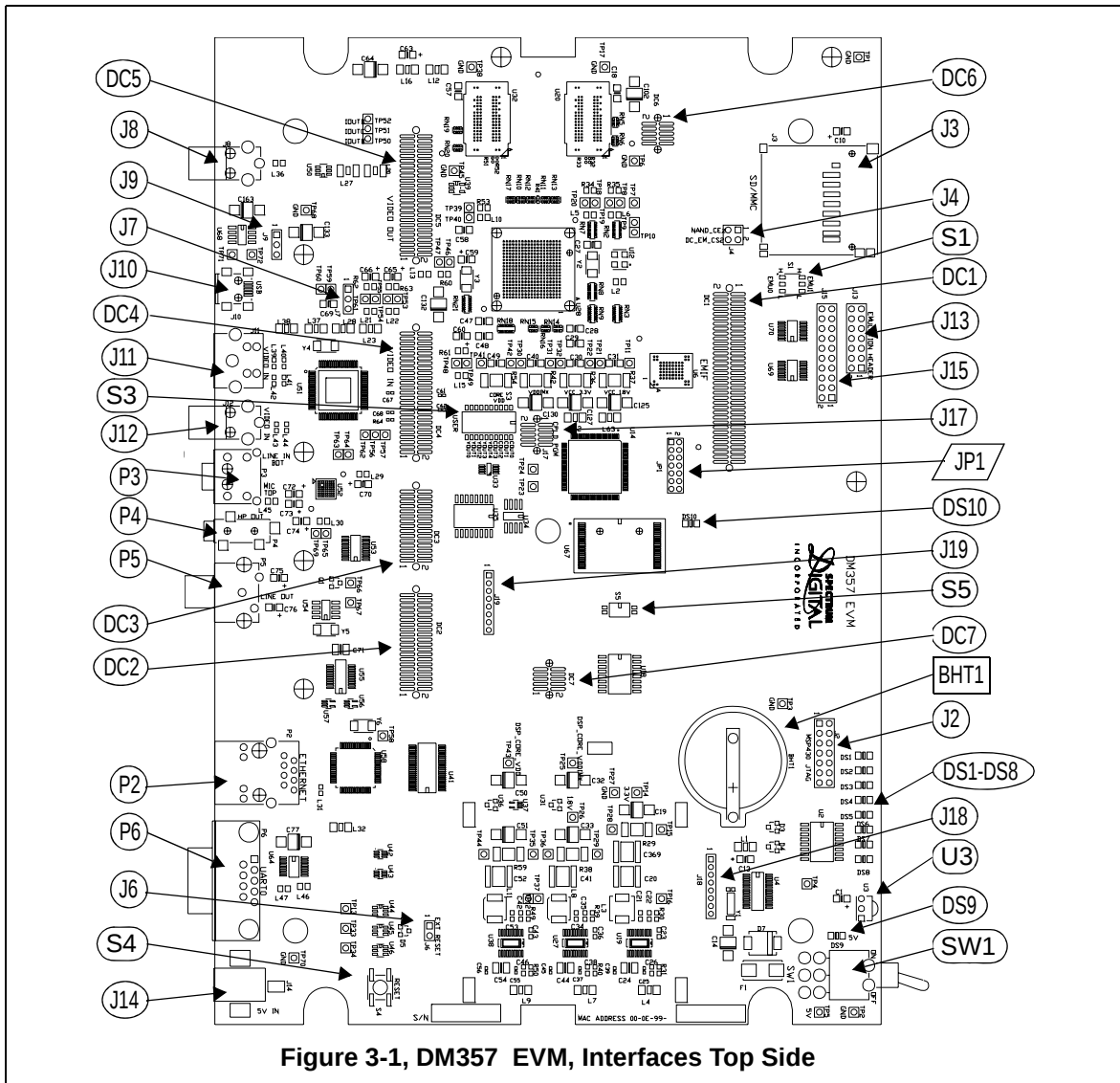
This chapter describes the physical layout of the DM357 EVM and its interfaces.

Topic	Page
3.1 Board Layout	3-3
3.2 Connectors	3-4
3.2.1 J2, MSP430 JTAG Header	3-5
3.2.2 J3, SD/MMC Connector	3-5
3.2.3 J4, EM_CS2 Routing Connector	3-6
3.2.4 J6, External RESET Interface	3-6
3.2.5 J7, USB Host/Gadget Termination	3-7
3.2.6 J8, Video Out	3-7
3.2.7 J9, USB Capacitance Select	3-8
3.2.8 J10, MiniAB USB Connector	3-9
3.2.9 J11, Composite Video In	3-10
3.2.10 J12, RCA Jack, Video In	3-11
3.2.11 J13, 14 Pin TI JTAG Emulation Header	3-12
3.2.12 J14, +5 Volt Input	3-13
3.2.13 J15, 20 Pin ARM JTAG Emulation Header	3-13
3.2.14 J17, CPLD Programming Header	3-14
3.2.15 J18, MSP430 I/O	3-14
3.2.16 J19, I ² C Bus Expander	3-15
3.2.17 P2, Ethernet Interface	3-15
3.2.18 P3, Stereo Line In	3-16
3.2.19 P4, Headphone Out	3-17
3.2.20 P5, Stereo Line Out	3-17
3.2.21 P6, RS-232 UART	3-18
3.2.22 U3, Infrared Interface	3-19

Topic	Page
3.3 Daughter Card Connectors	3-19
3.3.1 DC1, EMIF Expansion Connector	3-20
3.3.2 DC2, EMAC/GIO Connector	3-21
3.3.3 DC3, McBSP/SPI Expansion	3-22
3.3.4 DC4, Video Input expansion	3-23
3.3.5 DC5, Video Output Expansion	3-24
3.3.6 DC6, SD Interface Expansion	3-25
3.3.7 DC7, Power Expansion	3-25
3.4 LEDs	3-26
3.5 Switches	3-26
3.5.1 S1, EMU0/1 Select Switch	3-27
3.5.2 S3, Processor Configuration/Boot Load Options	3-28
3.5.3 S4, RESET	3-29
3.5.4 S5, User CPLD Option Switch	3-29
3.5.5 SW1, Power On/Off	3-29
3.6 Test Point Connector, JP1	3-30
3.7 Test Points	3-31

3.1 Board Layout

The DM357 EVM is a 6.75 x 10.0 inch (171 x 254 mm.) ten (10) layer printed circuit board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the DM357 EVM.



3.2 Connectors

The EVM has twenty-nine (29) connectors or interfaces to various peripherals. These connectors are described in the following sections.

Table 1: Connectors

Connector	Size	Function
J2	2 x 7	MSP430 JTAG
J3	24	SD/MMC
J4	2 x 2	EM_CS2 Routing
J6	2	External RESET Input
J7	2	USB Host/Client Termination
J8	RCA	Video Out
J9	1 x 3	USB Capacitance Select
J10	4	MiniAB USB
J11	4 Pin DIN	Composite Video In
J12	RCA	Video In
J13	2 x 7	14 Pin TI Emulation Header
J14	2.5 mm	+5 Volt Input
J15	2 x 10	20 Pin ARM Emulation Header
J17	5 x 2	CPLD Programming Header (Factory Use)
J18	1 x 8, 2mm	MSP430 I/O
J19	1 x 8, 2mm	I/O Header
P2	RJ-45	Ethernet
P3	Dual RCA	Stereo Line In
P4	3.5 mm	Headphone Out
P5	Dual RCA	Stereo Line Out
P6	9	RS-232 UART
DC1	2 x 35	EMIF Expansion
DC2	2 x 20	EMAC/GIO Expansion
DC3	2 x 15	McBSP/SPI Expansion
DC4	2 x 25	Video Input Expansion
DC5	2 x 25	Video Output Expansion
DC6	2 x 5	SD Expansion
DC7	2 x 5	Voltage Expansion
U3		IR Interface

3.2.1 J2, MSP430 JTAG Header

The J2, MSP430 JTAG header, is used to provide a programming interface to the MSP430 microcontroller. The pinout for the J2 connector is shown in the table below.

Table 2: J2, MSP430 JTAG Header

Pin #	Signal	Pin #	Signal
1	430_TDO	2	NC
3	430_TDI	4	MSP430_3V3
5	430_TMS	6	NC
7	430_TCK	8	430_TEST/VPP
9	GND	10	NC
11	NC	12	NC
13	NC	14	NC

3.2.2 J3, SD/MMC Connector

The J3 SD/MMC connector is used to provide an interface to a SD/MMC card. The pinout for the J3 connector is shown in the table below.

Table 3: J3, SD/MMC Connector

Pin #	Signal	Pin #	Signal
1	SD_DATA3	2	SD_CMD
3	GND	4	VCC_3.3V
5	SD_CLK	6	GND
7	SD_DATA0	8	SD_DATA1
9	SD_DATA2	10	GND

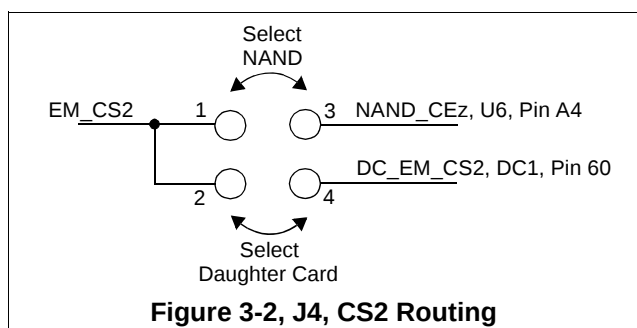
3.2.3 J4, EM_CS2 Routing Connector

The J4 connector is actually a 4 position jumper that is used to select the type of memory that the EM_CS2 signal is routed to. The EM_CS2 can be routed to either of the two signals shown in the figure below. Only one (1) device can be selected at a time. To reconfigure this signal, power down the EVM, change the jumper, and then power the board back up. Do **NOT** change this jumper with the power on. The pin outs are shown in the table below.

Table 4: J4, EM_CS2 Routing Connector

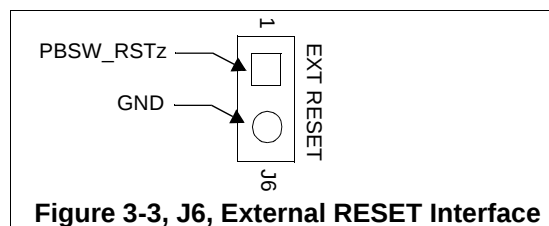
Pin #	Signal	Pin #	Signal
1	EM_CS2	3	NAND_CEx
2	EM_CS2	4	DC_EM_CS2

The figure below shows the two possible selections.



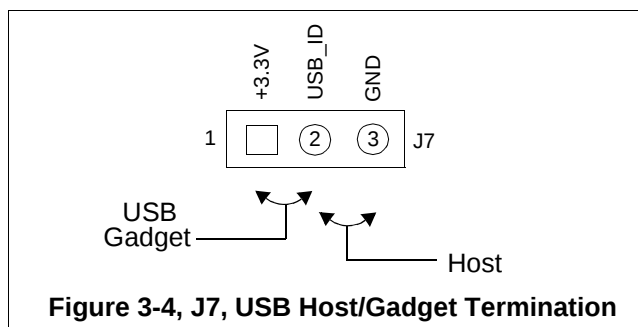
3.2.4 J6, External RESET Interface

The J6 connector is a 2 position jumper is used to externally reset the board. This connector is unpopulated as shipped from the factory. This circuitry parallels the RESET switch, S4. The figure below represents this connector.



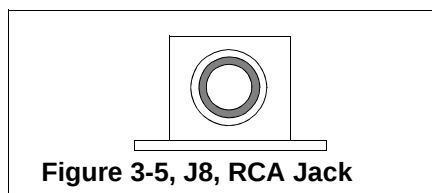
3.2.5 J7, USB Host/Gadget Termination

The J7 connector is a 3 position jumper that is used to select the termination for the USB host/gadget configuration on USB connector J10. Either the +3.3V (1-2 position) for USB Gadget or Ground (2-3 position) for Host must be selected to properly enable the mode of operation on the DM357 USB controller. To reconfigure this termination, power down the EVM, change the jumper, and then power the board back up. Do **NOT** change this jumper with the power on. The figure below shows the signals on this connector.



3.2.6 J8, Video Out

The J8 connector is an RCA jack providing 1 DAC output. Do **NOT** plug into these connectors with the power on. This connector is driven by the signal DAC_IOUTA through the op-amp U50. The figure below shows this connector as viewed from the card edge.



3.2.7 J9, USB Capacitance Select

The J9 jumper is a 3 position jumper header of which only pins 1 and 2 are used. This jumper is used to provide more capacitance when the USB connector is used in the host mode. When the jumper is shorted the extra capacitance is provided. These open and shorted position are shown below.

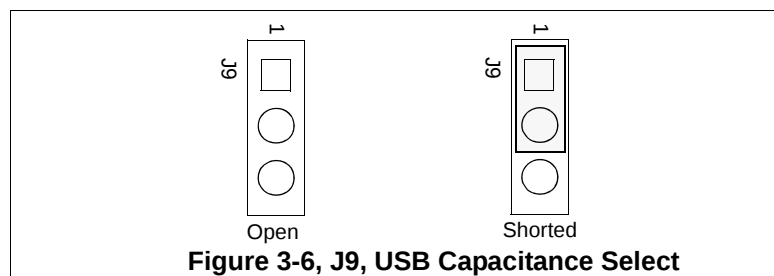


Table 5: J9, USB Capacitance Select

Position	Function
Open	6.8 uF Capacitance
Shorted	106.8 uF Capacitance

3.2.8 J10, MiniAB USB Connector

Connector J10 is a mini A/B USB connector. The pinout for the J10 connector is shown in the table below.

Table 6: J10, MiniAB USB Connector

Pins	Signal
1	USB_VBUS_CONN
2	USB_DM
3	USB_DP
4	USB_ID
5-9	USB_SHIELD/GND

The EVM incorporates the ability to toggle the ID pin on the USB connector via software control. The USB_ID pin on the DM357 controls this function.

For “USB ON The Go” mode remove header J7. This will allow the cable to configure the ID pin on the DM357 processor.

The EVM supplies up to 500 mA of current to the USB_VBUS via a TPS2065D DC/DC converter. This is enabled via the DM357's DRV_VBUS pin. J9 supplies extra capacitance for host mode operations.

3.2.9 J11, Composite Video In

Connector J11 is a four pin mini-din connector which interfaces to the TVP5146 encoder. This connector brings in a video signal (LUMA) to pin 9 on the TVP5146. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

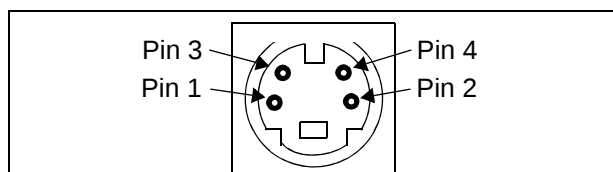


Figure 3-7, J11, Front View, Mini-Din Connector

Table 7: J11, Video In, Mini-Din Connector

Pin #	Signal Name
1	GND
2	GND
3	LUMA
4	Chroma

3.2.10 J12, RCA Jack, Video In

J13 is an RCA jack used as the CVBS/Y input to the TVP5146. The figure below shows this connector as viewed from the card edge.

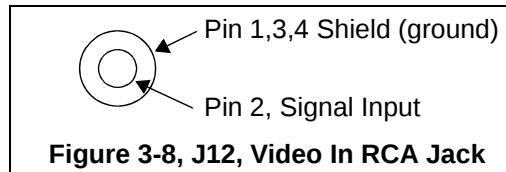


Table 8: J12, Video In RCA Jack

Pin #	Signal Name
1	DEC_GND
2	VI_2_B, U51, Pin 8, TVP5146
3	DEC_GND
2	DEC_GND

3.2.11 J13, 14 Pin TI JTAG Emulation Header

Connector J13 is a 2 x 7 double row male header with pin 6 clipped to serve as a key. This is the standard interface used by JTAG emulators to interface to Texas Instruments processors. The pinout for the connector is shown in the figure below.

TMS	1	2	TRST-	Header Dimensions
TDI	3	4	GND	
PD (+3.3V)	5	6	no pin (key)	
TDO	7	8	GND	
TCK-RET	9	10	GND	Pin-to-Pin spacing, 0.100 in. (X,Y)
TCK	11	12	GND	Pin width, 0.025-in. square post
EMU0	13	14	EMU1	Pin length, 0.235-in. nominal

Figure 3-9, J13, 14 Pin External JTAG Connector

The signal names for each pin are shown in the table below.

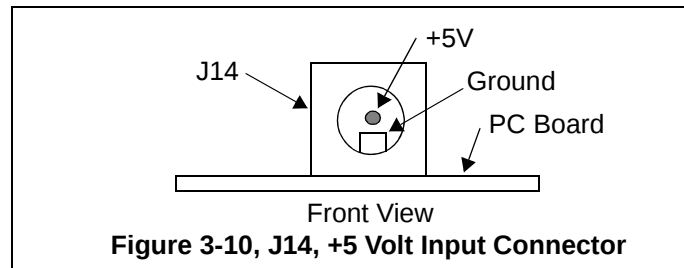
Table 9: J13, 14 Pin External JTAG Connector

Pin #	Signal Name	Pin #	Signal Name
1	TI TMS	2	TI TRSTn
3	TI TDI	4	GND
5	TI PWR DECT	6	no pin - key
7	TI TDO	8	GND
9	TI TCK RET	10	GND
11	TI TCK	12	GND
13	TI EMU0	14	TI EMU1

* **Note:** EMU0/EMU1 mode must be selected to ICEPICK mode

3.2.12 J14, +5 Volt Input

Connector J14 is the input power connector. This connector brings in +5 volts to the EVM. This is a 2.5mm. jack. Inside of the jack is tied to On/Off power switch SW1. The other side is tied to ground and LED DS9. The figure below shows this connector as viewed from the card edge.



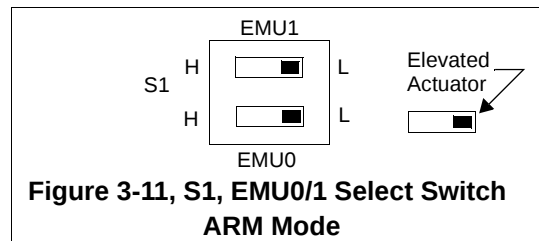
3.2.13 J15, 20 Pin ARM JTAG Emulation Header

The J15 emulation header is used to provide an interface to generic ARM9 JTAG emulators. The pinout for this connector is shown in the table below.

Table 10: J15, 20 Pin ARM JTAG Emulation Header

Pin #	Signal	Pin #	Signal
1	VCC_3V3	2	VCC_3V3
3	ARM_TRSTn	4	Ground
5	ARM_TDI	6	Ground
7	ARM_TMS	8	Ground
9	ARM_TCK	10	Ground
11	ARM_TCKRET	12	Ground
13	ARM_TDO	14	Ground
15	ARM_RSTn	16	Ground
17	NC	18	Ground
19	NC	20	Ground

Note: EMU0/EMU1 switch, S1, must be set to ARM mode. This is shown in the figure below. See section 3.5.1 for more details.



3.2.14 J17, CPLD Programming Header

Connector J17 is a 10 pin header that provides a programming interface to the FPGA, U14. Do **NOT** plug into this connector with the power on. The table below shows the signals on this connector. This connector is for factory use only. Reprogramming this CPLD affects the functionality of your EVM.

Table 11: J17, CPLD Programming Header

Pin #	Signal	Pin #	Signal
1	ISR_TCK	2	GND
3	ISR_TDO	4	VCC_1.8V
5	ISR_TMS	6	NC
7	NC	8	NC
9	ISR_TDI	10	GND

3.2.15 J18, MSP430 I/O

Connector J18 brings out the I/O lines from the MSP430. These lines are pulled up to +3.3 volts through RN22. The signals on this connector are shown in the table below.

Table 12: J18, MSP430 I/O

Pin #	Signal
1	P2.2/CAOUT/TA0
2	P2.3/CA0/TA1
3	P2.4/CA1/TA2
4	P3.0/STE0/A5
5	P3.1/SIMO0
6	P3.2/SOMI0
7	P3.3/UCLK0
8	P3.7/A7

3.2.16 J19, I²C Bus Expander

Connector J19 brings out the lines from U35, PCF8574A, the remote 8 bit expander for the I²C bus. The signals on this connector are shown in the table below.

Table 13: J18, I²C Bus Expander

Pin #	Signal
1	PIO 0, U35, Pin 4
2	VDDIMX EN, U35, Pin 5
3	PIO 2, U35, Pin 6
4	PIO 3, U35, Pin 7
5	PIO 4, U35, Pin 9
6	PIO 5, U35, Pin 10
7	PIO 6, U35, Pin 11
8	PIO 7, U35, Pin 12

3.2.17 P2, Ethernet

The P2 connector is used to provide an Ethernet interface. P2 integrates the magnetics and standard RJ-45 connector. The two tables below show the signals present on the magnetics interface and the connector side.

Table 14: P2, Magnetics/LEDs Interface Signals

Pin #	Signal	Pin #	Signal
1	TX+, U58, Pin 19	2	TX-, U58, Pin 20
3	RX+, U58, Pin 23	4	TXD-CT, U58, Pin 22
5	RXD-CT, NC	6	RXD-, U58, Pin 24
7	NC1	8	GND
9	LED1+	10	LED1-
11	LED2+	12	LED2-

3.2.18 P3, Dual Stereo Line In

The P3 connector provides a stereo input (lower) and microphone input (upper) to the TVL320AIC331 on the EVM. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.

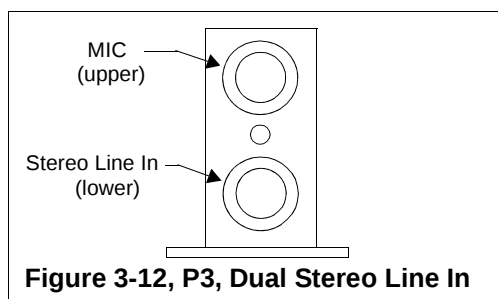


Table 15: P3, Dual Stereo Line In

Pin #	Signal	Input
1	Isolated Ground	Mic
2	MIC3L/MIC3R, U52, Pins A1,B3	Mic
3	MIC3L/MIC3R, U52, Pins A1,B3	Mic
4	Isolated Ground	Line In
5	LINE1R+/LINE2R+, U52, Pins B4,B7	Line In
6	LINE1L+/LINE2L+, U52, Pins A4,A6	Line In

3.2.19 P4, Headphone Out

The P4 connector is a 3.5 mm. stereo headphone output from the TVL320AIC331ZQE, U52, on the EVM. A view of the connector from the card edge is shown in the figure below.

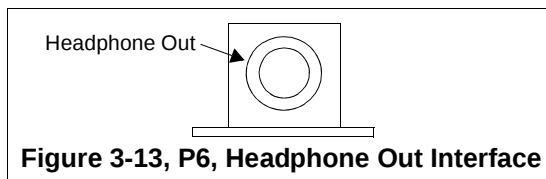


Figure 3-13, P4, Headphone Out Interface

The signals present on this connector are defined in the following table.

Table 16: P4, Headphone Out Interface

Pin #	AIC331 Signal
1	GND
2	HPLOUT, U52, Pin D1
3	HPROUT, U52, Pin G1
4	NC

3.2.20 P5, Stereo Line Out

The P5 connector is a dual output RCA jack bringing audio from the TVL320AIC331 on the EVM. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.

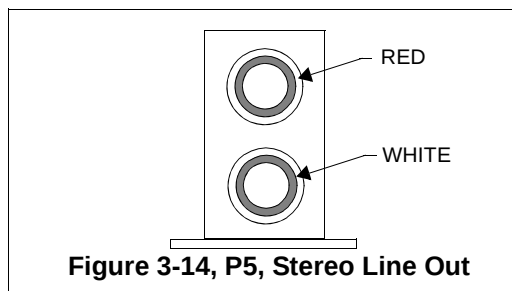


Figure 3-14, P5, Stereo Line Out

Table 17: P5, Stereo Line Out

Pin #	Signal
1	Isolated Ground
2	LEFT_LO+, U52, Pin J4
3	RIGHT_LO+, U52, Pin J6

3.2.21 P6, RS-232 UART

The P6 connector is a 9 pin male D-connector which provides a UART interface to the EVM. This connector interfaces to the MAX 3221 RS-232 line driver (U64) and is located on the top side of the board. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.

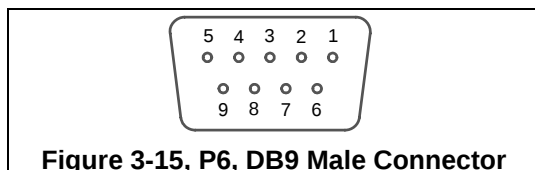


Figure 3-15, P6, DB9 Male Connector

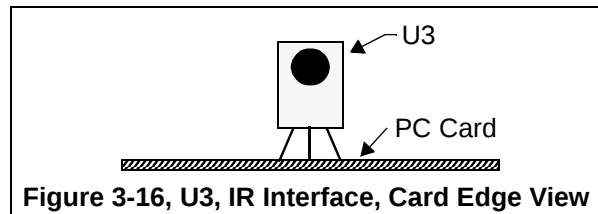
The pin numbers and their corresponding signals are shown in the table below. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

Table 18: P6, UART Pinout

Pin #	Signal Name	Direction
1	NC	N/A
2	S_A_RXD	In
3	S_A_TXD	Out
4	NC	N/A
5	GND	N/A
6	NC	N/A
7	Connected to pin 8	Out
8	Connected to pin 7	Out
9	NC	N/A
10,11	Earth Ground	N/A

3.2.22 U3, Infrared Interface

U3 is an infrared receiver mounted on the edge of the board. This device interfaces to the MSP430 microcontroller. The view of U3 is shown from a board edge view in the figure below.



The receiver supports interaction with an Infrared remote control included with your EVM.

Table 19: U3, Infrared Interface

U3 Pin #	MSP430 Signal, Pin #
1	P1.2/TA1, U4, Pin 23
2	GND
3	VCC_3V3

3.3 Daughter Card Connectors

The EVM has seven connectors that are available for daughter card connections. These connectors make many of the signals on the EVM available to be used by external logic. The signals on each of the connectors are described in the following tables. The table below lists the connectors.

Table 20: Daughter Card Connectors

Connector	Size	Function	Schematic Page
DC1	2x35	EMIF	29
DC2	2x20	GIOV33/Ethernet	31
DC3	2x15	SPI, McBSP, I ² C	31
DC4	2x20	Video In	30
DC5	2x25	Video Out	30
DC6	2x5	SD Interface	31
DC7	2x5	Power	35

3.3.1 DC1, EMIF Expansion Connector

Table 21: DC1, EMIF Expansion Connector

Pin #	Signal	Pin #	Signal
1	EM_A21	2	EM_A20
3	EM_A19	4	EM_A18
5	EM_A17	6	EM_A16
7	EM_A15	8	EM_A14
9	GND	10	GND
11	EM_A13	12	EM_A12
13	EM_A11	14	EM_A10
15	EM_A9	16	EM_A8
17	EM_A7	18	EM_A6
19	GND	20	GND
21	EM_A5	22	EM_A4
23	EM_A3	24	CLE_EM_A2
25	ALE_EM_A1	26	EM_A0
27	GND	28	GND
29	GPIO51	30	GPIO52
31	EM_BA1	32	EM_BA0
33	WRITE_WE	34	READ_OE
35	WAIT/BUSY	36	EM_RNW
37	GND	38	GND
39	EM_D15	40	EM_D14
41	EM_D13	42	EM_D12
43	EM_D11	44	EM_D10
45	GND	46	GND
47	EM_D9	48	EM_D8
49	EM_D7	50	EM_D6
51	EM_D5	52	EM_D4
53	GND	54	GND
55	EM_D3	56	EM_D2
57	EM_D1	58	EM_D0
59	EM_CS3	60	DC_EM_CS2
61	1.8V.SYS_RESETz	62	CLKOUT0
63	GND	64	GND
65	VCC_3.3V	66	VCC_3.3V
67	GND	68	GND
69	VCC_5V	70	VCC_1.8V

3.3.2 DC2, EMAC/GIO Connector

Table 22: DC2, EMAC/GIO Connector

Pin #	Signal	Pin #	Signal
1	GND	2	GND
3	GIOV33_0	4	GIOV33_1
5	GIOV33_2	6	GIOV33_3
7	GIOV33_4	8	GIOV33_5
9	GND	10	GND
11	GIOV33_6	12	GIOV33_7
13	GIOV33_8	14	GIOV33_9
15	GIOV33_10	16	GIOV33_11
17	GND	18	GND
19	GIOV33_12	20	GIOV33_13
21	GIOV33_14	22	GIOV33_15
23	GIOV33_16	24	GND
25	GND	26	3V3.SYS_RESETz
27	ENET_ENABLEz	28	GND
29	VCC_1.8V	30	3V3.UART_RXD1
31	VCC_1.8V	32	3V3.UART_TXD1
33	GND	34	GND
35	VCC_3.3V	36	VCC_3.3V
37	VCC_5V	38	VCC_5V
39	GND	40	GND

3.3.3 DC3, McBSP/SPI Expansion

Table 23: DC3, McBSP/SPI Expansion

Pin #	Signal	Pin #	Signal
1	SPI_EN1	2	SPI_EN0
3	SPI_DI	4	SPI_DO
5	SPI_CLK	6	TIMER_IN_DC3
7	GND	8	GND
9	DR	10	DX
11	CLKR	12	CLKX
13	FSR	14	FSX
15	GND	16	GND
17	1.8V.SYS_RESETz	18	1.8V.I2C_CLK
19	McBSP_EN	20	1.8V.I2C_DATA
21	AUDIO_CLK	22	GND
23	GND	24	1.8V_DC3_PCLK
25	VCC_3.3V	26	VCC_3.3V
27	GND	28	GND
29	VCC_5V	30	VCC_1.8V

3.3.4 DC4, Video Input Expansion

Table 24: DC4, Video Input Expansion

Pin #	Signal	Pin #	Signal
1	1.8V.SYS_RESETz	2	CAPTURE_EN
3	GND	4	GND
5	GIO1	6	GIO4
7	GND	8	GND
9	PWM1	10	PWM2
11	GND	12	GND
13	Y10	14	Y11
15	Y12	16	Y13
17	Y14	18	Y15
19	Y16	20	Y15
21	GND	22	GND
23	GND	24	HD
25	PCLK/1V8.DC_PCLK	26	VD
27	GND	28	GND
29	CI0	30	CI1
31	CI2	32	CI3
33	CI4	34	CI5
35	CI6	36	CI7
37	GND	38	GND
39	1V8.I2C_CLK	40	1V8.I2C_DATA
41	VCC_1.8V	42	VCC_1.8V
43	GND	44	GND
45	VCC_3.3V	46	VCC_3.3V
47	GND	48	GND
49	VCC_5V	50	VCC_5V

3.3.5 DC5, Video Output Expansion

Table 25: DC5, Video Output Expansion

Pin #	Signal	Pin #	Signal
1	GIO0	2	GIO2
3	GIO3	4	GIO5
5	GIO6	6	GIO38
7	GND	8	GND
9	COUT0	10	COUT1
11	COUT2	12	COUT3
13	COUT4	14	COUT5
15	COUT6	16	COUT7
17	GND	18	GND
19	VPBECLK/VID_CLK	20	HSYNC
21	GND	22	GND
23	VCLK	24	VSYNC
25	GND	26	GND
27	YOUT0	28	YOUT1
29	YOUT2	30	YOUT3
31	YOUT4	32	YOUT5
33	YOUT6	34	YOUT7
35	GND	36	GND
37	1.8V.I2C_CLK	38	1.8V.SYS_RESETz
39	1.8V.I2C_DATA	40	GND
41	VCC_1.8V	42	VCC_1.8V
43	GND	44	GND
45	VCC_3.3V	46	VCC_3.3V
47	GND	48	GND
49	VCC_5V	50	VCC_5V

3.3.6 DC6, SD Interface Expansion

Table 26: DC6, SD Interface Expansion

Pin #	Signal	Pin #	Signal
1	SD_CLK	2	SD_CMD
3	GND	4	GND
5	SD_DATA0	6	SD_DATA1
7	SD_DATA2	8	SD_DATA3
9	GND	10	GND

3.3.7 DC7, Power Expansion

Table 27: DC7, Power Expansion

Pin #	Signal	Pin #	Signal
1	VDDIMX_EN	2	GND
3	CORE_SUPPLY	4	CORE_SUPPLY
5	GND	6	GND
7	VCC_1.8V	8	VCC_1.8V
9	GND	10	GND

3.4 LEDs

The EVM has ten (10) LEDs which are located on the top side of the board. Eight of these LEDs (DS1-8) are under user control and addressed over the I²C bus. One LED (DS9) indicates the presence of +5 volts on the board. The remaining LED (DS10) is tied to the CPLD, U14, B2.PIN86, and +3.3 volts. Additional information regarding the LEDs are shown in the table below.

Table 28: LEDs

LED #	Use	Color	Schematic Page
DS1	User Defined	Green	23
DS2	User Defined	Green	23
DS3	User Defined	Green	23
DS4	User Defined	Green	23
DS5	User Defined	Green	23
DS6	User Defined	Green	23
DS7	User Defined	Green	23
DS8	User Defined	Green	23
DS9	+5V	Green	29
DS10	+3.3V, U14, B2.PIN86	Red	14

3.5 Switches

The EVM has five (5) switches. The function of these switches are shown in the table below.

Table 29: Switches

Switch	Function	Type	Schematic Page
S1	EMU0/1 Selection	DIP	28
S3	Boot Configuration Options	DIP	10
S4	RESET	Push button	29
S5	Pull Ups	DIP	14
SW1	Power On/Off	Toggle	29

3.5.1 S1, EMU0/1 Select Switch

S1 is a 2 position DIP switch providing 2 options in selecting the state of the EMU0 and EMU1 pins on the processor. A view of the switch is shown in the figure below. The selection options with this switch are in the table below.

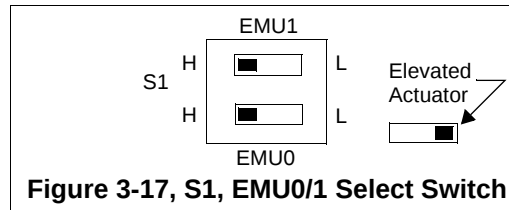


Table 30: S1, EMU0/1 Select

State at Reset EMU0 EMU1		Function	TAP Configuration
L	L	Emulation Debug ARM JTAG Enabled (20 pin JTAG connector)	14 bit = (Bypass(6) + ARM9(4) + Bypass(4))
L	H	Not Defined	
H	L	Not Defined	
H	H	TI Emulation Debug * ICE PICK Mode	6 bit = ICE PICK

* is the factory shipped configuration

3.5.2 S3, Processor Configuration/Boot Load Options

S3 is a 10 position DIP switch providing 9 options in selecting the processor configuration and boot load modes. The connections for this switch are shown on page 10 of the schematics in appendix A. A view of the switch is shown in the figure below. The selection options with this switch are in the table below.

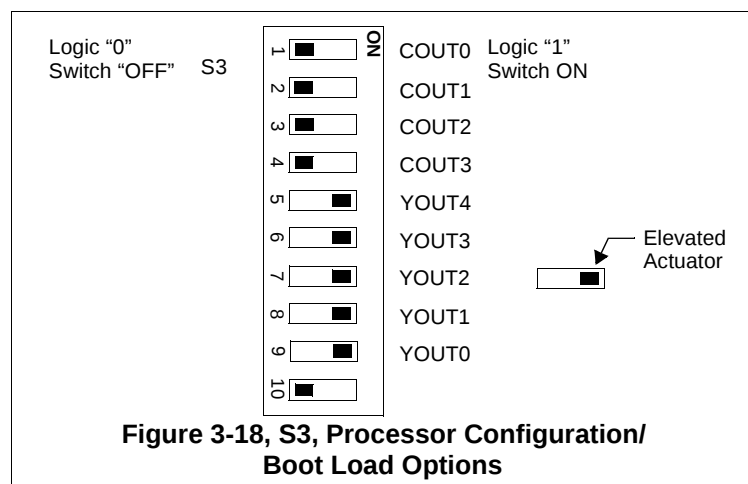


Table 31: S3, Processor Configuration/Boot Load Options

Position	Name	Function
1	COUT0	0 0 = Boot from ROM (NAND) * 0 1 = Boot from AEM IF 1 0 = Boot from ROM (HPI) 1 1 = Boot from ROM (UART)
2	COUT1	
3	COUT2	
4	COUT3	
5	YOUT4	Selects AEMIF CS2 Bus width: 0=8 bit *, 1=16 bit
6	YOUT3	Always Low
7	YOUT2	AEAW4
8	YOUT1	AEAW3
9	YOUT0	AEAW2
10		AEAW1
		AEAW0
		Composite Video Format

AEAW4:0 configure address pins required to boot. See the tables in the device data sheet for more information. For the DM357 all address active are selected.

3.5.3 S4, RESET

Switch S4 is a push button reset switch that will RESET the processor. This switch is in parallel with J6. The connections for this switch are shown on page 29 of the schematics in appendix A.

3.5.4 S5, User CPLD Option Switch

Switch S5 is a 2 position DIP switch that allows the user to select options on the PIN74 and PIN75 pins of the CPLD, U14. This switch is not used on the DM357 as shipped from the factory. This switch appears on page 14 of the schematics. The diagram below shows which position is associated with each signal.

3.5.5 SW1, Power On/Off

Switch S1 is a toggle switch that provides power to the EVM. The connections for this switch are shown on page 29 of the schematics in appendix A.

3.6 Jumper Block, JP1

The DM357 EVM has 6 position jumper that is not populated. This connector is used for test points on the CPLD internal operations during CPLD debug. The layout of the jumper block is shown below.

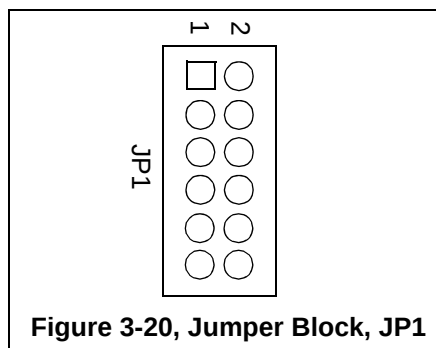


Figure 3-20, Jumper Block, JP1

The signals on each pin are shown in the table below.

Table 32: Jumper Block, JP1

Pin #	Signal	Pin #	Signal
1	U14, PIN92	2	U14, PIN95
3	U14, PIN91	4	U14, PIN96
5	U14, PIN90	6	U14, PIN97
7	U14, PIN89	8	U14, PIN98
9	U14, PIN88	10	U14, PIN99
11	U14, PIN87	12	U14, PIN100

3.8 Test Points

The EVM has 72 test points. All test points appear on the top of the board. The following figure identifies the position of each test point. the next table list each test point and the signal appearing on that test point.

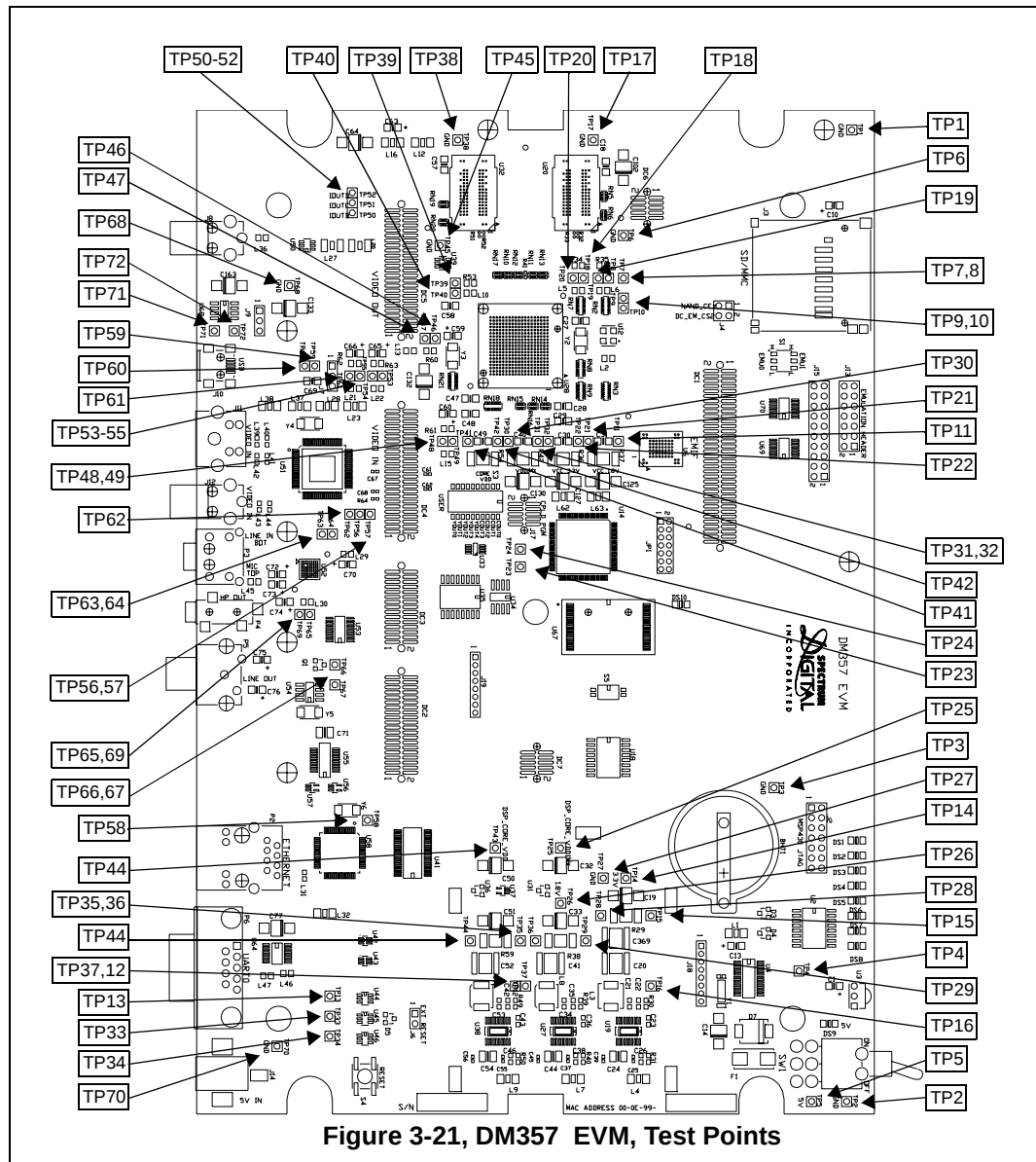


Table 33: DM357 EVM Test Points

TP #	Signal	Page	TP #	Signal	Page
TP1	GND	29	TP37	U27, P4, PWRGD, VCC_5V	30
TP2	GND	29	TP38	GND	4
TP3	GND	29	TP39	U28A,T10, DDR_VDDDLL, 1.8V	4
TP4	U4, P24, P1.3/TA2	24	TP40	VCC_1.8V	4
TP5	VCC_5V	29	TP41	CORE_VDD	9
TP6	GND	4	TP42	U28D, M12, CPU_CORE_VDD	9
TP7	U28A, R8, RSV7	4	TP43	CORE_VDD	30
TP8	U28E, M2, PLLVDD18, VCC_1.8V	8	TP44	CORE_SUPPLY	30
TP9	GND	8	TP45	GND	4
TP10	U28E, L3, RSV6	8	TP46	U28H, H17, USB_VDDA1P8, VCC_1.8V	7
TP11	U28D, T5, CPU_VCC_1.8V, VCC_1.8V	9	TP47	VCC_1.8V	7
TP12	U38, P4, PWRGD, VCC_5V	30	TP48	VCC_3.3V	7
TP13	U44, P1, RESET	29	TP49	U28H, J19, USB_VDDA3P3.1, VCC_3.3V	7
TP14	+3.3V	29	TP50	U28G, P18, DAC_IOUT_B	5
TP15	U19, P6, PH1	29	TP51	U28G, R19, DAC_IOUT_C	5
TP16	U19, P4, PWRGD, 3V3_PWR_OK	34	TP52	U28G, T19, RSV45	5
TP17	GND	4	TP53	U28G, R18, VDDA_1P8V, VCC_1.8V	5
TP18	U28E, M3, RSV24, CORE_VDD	8	TP54	VCC_1.8V	5
TP19	VCC_1.8V	8	TP55	U28G, P16, VDDA_1P1V, CORE_VDD	5
TP20	CORE_VDD	8	TP56	U51, Pin 36, AVID/GPIO	20
TP21	VCC_1.8V	9	TP57	U51, Pin 37, GLCO/12CA	20
TP22	U28D, E13, CPU_VCC_3.3V, VCC_3.3V	9	TP58	U58, PIN 64, MDINT	22
TP23	U14, Pin 49, B1.PIN49	14	TP59	J10, Pin 4, USB_ID	17
TP24	U14, Pin 29, B1.PIN29	14	TP60	J10, Pin 1, USB_VBUS	17
TP25	CORE_VDDMIX	30	TP61	CORE_VDD	5
TP26	VCC_1.8V	30	TP62	U51, Pin 30, INTREQ	20
TP27	GND	29	TP63	U52, A8, MPF2	22
TP28	VCC_3.3V	29	TP64	U52, A9, MPF3	22
TP29	U27, P6, PH1	30	TP65	U52, J8, GPIO2	22
TP30	CORE_VDDMIX	9	TP66	U28I, C15, PWM0/GIO45, VCC_1.8V	5
TP31	U28DM K11, CPU_CORE_VDDIMX	9	TP67	VIN, U54, PIN 3	5
TP32	VCC_3.3V	9	TP68	GND	29
TP33	U45, P1, RESET	29	TP69	U52, J9, GPIO1	22
TP34	U46, P1, RESET	29	TP70	GND	29
TP35	U38, P6, PH1	30	TP71	U68, Pin 4, USB.DRVVBUSz	17
TP36	VCC_1.8V	30	TP72	U68, Pin 5, USB.OVER_CURRENT	17

Appendix A

Schematics

This appendix contains the schematics for the DM357 EVM.

1

2

3

4

5

NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES IN OHMS.

2. CAPACITANCE VALUES IN MICROFARADS.

3. REFERENCE DESIGNATORS USED:

4. ALL 0.1 uF AND 0.01uF CAPACITORS ARE DECOUPLING CAPS UNLESS OTHERWISE NOTED. THEY ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS THEY SHOULD BE PLACED NEAR.

5. OBSERVE THE FOLLOWING LAYOUT NOTES:

6. BOARD PROPERTIES

7. ROUTE TO WITHIN 10% OF MANHATTAN DISTANCE

8. General layers 50 +/- 5 OHM MATCHED IMPEDANCE

9. USB layer 90 ohm differential

10. OUTER LAYERS 0.5 OZ CU / W 0.5 OZ AU PLATING

11. INNER LAYERS 1.0 OZ CU

12. MINIMUM TRACE WIDTH/SPACING 4 MILS

13. MINIMUM VIA SIZE 10/19 MIL

14. LAYER STACKUP:

15. TOP - SIGNAL ROUTING

16. INNER1 - SIGNAL ROUTING

17. VCC3 PLANE (3.3V BOARD)

18. VCC3 PLANE (3.3V BOARD)

19. INNER3 - SIGNAL ROUTING

20. VCC1 PLANE (1.8V BOARD)

21. GROUND PLANE

22. GROUND PLANE

23. BOTTOM - SIGNAL ROUTING

6

7

8

9

10

11

12

13

14

15

16

17

18

19

20

21

22

23

24

25

26

27

28

29

30

31

32

33

34

35

36

37

38

39

40

41

42

43

44

45

46

47

48

49

50

51

52

53

54

55

56

57

58

59

60

61

62

63

64

65

66

67

68

69

70

71

72

73

74

75

76

77

78

79

80

81

82

83

84

85

86

87

88

89

90

91

92

93

94

95

96

97

98

99

100

101

102

103

104

105

106

107

108

109

110

111

112

113

114

115

116

117

118

119

120

121

122

123

124

125

126

127

128

129

130

131

132

133

134

135

136

137

138

139

140

141

142

143

144

145

146

147

148

149

150

151

152

153

154

155

156

157

158

159

160

161

162

163

164

165

166

167

168

169

170

171

172

173

174

175

176

177

178

179

180

181

182

183

184

185

186

187

188

189

190

191

192

193

194

195

196

197

198

199

200

201

202

203

204

205

206

207

208

209

210

211

212

213

214

215

216

217

218

219

220

221

222

223

224

225

226

227

228

229

230

231

232

233

234

235

236

237

238

239

240

241

242

243

244

245

246

247

248

249

250

251

252

253

254

255

256

257

258

259

260

261

262

263

264

265

266

267

268

269

270

271

272

273

274

275

276

277

278

279

280

281

282

283

284

285

286

287

288

289

290

291

292

293

294

295

296

297

298

299

300

301

302

303

304

305

306

307

308

309

310

311

312

313

314

315

316

317

318

319

320

321

322

323

324

325

326

327

328

329

330

331

332

333

334

335

336

337

338

339

340

341

342

343

344

345

346

347

348

349

350

351

352

353

354

355

356

357

358

359

360

361

362

363

364

365

366

367

368

369

370

371

372

373

374

375

376

377

378

379

380

381

382

383

384

385

386

387

388

389

390

391

392

393

394

395

396

397

398

399

400

401

402

403

404

405

406

407

408

409

410

411

412

413

414

415

416

417

418

419

420

421

422

423

424

425

426

427

428

429

430

431

432

433

434

435

436

437

438

439

440

441

442

443

444

445

446

447

448

449

450

451

452

453

454

455

456

457

458

459

460

461

462

463

464

465

466

467

468

469

470

471

472

473

474

475

476

477

478

479

480

481

482

483

484

485

486

487

488

489

490

491

492

493

494

495

496

497

498

499

500

501

502

503

504

505

506

507

508

509

510

511

512

513

514

515

516

517

518

519

520

521

522

523

524

525

526

527

528

529

530

531

532

533

534

535

536

537

538

539

540

541

542

543

544

545

546

547

548

549

550

551

552

553

554

555

556

557

558

559

560

561

562

563

564

565

566

567

568

569

570

571

572

573

574

575

576

577

578

579

580

581

582

583

584

585

586

587

588

589

590

591

592

593

594

595

596

597

598

599

600

601

602

603

604

605

606

607

608

609

610

611

612

613

614

615

616

617

618

619

620

621

622

623

624

625

626

627

628

629

630

631

632

633

634

635

636

637

638

639

640

641

642

643

644

645

646

647

648

649

650

651

652

653

654

655

656

657

658

659

660

661

662

663

664

665

666

667

668

669

670

671

672

673

674

675

676

677

678

679

680

681

682

683

684

685

686

687

688

689

690

691

692

693

694

695

696

697

698

699

700

701

702

703

704

705

706

707

708

709

710

711

712

713

714

715

716

717

718

719

720

721

722

723

724

725

726

727

728

729

730

731

732

733

734

735

736

737

738

739

740

741

742

743

744

745

746

747

748

749

750

751

752

753

754

755

756

757

758

759

760

761

762

763

764

765

766

767

768

769

770

771

772

773

774

775

776

777

778

779

780

781

782

783

784

785

786

787

788

789

790

791

792

793

794

795

796

797

798

799

800

801

802

803

804

805

806

807

808

809

810

811

812

813

814

815

816

817

818

819

820

821

822

823

824

825

826

827

828

829

830

831

832

833

834

835

836

837

838

839

840

841

842

843

844

845

846

847

848

849

850

851

852

853

854

855

856

857

858

859

860

861

862

863

864

865

866

867

868

869

870

871

872

873

874

875

876

877

878

879

880

881

882

883

884

885

886

887

888

889

890

891

892

893

894

895

896

897

898

899

900

901

902

903

904

905

906

907

908

909

910

911

912

913

914

915

916

917

918

919

920

921

922

923

924

925

926

927

928

929

930

931

932

933

934

935

936

937

938

939

940

941

942

943

944

945

946

947

948

949

950

951

952

953

954

955

956

957

958

959

960

961

962

963

964

965

966

967

968

969

970

971

972

973

974

975

976

977

978

979

980

981

982

983

984

985

986

987

988

989

990

991

992

993

994

995

996

997

998

999

1000

1001

1002

1003

1004

1005

1006

1007

1008

1009

1010

1011

1012

1013

1014

1015

1016

1017

1018

1019

1020

1021

1022

1023

1024

1025

1026

1027

1028

1029

1030

1031

1032

1033

1034

1035

1036

1037

1038

1039

1040

1041

1042

1043

1044

1045

1046

1047

1048

1049

1050

1051

1052

1053

1054

1055

1056

1057

1058

1059

1060

1061

1062

1063

1064

1065

1066

1067

1068

1069

1070

1071

1072

1073

1074

1075

1076

1077

1078

1079

1080

1081

1082

1083

1084

1085

1086

1087

1088

1089

1090

1091

1092

1093

1094

1095

1096

1097

1098

1099

1100

1101

1102

1103

1104

1105

1106

1107

1108

1109

1110

1111

1112

1113

1114

1115

1116

1117

1118

1119

1120

1121

1122

1123

1124

1125

1126

1127

1128

1129

1130

1131

1132

1133

1134

1135

1136

1137

1138

1139

1140

1141

1142

1143

1144

1145

1146

1147

1148

1149

1150

1151

1152

1153

1154

1155

1156

1157

1158

1159

1160

1161

1162

1163

1164

1165

1166

1167

1168

1169

1170

1171

1172

1173

1174

1175

1176

1177

1178

1179

1180

1181

1182

1183

1184

1185

1186

1187

1188

1189

1190

1191

1192

1193

1194

1195

1196

1197

1198

1199

1200

1201

1202

1203

1204

1205

1206

1207

1208

1209

1210

1211

1212

1213

1214

1215

1216

1217

1218

1219

1220

1221

1222

1223

1224

1225

1226

1227

1228

1229

1230

1231

1232

1233

1234

1235

1236

1237

1238

1239

1240

1241

1242

1243

1244

1245

1246

1247

1248

1249

1250

1251

1252

1253

1254

1255

1256

1257

1258

1259

1260

1261

1262

1263

1264

1265

1266

1267

1268

1269

1270

1271

1272

1273

1274

1275

1276

1277

1278

1279

1280

1281

1282

1283

1284

1285

1286

1287

1288

1289

1290

1291

1292

1293

1294

1295

1296

1297

1298

1299

1300

1301

1302

1303

1304

1305

1306

1307

1308

1309

1310

1311

1312

1313

1314

1315

1316

1317

1318

1319

1320

1321

1322

1323

1324

1325

1326

1327

1328

1329

1330

1331

1332

1333

1334

1335

1336

1337

1338

1339

1340

1341

1342

1343

1344

1345

1346

1347

1348

1349

1350

1351

1352

1353

1354

1355

1356

1357

1358

1359

1360

1361

1362

1363

1364

1365

1366

1367

1368

1369

1370

1371

1372

1373

1374

1375

1376

1377

1378

1379

1380

1381

1382

1383

1384

1385

1386

1387

1388

1389

1390

1391

1392

1393

1394

1395

1396

1397

1398

1399

1400

1401

1402

1403

1404

1405

1406

1407

1408

1409

1410

1411

1412

1413

1414

1415

1416

1417

1418

1419

1420

1421

1422

1423

1424

1425

1426

1427

1428

1429

1430

1431

1432

1433

1434

1435

1436

1437

1438

1439

1440

1441

1442

1443

1444

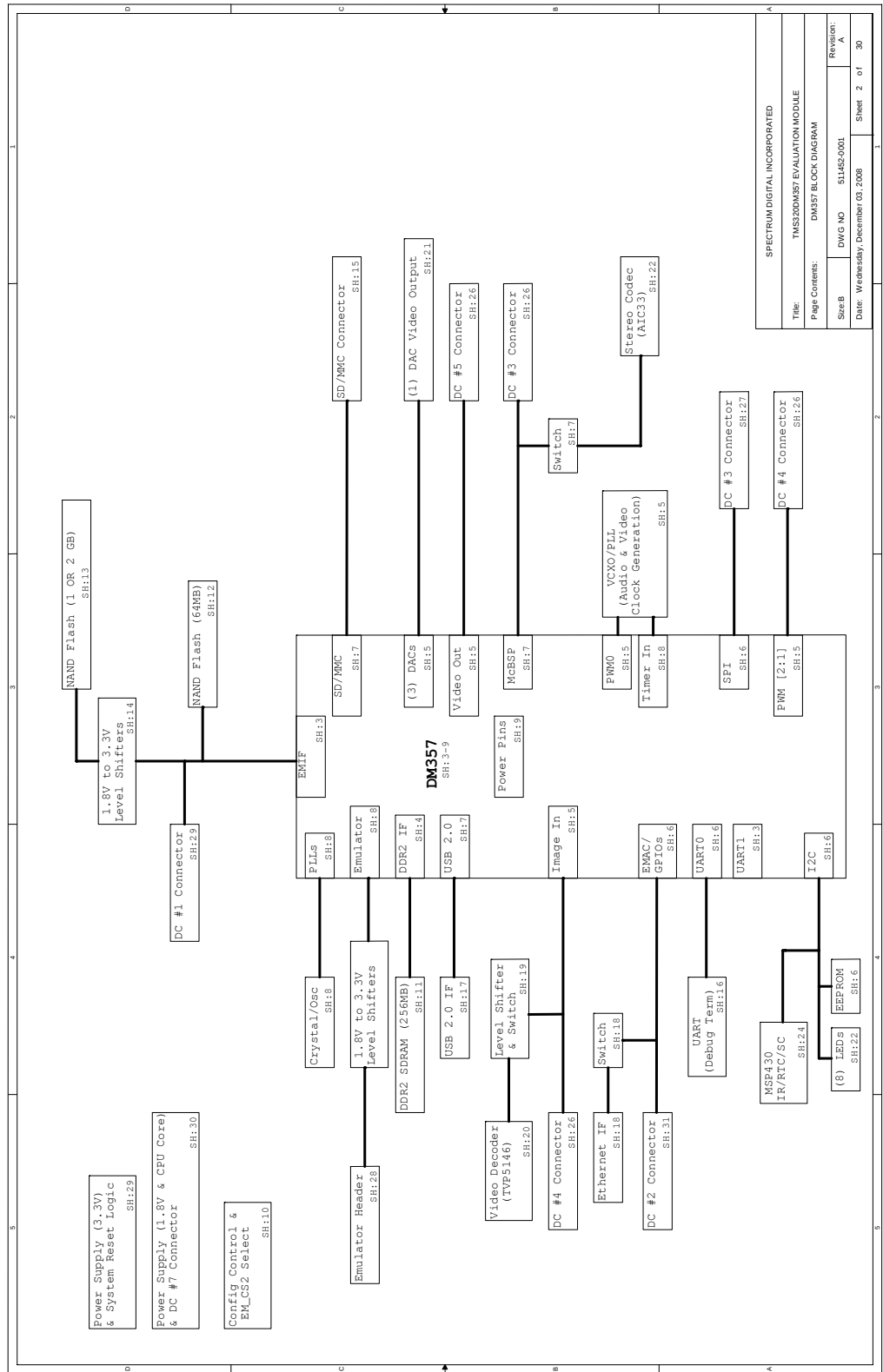
1445

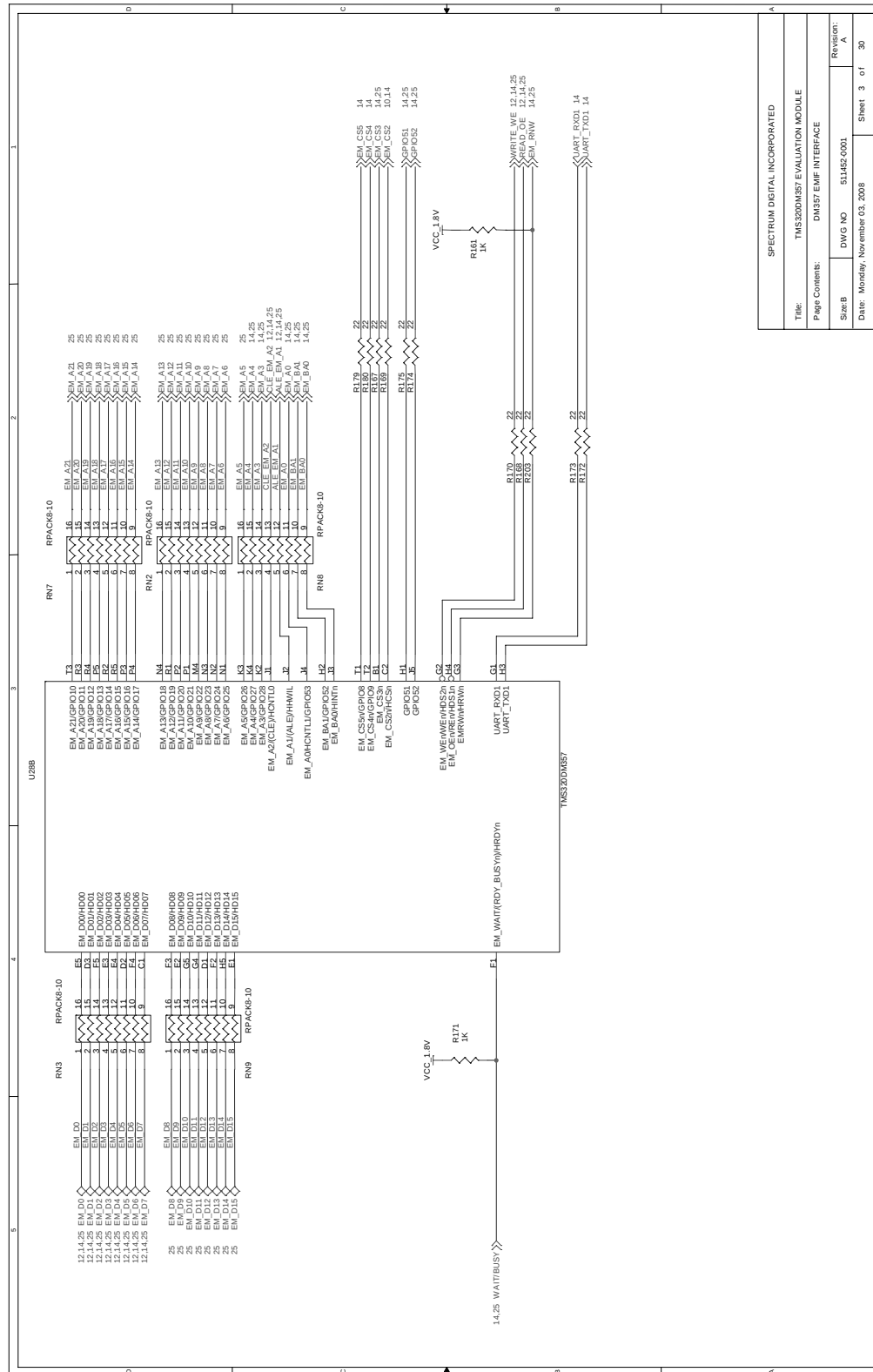
1446

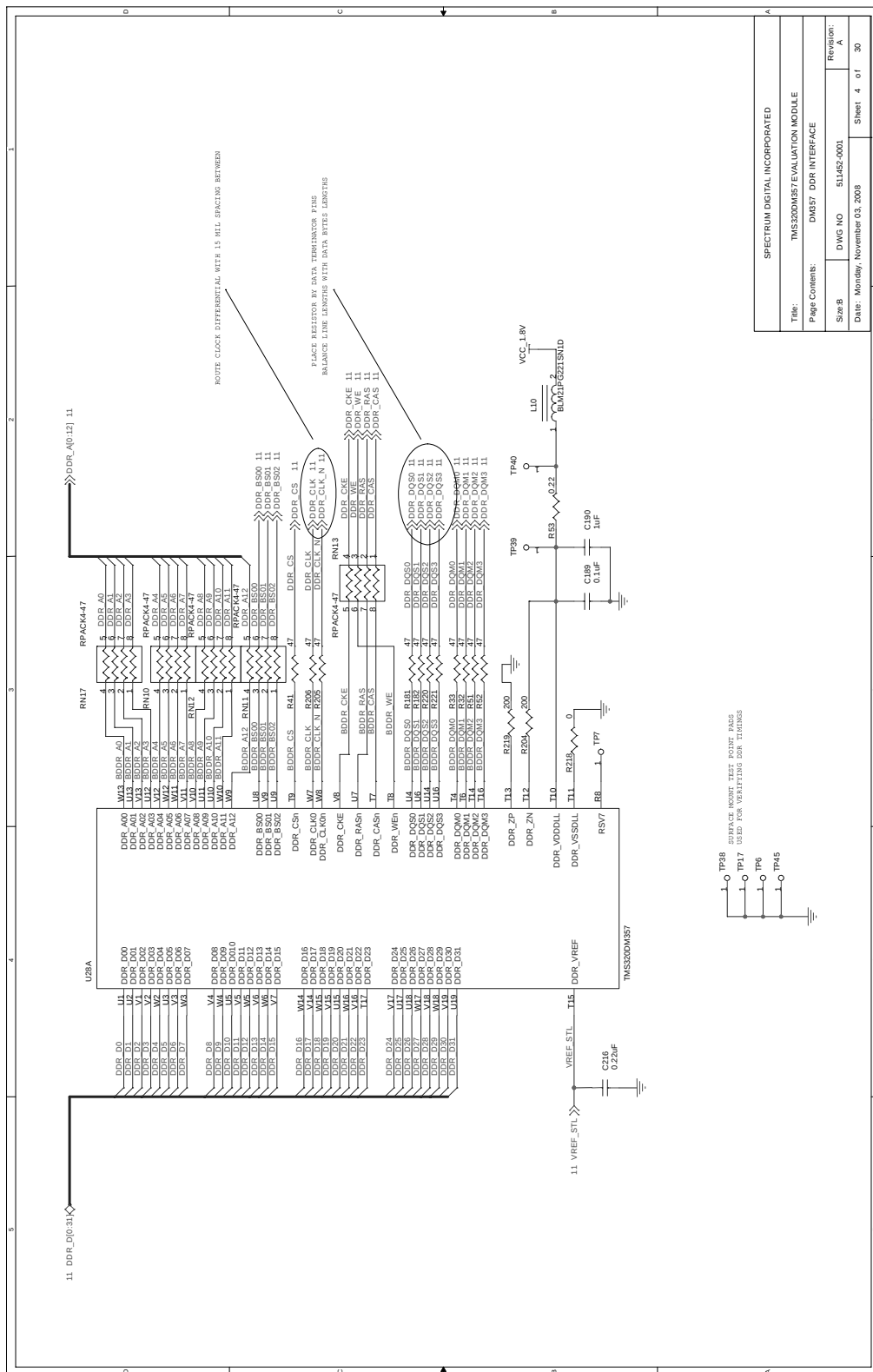
1447

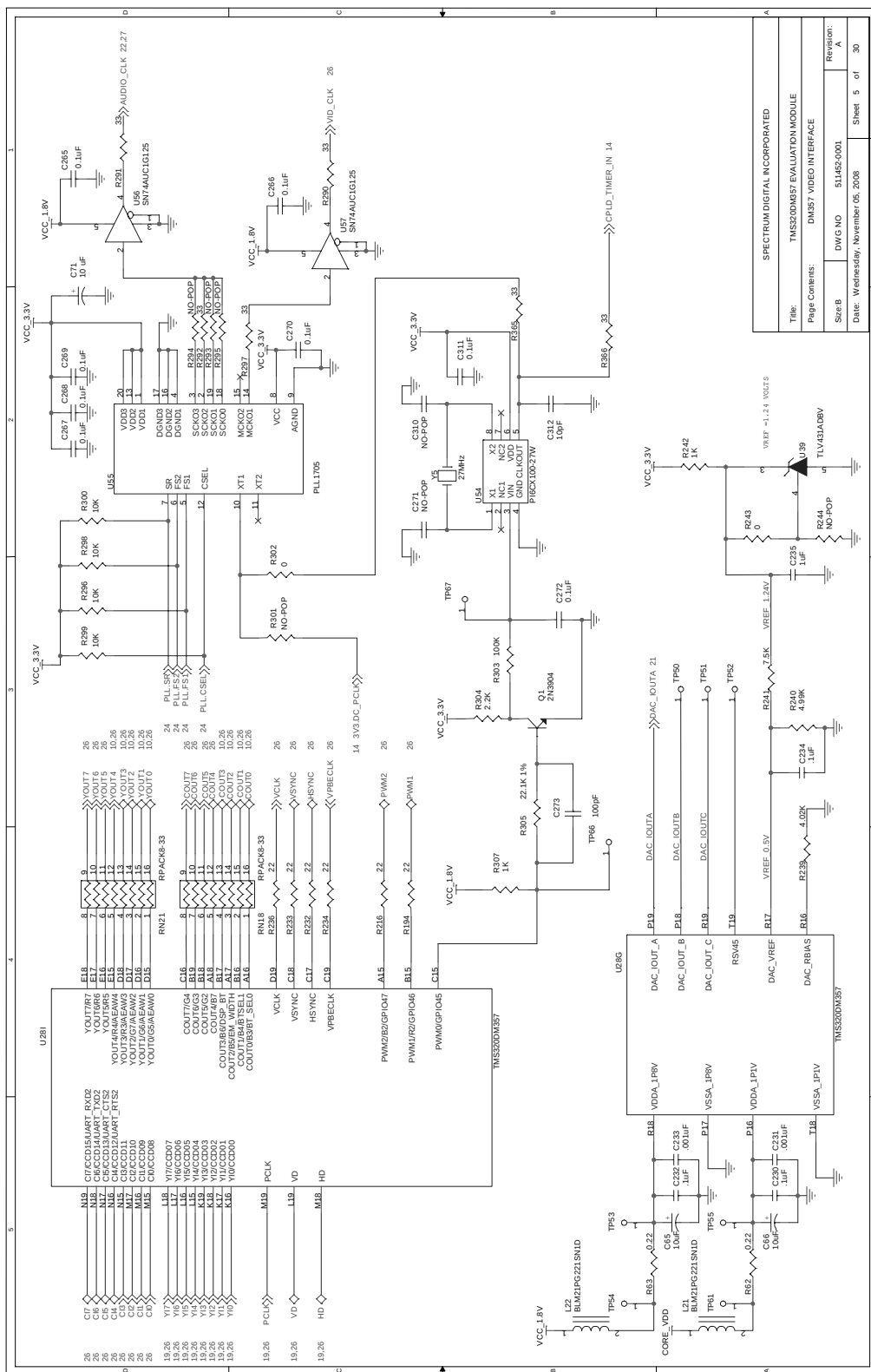
1448

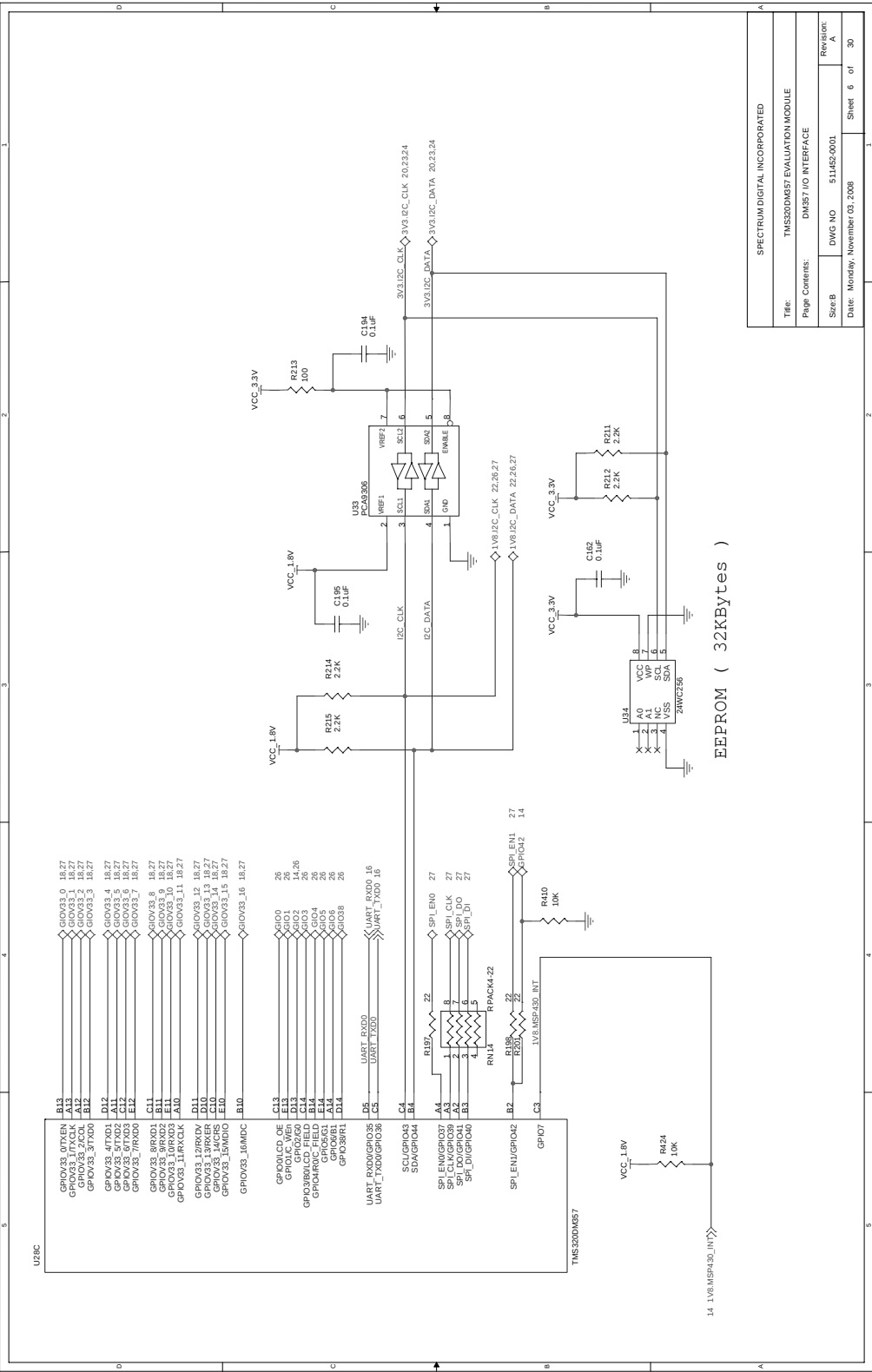
14

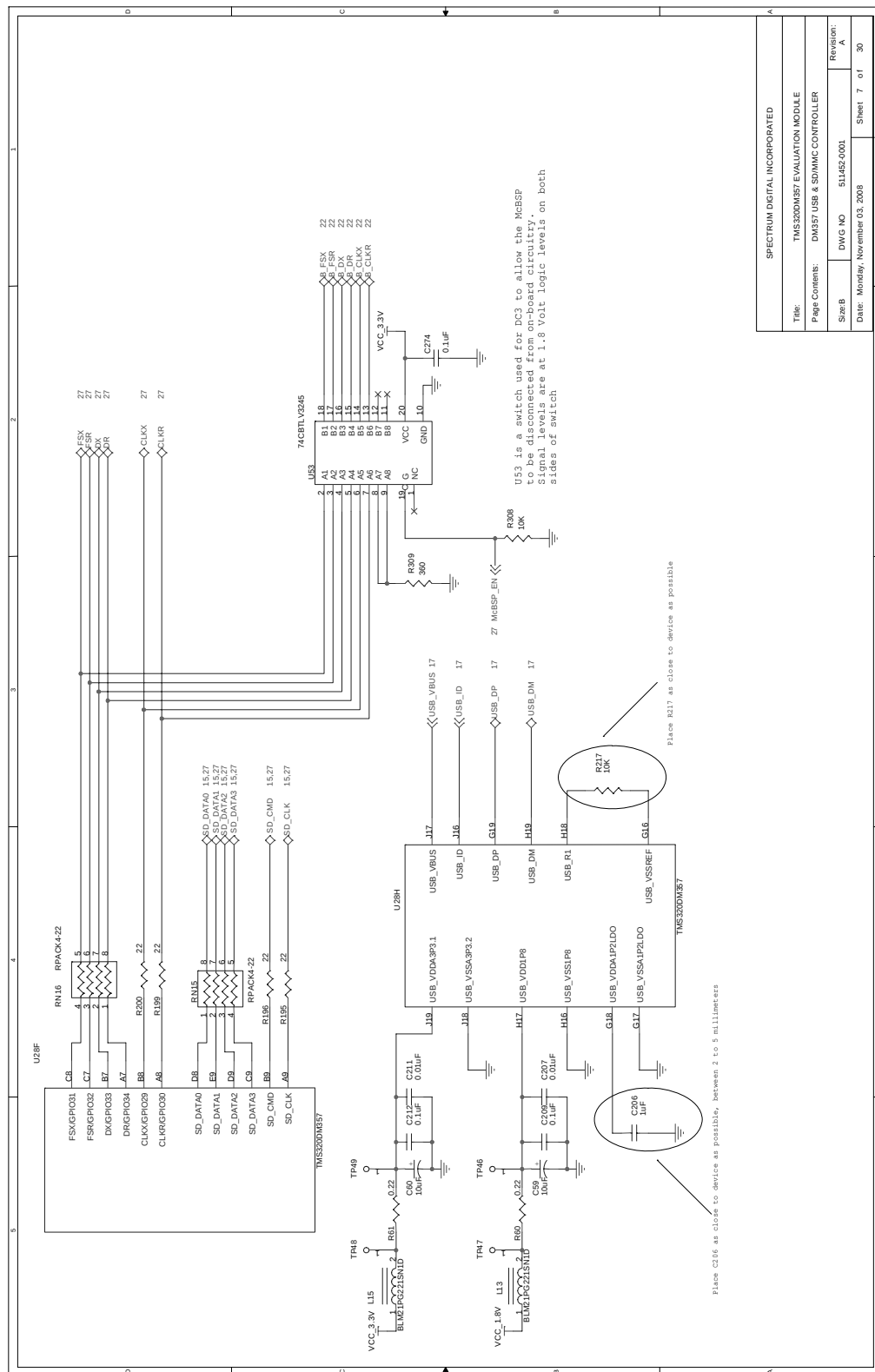




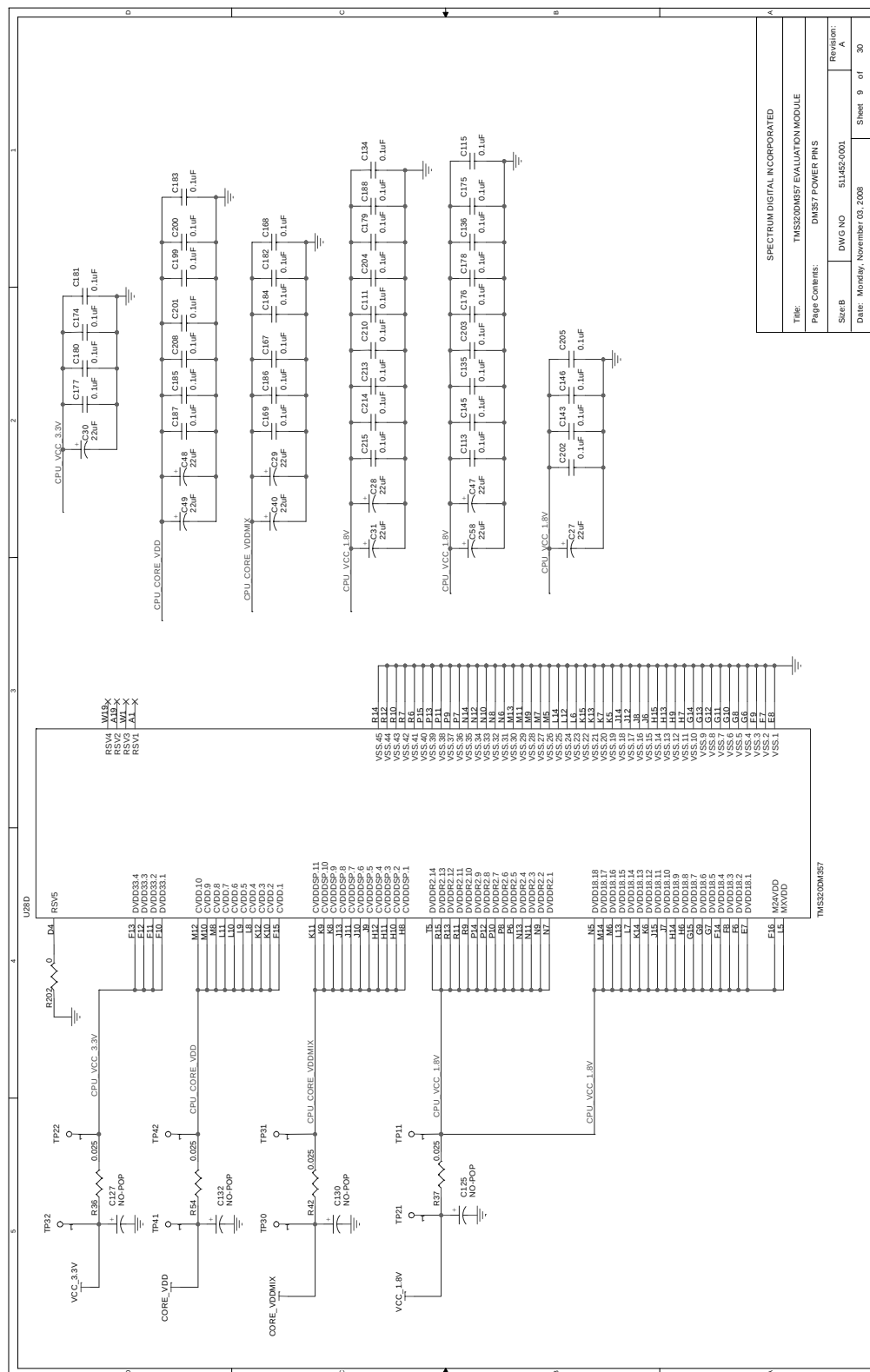




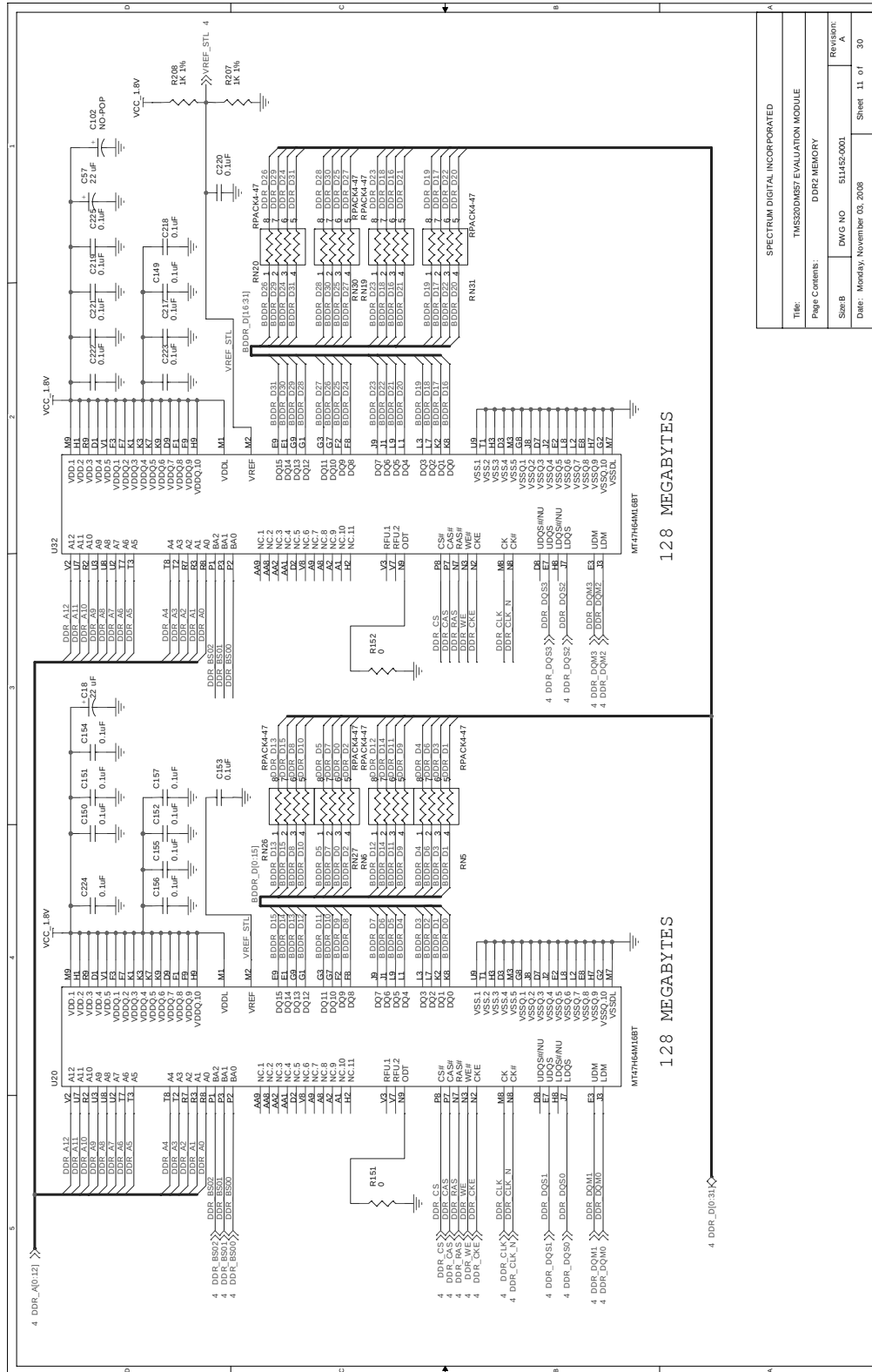




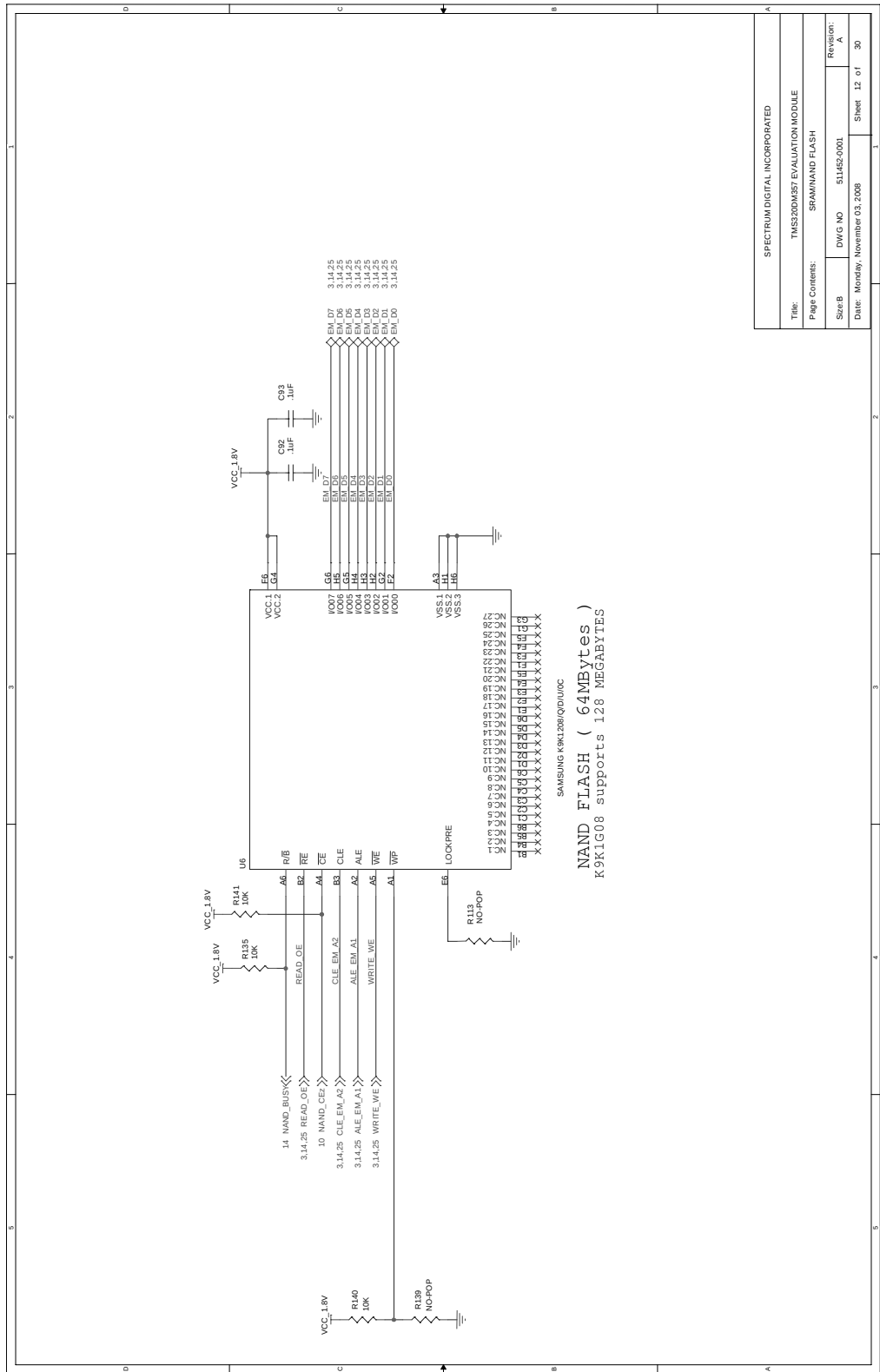


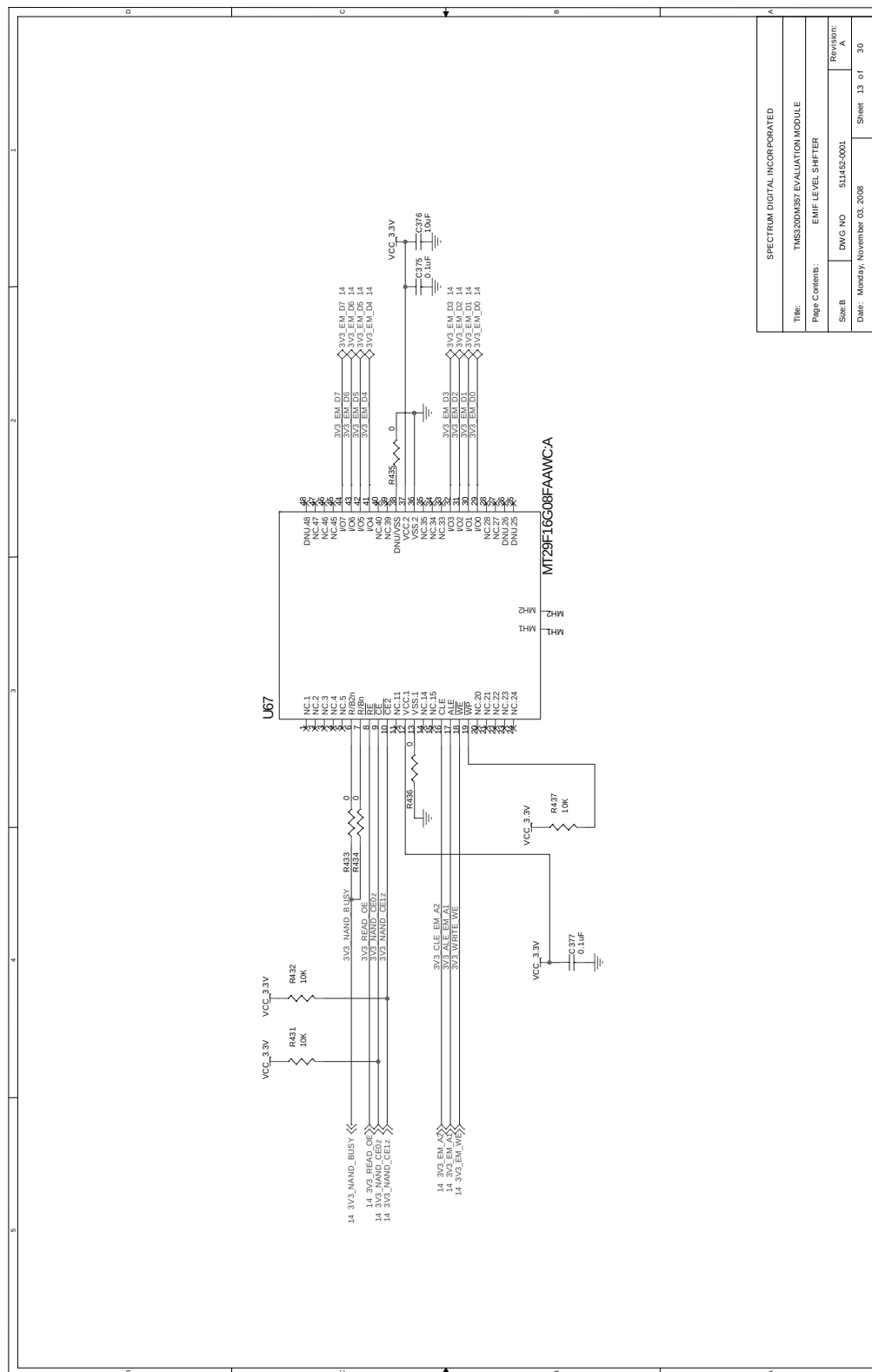


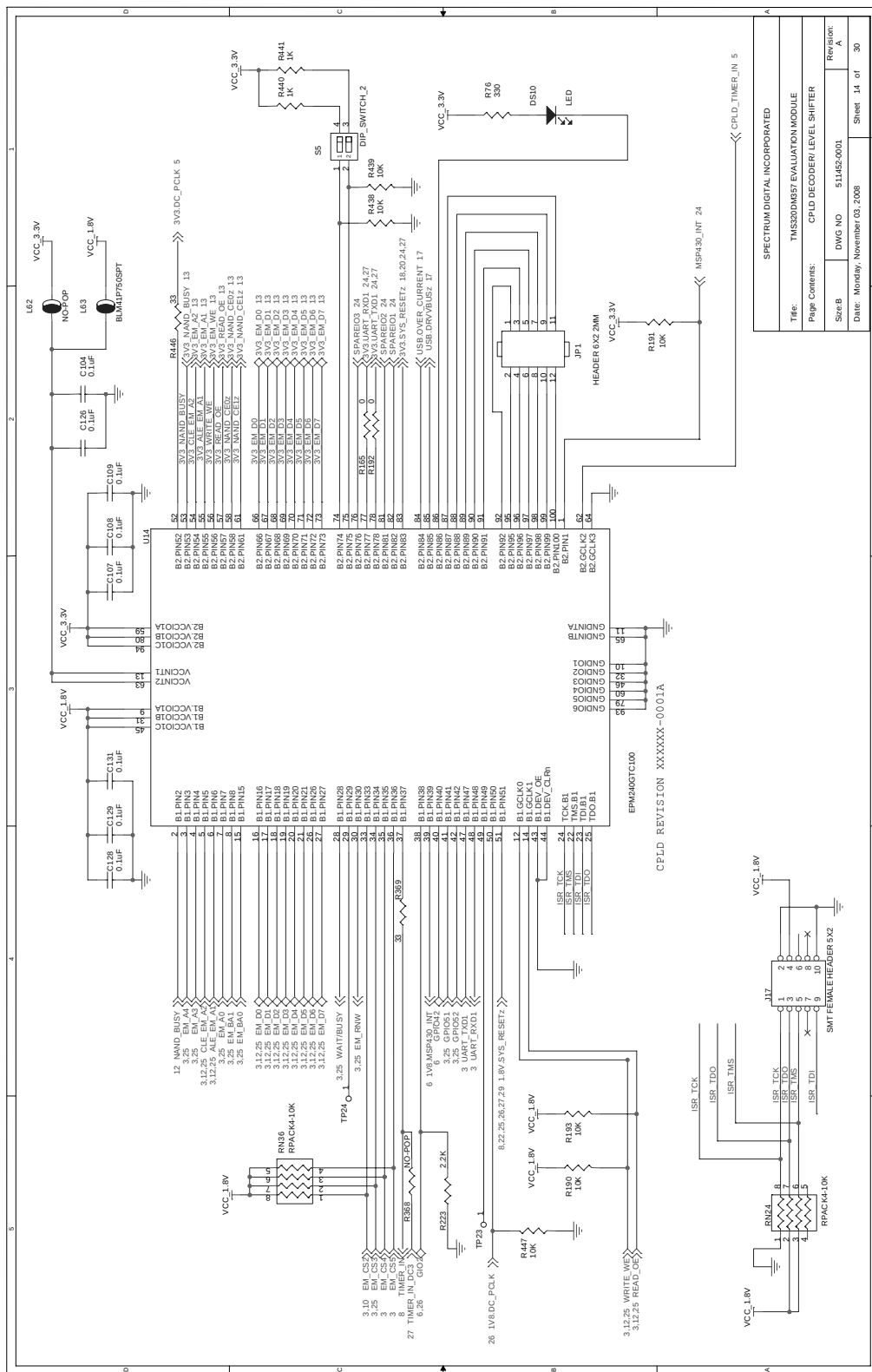


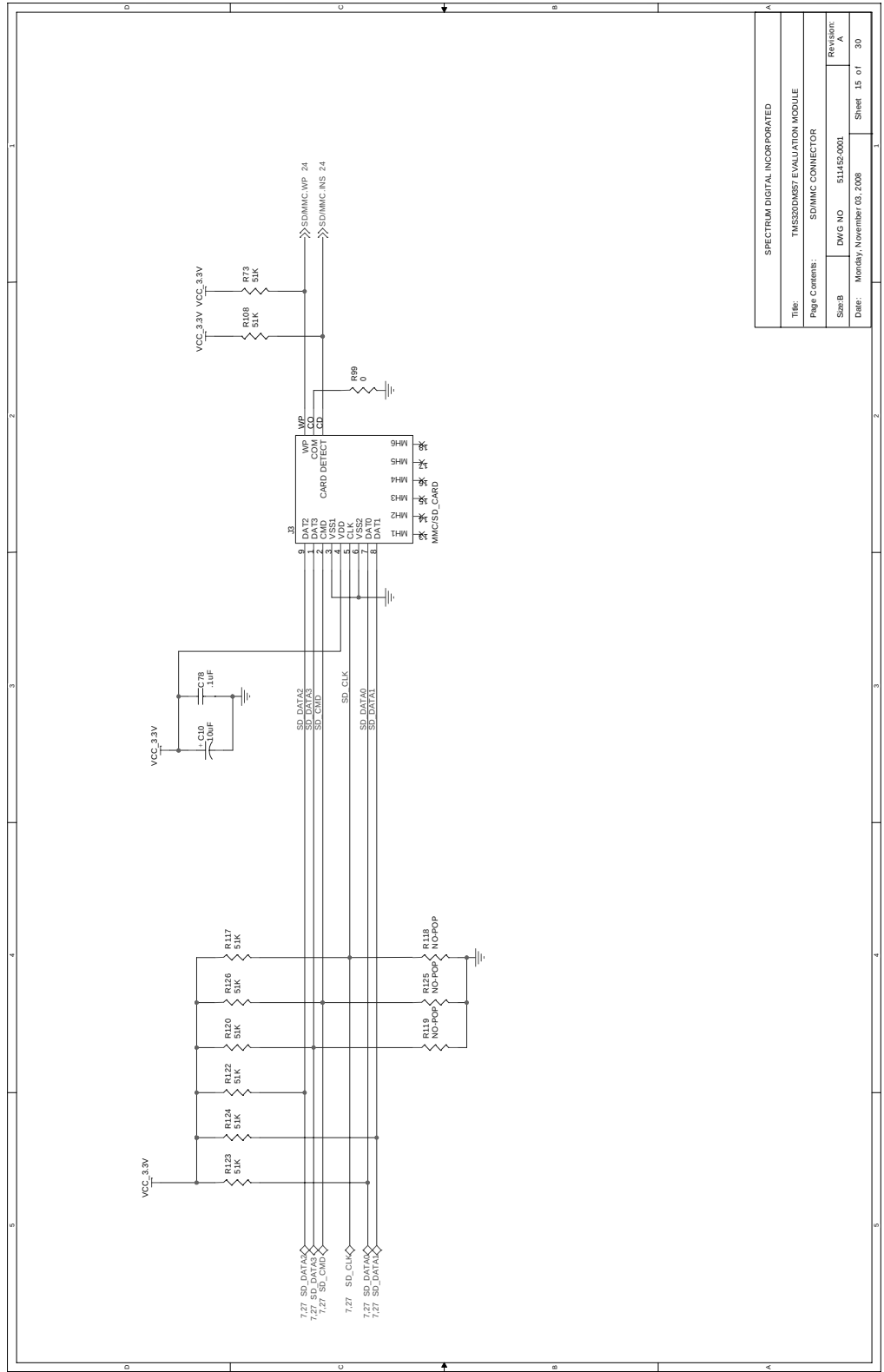


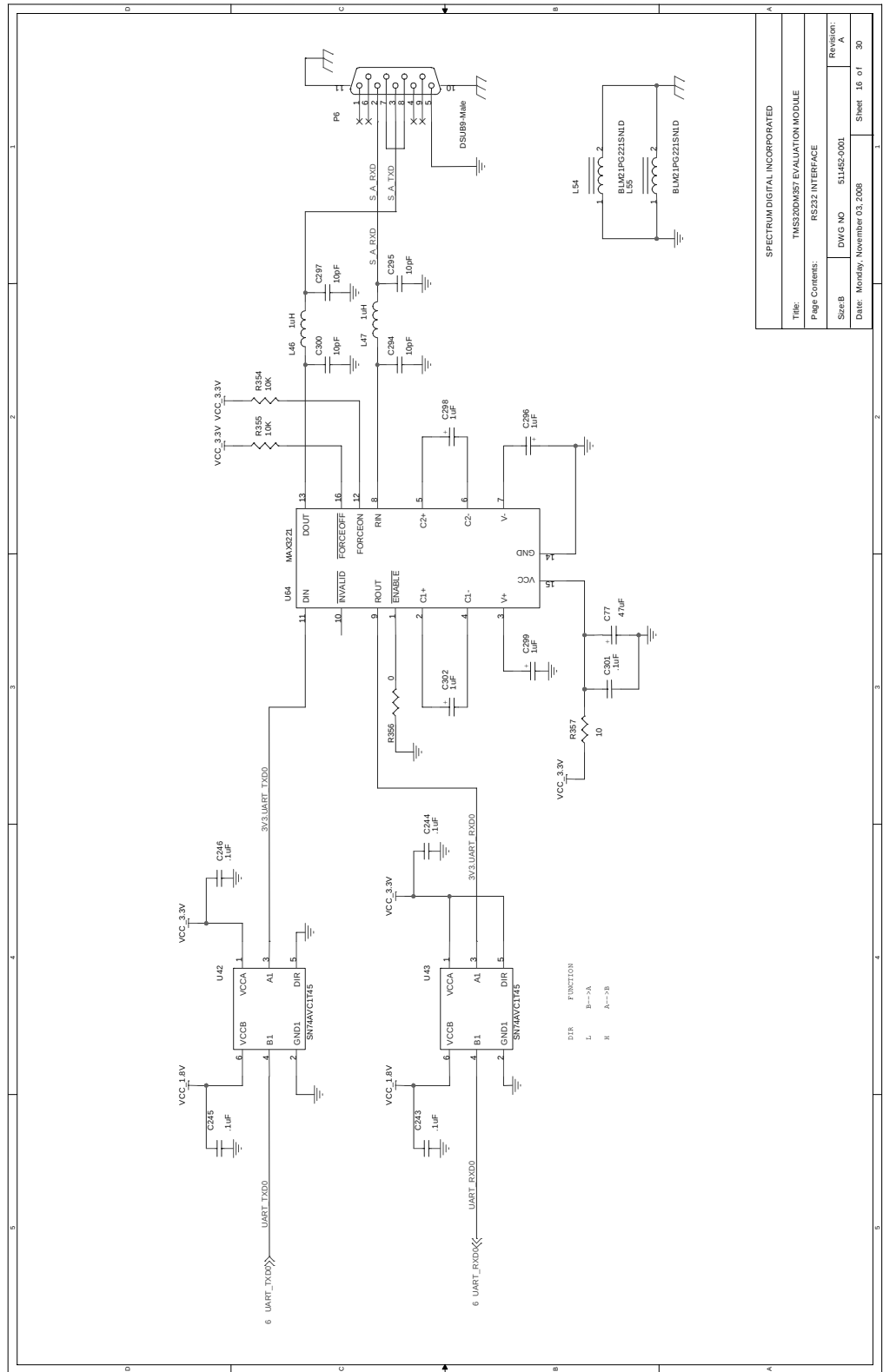
SPECTRUM DIGITAL INCORPORATED			
Title:	TMS320DM357 EVALUATION MODULE		
Page Comments:	DDR2 MEMORY		
Sheet:	DWG NO	511452-0001	Revision: 1.0
Date:	Monday, November 03, 2008		
Sheet	11	of	30





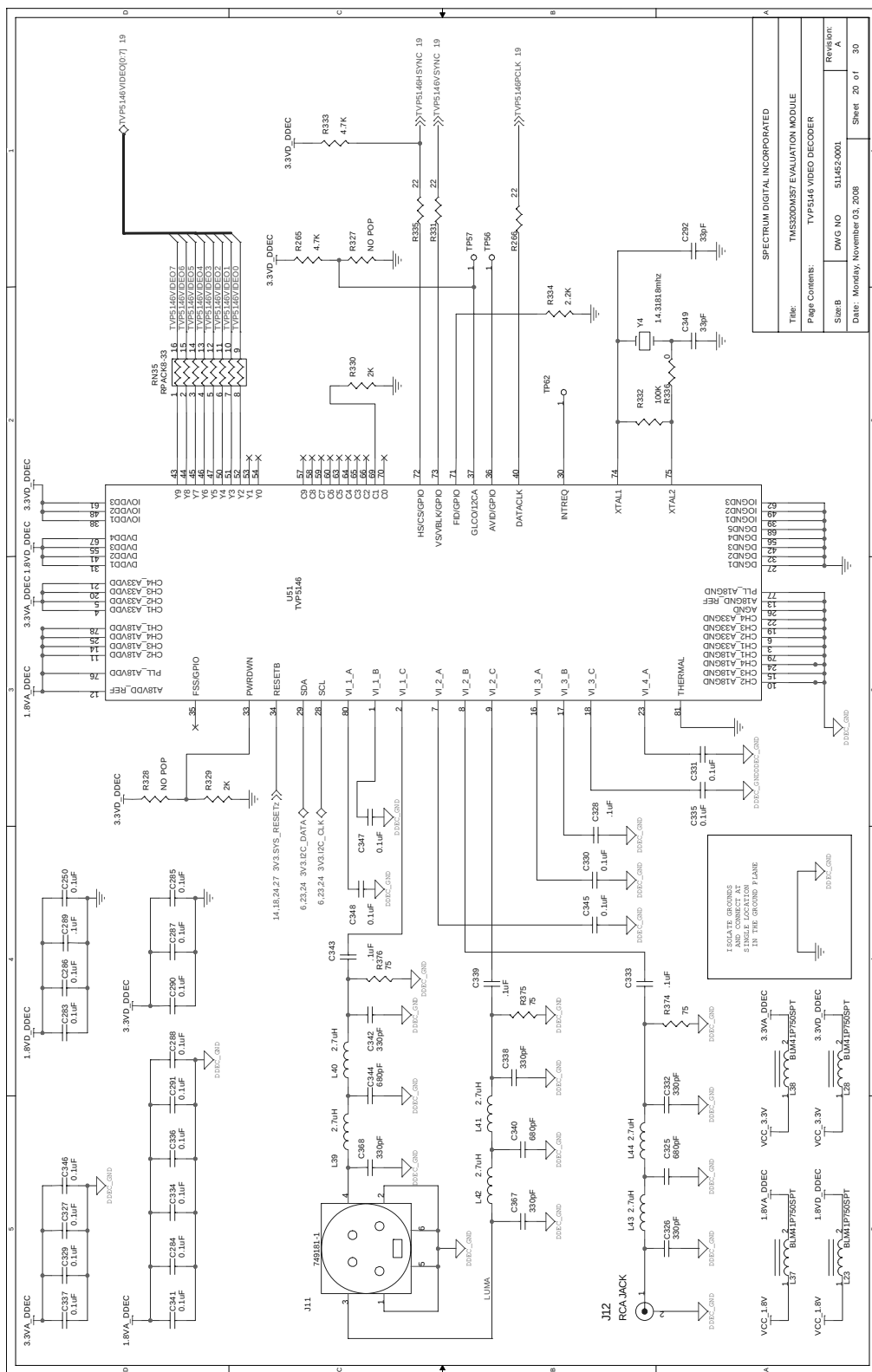


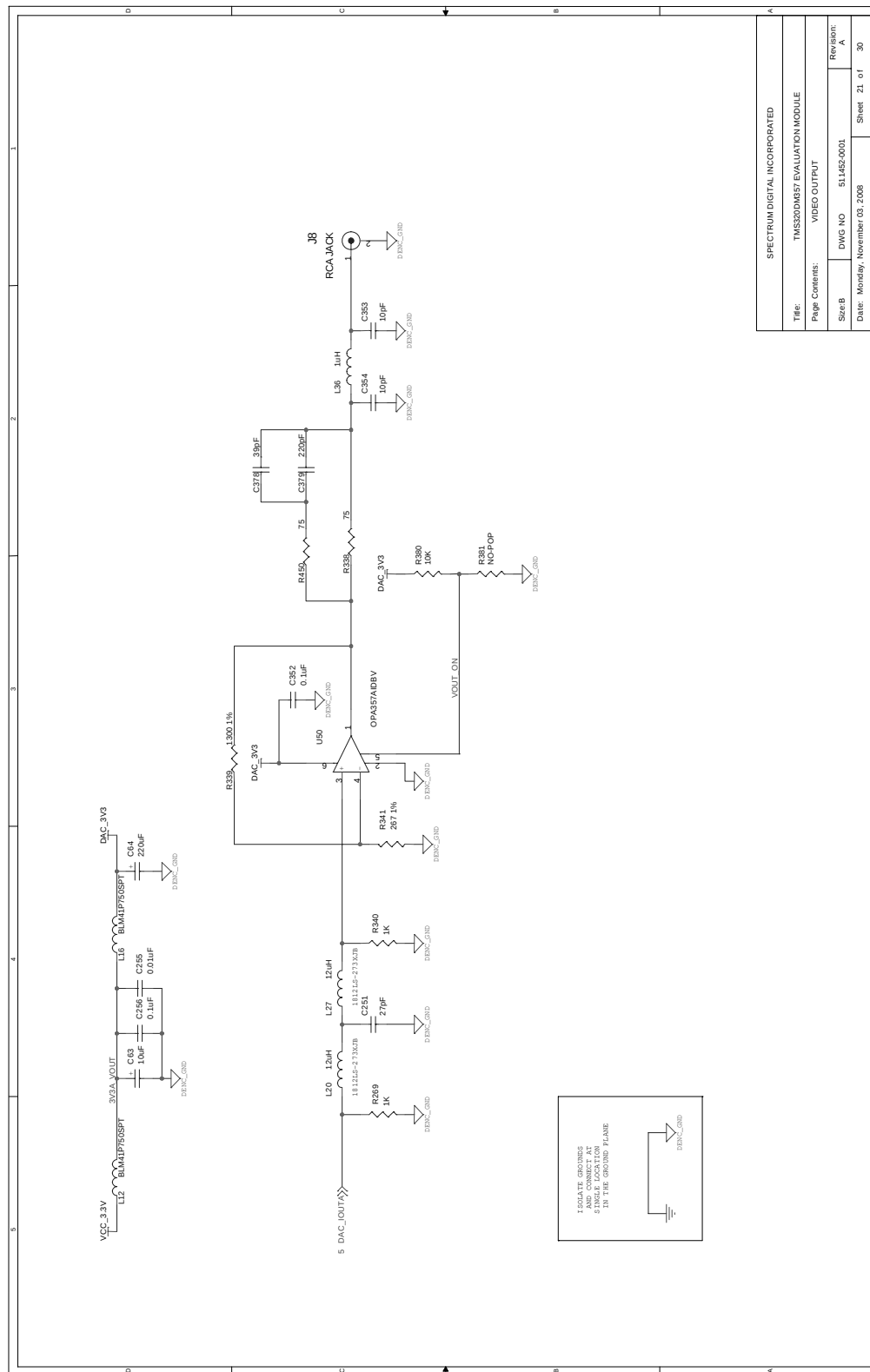


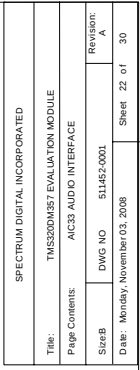


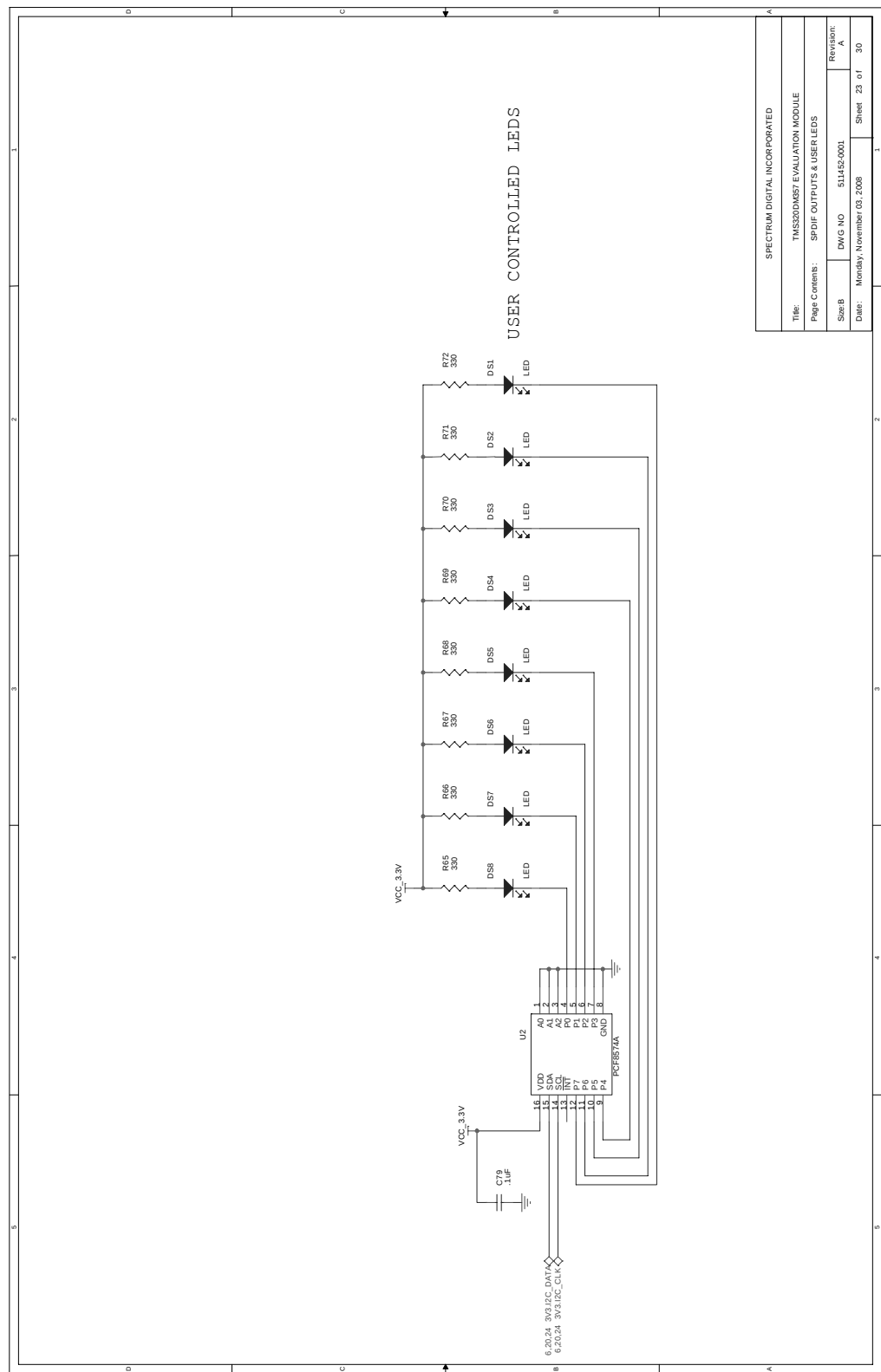


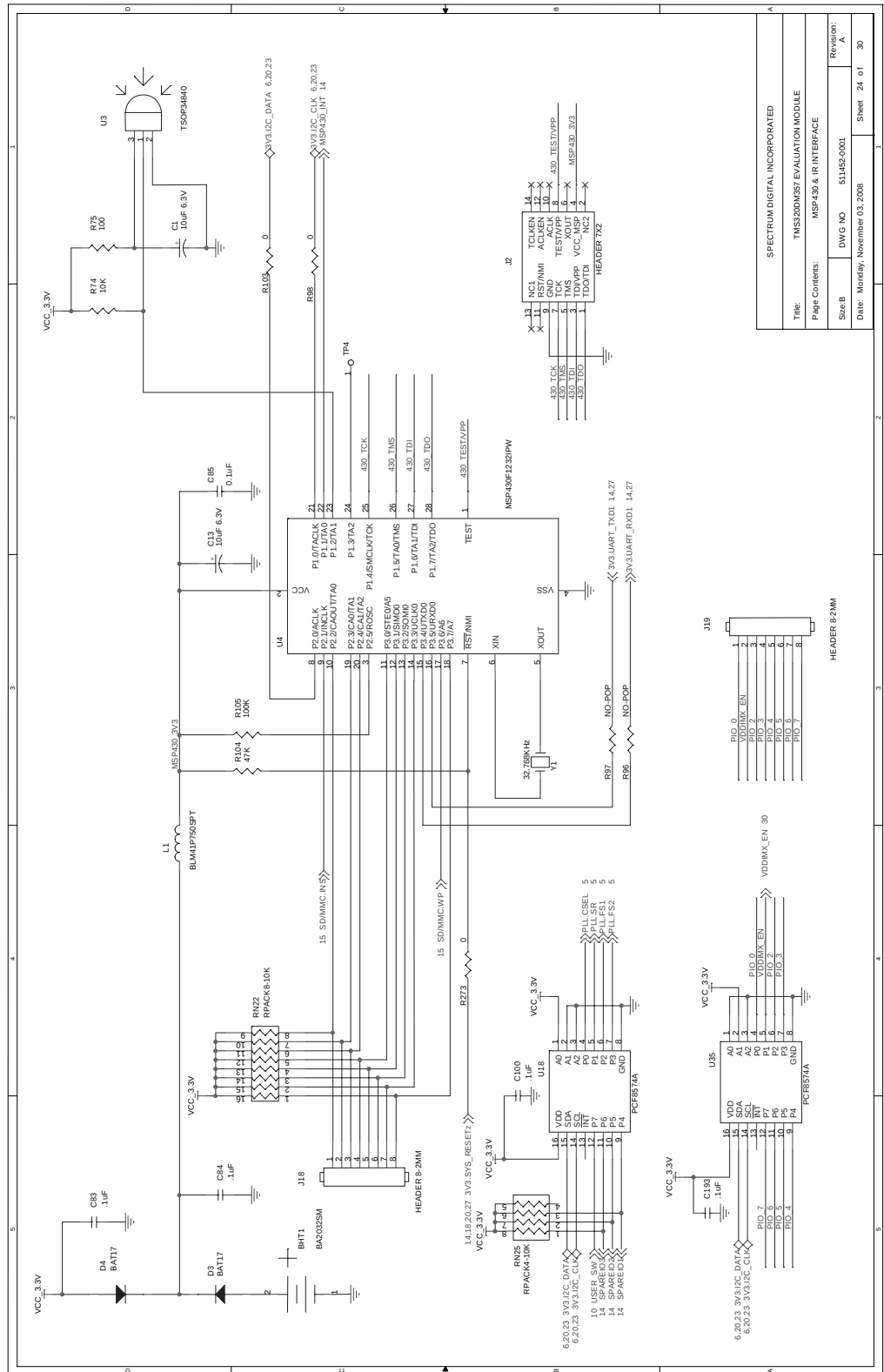


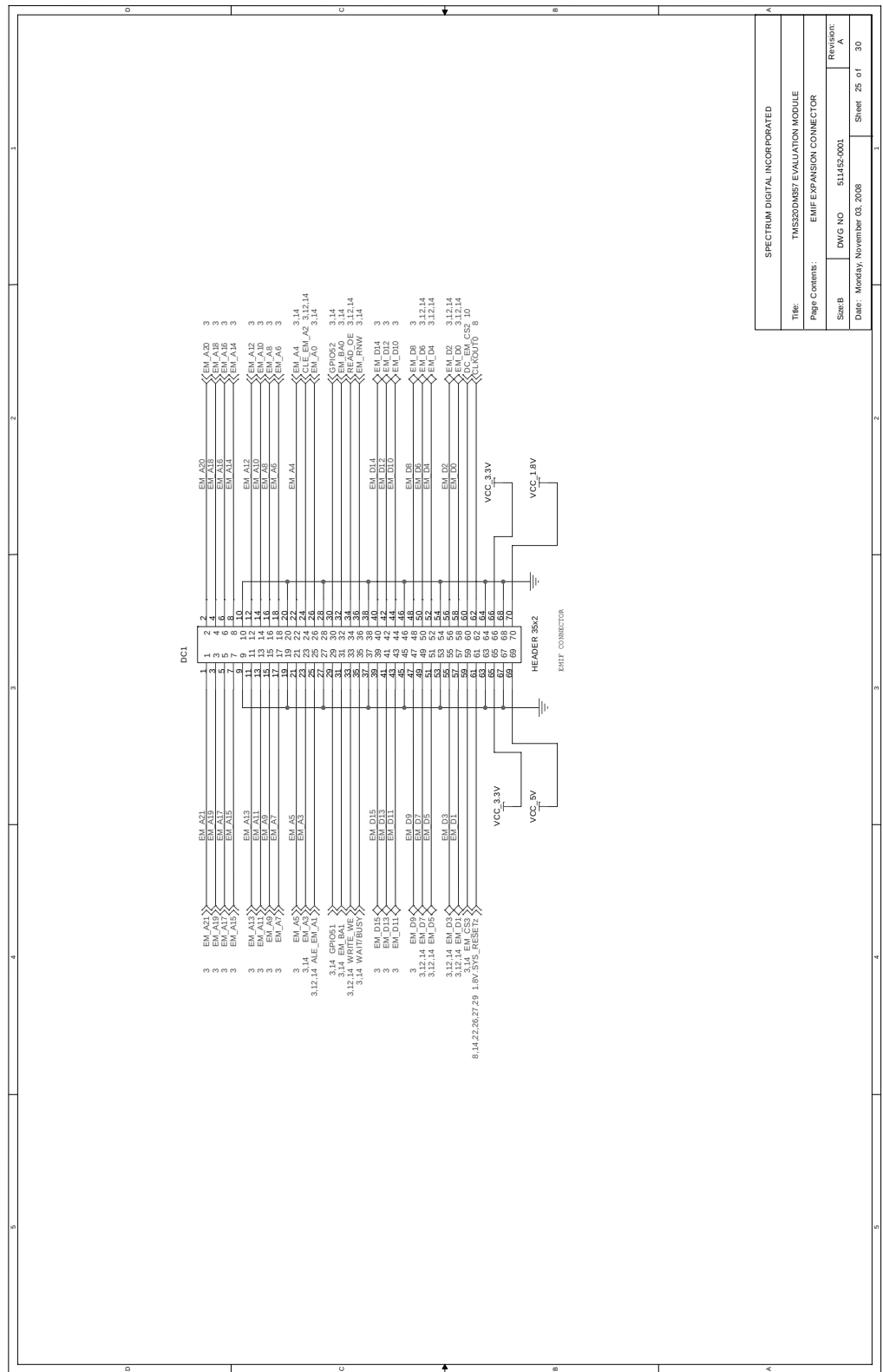






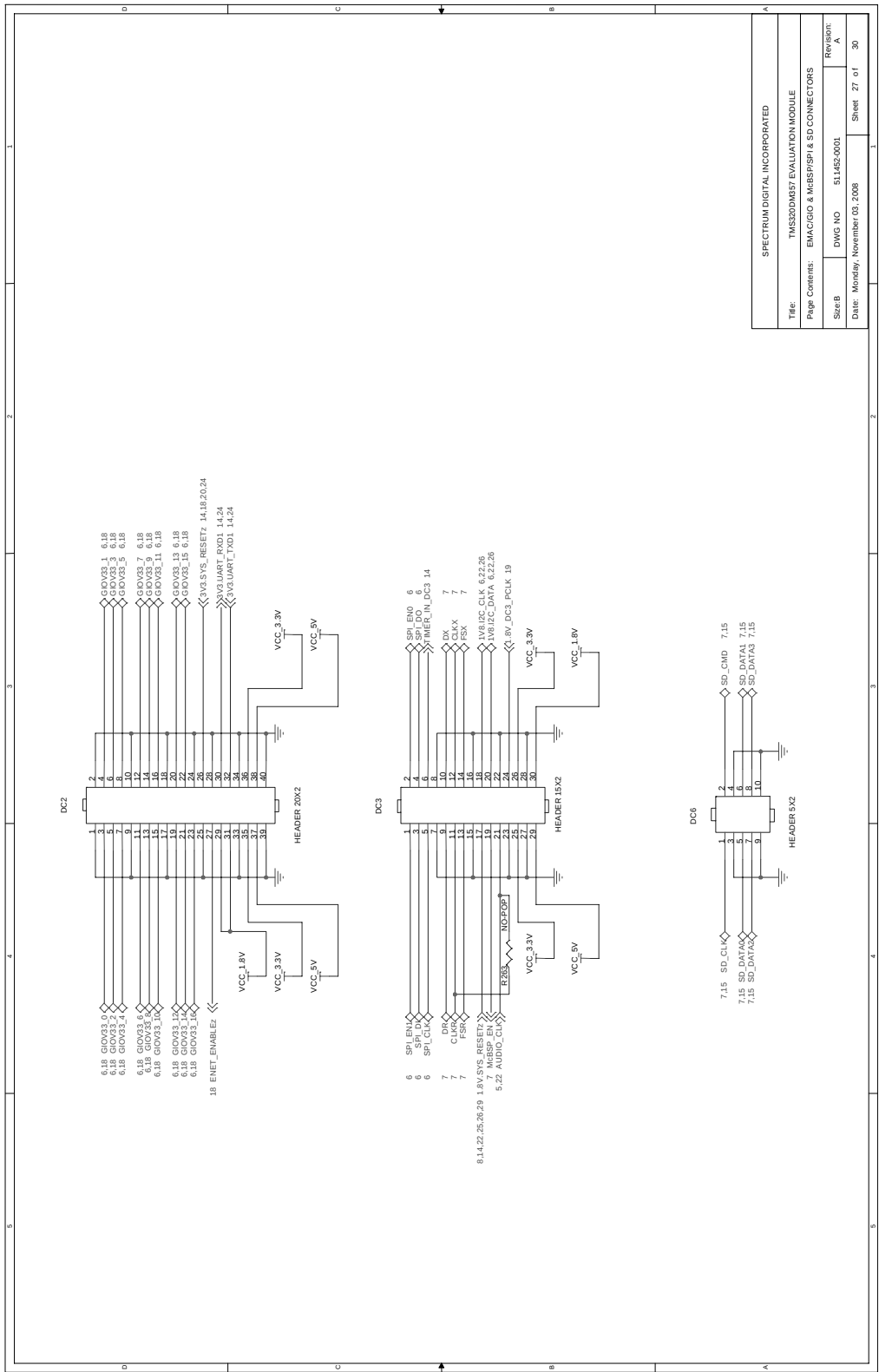




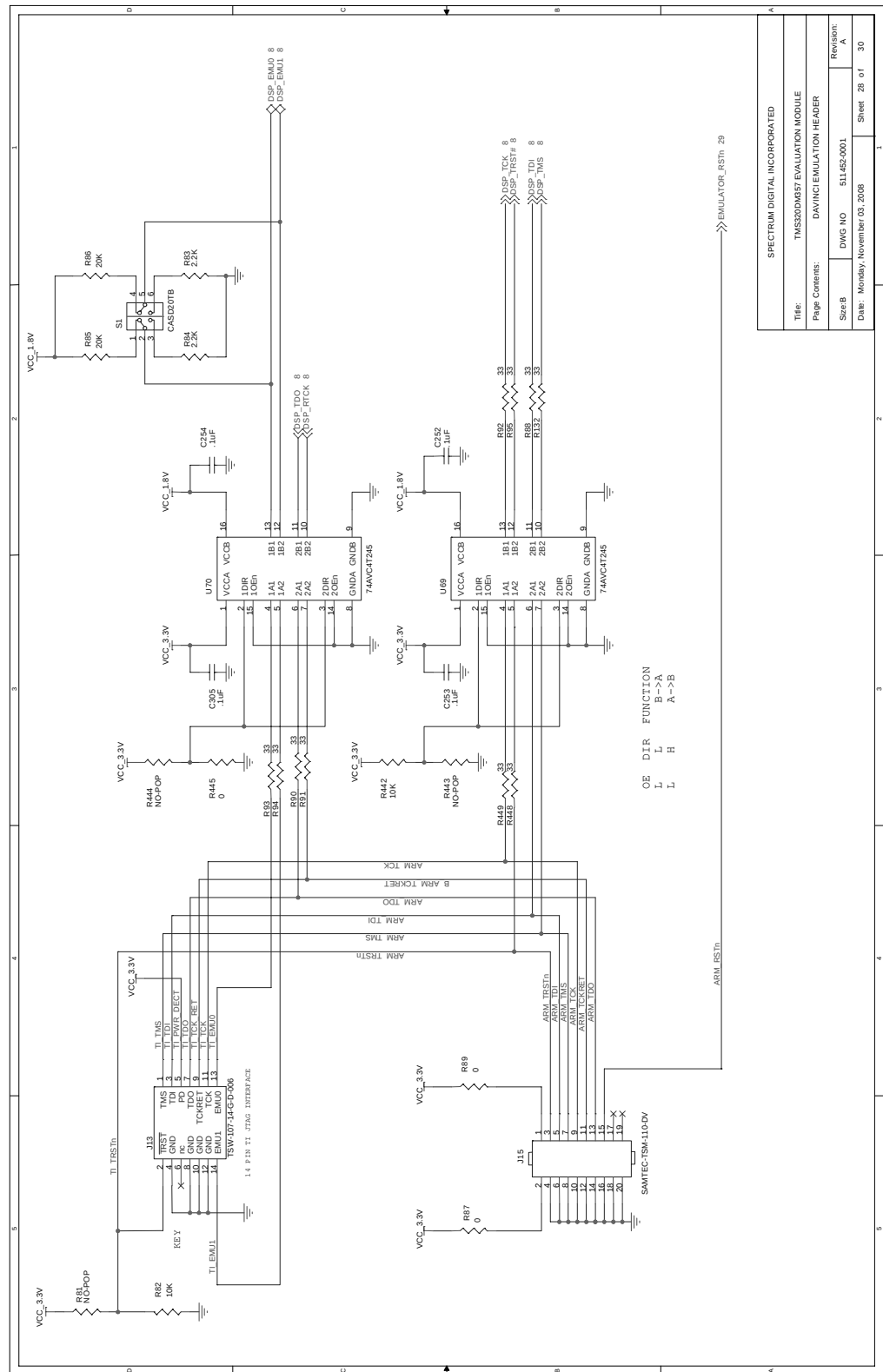


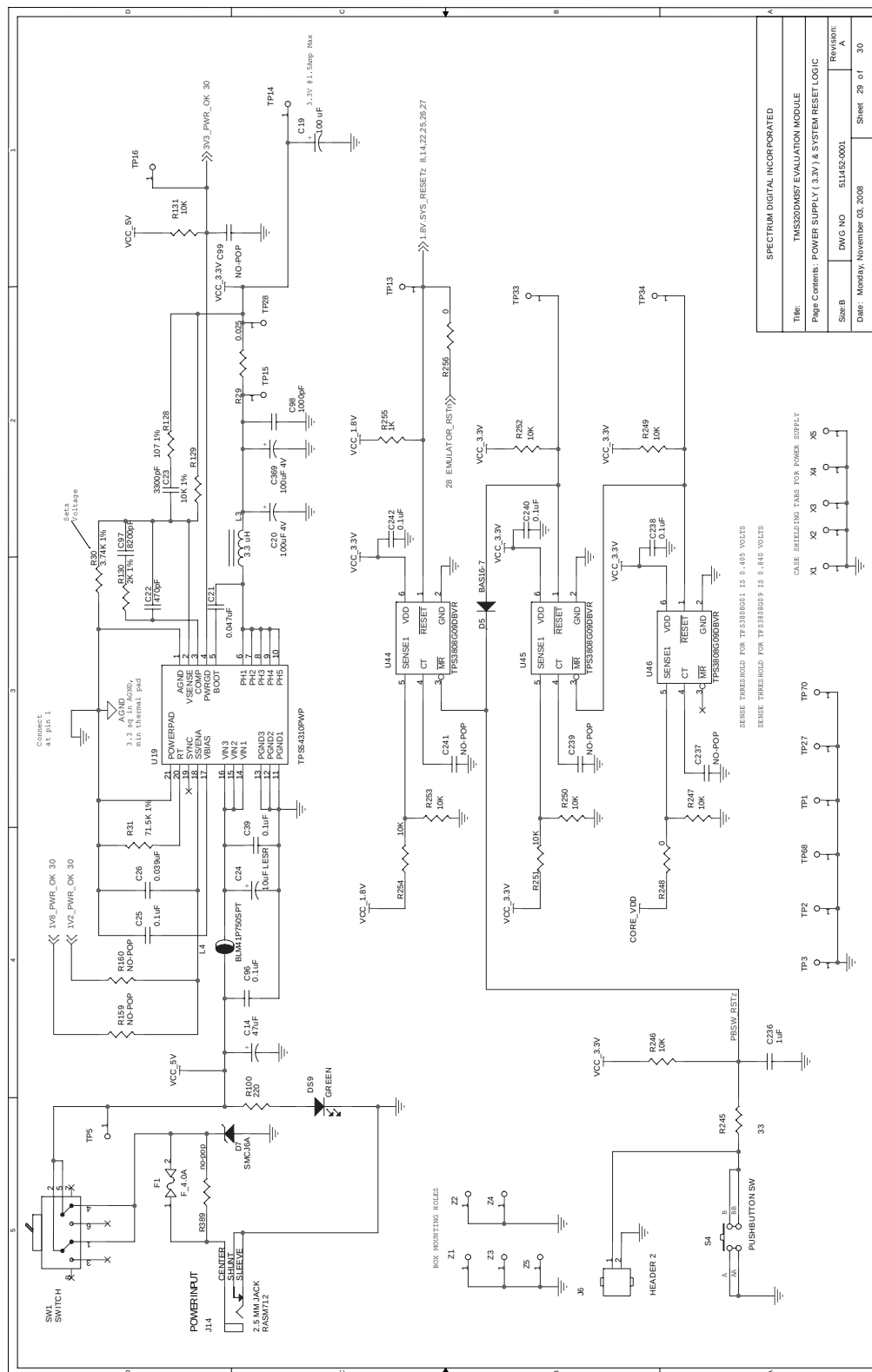
SPECTRUM DIGITAL INCORPORATED			
Title: TMS320DM357 EVALUATION MODULE			
Page Contents: EMIF EXPANSION CONNECTOR			
Size: B	DWG NO.	511452-0001	Revision: A
Date: Monday, November 03, 2008		Sheet	25 of 30

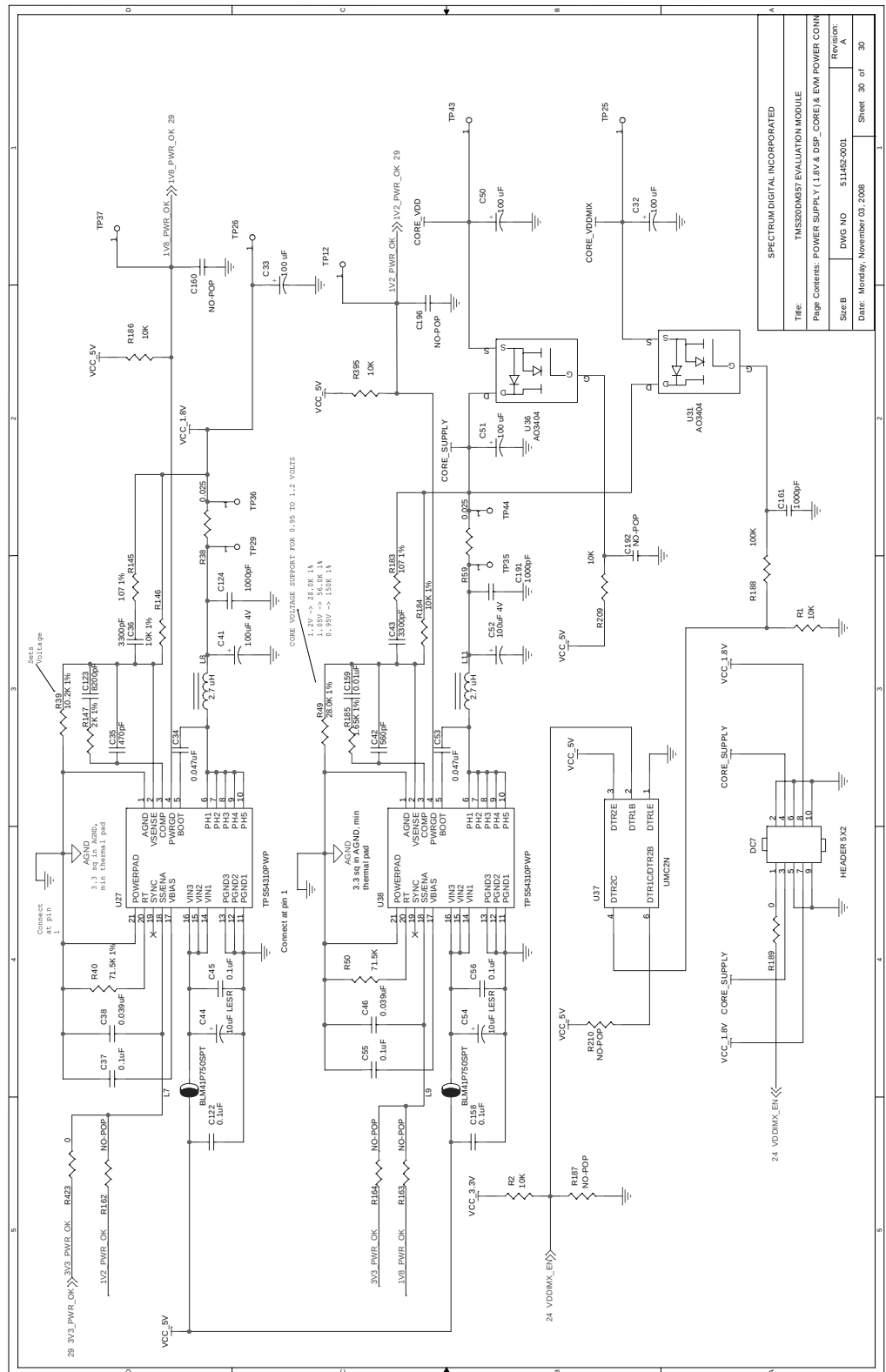




SPECTRUM DIGITAL INCORPORATED			
Title: TMS320DM357 EVALUATION MODULE			
Page Contents: EMAC/GIO & McBSP/SPI & SD CONNECTORS			
Size: B	DWG NO	511462-0001	Revision: A
Date: Monday, November 03, 2008	Sheet	27	of 30



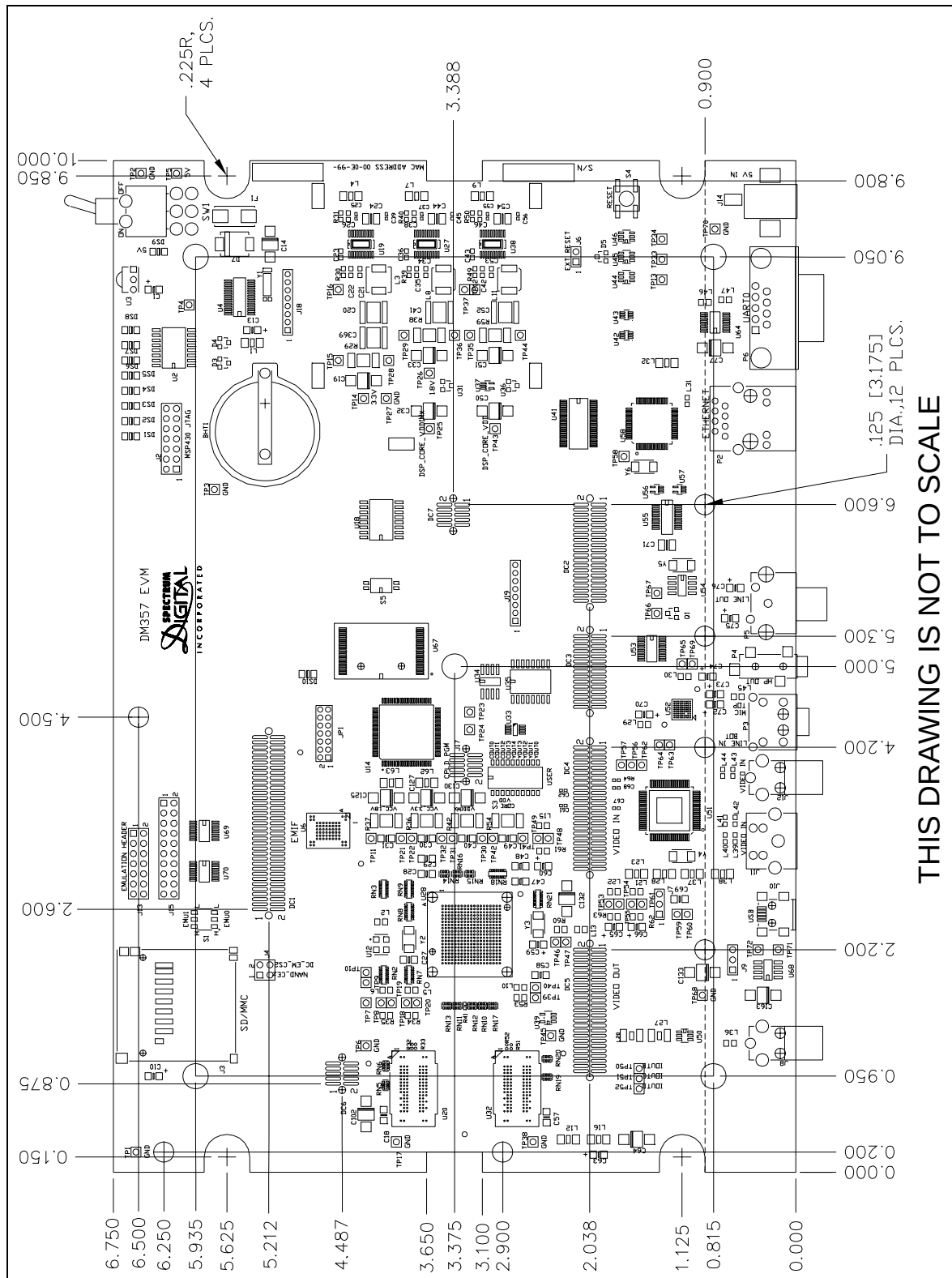


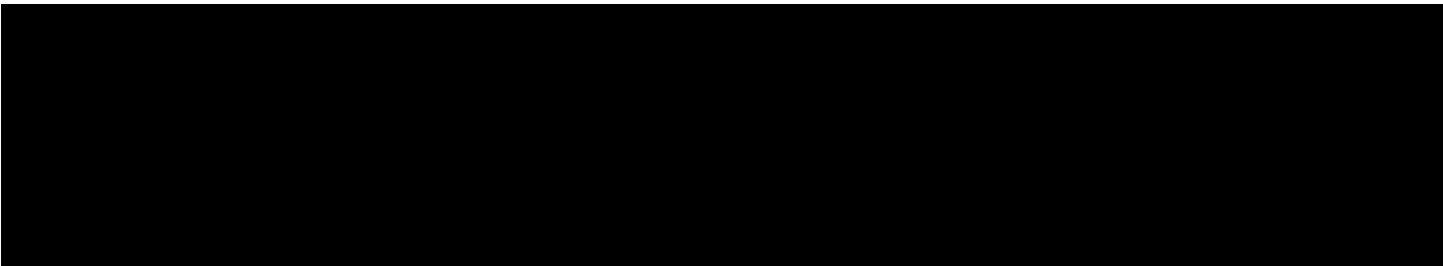


Appendix B

Mechanical Information

This appendix contains the mechanical information about the DM357 EVM produced by Spectrum Digital.





AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit www.ameya360.com

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype ameyasales1 ameyasales2

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com