

USB5533B

3-Port SS/HS USB Hub Controller

PRODUCT FEATURES

Datasheet

General Description

The SMSC USB5533B hub is a 3-port SuperSpeed/Hi-Speed, low-power, configurable hub controller family fully compliant with the *USB 3.0 Specification*. The USB5533B supports 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS) and 1.5 Mbps Low-Speed (LS) USB signalling for complete coverage of all defined USB operating speeds.

The USB5533B supports legacy USB speeds through its USB 2.0 hub controller. The new SuperSpeed hub controller operates in parallel with the USB 2.0 controller, so the 5 Gbps SuperSpeed data transfers are not affected by the slower USB 2.0 traffic.

The USB5533B supports battery charging on a per port basis. On battery charging enabled ports, the devices provide automatic USB data line handshaking. The handshaking supports USB 1.2 Charging Downstream Port (CDP), Dedicated Charging Port (DCP) and legacy devices.

The USB5533B is configured for operation through internal default settings, where custom configurations are supported through an on-chip OTP ROM, an external SPI ROM, or SMBus.

Features

- USB 3.0 compliant 5 Gbps, 480 Mbps, 12 Mbps and 1.5 Mbps operation, USB pins are 5 V tolerant
 - Integrated termination and pull-up/pull-down resistors
- Three downstream USB 3.0 ports
- Supports battery charging of most popular battery powered devices
 - USB-IF Battery Charging rev. 1.2 support (DCP & CDP)
 - Apple Portable product charger emulation
 - Blackberry charger emulation
 - Chinese YD/T 1591-2006 charger emulation
 - Chinese YD/T 1591-2009 charger emulation
 - Supports additional portable devices
- Emulates portable/handheld native wall chargers
 - Charging profiles emulate a handheld device's wall charger to enable fast charging (minutes vs. hours)
- Enables charging from a mobile platform that is off
- Support tablets' high current requirements
- Optimized for low-power operation and low thermal dissipation
- Vendor Specific Messaging (VSM) support for firmware upload over USB
- Configuration via OTP ROM, SPI ROM, or SMBus
- On-chip 8051 μ C manages VBUS, and other hub signals
- 8 K RAM, 32 K ROM
- One Time programmable (OTP) ROM: 8 kbit
 - Includes on-chip charge pump
- Single 25 MHz XTAL or clock input for all on-chip PLL and clocking requirements
- Supports JTAG boundary scan
- PHYBoost (USB 2.0)
 - Selectable drive strength for improved signal integrity
- VariSense (USB 2.0)
 - controls the receiver sensitivity enabling four programmable levels of USB signal receive sensitivity
- IETF RFC 4122 compliant 128-bit UUID

Software Features

- Compatible with Microsoft Windows 7, Vista, XP, Mac OSX10.4+, and Linux Hub Drivers

Datasheet

Order Numbers:

ORDER NUMBERS*	DESCRIPTION	ROHS COMPLIANT PACKAGE	TEMPERATURE RANGE
USB5533B-5000JZX	USB 3.0 3-Port Hub with VSM, Apple/BC 1.2 Charging & SMSC UCS1002 Control	64QFN 9 x 9mm 6.0 mm exposed pad	0°C to 70°C

* Add "TR" to the end of any order number to order tape and reel. Reel size is 2500 pieces.

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smssc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

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Conventions

Within this manual, the following abbreviations and symbols are used to improve readability.

Example	Description
BIT	Name of a single bit within a field
FIELD.BIT	Name of a single bit (BIT) in FIELD
x...y	Range from x to y, inclusive
BITS[m:n]	Groups of bits from m to n, inclusive
PIN	Pin Name
zzzzb	Binary number (value zzzz)
0xzzz	Hexadecimal number (value zzz)
zzh	Hexadecimal number (value zz)
rsvd	Reserved memory location. Must write 0, read value indeterminate
code	Instruction code, or API function or parameter
<i>Section Name</i>	Section or Document name
x	Don't care
<Parameter>	<> indicate a Parameter is optional or is only used under some conditions
{,Parameter}	Braces indicate Parameter(s) that repeat one or more times
[Parameter]	Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters.

Table of Contents

Chapter 1	Block Diagram	8
Chapter 2	Overview	9
2.1	Configurable Features	9
Chapter 3	Pin Information	10
3.1	Pin Configurations	10
3.2	Pin Descriptions (Grouped by Function)	11
3.3	Buffer Type Descriptions	15
Chapter 4	Configuration Options	16
4.1	SPI ROM	16
4.2	SMBus	16
4.2.1	SMBus Legacy Mode	16
4.2.2	SMBus Advanced Mode	16
Chapter 5	Interfacing to the USB5533B	17
5.1	SPI Interface	17
5.1.1	Operation of the Hi-Speed Read Sequence	17
5.1.2	Operation of the Dual Hi-Speed Read Sequence	18
5.1.3	32-Byte Cache	19
5.1.4	Interface Operation to SPI Port When Not Doing Fast Reads	19
5.1.5	SPI Timing	23
5.2	SMBus Slave Interface	24
5.2.1	Pull-Up Resistor for SMBus	24
5.2.2	Protocol Implementation	24
5.2.3	Slave Device Timeout	25
5.2.4	Stretching the SCLK Signal	25
5.2.5	Bus Reset Sequence	26
5.2.6	SMBus Alert Response Address	26
5.2.7	SMBus Timing	26
5.3	Reset	27
5.3.1	Internal POR	27
5.3.2	External Hardware Reset	27
Chapter 6	DC Parameters	28
6.1	Maximum Guaranteed Ratings	28
6.2	Operating Conditions	29
6.3	Power Consumption	30
6.4	DC Electrical Characteristics	30
6.5	Capacitance	32
Chapter 7	AC Specifications	33
7.1	Oscillator/Crystal	33
7.2	External Clock	34
7.2.1	SMBus Clock	34
7.2.2	USB 2.0	34
Chapter 8	Package Drawing	35

Chapter 9 Datasheet Revision History	37
Appendix A (Acronyms)	39
Appendix B (References)	40

Datasheet**List of Figures**

Figure 1.1	USB5533B Block Diagram	8
Figure 3.1	USB5533B 64-Pin QFN	10
Figure 5.1	SPI Hi-Speed Read Operation	17
Figure 5.2	SPI Hi-Speed Read Sequence	18
Figure 5.3	SPI Dual Hi-Speed Read Operation	18
Figure 5.4	SPI Dual Hi-Speed Read Sequence	19
Figure 5.5	SPI Internally-Controlled Operation	19
Figure 5.6	SPI Erase Sequence	20
Figure 5.7	SPI Byte Program	20
Figure 5.8	SPI Command Only Sequence	21
Figure 5.9	SPI JEDEC-ID Sequence	22
Figure 5.10	SPI Timing	23
Figure 5.11	SMBus Slave Connection	24
Figure 5.12	Block Write	25
Figure 5.13	Block Read	25
Figure 5.14	SMBus Slave Timing Diagram	26
Figure 6.1	Supply Rise Time Model	29
Figure 7.1	Typical Crystal Circuit	33
Figure 7.2	Formula to Find the Value of C1 and C2	33
Figure 8.1	USB5533B 64 Pin QFN Package	35
Figure 8.2	USB5533B Recommended PCB Land Pattern	36

List of Tables

Table 3.1	USB5533B Pin Descriptions	11
Table 3.2	PRT_PWR[3:1] Configuration Strap States	14
Table 3.3	Buffer Type Descriptions	15
Table 5.1	SPI Timing Operation	23
Table 5.2	SMBus Slave Timing Modes	26
Table 6.1	DC Electrical Characteristics	30
Table 6.2	Pin Capacitance	32
Table 7.1	Crystal Circuit Legend	33
Table 8.1	USB5533B 64-Pin QFN Dimensions	35
Table 8.2	USB5533B Recommended PCB Land Pattern Dimensions	36
Table 9.1	Customer Revision History	37

Chapter 1 Block Diagram

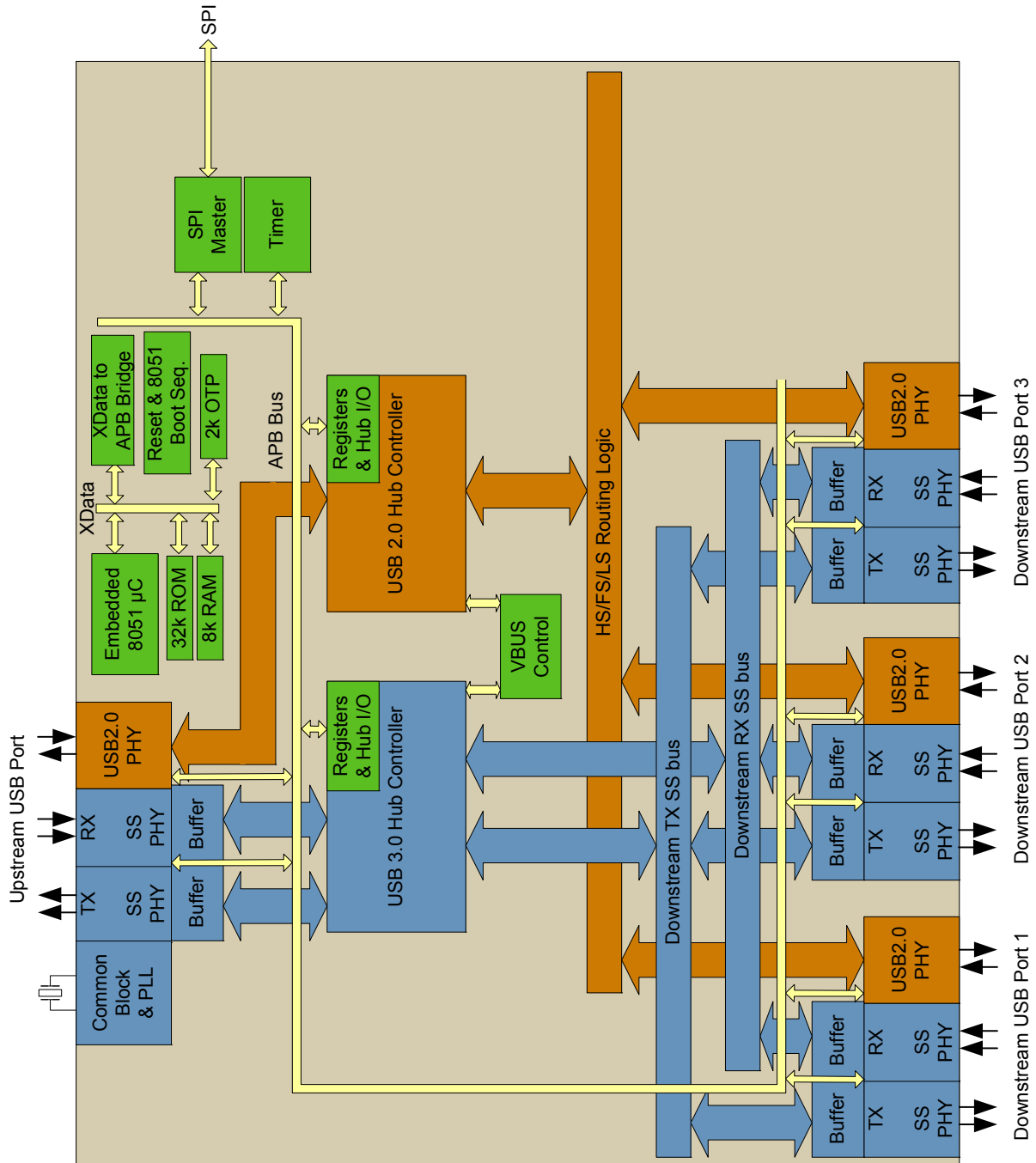


Figure 1.1 USB5533B Block Diagram

Chapter 2 Overview

The SMSC USB5533B hub is a 3-port, low-power, configurable Hub Controller fully compliant with the *USB 3.0 Specification* [2]. The USB5533B supports 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS) and 1.5 Mbps Low-Speed (LS) USB signalling for complete coverage of all defined USB operating speeds.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors and all required pull-down and pull-up resistors on D+ and D- pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

The USB5533B hub includes programmable features such as:

- **MultiTRAK™ Technology:** implements a dedicated Transaction Translator (TT) for each port. Dedicated TTs help maintain consistent full-speed data throughput regardless of the number of active downstream connections.
- **PortSwap:** allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.
- **PHYBoost:** enables 4 programmable levels of USB signal drive strength in downstream port transceivers. PHYBoost will also attempt to restore USB signal integrity.

2.1 Configurable Features

The SMSC USB5533B hub controller provides a default configuration that is sufficient for most applications. When the hub is initialized in the default configuration, the following features may be configured:

- Downstream non-removable ports, where the hub will automatically report as a compound device
- Downstream disabled ports
- Downstream port power control and over-current detection on a ganged or individual basis
- USB signal drive strength
- USB differential pair pin location

The USB5533B hub controllers can alternatively be configured by OTP or as an SMBus slave device. When the hub is configured by an OTP or over SMBus, the following configurable features are provided:

- Support for compound devices on a port-by-port basis
- Selectable over-current sensing and port power control on an individual or ganged basis to match the circuit board component selection
- Customizable vendor ID, product ID, and device ID
- Configurable delay time for filtering the over-current sense inputs
- Indication of the maximum current that the hub consumes from the USB upstream port
- Indication of the maximum current required for the hub controller
- Custom string descriptors (up to 30 characters):
Product, manufacturer, and serial number

Chapter 3 Pin Information

This chapter outlines the pinning configurations for each chip. The detailed pin descriptions are listed by function in [Section 3.2: Pin Descriptions \(Grouped by Function\)](#) on page 11.

3.1 Pin Configurations

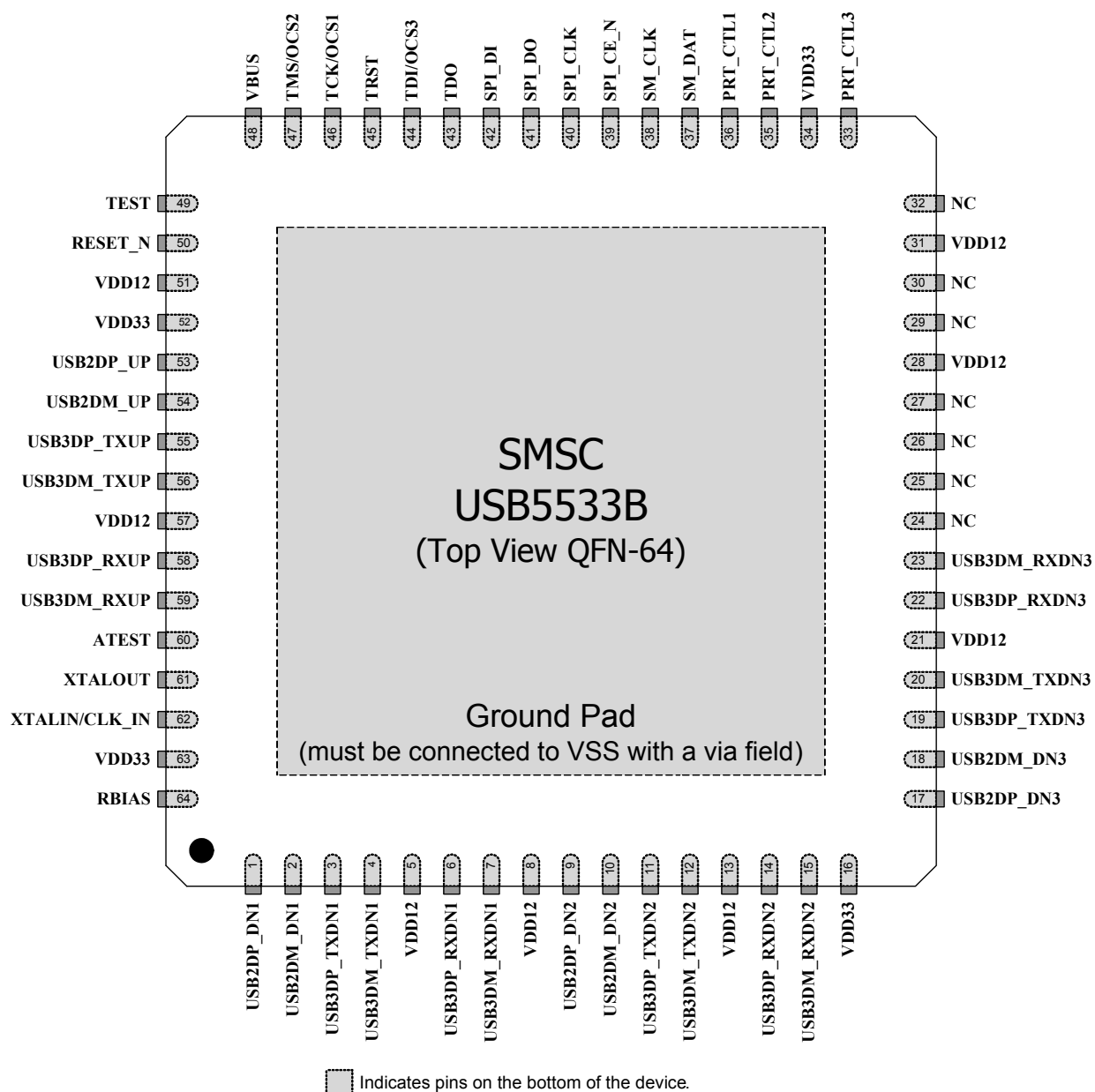


Figure 3.1 USB5533B 64-Pin QFN

3.2 Pin Descriptions (Grouped by Function)

An *N* at the end of a signal name indicates that the active (asserted) state occurs when the signal is at a low voltage level. When the *N* is not present, the signal is asserted when it is at a high voltage level. The terms assertion and negation are used exclusively in order to avoid confusion when working with a mixture of active low and active high signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Table 3.1 USB5533B Pin Descriptions

SYMBOL	BUFFER TYPE	DESCRIPTION
USB 3.0 INTERFACE		
USB3DP_TXUP	IO-U	USB 3 Upstream Upstream SuperSpeed transmit data plus
USB3DM_TXUP	IO-U	USB 3 Upstream Upstream SuperSpeed transmit data minus
USB3DP_RXUP	IO-U	USB 3 Upstream Upstream SuperSpeed receive data plus
USB3DM_RXUP	IO-U	USB 3 Upstream Upstream SuperSpeed receive data minus
USB3DP_TXDN[3:1]	IO-U	USB 3 Downstream Downstream SuperSpeed transmit data plus for ports 1 through 3.
USB3DM_TXDN[3:1]	IO-U	USB 3 Downstream Downstream SuperSpeed transmit data minus for ports 1 through 3.
USB3DP_RXDN[3:1]	IO-U	USB 3 Downstream Downstream SuperSpeed receive data plus for ports 1 through 3.
USB3DM_RXDN[3:1]	IO-U	USB 3 Downstream Downstream SuperSpeed receive data minus for ports 1 through 3.
USB 2.0 INTERFACE		
USB2DP_UP	IO-U	USB Bus Data These pins connect to the upstream USB bus data signals.
USB2DM_UP	IO-U	USB Bus Data These pins connect to the upstream USB bus data signals.
USB2DP_DN[3:1]	IO-U	USB Downstream Downstream Hi-Speed data plus for ports 1 through 3.
USB2DM_DN[3:1]	IO-U	USB Downstream Downstream Hi-Speed data minus for ports 1 through 3.

Table 3.1 USB5533B Pin Descriptions (continued)

SYMBOL	BUFFER TYPE	DESCRIPTION
USB PORT CONTROL		
PRT_PWR[3:1]/ PRT_CTL[3:1]	O12	USB Power Enable Enables power to USB peripheral devices downstream. Note: This pin also provides configuration strap functions. See Note 3.1 .
VBUS	I	Upstream VBUS Power Detect This pin can be used to detect the state of the upstream bus power.
SPI INTERFACE (4 PINS)		
SPI_CE_N	O12	SPI Enable
SPI_CLK	O12	SPI Clock
SPI_DO	O12	SPI Serial Data Out The output for the SPI port. Note: This pin also provides configuration strap functions. See Note 3.2 .
SPI_DI	I	SPI Serial Data In The SPI data in to the controller from the ROM. This pin has a weak internal pull-down applied at all times to prevent floating.
JTAG/OCS INTERFACE		
TRST	I	JTAG Asynchronous Reset Note: If using the SMBus interface, a pull-up on this signal will enable Legacy Mode, while leaving it unconnected or pulled-down will enable Advanced Mode. Note: Only available in test mode.
TCK	I	JTAG Clock This input is used for JTAG boundary scan and has a weak pull-down. It can be left floating or grounded when not used. If the JTAG is connected, then this signal will be detected high, and the software disables the pull up after reset. Note: Only available in test mode.
OCS1		Over-Current Sense 1 Input from external current monitor indicating an over-current condition. Note: This pin also provides configuration strap functions. See Note 3.3 .

Table 3.1 USB5533B Pin Descriptions (continued)

SYMBOL	BUFFER TYPE	DESCRIPTION
TMS	I	JTAG TMS Used for JTAG boundary scan. Note: Only available in test mode.
OCS2		Over-Current Sense 2 Input from external current monitor indicating an over-current condition. Note: This pin also provides configuration strap functions. See Note 3.3 .
TDI	I	JTAG TDI Used for JTAG boundary scan. Note: Only available in test mode.
OCS3		Over-Current Sense 3 Input from external current monitor indicating an over-current condition. Note: This pin also provides configuration strap functions. See Note 3.3 .
TDO	O12	JTAG TDO Used for JTAG boundary scan. Note: Only available in test mode.
MISC		
RESET_N	IS	Reset Input The system uses this active low signal to reset the chip. The active low pulse should be at least 1 μ s wide.
XTALIN	ICLKx	Crystal Input: 25 MHz crystal. This pin connects to either one terminal of the crystal or to an external 25 MHz clock when a crystal is not used.
CLK_IN		External Clock Input This pin connects to either one terminal of the crystal or to an external 25 MHz clock when a crystal is not used.
XTALOUT	OCLKx	Crystal Output The clock output, providing a crystal 25 MHz. When an external clock source is used to drive XTALIN/CLK_IN, this pin becomes a no connect.
TEST	IPD	Test Pin Treat as a no connect pin or connect to ground. No trace or signal should be routed or attached to this pin.
RBIAS	I-R	USB Transceiver Bias A12.0 k Ω (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.

Table 3.1 USB5533B Pin Descriptions (continued)

SYMBOL	BUFFER TYPE	DESCRIPTION
ATEST	A	Analog Test Pin This signal is used for testing the chip and must always be connected to ground.
SM_CLK	I/O12	SMBus Clock
SM_DAT	I/O12	SMBus Data Pin
(7) NC	-	No connect pins
DIGITAL AND POWER		
(4) VDD33		3.3 V Power
(8) VDD12		1.25 V Power
VSS		Ground Pad This exposed pad is the device's only connection to VSS and the primary thermal conduction path. Connect to an appropriate via field.

Note 3.1 The PRT_PWR[3:1] pins can optionally provide additional configuration strap functions to enable/disable the associated port and configure its battery charging capabilities. Configuration strap values are latched on device reset. [Table 3.2](#) details the functions associated with the various strap settings.

Strapping features are enabled by default and can be optionally disabled via the SMSC Pro-Touch software programming tool. For additional information on the Pro-Touch programming tool, contact your local SMSC sales representative.

Strapping functions are not supported for designs that support OCS but not power switching.

Table 3.2 PRT_PWR[3:1] Configuration Strap States

PRT_PWR[3:1] STRAP SETTING	PORT STATE	BATTERY CHARGING
No Pull-Up or Pull-Down	Enabled	Disabled
Pull-Down: <10 k Ω to VSS	Disabled	N/A
Pull-Up: <10 k Ω and >1 k Ω to VDD33	Enabled	Enabled

Note 3.2 The SPI_DO pin provides an additional SPI_SPD_SEL configuration strap function. SPI_SPD_SEL selects between the 30MHz SPI Mode when pulled-down to ground (default) and the 60MHz SPI Mode when pulled-up to VDD33. The SPI_SPD_SEL strap value is latched on Power-On Reset (POR) or RESET_N deassertion.

Note 3.3 The OCS[3:1] pins can optionally provide additional configuration strap functions. To set the associated port into the non-removable state, the OCS pin must be configured with a pull-down (<10 k Ω to VSS). Otherwise, the port will be configured in the removable state. Configuration strap values are latched on device reset.

Strapping features are enabled by default and can be optionally disabled via the SMSC Pro-Touch software programming tool. For additional information on the Pro-Touch programming tool, contact your local SMSC sales representative.

Strapping functions are not supported for designs that support OCS but not power switching.

3.3 Buffer Type Descriptions

Table 3.3 Buffer Type Descriptions

BUFFER TYPE	DESCRIPTION
I	Input
I/O	Input/output
IPD	Input with internal weak pull-down resistor
IPU	Input with internal weak pull-up resistor
IS	Input with Schmitt trigger
O12	Output 12 mA
I/O12	Input/output buffer with 12 mA sink and 12 mA source
I/OSD12	Open drain with Schmitt trigger and 12 mA sink.
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I-R	RBIAS
I/O-U	Analog input/output defined in USB specification

Chapter 4 Configuration Options

The USB5533B must be configured in order to correctly function when attached to a USB host controller. The hub can be configured either internally or externally depending on the implemented interface (see [Chapter 5: Interfacing to the USB5533B on page 17](#) for details).

4.1 SPI ROM

When the SPI interface is configured, the USB5533B will perform code execution from an external SPI ROM.

4.2 SMBus

Two SMBus modes (based on the used slave address) are available: Legacy and Advanced.

4.2.1 SMBus Legacy Mode

The SMBus Legacy Mode provides access to all internal USB 2.0 registers, and is enabled based on the 7-bit slave address of 0101100b. The hub will not respond to the general call address of 0000000b.

4.2.2 SMBus Advanced Mode

The SMBus Advanced Mode provides access to all USB 2.0 and USB 3.0 registers, and is enabled based on the 7-bit slave address of 0101101b. The hub will not respond to the general call address of 0000000b. The protocol is based on the SMBus block read/write, except the register offset is extended to 16 bits (high byte, low byte).

Chapter 5 Interfacing to the USB5533B

The hub will interface to external memory depending on configuration of the USB5533B pins associated with each interface type. The USB5533B will first check to see whether an external SPI Flash is present. If not, the USB5533B will operate from internal ROM. If SPI Flash is present, the chip will operate from the external ROM. Next, the USB5533B will look to receive configuration and commands from an optional SMBus master (if present). When SMBus is enabled, the SMBus can operate in either legacy (USB 2.0 only) or advanced mode (access to both USB 2.0 and 3.0 registers). Next, the USB5533B will look for (optional) configuration present in the internal OTP memory. Any register settings that are modified via the SMBus interface will overwrite the internal OTP settings.

5.1 SPI Interface

The USB5533B is capable of code execution from an external SPI ROM. On power up, the firmware looks for an external SPI flash device that contains a valid signature of 2DFU (device firmware upgrade) beginning at address 0xFFFFA. If a valid signature is found, then the external ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM. The following sections describe the interface options to the external SPI ROM.

5.1.1 Operation of the Hi-Speed Read Sequence

The SPI controller will automatically handle code reads going out to the SPI ROM Address. When the controller detects a read, the controller drops the **SPI_CE**, and puts out a 0x0B, followed by the 24-bit address. The SPI controller then puts out a DUMMY byte. The next eight clocks clock in the first byte. When the first byte is clocked in a ready signal is sent back to the processor, and the processor gets one byte.

After the processor gets the first byte, its address will change. If the address is one more than the last address, the SPI controller will clock out one more byte. If the address is anything other than one more than the last address, the SPI controller will terminate the transaction by taking **SPI_CE** high. As long as the addresses are sequential, the SPI Controller will keep clocking in data.

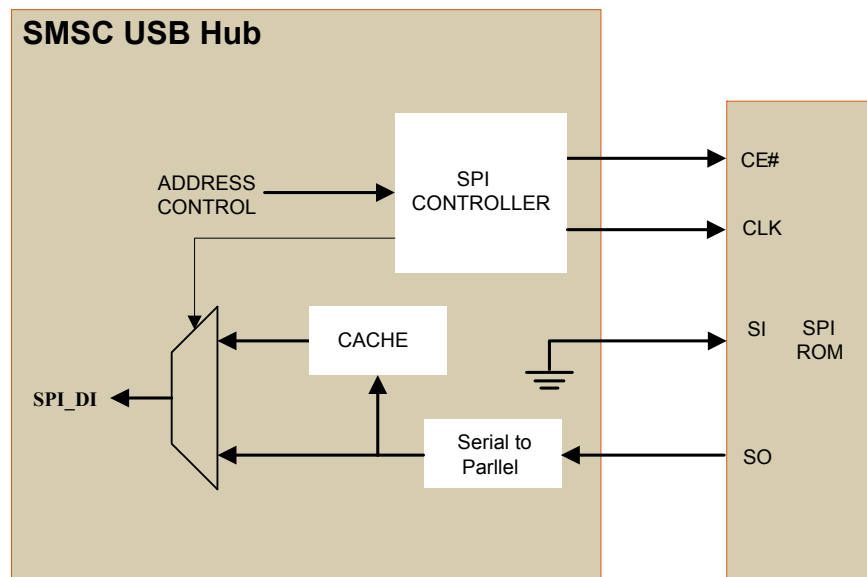


Figure 5.1 SPI Hi-Speed Read Operation

Datasheet

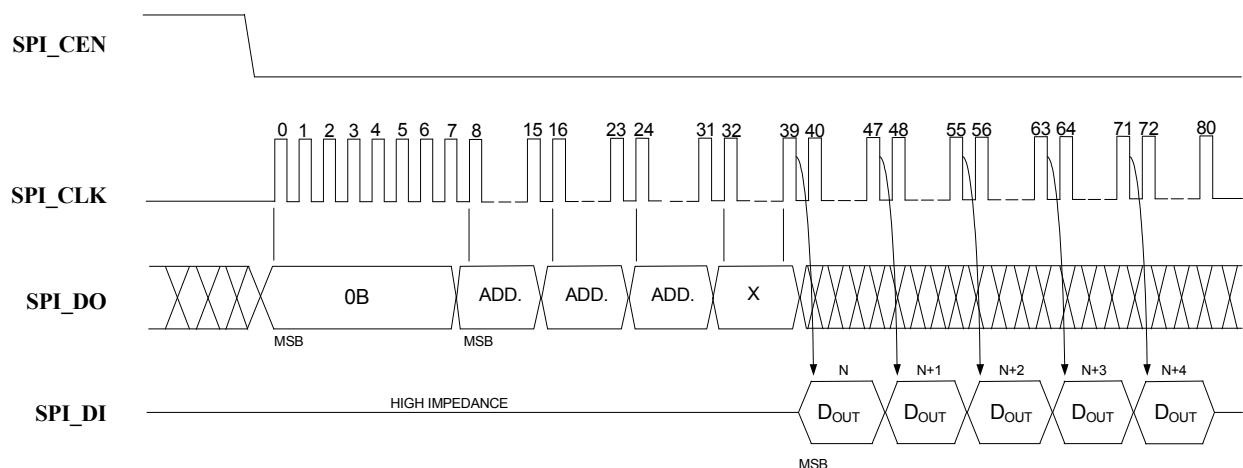


Figure 5.2 SPI Hi-Speed Read Sequence

5.1.2 Operation of the Dual Hi-Speed Read Sequence

The SPI controller also supports dual data mode (at 30 MHz SPI speed only). When configured in dual mode, the SPI controller will automatically handle reads going out to the SPI ROM. When the controller detects a read, the controller drops the **SPI_CE_N**, and puts out a 0x3B, followed by the 24-bit address. The SPI controller then puts out a DUMMY byte. The next four clocks clock in the first byte. The data appears two bits at a time on data out and data in. When the first byte is clocked in a ready signal is sent back to the processor, and the processor gets one byte.

After the processor gets the first byte, the address will change. If the address is one more than the last address, the SPI controller will clock out one more byte. If the address is anything other than one more than the last address, the SPI controller will terminate the transaction by taking **SPI_CE_N** high. As long as the addresses are sequential, the SPI Controller will keep clocking in data.

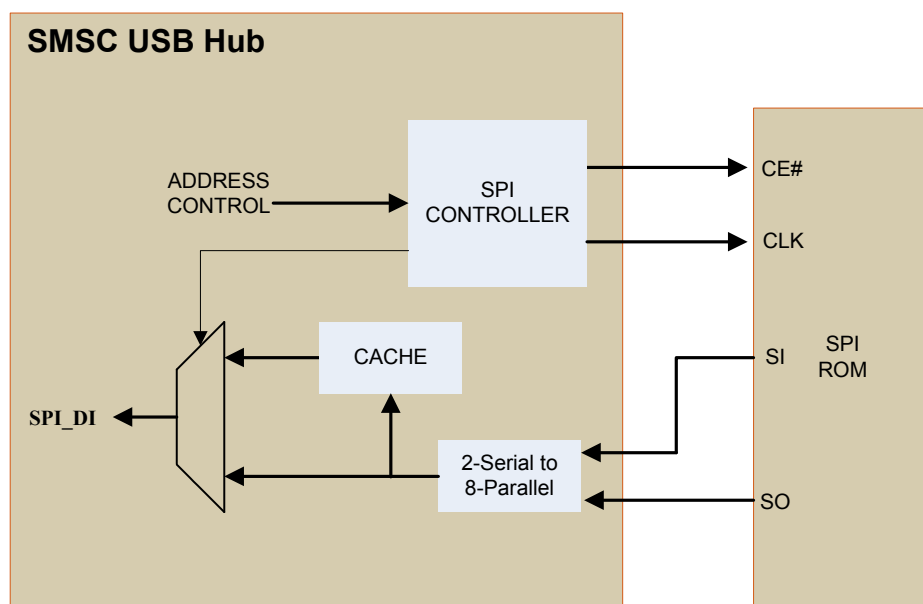


Figure 5.3 SPI Dual Hi-Speed Read Operation

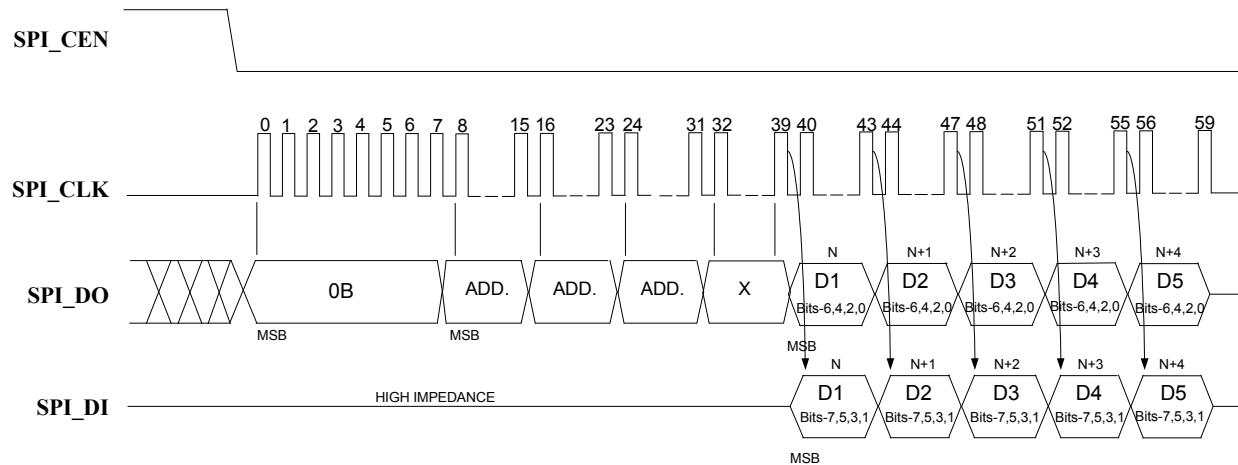


Figure 5.4 SPI Dual Hi-Speed Read Sequence

5.1.3 32-Byte Cache

There is a 32-byte pipeline cache, and associated with the cache is a base address pointer and a length pointer. Once the SPI controller detects a jump, the base address pointer is initialized to that address. As each new sequential data byte is fetched, the data is written into the cache, and the length is incremented. If the sequential run exceeds 32 bytes, the base address pointer is incremented to indicate the last 32 bytes fetched. If the USB5533B does a jump, and the jump is in the cache address range, the fetch is done in 1 clock from the internal cache instead of an external access.

5.1.4 Interface Operation to SPI Port When Not Doing Fast Reads

There is an 8-byte command buffer: SPI_CMD_BUF[7:0]; an 8-byte response buffer: SPI_RESP_BUF[7:0]; and a length register that counts out the number of bytes: SPI_CMD_LEN. Additionally, there is a self-clearing **GO** bit in the SPI_CTL Register. Once the **GO** bit is set, the device drops SPI_CE_N, and starts clocking. It will put out SPI_CMD_LEN X 8 number of clocks. After the first byte, the COMMAND, has been sent out, and the SPI_DI is stored in the SPI_RESP buffer. If the SPI_CMD_LEN is longer than the SPI_CMD_BUF, don't cares are sent out on the SPI_DO line. This mode is used for program execution out of internal RAM or ROM.

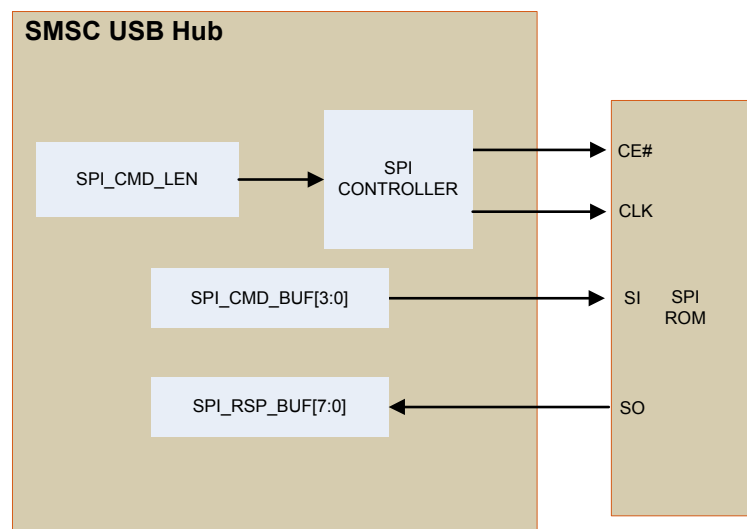


Figure 5.5 SPI Internally-Controlled Operation

Datasheet

5.1.4.1 ERASE EXAMPLE

To perform a SCTR_ERASE, 32BLK_ERASE, or 64BLK_ERASE, the device writes 0x20, 0x52, or 0xD8, respectively to the first byte of the command buffer, followed by a 3-byte address. The length of the transfer is set to 4 bytes. To do this, the device first drops **SPI_CE_N**, then counts out 8 clocks. It then puts out the 8 bits of command, followed by 24 bits of address of the location to be erased on the **SPI_DO** pin. When the transfer is complete, the **SPI_CE_N** goes high, while the **SPI_DI** line is ignored in this example.

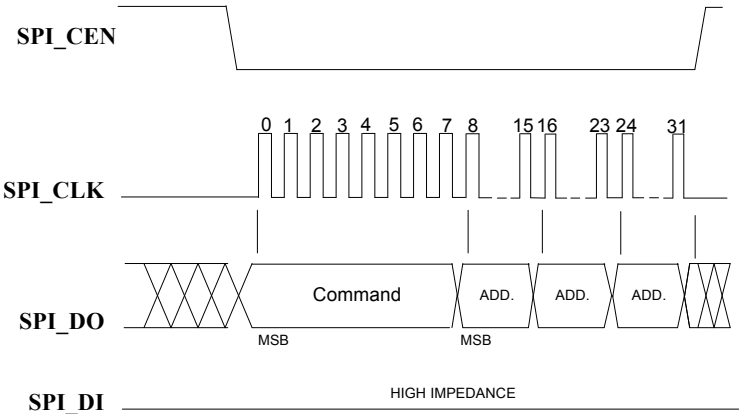


Figure 5.6 SPI Erase Sequence

5.1.4.2 BYTE PROGRAM EXAMPLE

To perform a Byte Program, the device writes 0x02 to the first byte of the command buffer, followed by a 3-byte address of the location that will be written to, and one data byte. The length of the transfer is set to 5 bytes. The device first drops **SPI_CE_N**, 8 bits of command are clocked out, followed by 24 bits of address, and one byte of data on the **SPI_DO** pin. The **SPI_DI** line is not used in this example.

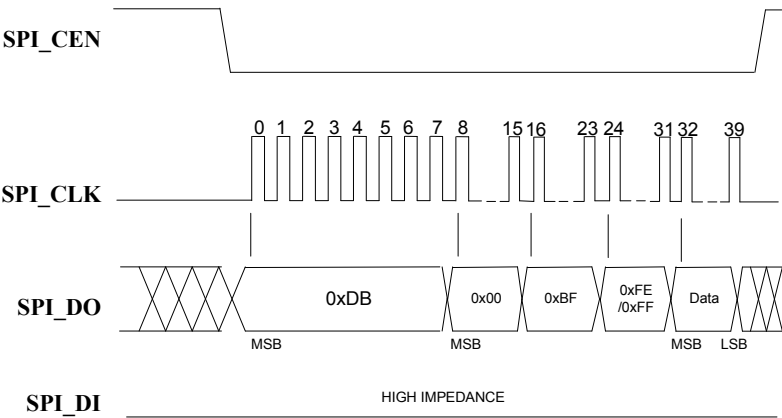


Figure 5.7 SPI Byte Program

5.1.4.3 COMMAND ONLY PROGRAM EXAMPLE

To perform a single byte command such as the following:

- WRDI
- WREN
- EWSR
- CHIP_ERASE
- EBSY
- DBSY

The device writes the opcode into the first byte of the SPI_CMD_BUF and the SPI_CMD_LEN is set to one. The device first drops **SPI_CE**, then 8 bits of the command are clocked out on the **SPI_DO** pin. The **SPI_DI** is not used in this example.

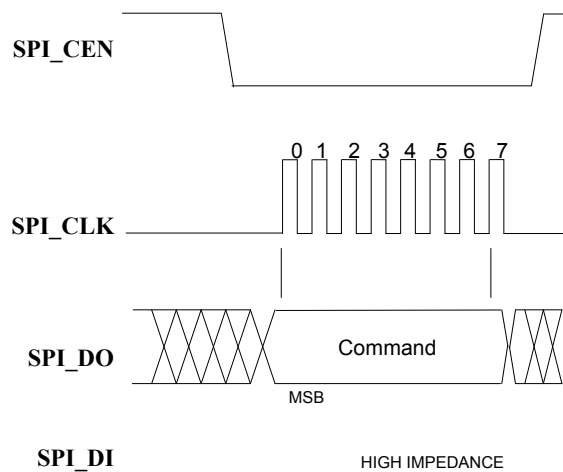


Figure 5.8 SPI Command Only Sequence

5.1.4.4 JEDEC-ID READ EXAMPLE

To perform a JEDEC-ID command, the device writes 0x9F into the first byte of the SPI_CMD_BUF and the length of the transfer is 4 bytes. The device first drops **SPI_CE_N**, then 8 bits of the command are clocked out, followed by the 24 bits of dummy bytes (due to the length being set to 4) on the **SPI_DO** pin. When the transfer is complete, the **SPI_CE_N** goes high. After the first byte, the data on **SPI_DI**

Datasheet

is clocked into the SPI_RSP_BUF. At the end of the command, there are three valid bytes in the SPI_RSP_BUF. In this example, 0xBF, 0x25, 0x8E.

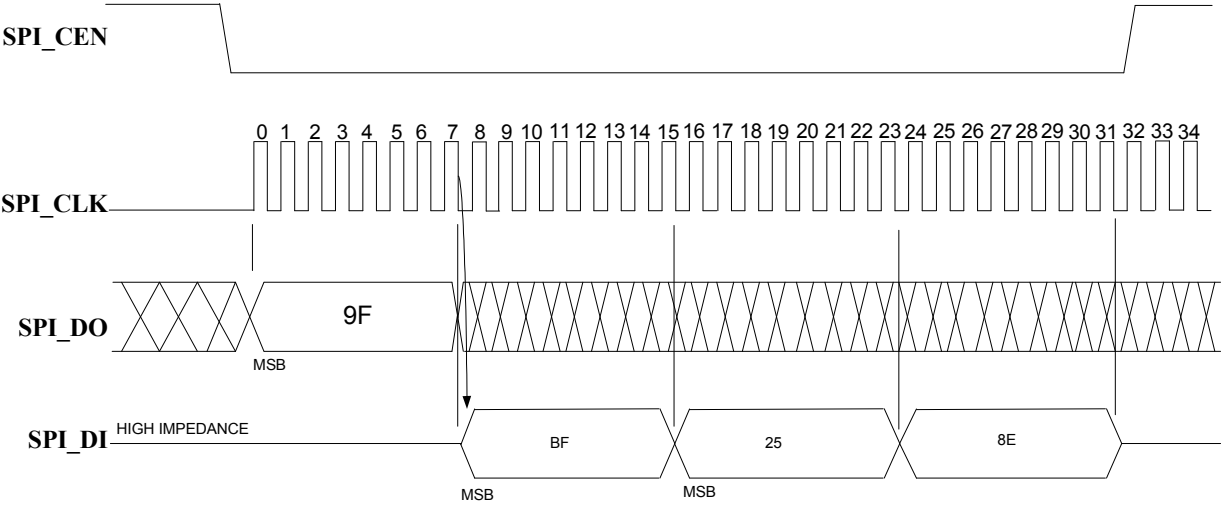


Figure 5.9 SPI JEDEC-ID Sequence

5.1.5 SPI Timing

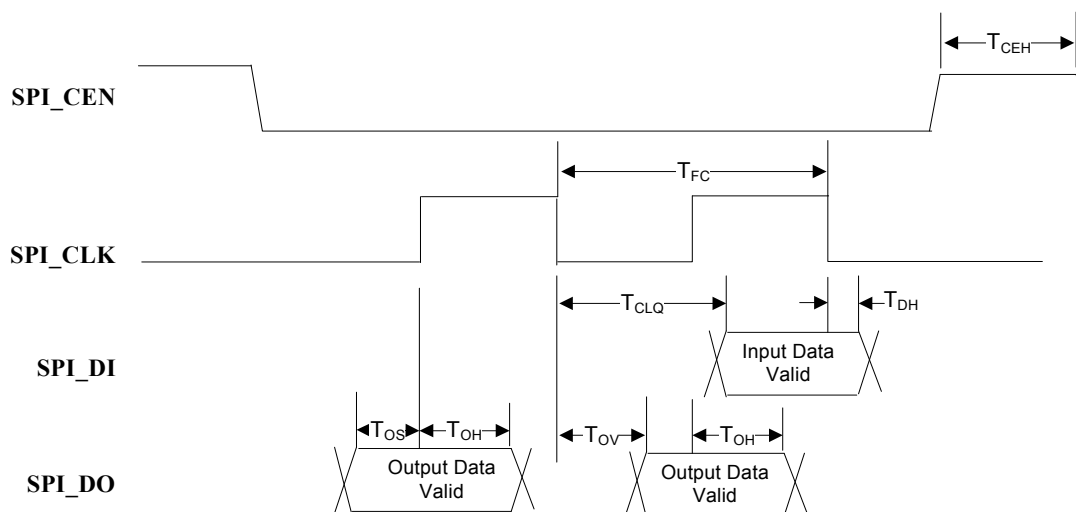


Figure 5.10 SPI Timing

Table 5.1 SPI Timing Operation

Name	Parameter	Min	Max	Unit
T_{FC}	Clock Frequency		60	MHz
T_{CEH}	Chip Enable High Time	50		ns
T_{CLQ}	Clock to Input Data		9	ns
T_{DH}	Input Data Hold Time	0		ns
T_{OS}	Output Set up Time	5		ns
T_{OH}	Output Hold Time	5		ns
T_{OV}	Clock to Output Valid	4		ns

5.2 SMBus Slave Interface

The SMBus slave interface is enabled when pull-up resistors are detected on both **SM_DAT** and **SM_CLK** for the first millisecond after reset. For operation in SMBus Legacy Mode, an additional pull-up resistor is required on **TRST**. If the SMBus interface is enabled, then the USB5533B will wait indefinitely for the SMBus host to configure the device. Once SMBus configuration is complete, device initialization will proceed. To disable the SMBus, a pull-down resistor of 10 k Ω must be applied to **SM_DAT**. If SMBus is disabled, the device proceeds directly to device initialization using the internal OTP ROM.

5.2.1 Pull-Up Resistor for SMBus

External pull-up resistors (10 k Ω recommended) are required on the **SM_DAT** and **SM_CLK** pins when implementing either SMBus mode.

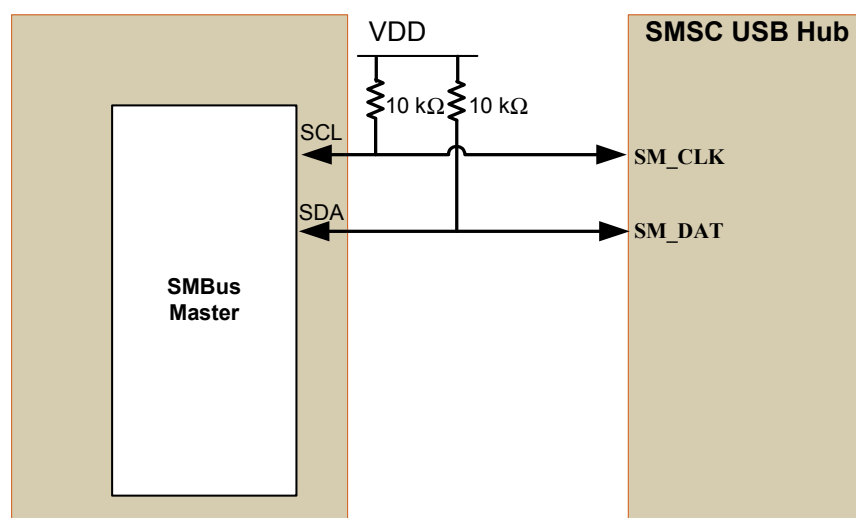


Figure 5.11 SMBus Slave Connection

5.2.2 Protocol Implementation

Typical block write and block read protocols are shown in [Figure 5.12](#) and [Figure 5.13](#). SMBus RAM buffer offset accesses are performed using 7-bit slave addressing, an 8- or 16-bit SMBus RAM buffer offset field (for legacy and advanced modes, respectively), and an 8-bit data field. The shading shown in the figures during a read or write indicates the hub is driving data on the **SM_DAT** line; otherwise, host data is on the **SM_DAT** line.

The SMBus slave address assigned to the hub (0101100b or 0101101b) allows it to be identified on the SMBus. The SMBus RAM buffer offset field is the internal offset in SMBus RAM to be accessed. The data field is the data that the host is attempting to read/write from/to the SMBus RAM buffer.

Note: Data bytes are transferred MSB first.

5.2.2.1 Block Write/Read

The block write begins with a slave address and a write condition. After the command code, the host issues a byte count which describes how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be zero. A block write or read allows a transfer maximum of 32 data bytes.

Note: For the following SMBus tables:

Denotes Master-to-Slave Denotes Slave-to-Master

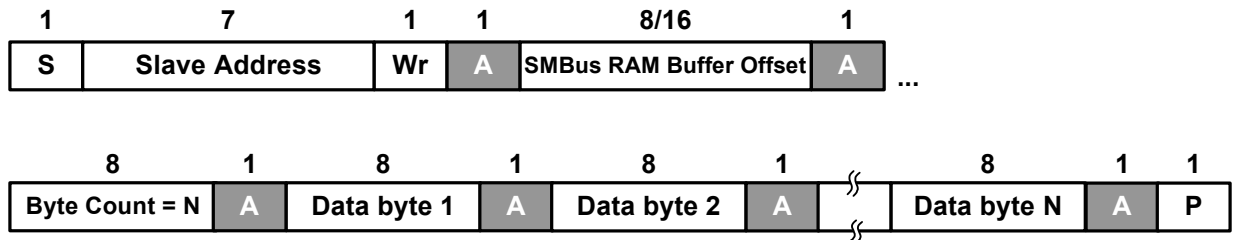


Figure 5.12 Block Write

5.2.2.2 Block Read

A block read differs from a block write in that the repeated start condition exists to satisfy the I²C specification's requirement for a change in the transfer direction.

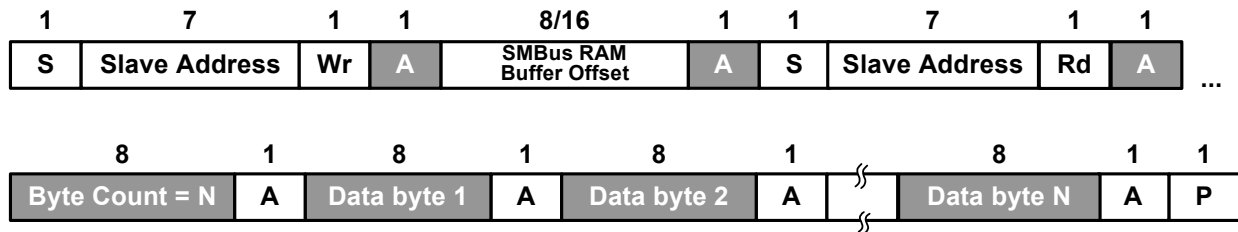


Figure 5.13 Block Read

5.2.2.3 Invalid Protocol Response Behavior

Note that any attempt to update registers with an invalid protocol will not be updated. The only valid protocols are write block and read block (described above), where the hub only responds to the 7-bit hardware selected slave addresses (0101100b or 0101101b). Additionally, the only valid registers for the hub are outlined in the *USB5533B Configuration Release Notes* documentation.

5.2.3 Slave Device Timeout

Devices in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds 25 ms ($T_{\text{TIMEOUT, MIN}}$). The master must detect this condition and generate a stop condition within or after the transfer of the interrupted data byte. Slave devices must reset their communication and be able to receive a new START condition no later than 35 ms ($T_{\text{TIMEOUT, MAX}}$).

Note: Some simple devices do not contain a clock low drive circuit; this simple kind of device typically resets its communications port after a start or stop condition. The slave device timeout must be implemented.

5.2.4 Stretching the SCLK Signal

The hub supports stretching of the SCLK by other devices on the SMBus. The hub will stretch the clock as needed.

5.2.5 Bus Reset Sequence

The SMBus slave interface resets and returns to the idle state upon a START condition followed immediately by a STOP condition.

5.2.6 SMBus Alert Response Address

The SMBALERT# signal is not supported by the USB5533B.

5.2.7 SMBus Timing

The SMBus slave interface complies with the *SMBus Specification Revision 1.0*. See Section 2.1, *AC Specifications* on page 3 for more information.

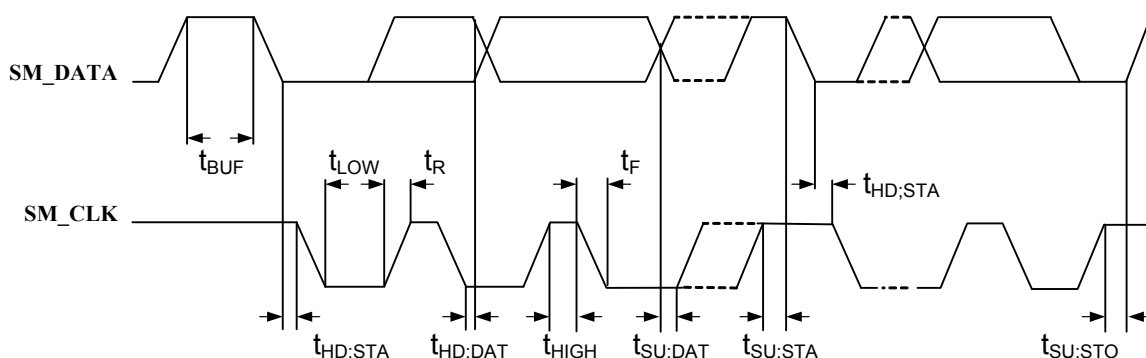


Figure 5.14 SMBus Slave Timing Diagram

Table 5.2 SMBus Slave Timing Modes

SYMBOL	PARAMETER	MIN	MAX	UNIT
f_{SCL}	SM_CLK clock frequency	0	100	KHz
$t_{HD;STA}$	Hold time START condition	4	-	μs
t_{LOW}	LOW period of the SM_CLK clock	4.7	-	μs
t_{HIGH}	HIGH period of the SM_CLK clock	4	-	μs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	μs
$t_{HD;DAT}$	DATA hold time\	0	-	ns
$t_{SU;DAT}$	DATA set-up time	250	-	ns
t_R	Rise time of both SM_DATA and SM_CLK signals	-	1000	ns
t_F	Fall time of both SM_CLK and SM_DATA lines	-	300	ns
$t_{SU;STO}$	Set-up time for a STOP condition	4	-	μs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	μs

5.3 Reset

There are two different resets that the device experiences. One is a hardware reset (either from the internal POR reset circuit or via the **RESET_N** pin) and the second is a USB Bus Reset.

5.3.1 Internal POR

All reset timing parameters are guaranteed by design.

5.3.2 External Hardware Reset

A valid hardware reset is defined as assertion of **RESET_N** for a minimum of 1 μ s after all power supplies are within operating range.

Assertion of **RESET_N** (external pin) causes the following:

1. The PHY is disabled, and the differential pairs will be in a high-impedance state.
2. All transactions immediately terminate; no states are saved.
3. All internal registers return to the default state.
4. The external crystal oscillator is halted.
5. The PLL is halted.

Chapter 6 DC Parameters

6.1 Maximum Guaranteed Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Storage Temperature	T_A	-55	150	°C	
Lead Temperature				°C	Refer to JEDEC Specification J-STD-020D.
1.25 V supply voltage	V_{DD12}	-0.5	1.6	V	
3.3 V supply voltage	V_{DD33}	-0.5	4.0	V	
Voltage on USB+ and USB- pins		-0.5	(3.3 V supply voltage + 2) $\leq$ 6	V	
Voltage on any signal powered by VDD33 rail		-0.5	$V_{DD33} + 0.3$	V	
Voltage on any signal pin powered by the VDD12		-0.5	$V_{DD12} + 0.3$	V	
HBM ESD Performance			2	kV	
Power Consumption			1.6	W	

Notes:

- Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only. Therefore, functional operation of the device at any condition above those indicated in the operation sections of this specification are not implied.
- When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

6.2 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
USB5533B Operating Temperature	T_A	0	70	$^{\circ}\text{C}$	
Die Temperature	T_J		115	$^{\circ}\text{C}$	
1.25 V supply voltage	V_{DD12}	1.22	1.31	V	
3.3 V supply voltage	V_{DD33}	3.0	3.6	V	
1.25 V supply rise time	t_{RT}	0	400	μs	(Figure 6.1)
3.3 V supply rise time	t_{RT}	0	400	μs	(Figure 6.1)
Voltage on USB+ and USB- pins		-0.3	5.5	V	If any 3.3 V supply voltage drops below 3.0 V, then the MAX becomes: (3.3 V supply voltage) + 0.5 $\leq$ 5.5
Voltage on any signal powered by VDD33 rail		-0.3	V_{DD33}	V	

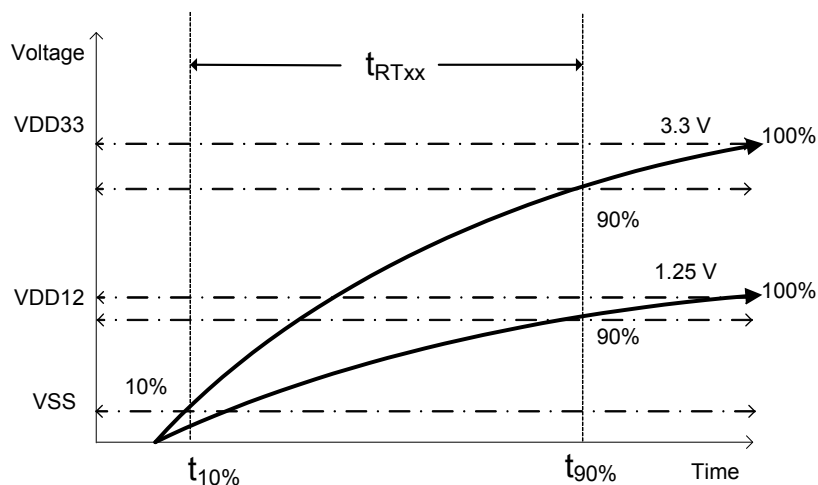


Figure 6.1 Supply Rise Time Model

6.3 Power Consumption

This section details the power consumption of the device as measured during various modes of operation. All typical measurements were taken with power supplies at nominal values (VDD12 = 1.25 V, VDD33 = 3.3 V).

	TYPICAL SUPPLY CURRENT (mA)		TYPICAL POWER (mW)
	VDD33	VDD12	
Reset	0.2	5.0	7.0
No VBUS	5.6	25.0	48.7
Global Suspend	9	29	65
3 FS Ports	23	70	161
3 HS Ports	46	78	245
3 SS Ports	18	971	1071
3 SS/HS Ports	56	1029	1255

6.4 DC Electrical Characteristics

Table 6.1 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Hysteresis (IS only)	V_{HYSI}		420		mV	
I, IPU, IPD Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Pull Down	PD		72		μ A	$V_{IN} = 0$
Pull Up	PU		58		μ A	$V_{IN} = VDD33$
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.3	V	$V_{IN} = 0$ to VDD33
High Input Level	V_{IHCK}	0.8			V	
Input Leakage	I_{IL}	-10		+10	μ A	

Table 6.1 DC Electrical Characteristics (continued)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	μA	$V_{IN} = 0$
High Input Leakage	I_{IH}	-10		+10	μA	$V_{IN} = V_{DD33}$
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 12 \text{ mA @ } V_{DD33} = 3.3 \text{ V}$
High Output Level	V_{OH}	$V_{DD33} - 0.4$			V	$I_{OH} = -12 \text{ mA @ } V_{DD33} = 3.3 \text{ V}$
Output Leakage	I_{OL}	-10		+10	μA	$V_{IN} = 0 \text{ to } V_{DD33}$ (Note 6.1)
I/O12, I/O12PU & I/O12PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 12 \text{ mA @ } V_{DD33} = 3.3 \text{ V}$
High Output Level	V_{OH}	$V_{DD33} - 0.4$			V	$I_{OH} = -12 \text{ mA @ } V_{DD33} = 3.3 \text{ V}$
Output Leakage	I_{OL}	-10		+10	μA	$V_{IN} = 0 \text{ to } V_{DD33}$ (Note 6.1)
Pull Down	PD		72		μA	
Pull Up	PU		58		μA	
IO-U (Note 6.2)						

Note 6.1 Output leakage is measured with the current pins in high impedance.

Note 6.2 See *USB 2.0 Specification [1]* for USB DC electrical characteristics.

6.5 Capacitance

Table 6.2 Pin Capacitance

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C _{XTAL}			2	pF	
Input Capacitance	C _{IN}			5	pF	
Output Capacitance	C _{OUT}			10	pF	

Note 6.3 Capacitance T_A = 25°C; f_c = 1 MHz; VDD33 = 3.3 V

Chapter 7 AC Specifications

7.1 Oscillator/Crystal

Crystal: Parallel resonant, fundamental mode, 25 MHz $\pm$ 30 ppm

External Clock: 50% duty cycle $\pm$ 10%, 25 MHz $\pm$ 30 ppm, jitter < 100 ps rms

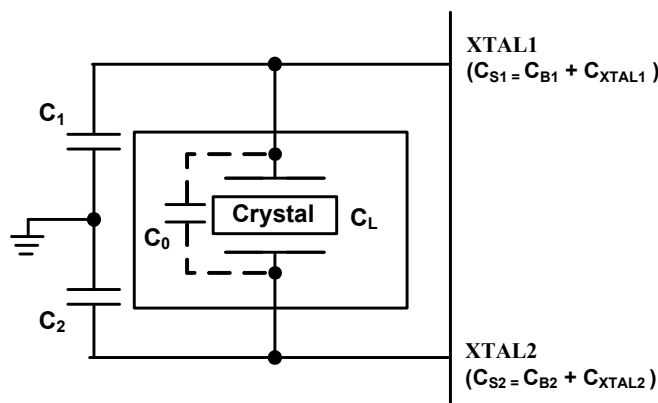


Figure 7.1 Typical Crystal Circuit

Table 7.1 Crystal Circuit Legend

SYMBOL	DESCRIPTION	IN ACCORDANCE WITH
C_0	Crystal shunt capacitance	Crystal manufacturer's specification (Note 7.1)
C_L	Crystal load capacitance	
C_B	Total board or trace capacitance	OEM board design
C_S	Stray capacitance	SMSC IC and OEM board design
C_{XTAL}	XTAL pin input capacitance	SMSC IC
C_1	Load capacitors installed on OEM board	Calculated values based on Figure 7.2 (Note 7.2)
C_2		

$$C_1 = 2 \times (C_L - C_0) - C_{S1}$$

$$C_2 = 2 \times (C_L - C_0) - C_{S2}$$

Figure 7.2 Formula to Find the Value of C_1 and C_2

Note 7.1 C_0 is usually included (subtracted by the crystal manufacturer) in the specification for C_L and should be set to 0 for use in the calculation of the capacitance formulas in [Figure 7.2](#). However, the PCB itself may present a parasitic capacitance between XTALIN and XTALOUT. For an accurate calculation of C_1 and C_2 , take the parasitic capacitance between traces XTALIN and XTALOUT into account.

Note 7.2 Consult crystal manufacturer documentation for recommended capacitance values.

Datasheet

7.2 External Clock

50% duty cycle $\pm 10\%$, 25 MHz ± 30 ppm, jitter < 100 ps rms.

Note: The external clock is based upon 1.2 V CMOS Logic. **XTALOUT** should be treated as a no connect when an external clock is supplied.

7.2.1 SMBus Clock

The maximum frequency allowed on the SMBus clock line is 100 kHz.

7.2.2 USB 2.0

The SMSC hub conforms to all voltage, power, and timing characteristics and specifications as set forth in the *USB 2.0 Specification* [\[1\]](#).

TOP VIEW

BOTTOM VIEW

SIDE VIEW

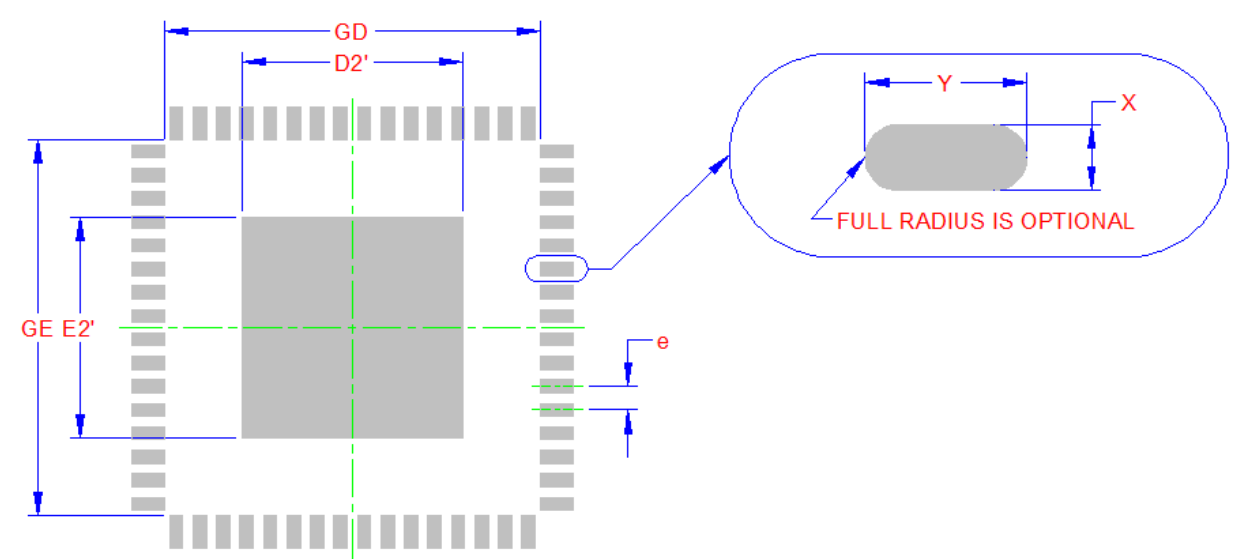
3-D VIEWS

Table 8.1 USB5533B 64-Pin QFN Dimensions

Notes:

1. All dimensions are in millimeters unless otherwise noted.
2. Dimension "b" applies to plated terminals and is measured between 0.15 and 0.30 mm from the terminal tip.
3. The pin 1 identifier may vary, but is always located within the zone indicated.

Datasheet



THE USER MAY MODIFY THE PCB LAND PATTERN DIMENSIONS
BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

Figure 8.2 USB5533B Recommended PCB Land Pattern

Table 8.2 USB5533B Recommended PCB Land Pattern Dimensions

	MIN (mm)	NOMINAL (mm)	MAX (mm)
GD/GE	7.93	-	-
D2'/E2'	-	6.00	-
X	-	-	0.28
Y	-	-	0.69
e	0.50		

Chapter 9 Datasheet Revision History

Table 9.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.2 (05-31-13)	All	Removed industrial temp. SKU information from document.
	Section 6.1: <i>Maximum Guaranteed Ratings</i> on page 28	Added maximum power consumption row/data to table.
	Section 6.2: <i>Operating Conditions</i> on page 29	Added maximum die temperature row/data to table.
	Section 6.3: <i>Power Consumption</i> on page 30	Added power consumption numbers
	Note 3.1 on page 14 and Note 3.3 on page 14	Updated note to reflect configuration straps are enabled by default.
	Chapter 3: <i>Pin Information</i> on page 10	Updated TRST pin description with the following note: "If using the SMBus interface, a pull-up on this signal will enable Legacy Mode, while leaving it unconnected or pulled-down will enable Advanced Mode."
	Chapter 8: <i>Package Drawing</i> on page 35	Updated recommended land pattern drawings and information.

Datasheet

Table 9.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.1 (03-05-13)	Ordering Codes	Updated ordering codes to for A2 material
	Ordering Codes	Corrected tape and reel quantity from 3000 to 2500.
	Section 3.2: Pin Descriptions (Grouped by Function) on page 11	Added Note 3.1 and Note 3.3 explaining the configuration strap functions on the PRT_PWRx and OCSx pins.
	Section 5.1.2: Operation of the Dual Hi-Speed Read Sequence on page 18	Updated first sentence to state that dual data mode is supported only at an SPI speed of 30 MHz
	Chapter 5: Interfacing to the USB5533B on page 17	Clarified interface ordering explanation.
	Section 5.2: SMBus Slave Interface on page 24	Removed “either an external I2C (if present) and” from last sentence of section.
	Section 5.2: SMBus Slave Interface on page 24	Added additional sentence: “For operation in SMBus Legacy Mode, an additional pull-up resistor is required on TRST .”
	Section 5.2.2: Protocol Implementation on page 24, Figure 5.12: Block Write on page 25, Figure 5.13: Block Read on page 25	Updated “register address” references to “SMBus RAM buffer offset”.
	SPI_DO pin description & Note 3.2	Added note to describe the SPI_SPD_SEL configuration strap function on the SPI_DO.
Rev. 1.0 (09-06-12)	All	Removed references to GPIOs and LEDs
	All	Initial revision.

Appendix A (Acronyms)

I²C[®]:	Inter-Integrated Circuit ¹
OCS:	Over-Current Sense
PCB:	Printed Circuit Board
PHY:	Physical Layer
PLL:	Phase-Locked Loop
QFN:	Quad Flat No Leads
RoHS:	Restriction of Hazardous Substances Directive
SCL:	Serial Clock
SIE:	Serial Interface Engine
SMBus:	System Management Bus
TT:	Transaction Translator

¹.I²C is a registered trademark of Philips Corporation.

Appendix B (References)

- [1] Universal Serial Bus Specification, Version 2.0, April 27, 2000 (12/7/2000 and 5/28/2002 Errata)
USB Implementers Forum, Inc. <http://www.usb.org>
- [2] Universal Serial Bus Specification, Version 3.0, November 13, 2008
USB Implementers Forum, Inc. <http://www.usb.org>
- [3] System Management Bus Specification, version 1.0
SMBus. <http://smbus.org/specs/>
- [4] MicroChip 24AA02/24LC02B (Revision C)
Microchip Technology Inc. <http://www.microchip.com/>

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