FAIRCHILD

SEMICONDUCTOR®

December 2013

74LCX245
Low Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

Features

- 5V tolerant inputs and outputs
- 2.3V to 3.6V V_{CC} specifications provided
- 7.0ns t_{PD} max. (V_{CC} = 3.3V), 10µA I_{CC} max.
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal[1]
- ±24mA output drive (V_{CC} = 3.0V)
- Implements proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds 500mA
- ESD performance:
  – Human body model > 2000V
  – Machine model > 200V
- Leadless DQFN package

Note:

1. To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

General Description

The LCX245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5V and 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The T/$\overline{R}$ input determines the direction of data flow through the device. The $\overline{OE}$ input disables both the A and B ports by placing them in a high impedance state.

The LCX245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Ordering Information

Order Number	Package Number	Package Description
74LCX245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX245BQX[2]	MLP20B	20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm
74LCX245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LCX245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Note:
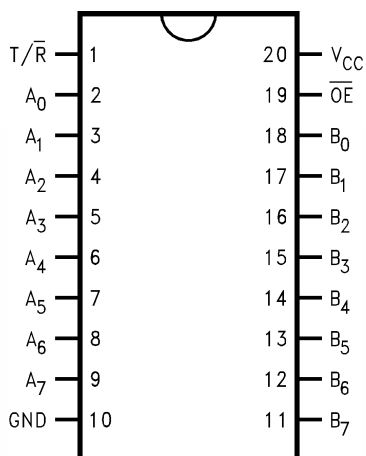
2. DQFN package available in Tape and Reel only.

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.
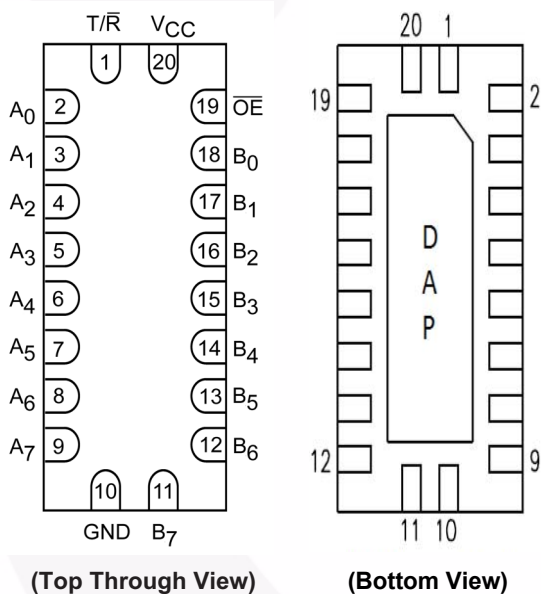
♺ All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagrams
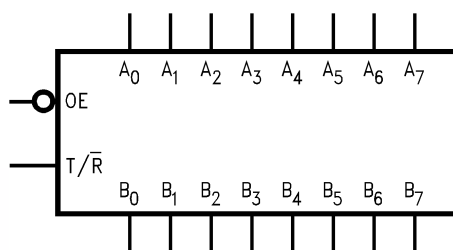
Pin Assignments for SOIC, SOP, SSOP, and TSSOP

$T/\overline{R}$	1	20	V_{CC}
A_0	2	19	$\overline{OE}$
A_1	3	18	B_0
A_2	4	17	B_1
A_3	5	16	B_2
A_4	6	15	B_3
A_5	7	14	B_4
A_6	8	13	B_5
A_7	9	12	B_6
GND	10	11	B_7

Pin Assignment for DQFN

(Top Through View)   (Bottom View)

Logic Symbol

Truth Table

Inputs		
OE	$T/\overline{R}$	Outputs
L	L	Bus $B_0 - B_7$ Data to Bus $A_0 - A_7$
L	H	Bus $A_0 - A_7$ Data to Bus $B_0 - B_7$
H	X	HIGH Z State on $A_0 - A_7$, $B_0 - B_7$ [3]

H = HIGH Voltage Level

L = LOW Voltage Level
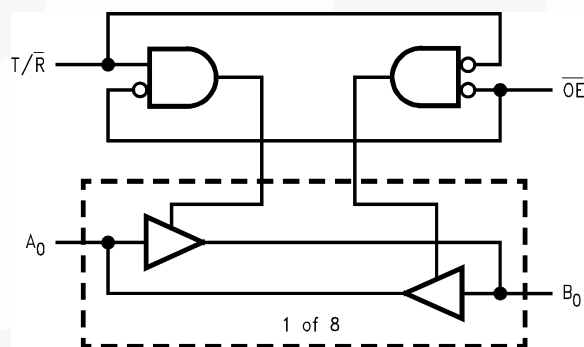
X = Immaterial

Z = High Impedance

Note:

3. Unused bus terminals during HIGH Z State must be held HIGH or LOW.

Logic Diagram

1 of 8

Pin Description

Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-STATE Outputs
B_0–B_7	Side B Inputs or 3-STATE Outputs
DAP	No Connect

Note: DAP (Die Attach Pad)

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_I	DC Input Voltage	–0.5V to +7.0V
V_O	DC Output Voltage	
	Output in 3-STATE	–0.5V to +7.0V
	Output in HIGH or LOW State[4]	–0.5V to V_{CC} + 0.5V
I_{IK}	DC Input Diode Current, V_I < GND	–50mA
I_{OK}	DC Output Diode Current	
	V_O < GND	–50mA
	V_O > V_{CC}	+50mA
I_O	DC Output Source/Sink Current	±50mA
I_{CC}	DC Supply Current per Supply Pin	±100mA
I_{GND}	DC Ground Current per Ground Pin	±100mA
T_{STG}	Storage Temperature	–65°C to +150°C

Note:

4. I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions[5]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage			
	Operating	2.0	3.6	V
	Data Retention	1.5	3.6	
V_I	Input Voltage	0	5.5	V
V_O	Output Voltage			
	3-STATE	0	5.5	V
	HIGH or LOW State	0	V_{CC}	
I_{OH} / I_{OL}	Output Current			
	V_{CC} = 3.0V–3.6V		±24	mA
	V_{CC} = 2.7V–3.0V		±12	
	V_{CC} = 2.3V–2.7V		±8	
T_A	Free-Air Operating Temperature	–40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns / V

Note:

5. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = –40°C to +85°C		Units
				Min.	Max.	
V_{IH}	HIGH Level Input Voltage	2.3–2.7		1.7		V
		2.7–3.6		2.0		
V_{IL}	LOW Level Input Voltage	2.3–2.7			0.7	V
		2.7–3.6			0.8	
V_{OH}	HIGH Level Output Voltage	2.3–3.6	I_{OH} = –100µA	V_{CC} – 0.2		V
		2.3	I_{OH} = –8mA	1.8		
		2.7	I_{OH} = –12mA	2.2		
		3.0	I_{OH} = –18mA	2.4		
			I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	2.3–3.6	I_{OL} = 100µA		0.2	V
		2.3	I_{OL} = 8mA		0.6	
		2.7	I_{OL} = 12mA		0.4	
		3.0	I_{OL} = 16mA		0.4	
			I_{OL} = 24mA		0.55	
I_I	Input Leakage Current	2.3–3.6	$0 \leq V_I \leq 5.5V$		±5.0	µA
I_{OZ}	3-STATE Output Leakage	2.3–3.6	$0 \leq V_O \leq 5.5V$, $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power-Off Leakage Current	0	V_I or V_O = 5.5V		10	µA
I_{CC}	Quiescent Supply Current	2.3–3.6	$V_I = V_{CC}$ or GND		10	µA
			$3.6V \leq V_I$, $V_O \leq 5.5V$[6]		±10	
ΔI_{CC}	Increase in I_{CC} per Input	2.3–3.6	$V_{IH} = V_{CC} – 0.6V$		500	µA

Note:

6. Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	T_A = –40°C to +85°C, R_L = 500Ω						Units
		V_{CC} = 3.3V ± 0.3V, C_L = 50pF		V_{CC} = 2.7V, C_L = 50pF		V_{CC} = 2.5V ± 0.2V, C_L = 30pF		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay, A_n to B_n or B_n to A_n	1.5	7.0	1.5	8.0	1.5	8.4	ns
t_{PZL}, t_{PZH}	Output Enable Time	1.5	8.5	1.5	9.5	1.5	10.5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	1.5	7.5	1.5	8.5	1.5	9.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew[7]		1.0					ns

Note:

7. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$ Typical	Unit
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	3.3	$C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$	0.8	V
		2.5	$C_L = 30pF$, $V_{IH} = 2.5V$, $V_{IL} = 0V$	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	3.3	$C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$	−0.8	V
		2.5	$C_L = 30pF$, $V_{IH} = 2.5V$, $V_{IL} = 0V$	−0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7.0	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8.0	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10MHz	25.0	pF

AC Loading and Waveforms (Generic for LCX Family)

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V
t_{PZH}, t_{PHZ}	GND
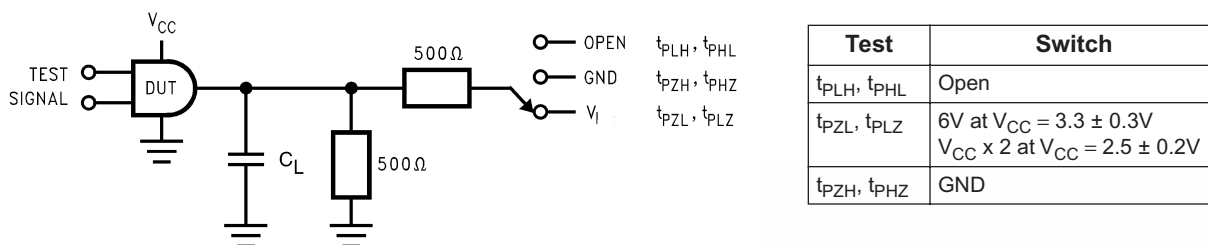
Figure 1. AC Test Circuit (C_L includes probe and jig capacitance)

Waveform for Inverting and Non-Inverting Functions

3-STATE Output High Enable and Disable Times for Logic
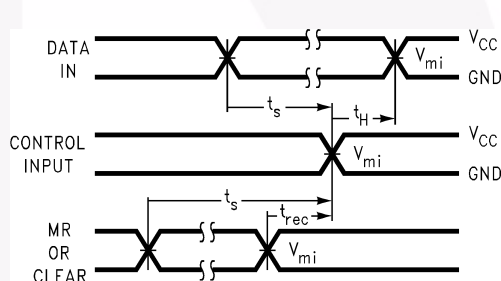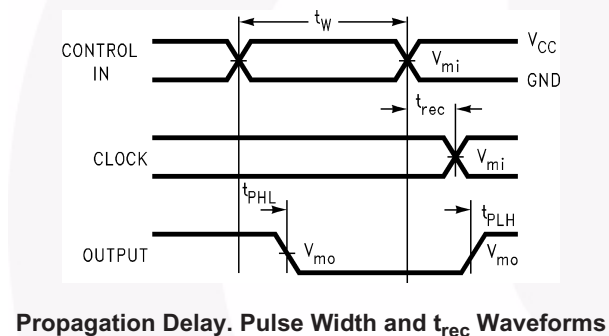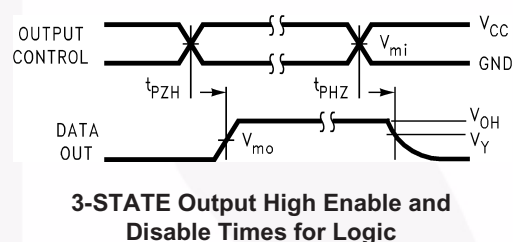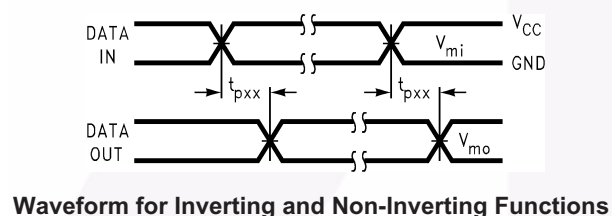
Propagation Delay. Pulse Width and t_{rec} Waveforms

Setup Time, Hold Time and Recovery Time for Logic
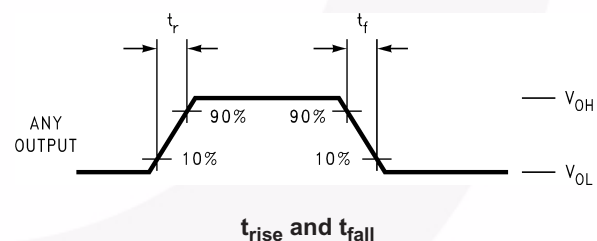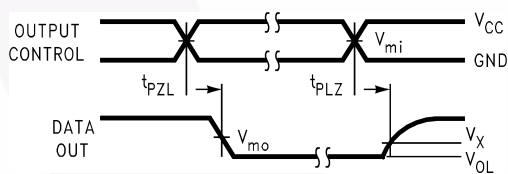
3-STATE Output Low Enable and Disable Times for Logic

t_{rise} and t_{fall}

Symbol	V_{CC}		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V_{mi}	1.5V	1.5V	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V

Figure 2. Waveforms (Input Characteristics; f = 1MHz, t_r = t_f = 3ns)

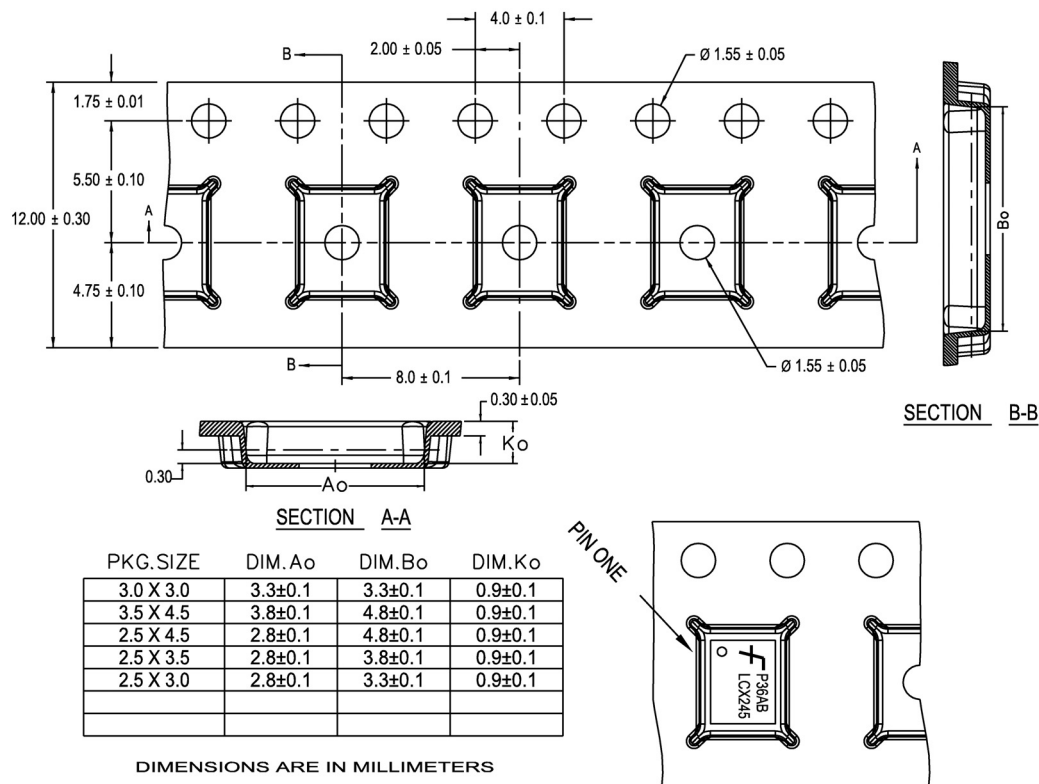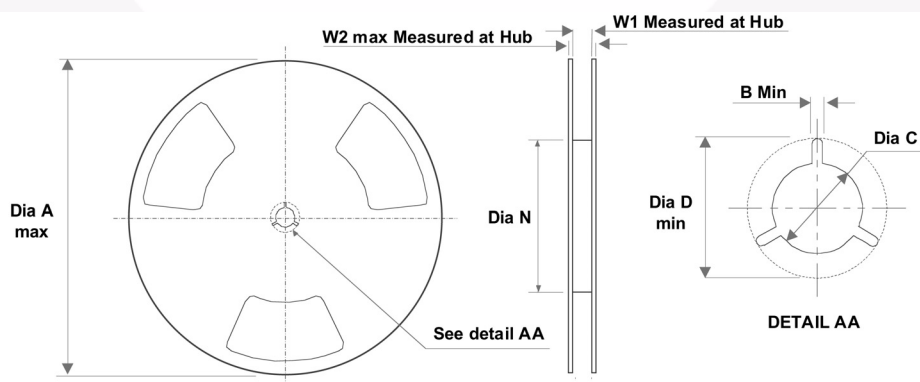## Schematic Diagram (Generic for LCX Family)
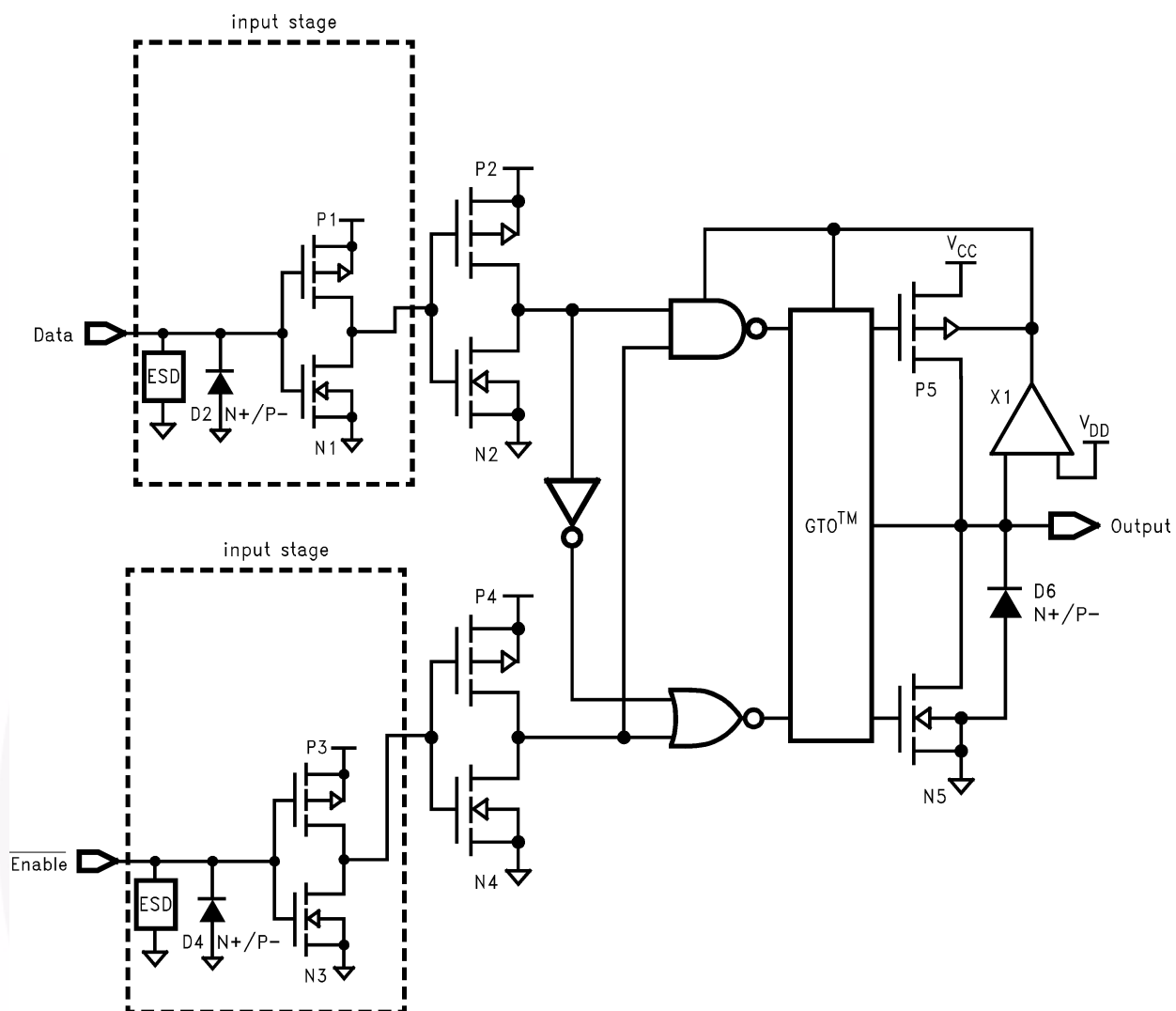
Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number of Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

Tape Dimension inches (millimeters)

SECTION B-B

SECTION A-A

PKG.SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.0 X 3.0	3.3±0.1	3.3±0.1	0.9±0.1
3.5 X 4.5	3.8±0.1	4.8±0.1	0.9±0.1
2.5 X 4.5	2.8±0.1	4.8±0.1	0.9±0.1
2.5 X 3.5	2.8±0.1	3.8±0.1	0.9±0.1
2.5 X 3.0	2.8±0.1	3.3±0.1	0.9±0.1

DIMENSIONS ARE IN MILLIMETERS

PIN ONE

Reel Dimensions inches (millimeters)

DETAIL AA

Tape Size	A	B	C	D	N	W1	W2
12mm	13.0 (330.0)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.488 (12.4)	0.724 (18.4)

Physical Dimensions

13.00
12.60

11.43

A

B

20   11

10.65   7.60
10.00   7.40

9.50

2.25

PIN ONE
INDICATOR

1   10

0.51
0.35

1.27

1.27   0.65

⊕ 0.25 Ⓜ C B A

LAND PATTERN RECOMMENDATION

2.65 MAX

SEE DETAIL A

C

0.30
0.10

⌒ 0.10 C

0.33
0.20

SEATING PLANE

0.75
0.25 X 45°

(R0.10)

(R0.10)

GAGE PLANE

0.25

8°
0°

1.27
0.40

SEATING PLANE

(1.40)

DETAIL A
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC
    MS-013, VARIATION AC, ISSUE E

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE MOLD
    FLASH OR BURRS.

D) CONFORMS TO ASME Y14.5M-1994

E) LANDPATTERN STANDARD: SOIC127P1030X265-20L

F) DRAWING FILENAME: MKT-M20BREV3

Figure 3. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

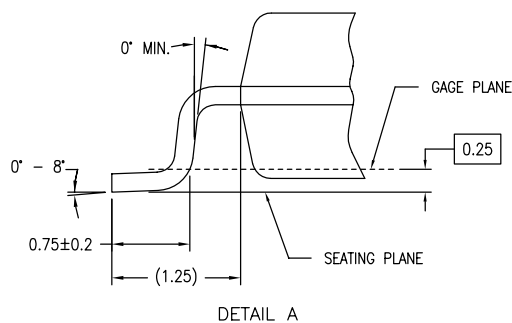*Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:*

http://www.fairchildsemi.com/packaging/

Physical Dimensions (Continued)

12.6±0.10
−A−

0.40 TYP

20   11

7.8

5.3±0.10
−B−

3.9

△ | 0.2 | C | B | A
ALL LEAD TIPS

PIN #1 IDENT.   1   10

LAND PATTERN RECOMMENDATION

20   19   12   11

5.01 TYP

9.27 TYP

(2.13 TYP)

1   2   9   10

1.27 TYP   0.6 TYP

ALL LEAD TIPS
△ | 0.1 | C

2.1 MAX.

1.8±0.1

−C−

0.15±0.05

1.27 TYP

0.35−0.51

⊕ | 0.12Ⓜ | C | A

DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO EIAJ EDR−7320 REGISTRATION,
   ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
   FLASH, AND TIE BAR EXTRUSIONS.

SEE DETAIL A

0.15−0.25

7° TYP

GAGE PLANE

0° − 8° TYP

0.25

0.60±0.15

1.25

SEATING PLANE

DETAIL A

M20DREVC

Figure 4. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)

TOP VIEW

SIDE VIEW

BOTTOM VIEW

RECOMMENDED LAND PATTERN

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO—241, VARIATION AC

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP20BrevA

Figure 5. 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm

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Physical Dimensions (Continued)
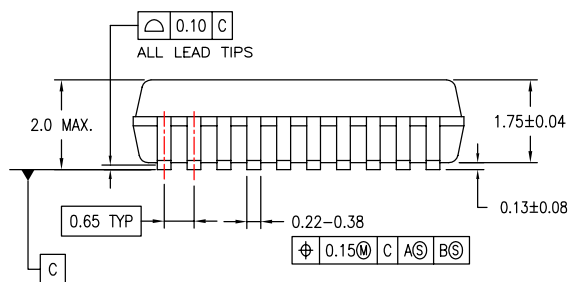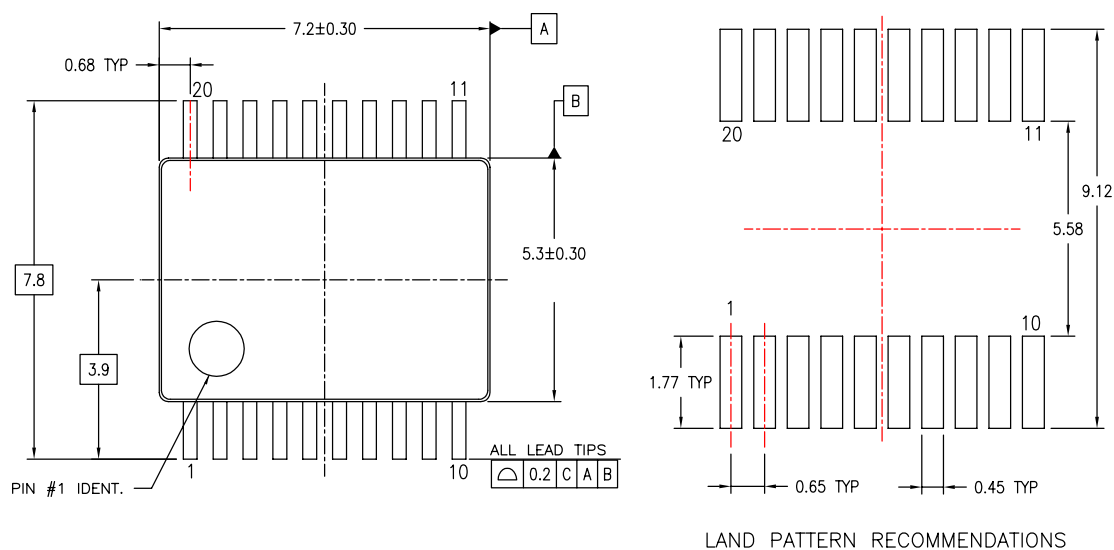
NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO−150, VARIATION AE, DATE 1/94.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M − 1994.

MSA20REVB

Figure 6. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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Physical Dimensions (Continued)

6.5±0.1
-A-
-0.20
20
11
-C-
6.4
4.4±0.1 -B-
3.2
1
10
◻ 0.2 C B A
ALL LEAD TIPS
PIN #1 IDENT.

LAND PATTERN RECOMMENDATION

4.16   7.72
1.78
0.42
0.65

◻ 0.1 C
ALL LEAD TIPS

$0.90^{+0.15}_{-0.10}$

1.2 max
-C-
0.1±0.05

0.65
0.19−0.30
⊕ 0.10 Ⓜ A B Ⓢ C Ⓢ

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.09−0.20

12.00°
R0.09min
GAGE PLANE
0 − 8°
0.6±0.1
1.00
SEATING PLANE
0.25
R0.09min

DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−153, VARIATION AC,
   REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH,
   AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

Figure 8. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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