

FDD850N10L

N-Channel PowerTrench® MOSFET

100 V, 15.7 A, 75 mΩ

Features

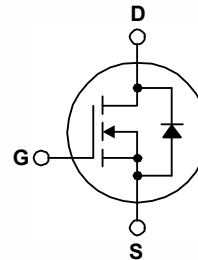
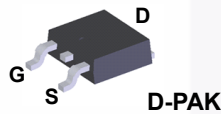
- $R_{DS(on)} = 61 \text{ m}\Omega$ (yp.) @ $V_{GS} = 10 \text{ V}$, $I_D = 12 \text{ A}$
- $R_{DS(on)} = 64 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 5 \text{ V}$, $I_D = 12 \text{ A}$
- Low Gate Charge (Typ. 22.2 nC)
- Low C_{rss} (Typ. 42 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance and maintain superior switching performance.

Application

- Consumer Appliances
- LED TV and Monitor
- Synchronous Rectification
- Uninterruptible Power Supply
- Micro Solar Inverter



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDD850N10L	Unit
V_{DSS}	Drain to Source Voltage	100	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	15.7
		- Continuous ($T_C = 100^\circ\text{C}$)	11.1
I_{DM}	Drain Current	- Pulsed (Note 1)	63
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	41
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.0
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	50
		- Derate Above 25°C	0.33
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDD850N10L	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	87	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD850N10L	FDD850N10L	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.1	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 80 \text{ V}, T_C = 150^\circ\text{C}$	-	-	1 500	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1.0	-	2.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$ $V_{GS} = 5 \text{ V}, I_D = 12 \text{ A}$	-	61 64	75 96	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 15.7 \text{ A}$	-	31	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	-	1100	1465	pF	
C_{oss}	Output Capacitance		-	80	105	pF	
C_{rSS}	Reverse Transfer Capacitance		-	42	-	pF	
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{GS} = 10 \text{ V}$	$V_{DS} = 80 \text{ V},$ $I_D = 15.7 \text{ A}$	-	22.2	28.9	nC
$Q_{g(tot)}$	Total Gate Charge at 5V	$V_{GS} = 5 \text{ V}$		-	12.3	16.0	nC
Q_{gs}	Gate to Source Gate Charge			-	3.0	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	5.7	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, I_D = 15.7 \text{ A},$ $V_{GS} = 5 \text{ V}, R_G = 4.7 \Omega$	-	17	44	ns
t_r	Turn-On Rise Time		-	21	52	ns
$t_{d(off)}$	Turn-Off Delay Time		-	27	64	ns
t_f	Turn-Off Fall Time		(Note 4)	-	8	26
ESR	Equivalent Series Resistance (G-S)	$f = 1 \text{ MHz}$	-	1.75	-	Ω

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	15.7	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	63	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 12 \text{ A}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, V_{DS} = 80 \text{ V}, I_{SD} = 15.7 \text{ A},$	-	38	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100 \text{ A}/\mu\text{s}$	-	50	-	nC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 1 \text{ mH}, I_{AS} = 9.1 \text{ A}, R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 15.7 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

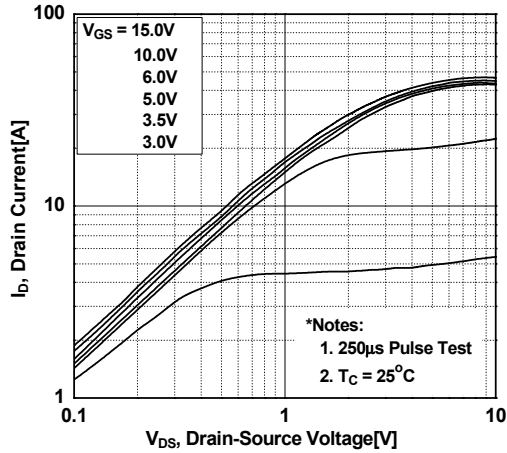


Figure 2. Transfer Characteristics

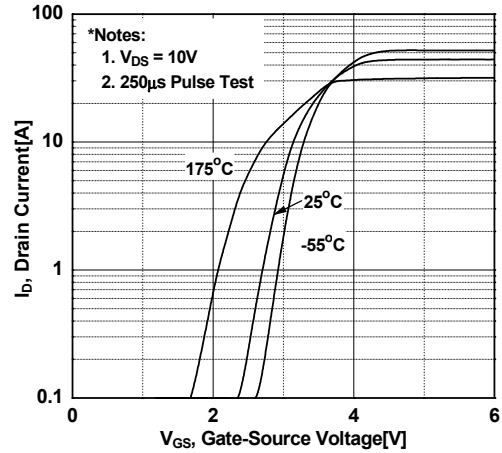


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

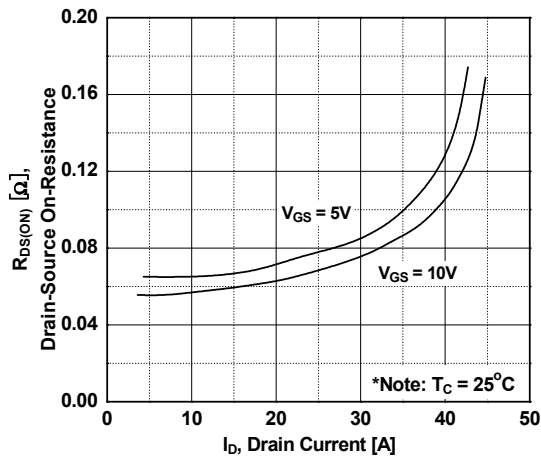


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

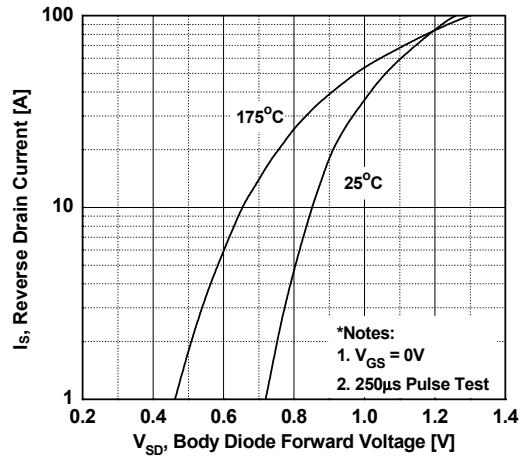


Figure 5. Capacitance Characteristics

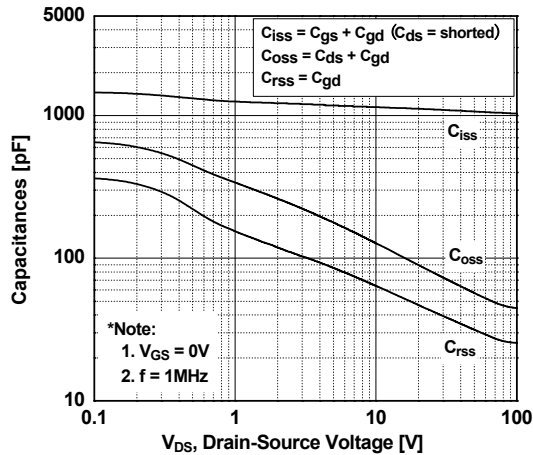
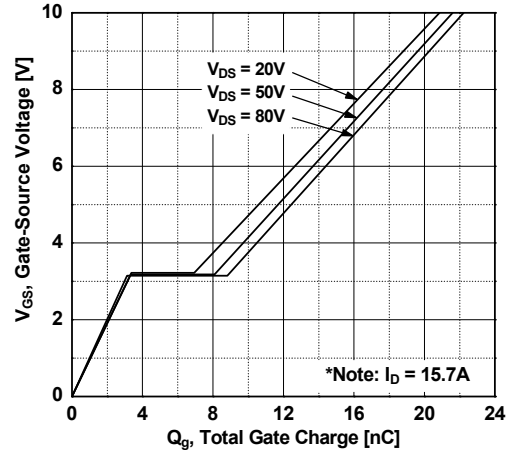


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

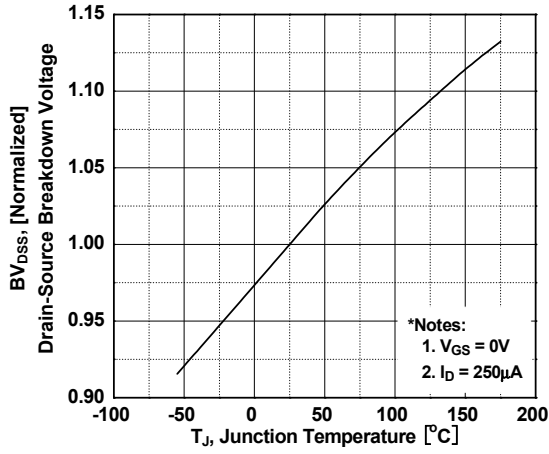


Figure 8. On-Resistance Variation vs. Temperature

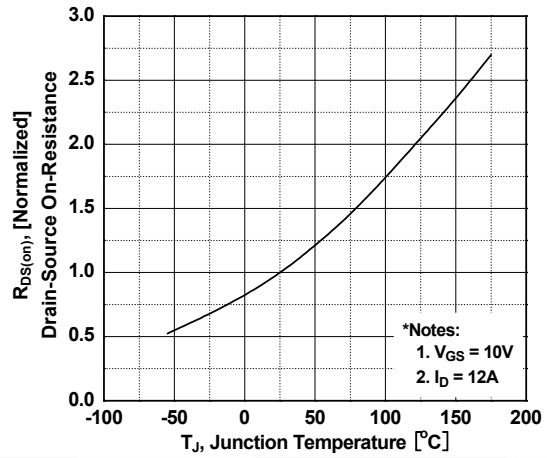


Figure 9. Maximum Safe Operating Area

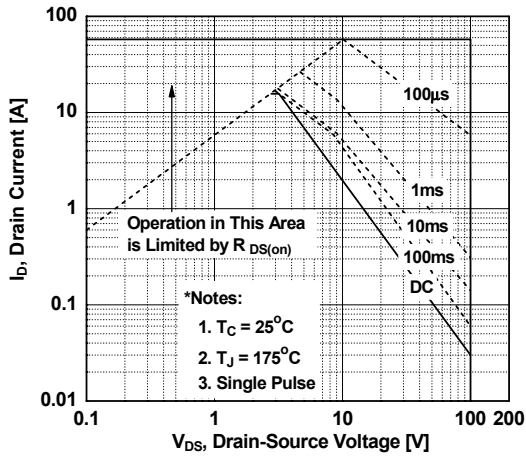


Figure 10. Maximum Drain Current vs. Case Temperature

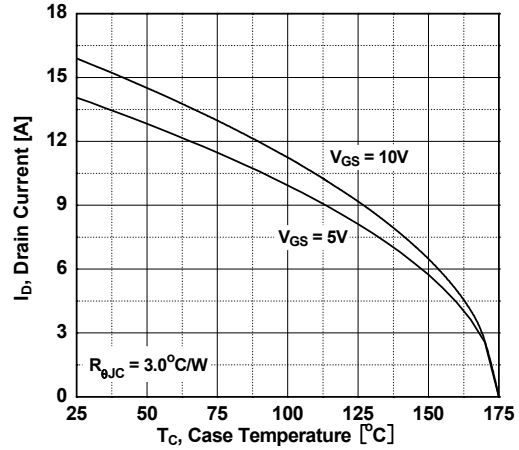


Figure 11. Transient Thermal Response Curve

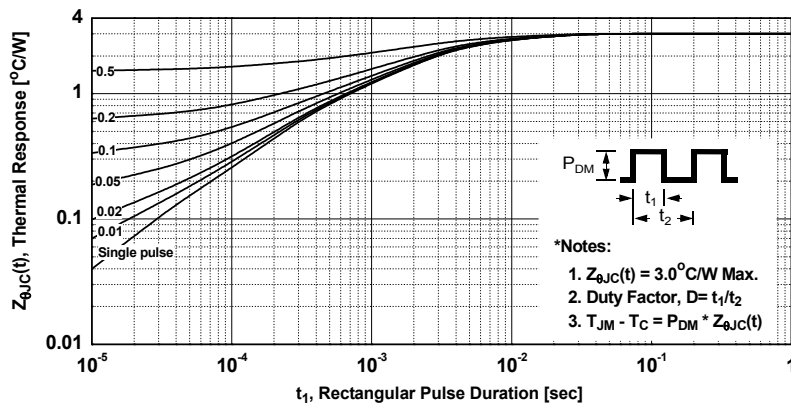




Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms

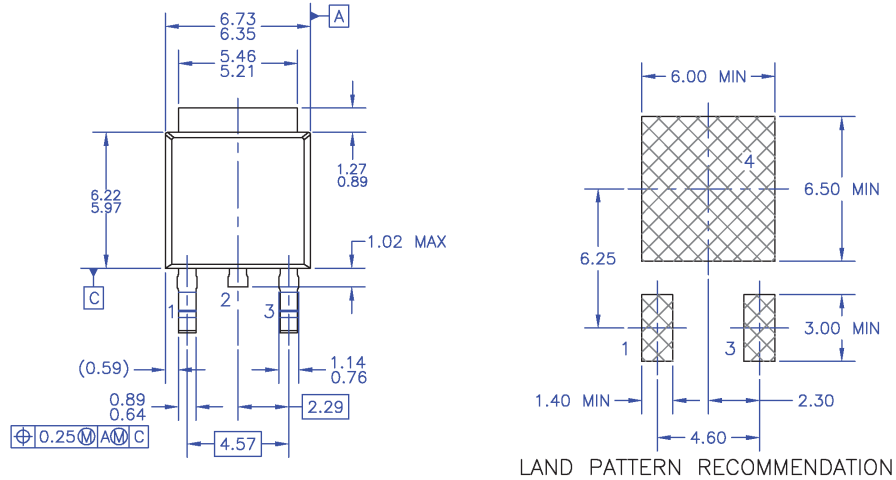


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
 - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC351A STD TO220P1003X238-3N.
 - H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

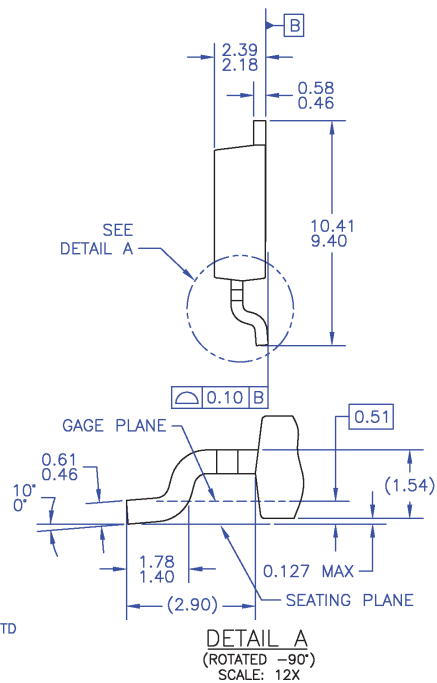


Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype [ameyasales1](#) [ameyasales2](#)

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com