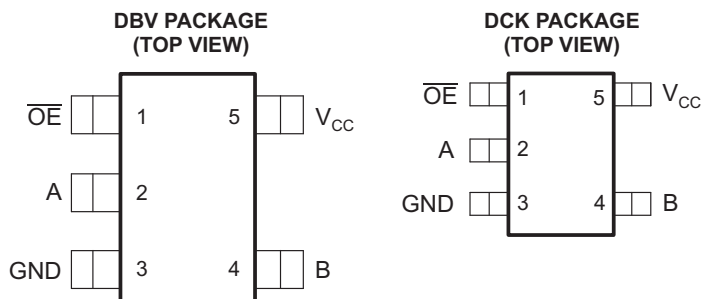


## FEATURES

- **5-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I<sub>off</sub> Supports Partial-Power-Down Mode Operation**



See mechanical drawings for dimensions.

## DESCRIPTION/ORDERING INFORMATION

The SN74CBTLV1G125 features a single high-speed line switch. The switch is disabled when the output-enable ( $\overline{OE}$ ) input is high.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
–40°C to 85°C	SOT (SOT-23) – DBV	Reel of 3000	SN74CBTLV1G125DBVR	V25_
	SOT (SC-70) – DCK	Reel of 3000	SN74CBTLV1G125DCKR	VM_

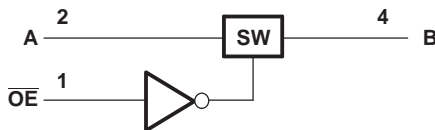
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) The actual top-side marking has one additional character that designates the assembly/test site.

## FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

## LOGIC DIAGRAM (POSITIVE LOGIC)



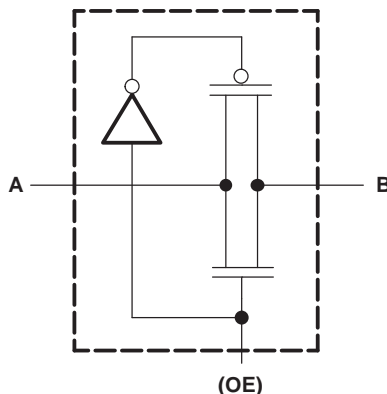
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# SN74CBTLV1G125

## LOW-VOLTAGE SINGLE FET BUS SWITCH

SCDS057H—MARCH 1998—REVISED JUNE 2006

### SIMPLIFIED SCHEMATIC, EACH FET SWITCH



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		−0.5	4.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>		−0.5	4.6	V
Continuous channel current				128	V
I <sub>IK</sub>	Input clamp current	V <sub>I/O</sub> < 0		−50	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup>	DBV package		206	°C/W
		DCK package		252	
T <sub>stg</sub>	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.3	3.6	V
V <sub>IH</sub>	High-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		
V <sub>IL</sub>	Low-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8		
T <sub>A</sub>	Operating free-air temperature		−40	85	°C

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>IK</sub>		V <sub>CC</sub> = 3 V, I <sub>I</sub> = −18 mA				−1.2	V	
I <sub>I</sub>		V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND				±1	μA	
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V				10	μA	
I <sub>CC</sub>		V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND				10	μA	
ΔI <sub>CC</sub> <sup>(2)</sup>	Control inputs	V <sub>CC</sub> = 3.6 V, One input at 3 V, Other inputs at V <sub>CC</sub> or GND				300	μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3 V or 0				2.5	pF	
C <sub>io</sub> (OFF)		V <sub>O</sub> = 3 V or 0, $\overline{OE}$ = V <sub>CC</sub>				7	pF	
r <sub>on</sub> <sup>(3)</sup>	V <sub>CC</sub> = 2.3 V, TYP at V <sub>CC</sub> = 2.5 V	V <sub>I</sub> = 0	I <sub>I</sub> = 64 mA			7	10	Ω
			I <sub>I</sub> = 24 mA			7	10	
		V <sub>I</sub> = 1.7 V,	I <sub>I</sub> = 15 mA			15	25	
	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0	I <sub>I</sub> = 64 mA			5	7	
			I <sub>I</sub> = 24 mA			5	7	
		V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA			10	15	

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

(2) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

(3) Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

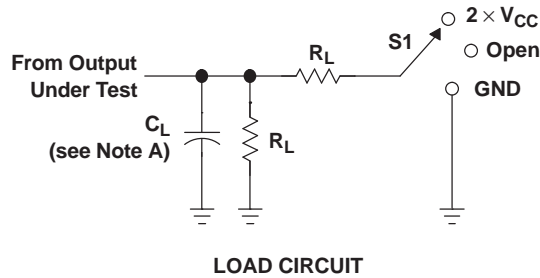
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^{(1)}$	A or B	B or A		0.15		0.25	ns
$t_{en}$	$\overline{OE}$	A or B	1	4	1	4	ns
$t_{dis}$	$\overline{OE}$	A or B	1	5	1	4.1	ns

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance of  $50\text{ pF}$ , when driven by an ideal voltage source (zero output impedance).

# SN74CBTLV1G125 LOW-VOLTAGE SINGLE FET BUS SWITCH

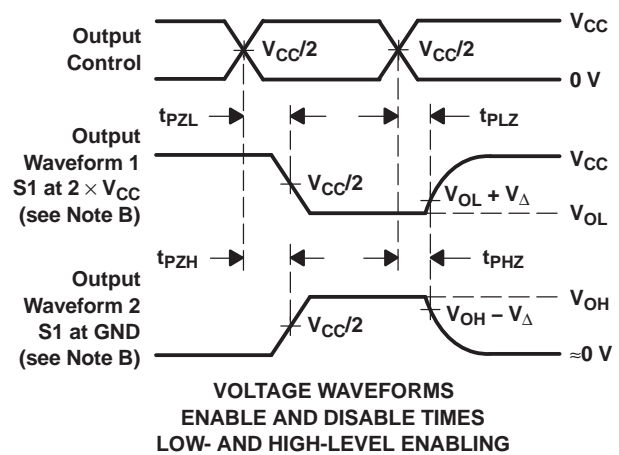
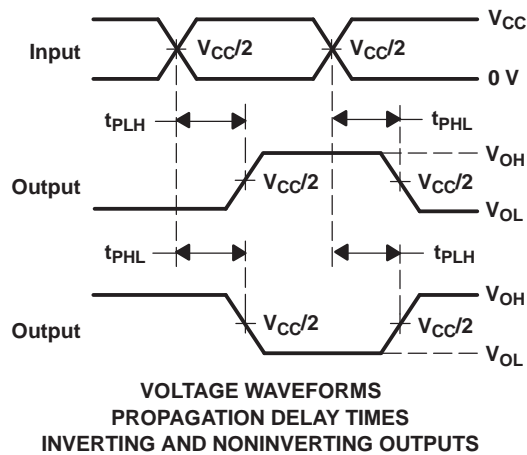
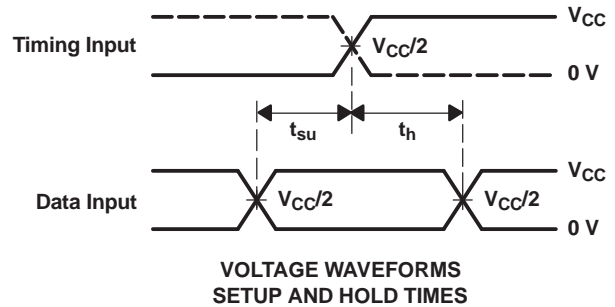
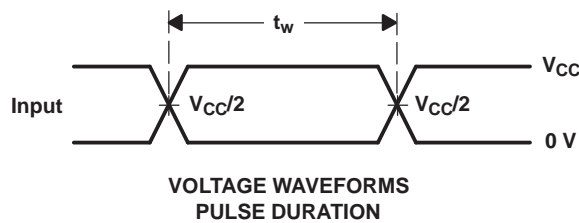
SCDS057H—MARCH 1998—REVISED JUNE 2006

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$C_L$	$R_L$	$V_{\Delta}$
2.5 V $\pm 0.2$ V	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm 0.3$ V	50 pF	500 $\Omega$	0.3 V



- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2$  ns,  $t_f \leq 2$  ns.
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74CBTLV1G125CRE4	ACTIVE	SC70	DCK	5		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
74CBTLV1G125CRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(VM5 ~ VMK ~ VMO ~ VMR)	<a href="#">Samples</a>
74CBTLV1G125DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(V25K ~ V25R)	<a href="#">Samples</a>
74CBTLV1G125DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(V25K ~ V25R)	<a href="#">Samples</a>
74CBTLV1G125DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(VM5 ~ VMK ~ VMO ~ VMR)	<a href="#">Samples</a>
SN74CBTLV1G125DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(V25K ~ V25R)	<a href="#">Samples</a>
SN74CBTLV1G125DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(VM5 ~ VMK ~ VMO ~ VMR)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN74CBTLV1G125 :**

- Automotive: [SN74CBTLV1G125-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTLV1G125DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74CBTLV1G125DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74CBTLV1G125DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTLV1G125DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74CBTLV1G125DBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
SN74CBTLV1G125DCKR	SC70	DCK	5	3000	205.0	200.0	33.0



DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## DCK (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE

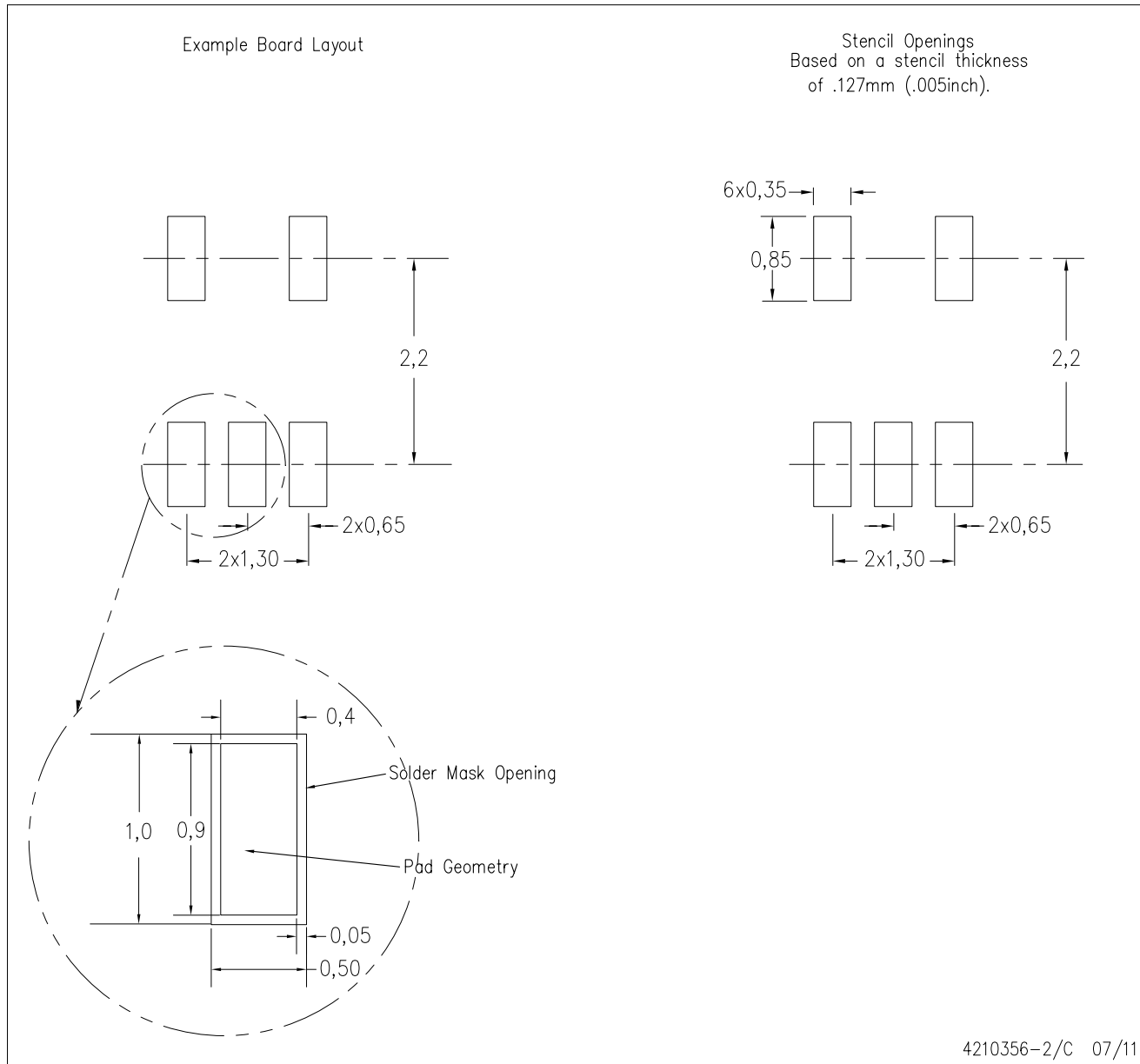


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- NOTES:
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  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
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