TVS Diodes

Transient Voltage Suppressor Diodes

ESD101-B1-02 Series

Bi-directional Ultra Low Capacitance TVS Diode

ESD101-B1-02ELS
ESD101-B1-02EL

Data Sheet

Revision 1.2, 2013-07-22
Final

Power Management & Multimarket

Edition 2013-07-22

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History: Rev. .1.1, 2013-06-12	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.2, 2013-07-22	
All	ESD101-B1-02EL status change to final

Trademarks of Infineon Technologies AG

AURIX™, BlueMoon™, COMNEON™, C166™, CROSSAVE™, CanPAK™, CIPOS™, CoolMOS™, CoolSET™, CORECONTROL™, DAVE™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, EUPEC™, FCOS™, HITFET™, HybridPACK™, ISOFACE™, I²RF™, IsoPACK™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OptiMOS™, ORIGA™, PROFET™, PRO-SIL™, PRIMARION™, PrimePACK™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SINDRION™, SMARTi™, SmartLEWIS™, TEMPFET™, thinQ!™, TriCore™, TRENCHSTOP™, X-GOLD™, XMM™, X-PMU™, XPOSYS™.

Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, PRIMECELL™, REALVIEW™, THUMB™ of ARM Limited, UK. AUTOSAR™ is licensed by AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. FlexRay™ is licensed by FlexRay Consortium. HYPERTERMINAL™ of Hilgraeve Incorporated. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. Mifare™ of NXP. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ Openwave Systems Inc. RED HAT™ Red Hat, Inc. RFMD™ RF Micro Devices, Inc. SIRIUS™ of Sirius Sattelite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Last Trademarks Update 2010-06-09

1 Bi-directional Ultra Low Capacitance TVS Diode

1.1 Features

- ESD / Transient protection of RF signal lines according to
  - **IEC61000-4-2: ±12 kV** (contact), **±14 kV** (air)
- Extremely low capacitance C_L **= 0.1 pF** (typical)
- Maximum working voltage: V_{RWM} **= ±5.5 V**
- Very low reverse current: I_R **< 0.1 nA**
- Very low series inductance down to 0.2 nH typical (TSSLP-2-4)
- Extremely small form factor down to 0.62 x 0.32 x 0.31 mm²
- Pb-free package (RoHS compliant)

1.2 Application Examples

- Tailored for ESD Protection of capacitance-susceptible application like
  - Super high speed interface
  - RF antenna

1.3 Product Description

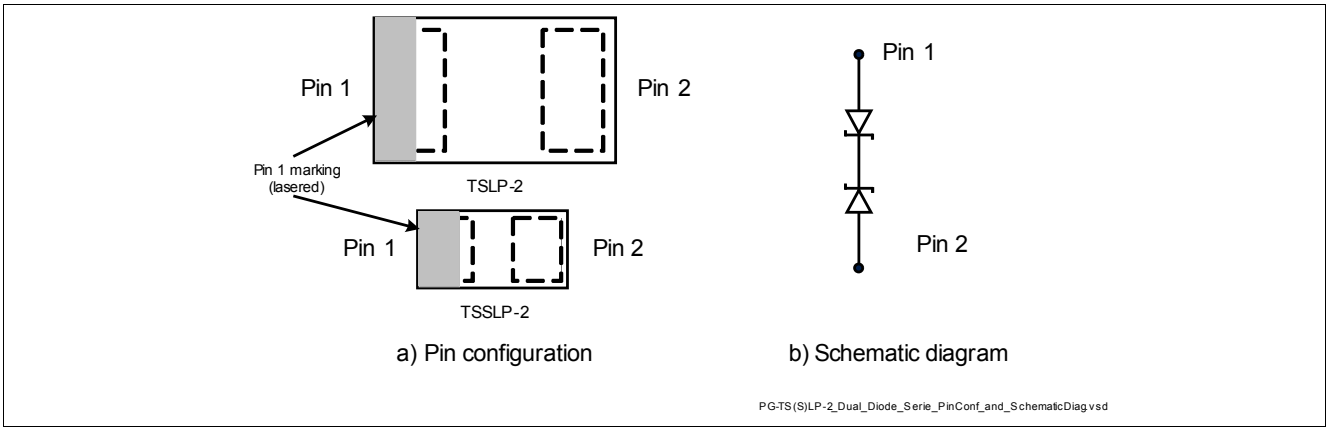

Figure 1 Pin configuration and Schematic diagram

Table 1 Ordering Information

Type	Package	Configuration	Marking code
ESD101-B1-02ELS	TSSLP-2-4	1 line, bi-directional	R
ESD101-B1-02EL	TSLP-2-20	1 line, bi-directional	R

2 Characteristics

Table 2 Maximum Ratings at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD contact discharge[1)] contact air	V_{ESD}	 -12 -14	 – –	 12 14	kV
Operating temperature	T_{OP}	-55	–	125	°C
Storage temperature	T_{stg}	-65	–	150	°C

1) V_{ESD} according to IEC61000-4-2

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.1 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

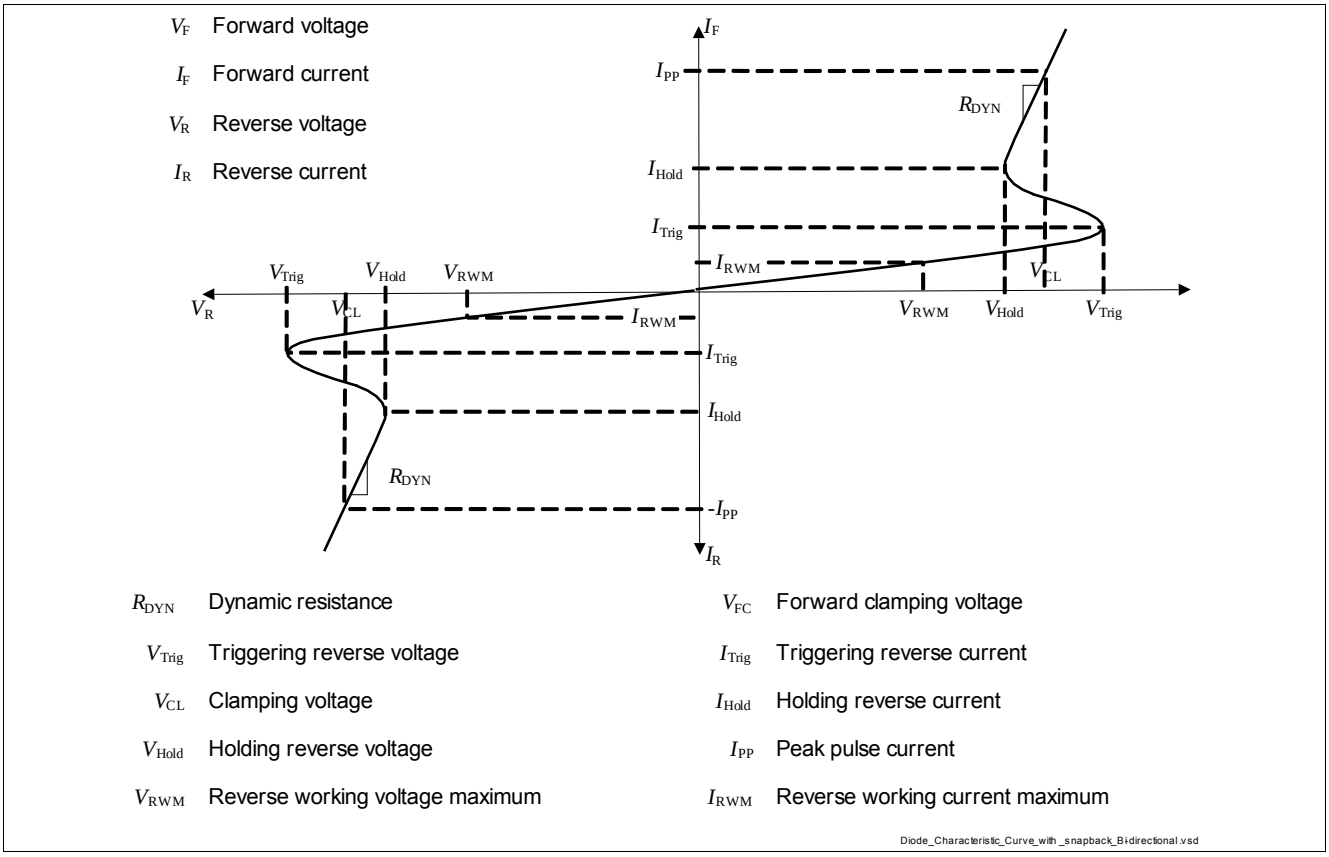

Figure 2 Definitions of electrical characteristics

Table 3 DC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	-5.5	–	5.5	V	
Trigger voltage	V_{Trig}	–	7.3	–	V	I_{BR} = 1 mA, from Pin 1 to Pin 2
		–	7.3	–	V	I_{BR} = 1 mA, from Pin 2 to Pin 1
Reverse current	I_R	–	<1	50	nA	V_R = 5.5 V

Table 4 RF Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	–	0.2	pF	V_R = 0 V, f = 1 MHz
		–	0.1	–	pF	V_R = 0V, f = 1 GHz
Serie inductance	L_S				nH	
		–	0.2	–		ESD101-B1-02ELS
		–	0.4	–		ESD101-B1-02EL

Table 5 ESD Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[1)]	V_{CL}	–	18	–	V	I_{TLP} = 8 A
		–	30	–	V	I_{TLP} = 16 A
Dynamic resistance[1)]	R_{DYN}	–	1.5	–	Ω	t_p = 100 ns

1) ANSI/ESD STM5.5.1 - Electrostatic Discharge Sensitive Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 0.6 ns I_{TLP} and V_{TLP} averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristic between I_{TLP1} = 10 A and I_{TLP2} = 30 A. Please refer to Application Note AN210[1].

3 Typical Characteristic

The curves are all specified at T_A = 25 °C

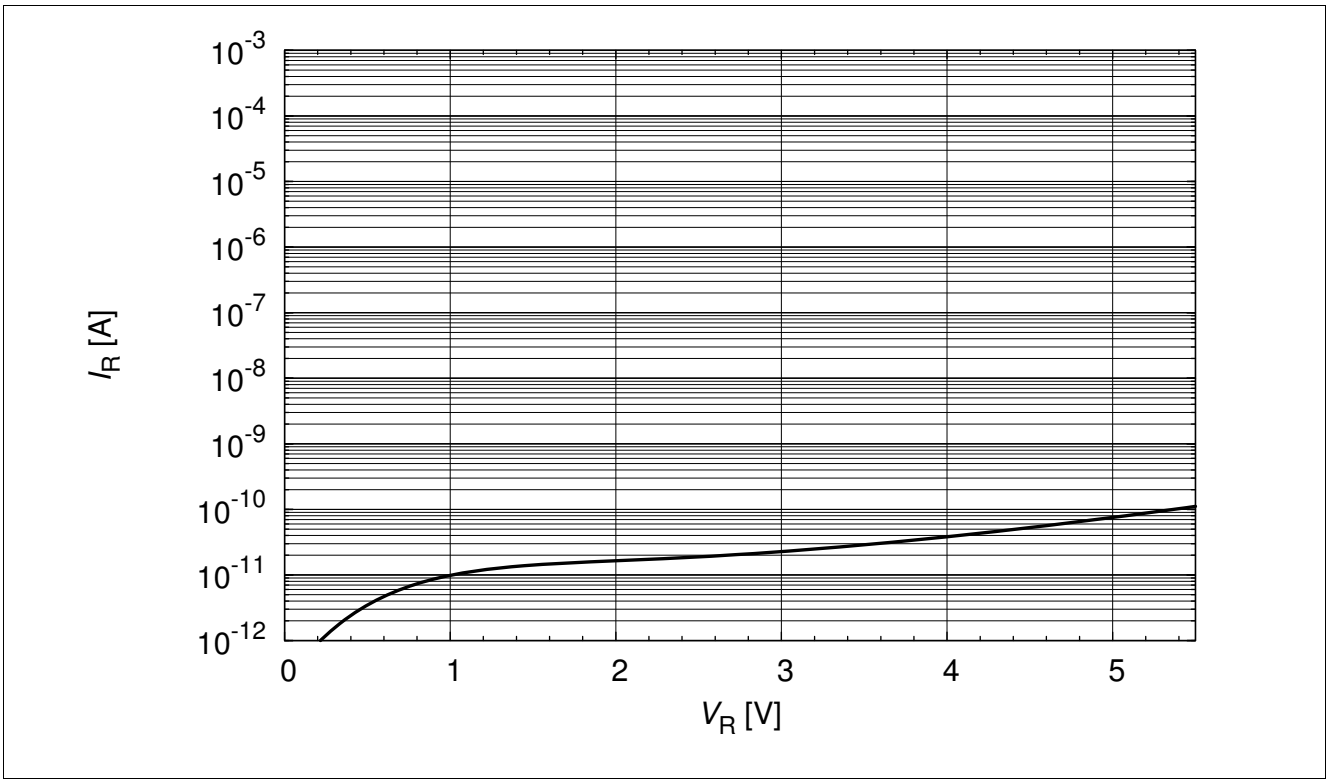

Figure 3 Reverse current: $I_R = f(V_R)$

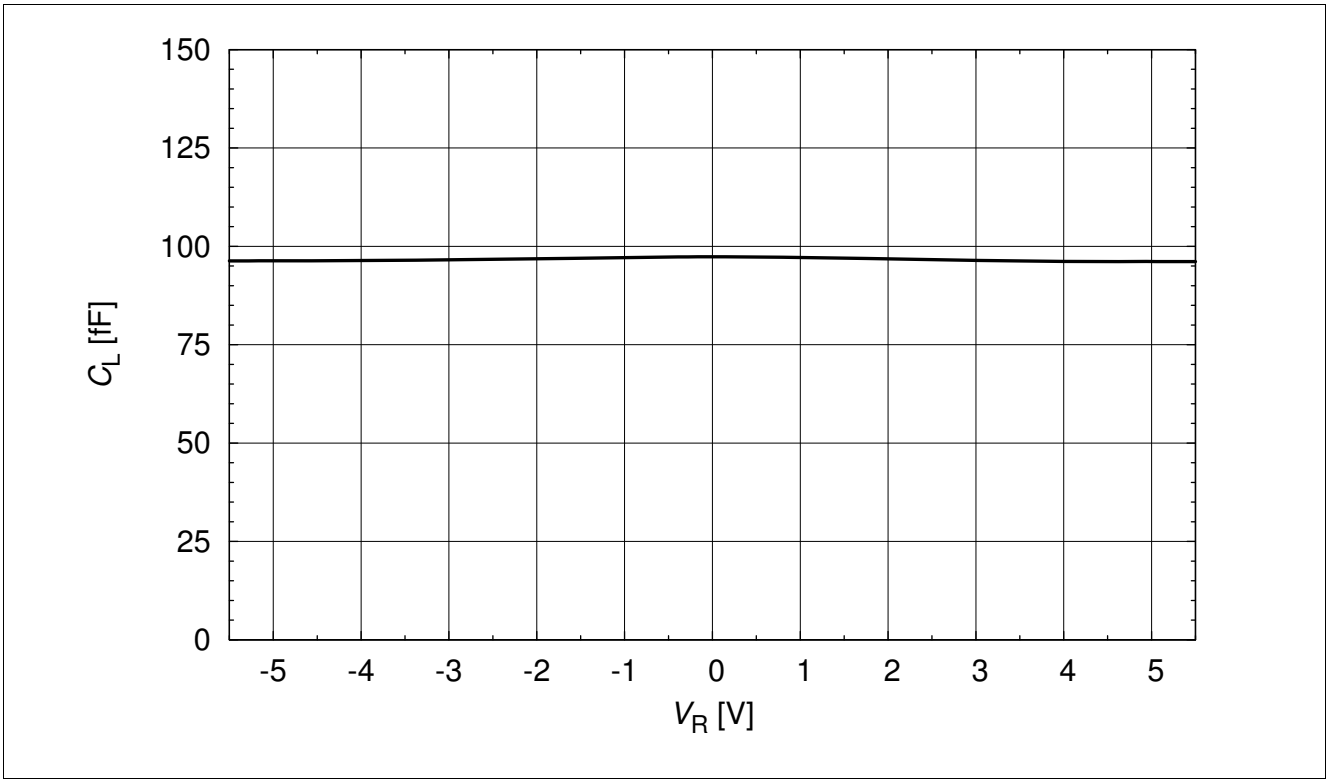

Figure 4 Line capacitance $C_L = f(V_R)$, f z= 1 GHz

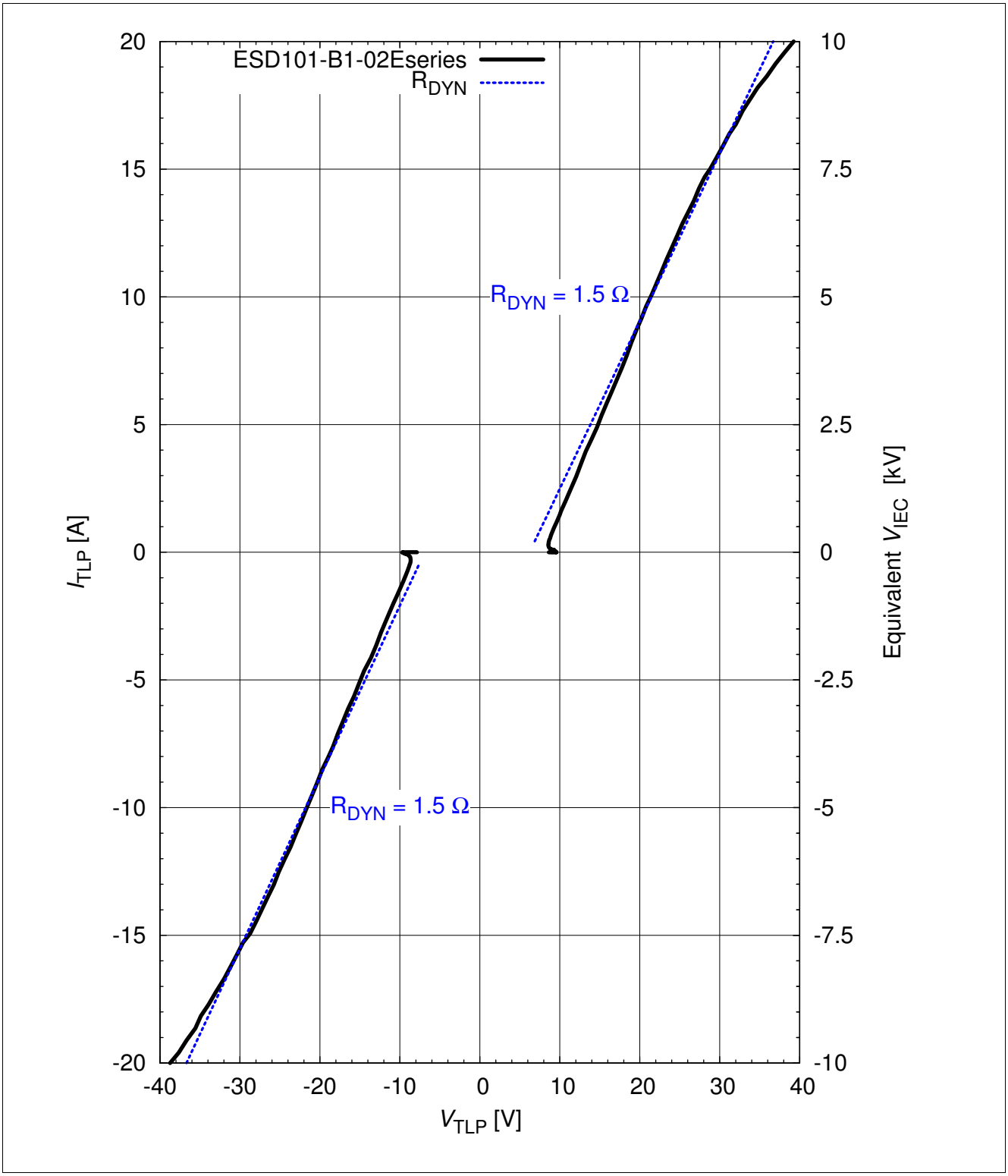

Figure 5 **Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ according ANSI/ESD STM5.5.1- Electrostatic Dischange Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 0.6 ns, I_{TLP} and V_{TLP} averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using squares fit to ELP characterisitic between I_{TLP1} = 5 A and I_{TLP2} = 40 A. Please refer to Application Note AN210 [1]**

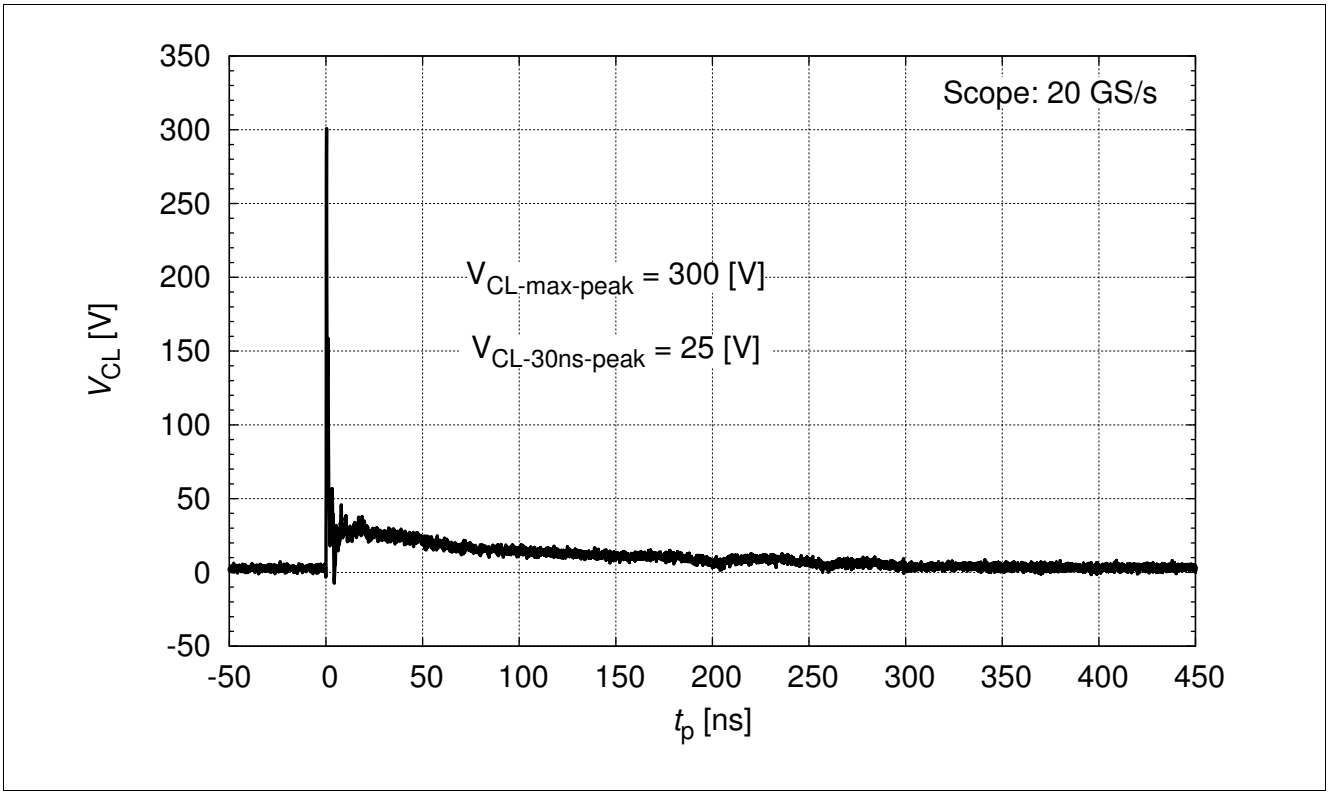

Figure 6 Clamping voltage at +8 kV discharge according IEC61000-4-2 (R = 330 Ω, C = 150 pF)

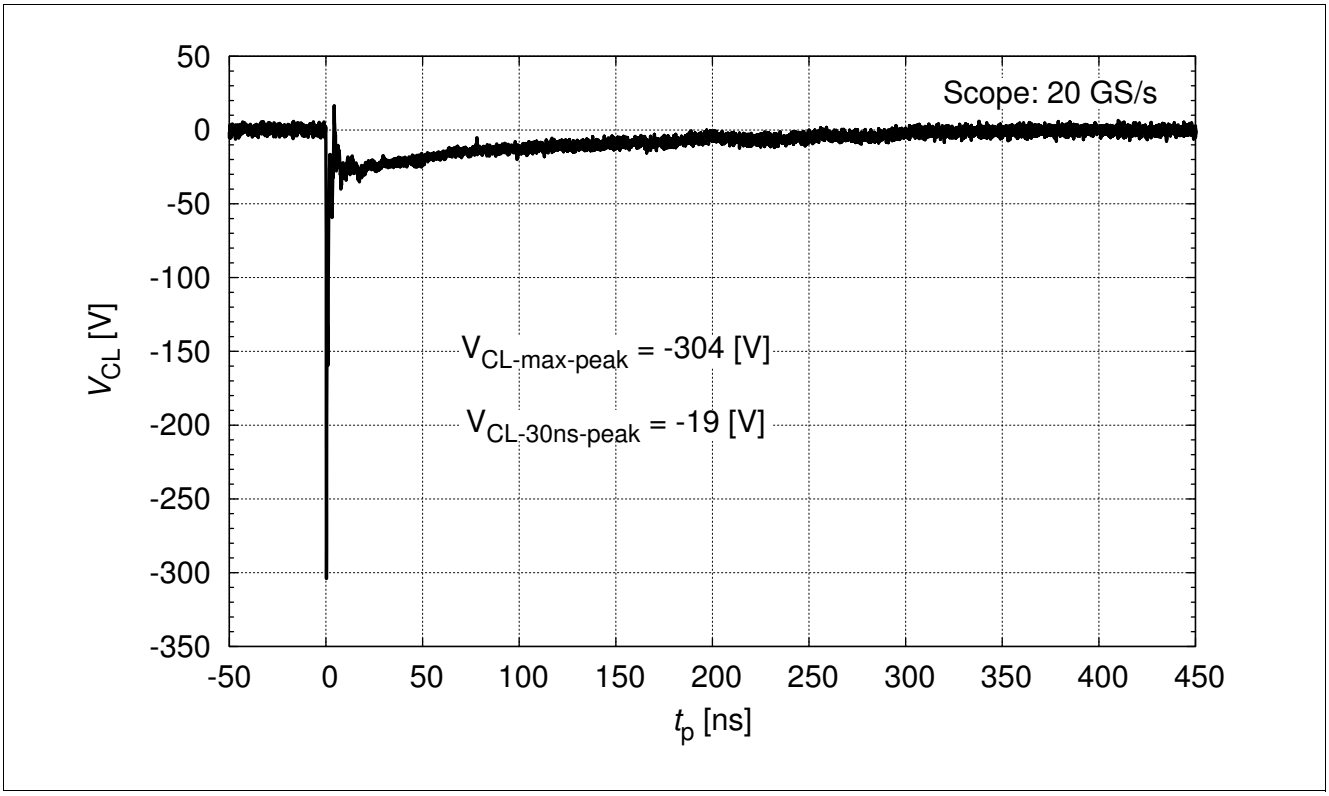

Figure 7 Clamping voltage at -8 kV discharge according IEC61000-4-2 (R = 330 Ω, C = 150 pF)

4 Package Information

4.1 TSSLP-2-4

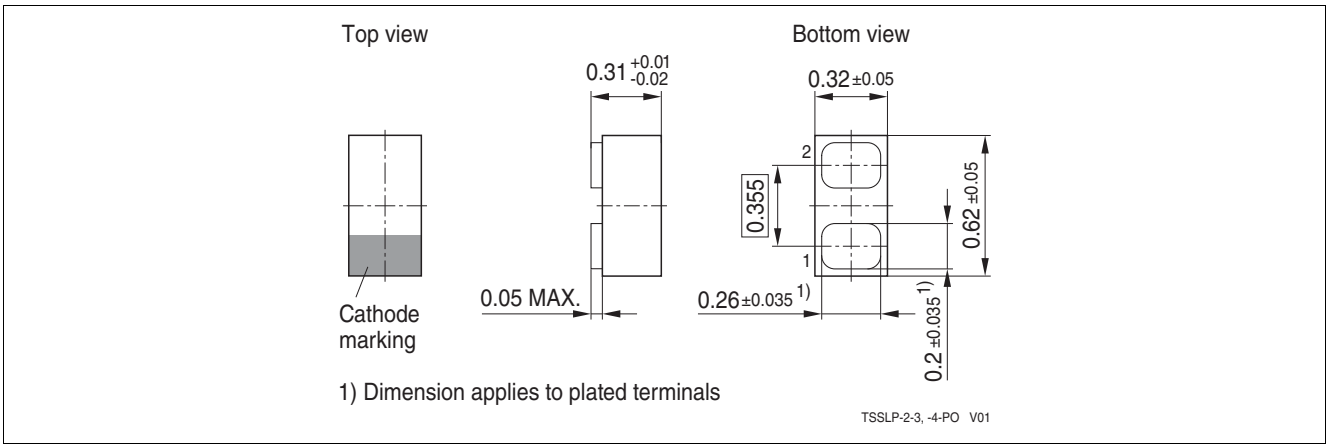

Figure 8 **TSSLP-2-4** Package outline

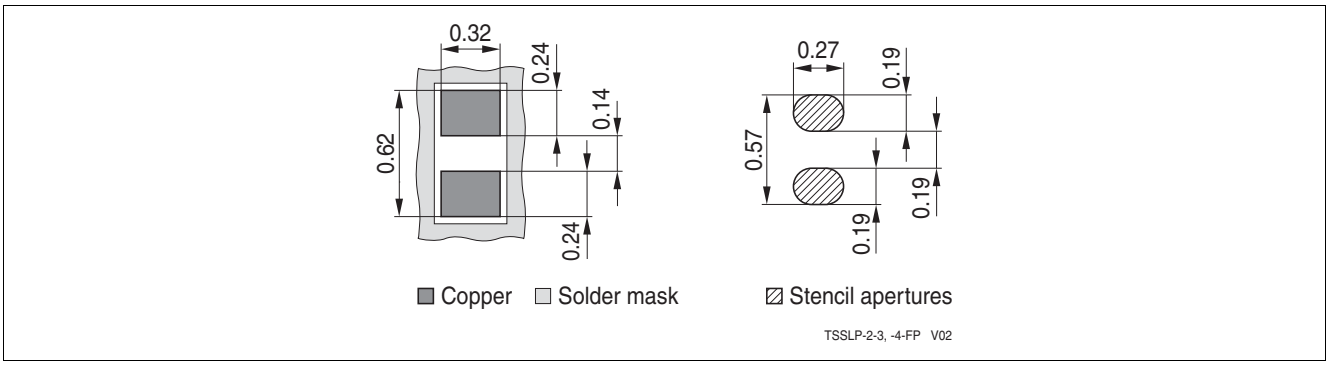

Figure 9 **TSSLP-2-4** Footprint

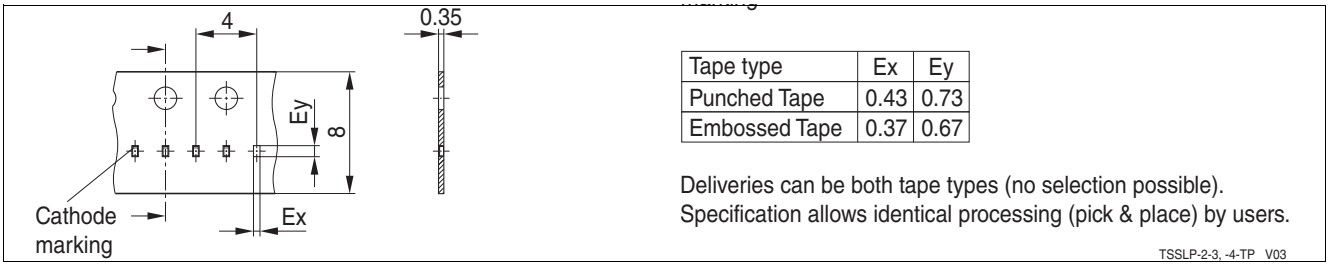

Figure 10 **TSSLP-2-4** Packing

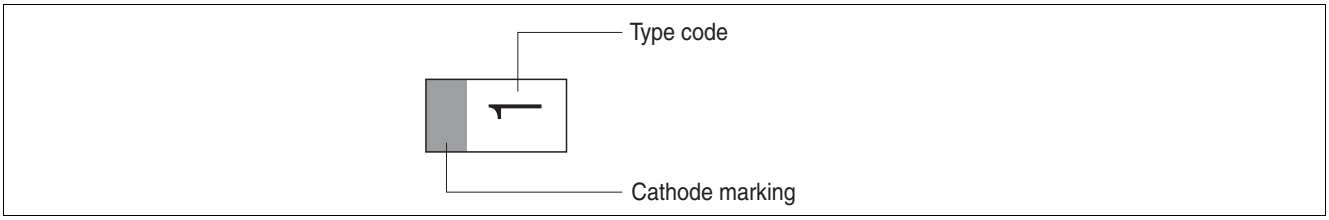

Figure 11 **TSSLP-2-4** Marking (example)

4.2 TSLP-2-20

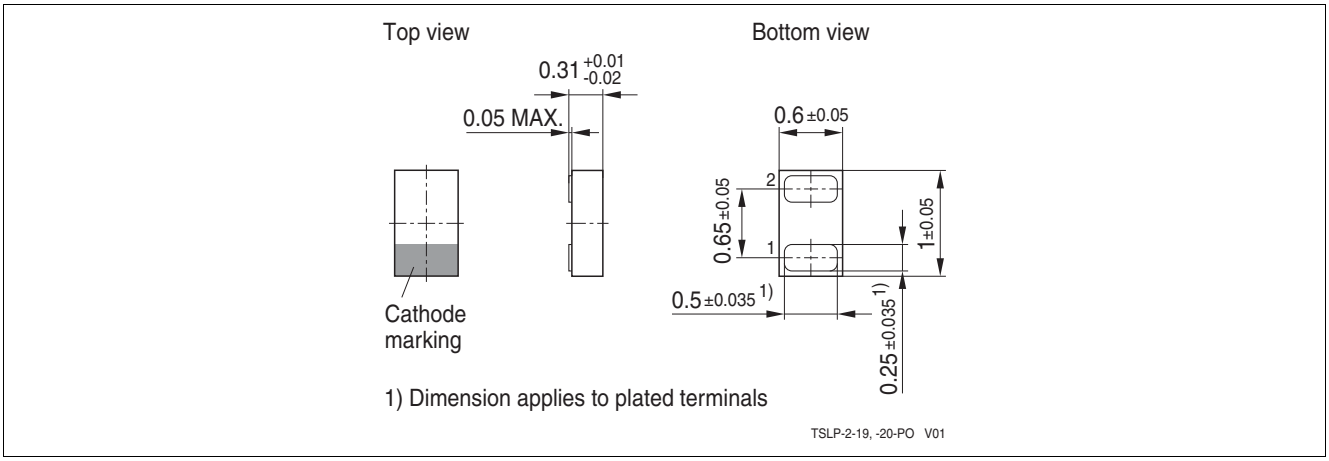

Figure 12 TSLP-2-20 Package outline

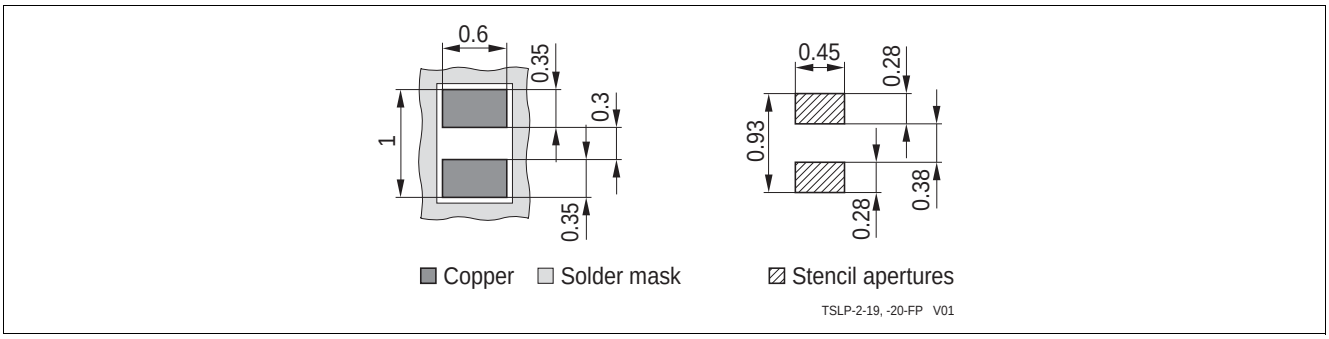

Figure 13 TSLP-2-20 Footprint

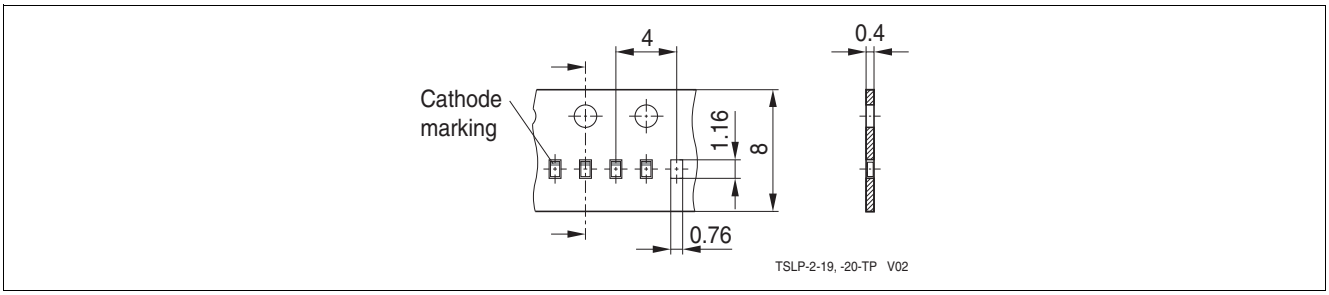

Figure 14 TSLP-2-20 Packing

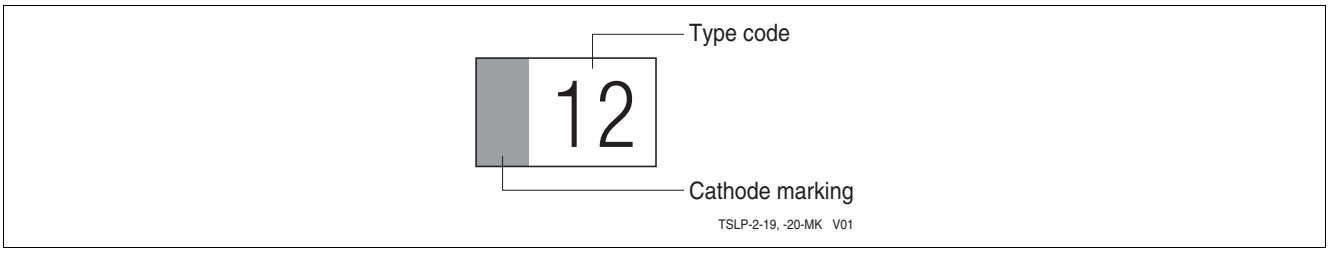

Figure 15 TSLP-2-20 Marking (example)

References

[1] Infineon Technologies AG, “Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology”, Application Note 210, RF and Protection Devices, April 22, 2010, Rev.1.0

[2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG

AMEYA360
Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com