TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor SCHS143C

November 1997 - Revised August 2003

CD54HC125, CD74HC125, CD54HCT125, CD74HCT125

High-Speed CMOS Logic Quad Buffer, Three-State

Features

- Three-State Outputs
- Separate Output Enable Inputs
- Fanout (Over Temperature Range)
 - Standard Outputs..... 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range \ldots -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, II \leq 1 μA at VOL, VOH

Description

The 'HC125 and 'HCT125 contain 4 independent three-state buffers, each having its own output enable input, which when "HIGH" puts the output in the high impedance state.

Ordering Information

PART NUMBER	TEMP. RANGE (^o C)	PACKAGE
CD54HC125F3A	-55 to 125	14 Ld CERDIP
CD54HCT125F3A	-55 to 125	14 Ld CERDIP
CD74HC125E	-55 to 125	14 Ld PDIP
CD74HC125M	-55 to 125	14 Ld SOIC
CD74HC125MT	-55 to 125	14 Ld SOIC
CD74HC125M96	-55 to 125	14 Ld SOIC
CD74HCT125E	-55 to 125	14 Ld PDIP
CD74HCT125M	-55 to 125	14 Ld SOIC
CD74HCT125MT	-55 to 125	14 Ld SOIC
CD74HCT125M96	-55 to 125	14 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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Functional Diagram



TRUTH TABLE

INP	OUTPUTS	
nA	nOE	nY
Н	L	Н
L	L	L
Х	Н	Z

H= High Voltage Level

L= Low Voltage Level X= Don't Care

Z= High Impedance, OFF State

Logic Diagram



Absolute Maximum Ratings

DC Supply Voltage, V _{CC} 0.5V to 7V
DC Input Diode Current, IIK
For V _I < -0.5V or V _I > V _{CC} + 0.5V
DC Output Diode Current, I _{OK}
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$
DC Drain Current, per Output, I _O
For -0.5V < V _O < V _{CC} + 0.5V±35mA
DC Output Source or Sink Current per Output Pin, IO
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$
DC V _{CC} or Ground Current, I _{CC}

Operating Conditions

Temperature Range (T _A)	
Supply Voltage Range, V _{CC}	
НС Турез	
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, VI, VO	\ldots 0V to V _{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ _{JA} (^o C/W)
E (PDIP) Package	80
M (SOIC) Package	86
Maximum Junction Temperature	150 ⁰ C
Maximum Storage Temperature Range6	65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	
(SOIC - Lead Tips Only)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

		TEST CONDITIONS			25 ⁰ C			-40 ⁰ C T	O 85°C	-55°C T			
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	ТҮР	MAX	MIN	MAX	MIN	MAX	UNITS	
HC TYPES			_							-	_	-	
High Level Input	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
High Level Output	V _{OH}	V _{IH} or	-0.02	2	1.9	-	-	1.9	-	1.9	-	V	
Voltage CMOS Loads		VIL	VIL	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V	
High Level Output			-6	4.5	3.98	-	-	3.84	-	3.7	-	V	
Voltage TTL Loads			-7.8	6	5.48	-	-	5.34	-	5.2	-	V	
Low Level Output	V _{OL}	V _{IH} or	0.02	2	-	-	0.1	-	0.1	-	0.1	V	
Voltage CMOS Loads		VIL	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V	
			0.02	6	-	-	0.1	-	0.1	-	0.1	V	
Low Level Output	1		6	4.5	-	-	0.26	-	0.33	-	0.4	V	
Voltage TTL Loads			7.8	6	-	-	0.26	-	0.33	-	0.4	V	
Input Leakage Current	lı	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA	

CD54HC125, CD74HC125, CD54HCT125, CD74HCT125

DC Electrical Spe	cification	S (Con	tinued)											
		TEST CONDITIONS				25 ⁰ C		-40°C TO 85°C		-55°C TO 125°C				
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	ТҮР	MAX	MIN	MAX	MIN	MAX	UNITS		
Quiescent Device Current	ICC	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μΑ		
Three-State Leakage Current	loz	V _{IL} or V _{IH}	-	6	-	-	±0.5	-	±5	-	±10	μΑ		
HCT TYPES														
High Level Input Voltage	VIH	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V		
Low Level Input Voltage	VIL	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V		
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V		
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V		
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V		
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V		
Input Leakage Current	lı	V _{CC} to GND	0	5.5	-	-	±0.1	-	±1	-	±1	μΑ		
Quiescent Device Current	Icc	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA		
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA		
Three-State Leakage Current	I _{OZ}	V _{IL} or V _{IH}	-	5.5	-	-	±0.5	-	±5	-	±10	μA		

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
nA, n OE	1

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., $360\mu A$ max at $25^{\circ}C$.

CD54HC125, CD74HC125, CD54HCT125, CD74HCT125

Switching Specifications Input t_r, t_f = 6ns

		теет		25	°C	-40°C TO 85°C	-55°C TO 125°C	
PARAMETER	SYMBOL	CONDITIONS	V _{CC} (V)	ТҮР	МАХ	МАХ	МАХ	UNITS
HC TYPES								<u> </u>
Propagation Delay Time	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	100	125	150	ns
na to ny			4.5	-	20	25	30	ns
		C _L = 15pF	5	8	-	-	-	ns
		CL = 50pF	6	-	17	21	26	ns
Enable Delay Time	t _{PZL} , t _{PZH}	C _L = 50pF	2	-	125	155	190	ns
			4.5	-	25	31	38	ns
		C _L = 15pF	5	10	-	-	-	ns
		CL = 50pF	6	-	21	26	32	ns
Disable Delay Time	t _{PLZ} , t _{PHZ}	CL = 50pF	2	-	125	155	190	ns
		C _L = 50pF	4.5	-	25	31	38	ns
		C _L = 15pF	5	10	-	-	-	ns
		CL = 50pF	6	-	21	26	32	ns
Output Transition Time	t _{TLH} , t _{THL}	C _L = 50pF	2	-	60	75	90	ns
			4.5	-	12	15	18	ns
			6	-	10	13	15	ns
Input Capacitance	CI	-	-	-	10	10	10	pF
Three-State Output Capacitance	CO	-	-	-	20	20	20	pF
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	-	5	29	-	-	-	pF
HCT TYPES								
Propagation Delay Time	t _{PLH} , t _{PHL}	$C_L = 50 pF$	4.5	-	25	31	38	ns
TIA LOTIT		C _L = 15pF	5	10	-	-	-	ns
Output Enable Time	t _{PZL} , t _{PZH}	C _L = 50pF	4.5	-	25	31	38	ns
		C _L = 15pF	5	10	-	-	-	ns
Output Disabling Time	t _{PLZ} , t _{PHZ}	C _L = 50pF	4.5	-	28	35	42	ns
		C _L = 15pF	5	11	-	-	-	ns
Output Transition Times	t _{TLH} , t _{THL}	C _L = 50pF	4.5	-	12	15	18	ns
Input Capacitance	Cl	-	-	-	10	10	10	pF
Three-State Output Capacitance	CO	-	-	-	20	20	20	pF
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	-	5	34	-	-	-	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per channel. 4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.



FIGURE 5. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT



17-May-2014

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
CD54HC125F	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC125F	Samples
CD54HC125F3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8772101CA CD54HC125F3A	Samples
CD54HCT125F3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HCT125F3A	Samples
CD74HC125E	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC125E	Samples
CD74HC125EE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC125E	Samples
CD74HC125M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC125M	Samples
CD74HC125M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC125M	Samples
CD74HC125M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC125M	Samples
CD74HC125M96G4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125		Samples
CD74HC125ME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC125M	Samples
CD74HC125MG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC125M	Samples
CD74HC125MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC125M	Samples
CD74HC125MTE4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125		Samples
CD74HC125MTG4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125		Samples
CD74HCT125E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT125E	Samples
CD74HCT125EE4	ACTIVE	PDIP	Ν	14		TBD	Call TI	Call TI	-55 to 125		Samples
CD74HCT125M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT125M	Samples
CD74HCT125M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT125M	Samples



17-May-2014

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
CD74HCT125M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT125M	Samples
CD74HCT125M96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT125M	Samples
CD74HCT125ME4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125		Samples
CD74HCT125MG4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125		Samples
CD74HCT125MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT125M	Samples
CD74HCT125MTE4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125		Samples
CD74HCT125MTG4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125		Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



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PACKAGE OPTION ADDENDUM

17-May-2014

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD54HC125, CD54HCT125, CD74HC125, CD74HC125;

- Catalog: CD74HC125, CD74HCT125
- Automotive: CD74HC125-Q1, CD74HC125-Q1
- Military: CD54HC125, CD54HCT125

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TEXAS INSTRUMENTS





TAPE AND REEL INFORMATION

TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal													
	Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	CD74HC125M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
	CD74HC125MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
	CD74HCT125M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
ſ	CD74HCT125MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

14-Jul-2012



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC125M96	SOIC	D	14	2500	367.0	367.0	38.0
CD74HC125MT	SOIC	D	14	250	367.0	367.0	38.0
CD74HCT125M96	SOIC	D	14	2500	367.0	367.0	38.0
CD74HCT125MT	SOIC	D	14	250	367.0	367.0	38.0

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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