KS8995XA

Integrated 5-Port 10/100 QoS Switch

Rev 2.6

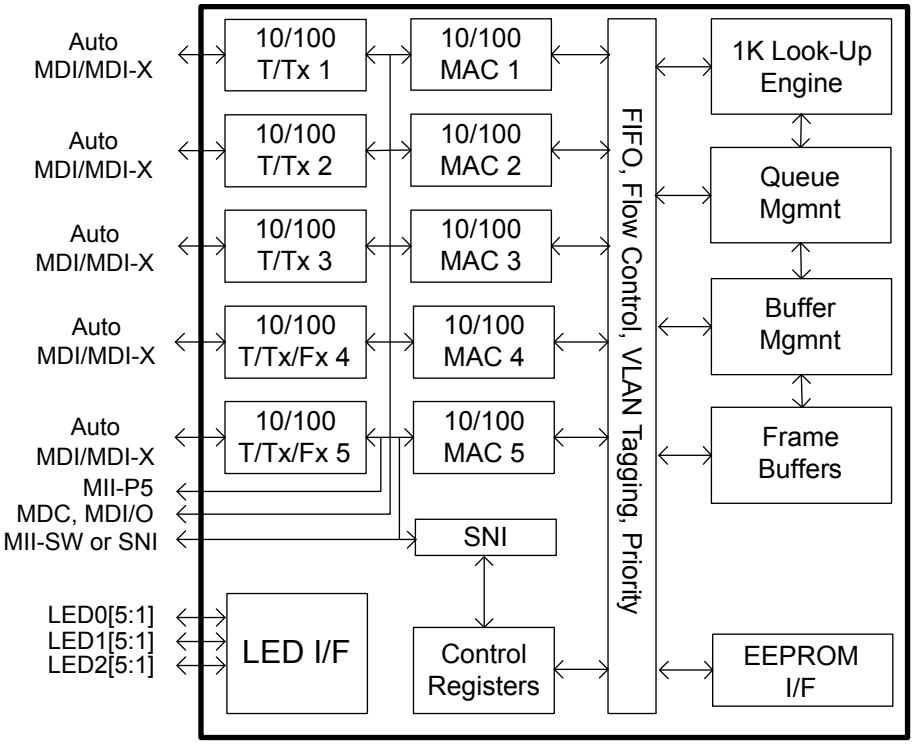
General Description

The KS8995XA is a highly integrated Layer-2 quality of service (QoS) switch with optimized bill of materials (BOM) cost for low port count, cost-sensitive 10/100Mbps switch systems. It also provides an extensive feature set including three different QoS priority schemes, a dual MII interface for BOM cost reduction, rate limiting to offload CPU tasks, software and hardware power-down, a MDC/MDIO control interface and port mirroring/monitoring to effectively address both current and emerging Fast Ethernet applications.

The KS8995XA contains five 10/100 transceivers with patented mixed-signal low-power technology, five media access control (MAC) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory.

All PHY units support 10BASE-T and 100BASE-TX. In addition, two of the PHY units support 100BaseFX (Ports 4 and 5).

Functional Diagram



KS8995XA

Features

- Integrated switch with five MACs and five Fast Ethernet transceivers fully compliant to IEEE 802.3u standard
- Shared memory based switch fabric with fully nonblocking configuration
- 10BASE-T, 100BASE-TX and 100BASE-FX modes (FX in Ports 4 and 5)
- Dual MII configuration: MII-Switch (MAC or PHY mode MII) and MII-P5 (PHY mode MII)
- VLAN ID tag/untag options, per-port basis
- Enable/disable option for huge frame size up to 1916 bytes per frame
- Broadcast storm protection with percent control – global and per-port basis
- Optimization for fiber-to-copper media conversion
- Full-chip hardware power-down support (register configuration not saved)
- Per-port-based software power-save on PHY (idle link detection, register configuration preserved)
- QoS/CoS packets prioritization supports: per port, 802.1p and DiffServ-based
- 802.1p/q tag insertion or removal on a per-port basis (egress)
- Port-based VLAN support
- MDC and MDI/O interface support to access the MII PHY control registers (not all control registers)
- MII local loopback support
- On-chip 64Kbyte memory for frame buffering (not shared with 1K unicast address table)
- 1.4Gbps high performance memory bandwidth
- Wire-speed reception and transmission
- Integrated look-up engine with dedicated 1K unicast MAC addresses
- Automatic address learning, address aging and address migration
- Full-duplex IEEE 802.3x and half-duplex back pressure flow control
- Comprehensive LED support
- 7-wire SNI support for legacy MAC interface
- Automatic MDI/MDI-X crossover for plug-and-play
- Disable automatic MDI/MDI-X option
- Low power
  Core: 1.8V
  Digital I/O: 3.3V
  Analog I/O: 2.5 or 3.3V
- 0.18µm CMOS technology
- Commercial temperature range: 0°C to +70°C
- Available in 128-pin PQFP package

Applications

- Broadband gateway/firewall/VPN
- Integrated DSL or cable modem multi-port router
- Wireless LAN access point plus gateway
- Home networking expansion
- Standalone 10/100 switch
- Hotel/campus/MxU gateway
- Enterprise VoIP gateway/phone
- FTTx customer premise equipment
- Media converter

Ordering Information

Part Number		Temperature Range	Package
Standard	**Pb-Free**		
KS8995XA	KSZ8995XA	0°C to +70°C	128-Pin PQFP

Revision History

Revision	Date	Summary of Changes
2.0	10/15/03	Created.
2.1	4/1/04	Editorial changes on TTL input and output electrical characteristics.
2.2	1/19/05	Insert recommended reset circuit.
2.3	4/13/05	Switched pins names for pins 7 & 8 on page 16. Changed VDDIO to 3.3V. Changed Jitter to 16 ns Max.
2.4	7/14/06	Update pin description for PCRS, PCOL, etc. Update the description of the register and MIIM register for the loop-back, etc. And update the MII timing diagram.
2.5	6/01/07	Add package thermal information in the operating rating and the transformer power consumption information in the electrical characteristics note.
2.6	9/15/08	Add description for the revision ID and LED mode, etc.

Contents

System Level Applications

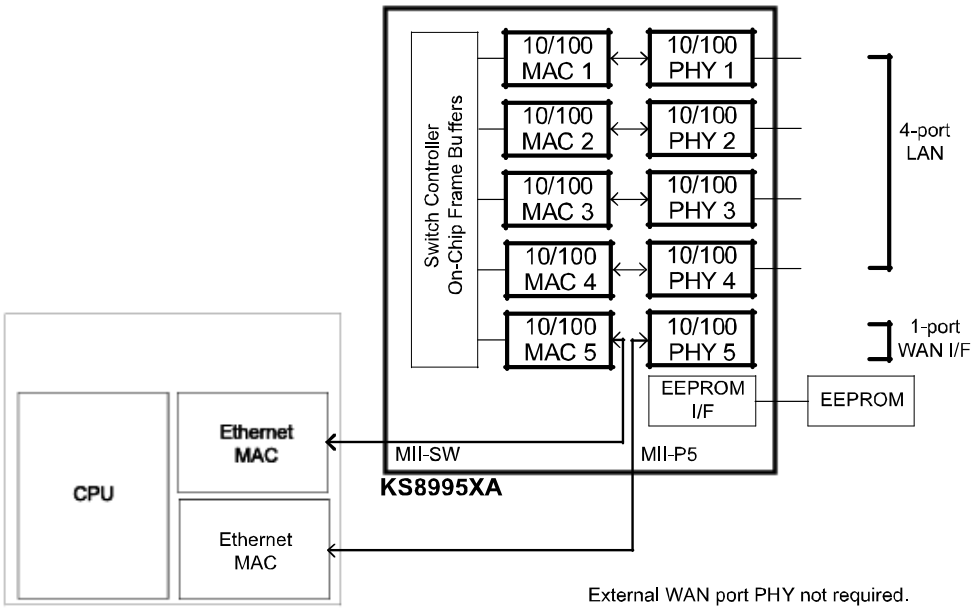


Figure 1. Broadband Gateway

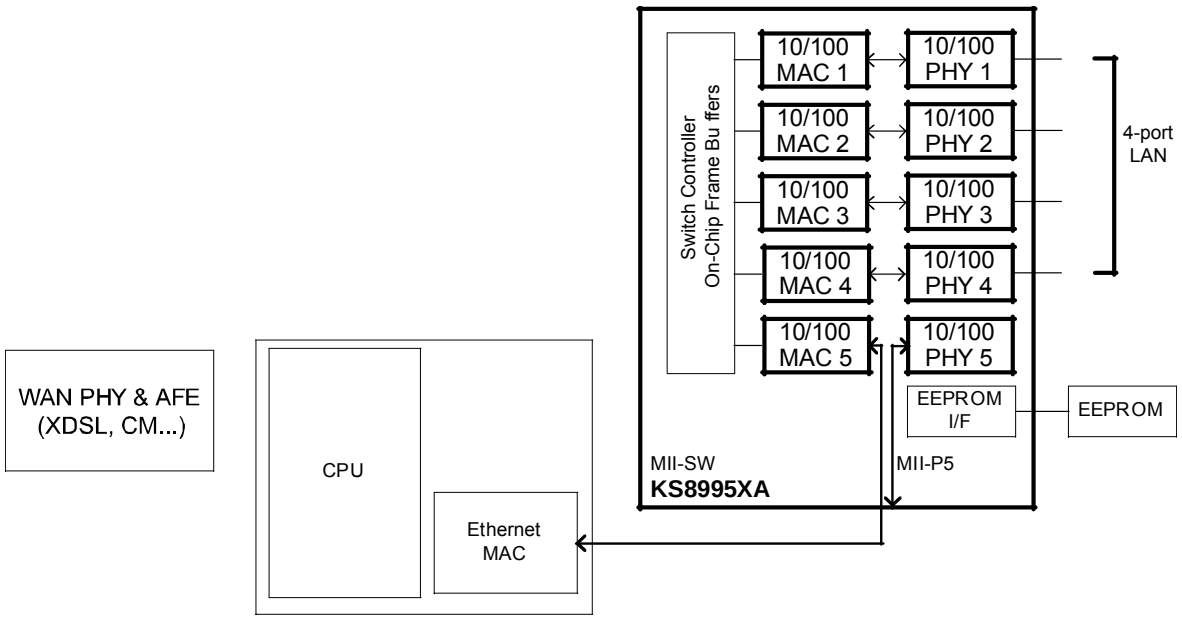


Figure 2. Integrated Broadband Router

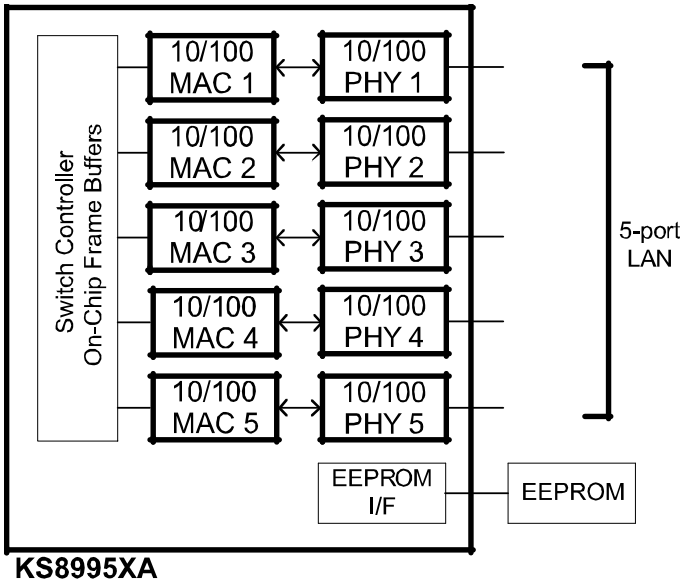
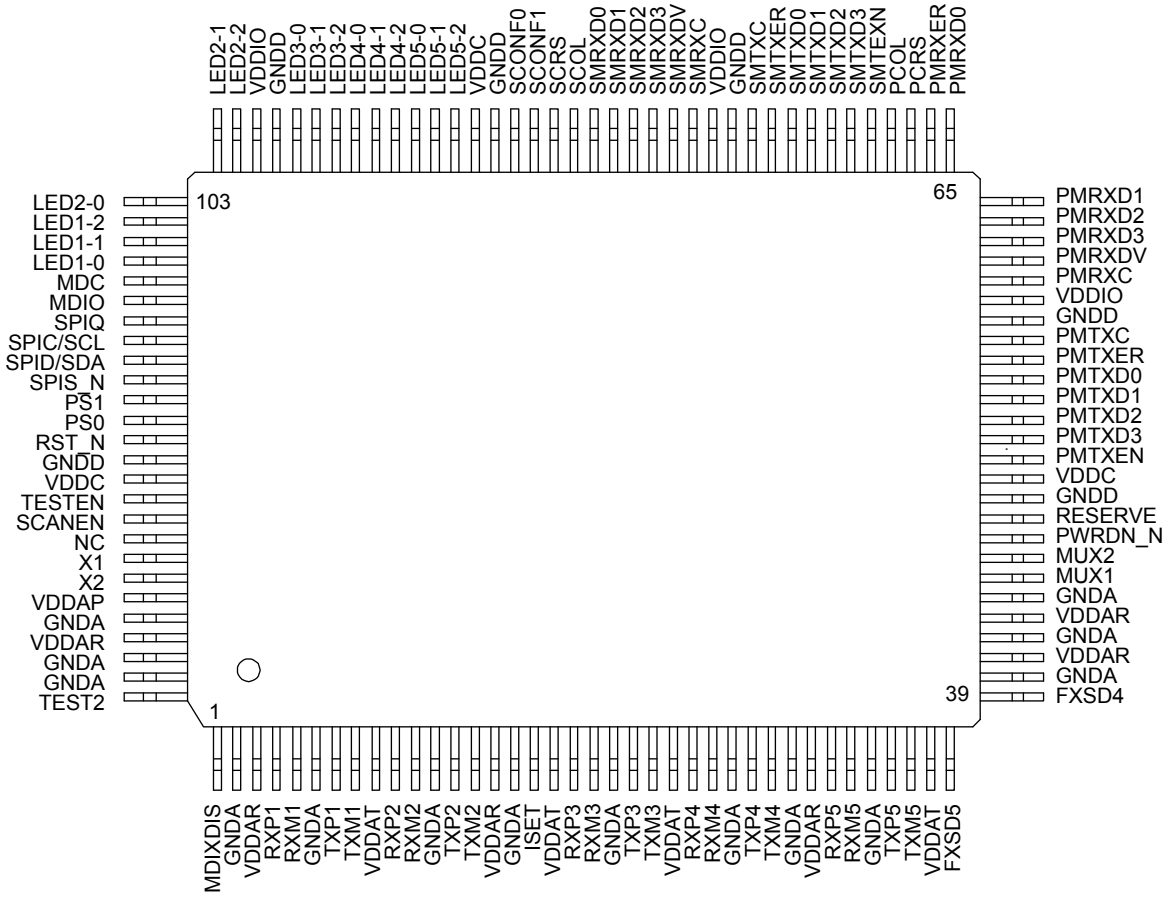


Figure 3. Standalone Switch

Pin Configuration



128-Pin PQFP (PQ)

Pin Description (by Number)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
1	MDI-XDIS	Ipd	1-5	Disable auto MDI/MDI-X. PD (default) = normal operation. PU = disable auto MDI/MDI-X on all ports.
2	GNDA	Gnd		Analog ground.
3	VDDAR	P		1.8V analog V_{DD}.
4	RXP1	I	1	Physical receive signal + (differential).
5	RXM1	I	1	Physical receive signal – (differential).
6	GNDA	Gnd		Analog ground.
7	TXP1	O	1	Physical transmit signal + (differential).
8	TXM1	O	1	Physical transmit signal – (differential).
9	VDDAT	P		2.5V or 3.3V analog V_{DD}.
10	RXP2	I	2	Physical receive signal + (differential).
11	RXM2	I	2	Physical receive signal – (differential).
12	GNDA	Gnd		Analog ground.
13	TXP2	O	2	Physical transmit signal + (differential).
14	TXM2	O	2	Physical transmit signal – (differential).
15	VDDAR	P		1.8V analog V_{DD}.
16	GNDA	Gnd		Analog ground.
17	ISET			Set physical transmit output current. Pull-down with a 3.01kΩ1% resistor.
18	VDDAT	P		2.5V or 3.3V analog V_{DD}.
19	RXP3	I	3	Physical receive signal + (differential).
20	RXM3	I	3	Physical receive signal - (differential).
21	GNDA	Gnd		Analog ground.
22	TXP3	O	3	Physical transmit signal + (differential).
23	TXM3	O	3	Physical transmit signal – (differential).
24	VDDAT	P		2.5V or 3.3V analog V_{DD}.
25	RXP4	I	4	Physical receive signal + (differential).
26	RXM4	I	4	Physical receive signal - (differential).
27	GNDA	Gnd		Analog ground.
28	TXP4	O	4	Physical transmit signal + (differential).
29	TXM4	O	4	Physical transmit signal – (differential).
30	GNDA	Gnd		Analog ground.

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   Gnd = Ground.
   Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.
   Otri = Output tristated.

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
31	VDDAR	P		1.8V analog V_{DD}.
32	RXP5	I	5	Physical receive signal + (differential).
33	RXM5	I	5	Physical receive signal – (differential).
34	GNDA	Gnd		Analog ground.
35	TXP5	O	5	Physical transmit signal + (differential).
36	TXM5	O	5	Physical transmit signal – (differential).
37	VDDAT	P		2.5V or 3.3V analog V_{DD}.
38	FXSD5	I	5	Fiber signal detect/factory test pin.
39	FXSD4	I	4	Fiber signal detect/factory test pin.
40	GNDA	Gnd		Analog ground.
41	VDDAR	P		1.8V analog V_{DD}.
42	GNDA	Gnd		Analog ground.
43	VDDAR	P		1.8V analog V_{DD}.
44	GNDA	Gnd		Analog ground.
45	NC / MUX1	I		No connect. Factory test pin.
46	NC / MUX2	I		No connect. Factory test pin.
47	PWRDN_N	Ipu		Full-chip power down. Active low.
48	RESERVE/NC			Reserved pin. No connect.
49	GNDD	Gnd		Digital ground.
50	VDDC	P		1.8V digital core V_{DD}.
51	PMTXEN	Ipd	5	PHY[5] MII transmit enable.
52	PMTXD3	Ipd	5	PHY[5] MII transmit bit 3.
53	PMTXD2	Ipd	5	PHY[5] MII transmit bit 2.
54	PMTXD1	Ipd	5	PHY[5] MII transmit bit 1.
55	PMTXD0	Ipd	5	PHY[5] MII transmit bit 0.
56	PMTXER	Ipd	5	PHY[5] MII transmit error.
57	PMTXC	O	5	PHY[5] MII transmit clock. PHY mode MII.
58	GNDD	Gnd		Digital ground.
59	VDDIO	P		3.3V digital V_{DD} for digital I/O circuitry.
60	PMRXC	O	5	PHY[5] MII receive clock. PHY mode MII.

Notes:

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   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.
   Otri = Output tristated.

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
61	PMRXDV	Ipd/O	5	PHY[5] MII receive data valid.
62	PMRXD3	Ipd/O	5	PHY[5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control.
63	PMRXD2	Ipd/O	5	PHY[5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure.
64	PMRXD1	Ipd/O	5	PHY[5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.
65	PMRXD0	Ipd/O	5	PHY[5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.
66	PMRXER	Ipd/O	5	PHY[5] MII receive error. Strap option: PD (default) = packet size 1518/1522 bytes; PU = 1536 bytes.
67	PCRS	Ipd/O	5	PHY[5] MII carrier sense/strap option for port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto negotiation is disabled or fails. Refer to Register 76.
68	PCOL	Ipd/O	5	PHY[5] MII collision detect/ strap option for port 4 only. PD (default) = no force flow control, normal operation. PU = force flow control. Refer to Register 66.
69	SMTXEN	Ipd		Switch MII transmit enable.
70	SMTXD3	Ipd		Switch MII transmit bit 3.
71	SMTXD2	Ipd		Switch MII transmit bit 2.
72	SMTXD1	Ipd		Switch MII transmit bit 1.
73	SMTXD0	Ipd		Switch MII transmit bit 0.
74	SMTXER	Ipd		Switch MII transmit error.
75	SMTXC	I/O		Switch MII transmit clock. PHY or MAC mode MII.
76	GNDD	Gnd		Digital ground.
77	VDDIO	P		3.3V digital V_{DD} for digital I/O circuitry.
78	SMRXC	I/O		Switch MII receive clock. PHY or MAC mode MII.
79	SMRXDV	Ipd/O		Switch MII receive data valid.
80	SMRXD3	Ipd/O		Switch MII receive bit 3. Strap option: PD (default) = Disable Switch MII full-duplex flow control; PU = Enable Switch MII full-duplex flow control.
81	SMRXD2	Ipd/O		Switch MII receive bit 2. Strap option: PD (default) = Switch MII in full-duplex mode; PU = Switch MII in half-duplex mode.
82	SMRXD1	Ipd/O		Switch MII receive bit 1. Strap option: PD (default) = Switch MII in 100Mbps mode; PU = Switch MII in 10Mbps mode.
83	SMRXD0	Ipd/O		Switch MII receive bit 0; Strap option: see “Register 11[1].”
84	SCOL	Ipd/O		Switch MII collision detect.
85	SCRS	Ipd/O		Switch mode carrier sense.

Notes:

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   Gnd = Ground.
   Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.
   Otri = Output tristated.

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]		
86	SCONF1	Ipd		Dual MII configuration pin.		
				Pin# (91, 86, 87):	**Switch MII**	**PHY [5] MII**
				000	Disable, Otri	Disable, Otri
				001	PHY Mode MII	Disable, Otri
				010	MAC Mode MII	Disable, Otri
				011	PHY Mode SNI	Disable, Otri
				100	Disable	Disable
				101	PHY Mode MII	PHY Mode MII
				110	MAC Mode MII	PHY Mode MII
				111	PHY Mode SNI	PHY Mode MII
87	SCONF0	Ipd		Dual MII configuration pin.		
88	GNDD	Gnd		Digital ground.		
89	VDDC	P		1.8V digital core V_{DD}.		
90	LED5-2	Ipu/O	5	LED indicator 2. Aging setup. See “Aging” section.		
91	LED5-1	Ipu/O	5	LED indicator 1. Strap option: PU (default): enable PHY[5] MII I/F. PD: tristate all PHY[5] MII output. See “Pin# 86 SCONF1.”		
92	LED5-0	Ipu/O	5	LED indicator 0.		
93	LED4-2	Ipu/O	4	LED indicator 2.		
94	LED4-1	Ipu/O	4	LED indicator 1.		
95	LED4-0	Ipu/O	4	LED indicator 0.		
96	LED3-2	Ipu/O	3	LED indicator 2.		
97	LED3-1	Ipu/O	3	LED indicator 1.		
98	LED3-0	Ipu/O	3	LED indicator 0.		
99	GNDD	Gnd		Digital ground.		
100	VDDIO	P		3.3V digital V_{DD} for digital I/O.		
101	LED2-2	Ipu/O	2	LED indicator 2.		
102	LED2-1	Ipu/O	2	LED indicator 1.		
103	LED2-0	Ipu/O	2	LED indicator 0.		
104	LED1-2	Ipu/O	1	LED indicator 2.		
105	LED1-1	Ipu/O	1	LED indicator 1.		
106	LED1-0	Ipu/O	1	LED indicator 0.		

Notes:

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   I/O = Bidirectional.
   Gnd = Ground.
   Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.
   Otri = Output tristated.

Pin Number	Pin Name	Type[1]	Port	Pin Function
106	LED1-0	Ipu/O	1	LED indicator 0.[2]
107	MDC	Ipu	All	Switch or PHY[5] MII management data clock.[2]
108	MDIO	Ipu/O	All	Switch or PHY[5] MII management data I/O.
109	Reserved		All	No connect.
110	SCL	I/O	All	Output clock at 81kHz in I^2C master mode.
111	SDA	I/O	All	Serial data input/output in I^2C master mode.
112	Reserved		All	No connect
113	PS1	Ipd		No connect or pull-down.
114	PS0	Ipd		No connect or pull-down.
115	RST_N	Ipu		Reset the KS8995XA. Active low.
116	GNDD	Gnd		Digital ground.
117	VDDC	P		1.8V digital core V_{DD}.
118	TESTEN	Ipd		Factory test pin.
119	SCANEN	Ipd		Factory test pin.
120	NC	NC		No connection.
121	X1	I		25MHz crystal clock connection/or 3.3V tolerant oscillator input. Oscillator should be ±100ppm.
122	X2	O		25MHz crystal clock connection.
123	VDDAP	P		1.8V analog V_{DD} for PLL.
124	GNDA	Gnd		Analog ground.
125	VDDAR	P		1.8V analog V_{DD}.
126	GNDA	Gnd		Analog ground.
127	GNDA	Gnd		Analog ground.
128	TEST2			Factory test pin.

Notes:

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   Gnd = Ground.
   Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.
   Otri = Output tristated.

Pin Description (by Name)

Pin Number	Pin Name	Type[1]	Port	Pin Function
39	FXSD4	I	4	Fiber signal detect/factory test pin.
38	FXSD5	I	5	Fiber signal detect/factory test pin.
2	GNDA	Gnd		Analog ground.
6	GNDA	Gnd		Analog ground.
12	GNDA	Gnd		Analog ground.
16	GNDA	Gnd		Analog ground.
21	GNDA	Gnd		Analog ground.
27	GNDA	Gnd		Analog ground.
30	GNDA	Gnd		Analog ground.
34	GNDA	Gnd		Analog ground.
40	GNDA	Gnd		Analog ground.
42	GNDA	Gnd		Analog ground.
44	GNDA	Gnd		Analog ground.
120	NC	NC		No connection.
124	GNDA	Gnd		Analog ground.
126	GNDA	Gnd		Analog ground.
127	GNDA	Gnd		Analog ground.
49	GNDD	Gnd		Digital ground.
58	GNDD	Gnd		Digital ground.
76	GNDD	Gnd		Digital ground.
88	GNDD	Gnd		Digital ground.
99	GNDD	Gnd		Digital ground.
116	GNDD	Gnd		Digital ground.
17	ISET			Set physical transmit output current. Pull down with a 3.01kΩ1% resistor.
106	LED1-0	Ipu/O	1	LED indicator 0.
105	LED1-1	Ipu/O	1	LED indicator 1.
104	LED1-2	Ipu/O	1	LED indicator 2.
103	LED2-0	Ipu/O	2	LED indicator 0.
102	LED2-1	Ipu/O	2	LED indicator 1.
101	LED2-2	Ipu/O	2	LED indicator 2.
98	LED3-0	Ipu/O	3	LED indicator 0.
97	LED3-1	Ipu/O	3	LED indicator 1.

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   Gnd = Ground.
   Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
96	LED3-2	Ipu/O	3	LED indicator 2.
95	LED4-0	Ipu/O	4	LED indicator 0.
94	LED4-1	Ipu/O	4	LED indicator 1.
93	LED4-2	Ipu/O	4	LED indicator 2.
92	LED5-0	Ipu/O	5	LED indicator 0.
91	LED5-1	Ipu/O	5	LED indicator 1. Strap option: PU (default): enable PHY MII I/F Pd: tristate all PHY MII output. See “Pin# 86 SCONF1.”
90	LED5-2	Ipu/O	5	LED indicator 2. Aging setup. See “Aging” section.
107	MDC	Ipu	All	Switch or PHY[5] MII management data clock.
108	MDIO	Ipu/O	All	Switch or PHY[5] MII management data I/O.
45	NC / MUX1		I	No connect. Factory test pin.
46	NC / MUX2		I	No connect. Factory test pin.
68	PCOL	Ipd/O	5	PHY[5] MII collision detect/ strap option for port 4 only. PD (default) = no force flow control, normal operation. PU = force flow control. Refer to Register 66.
67	PCRS	Ipd/O	5	PHY[5] MII carrier sense/strap option for port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto negotiation is disabled or fails. Refer to Register 76.
60	PMRXC	O	5	PHY[5] MII receive clock. PHY mode MII.
65	PMRXD0	Ipd/O	5	PHY[5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.
64	PMRXD1	Ipd/O	5	PHY[5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.
63	PMRXD2	Ipd/O	5	PHY[5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure.
62	PMRXD3	Ipd/O	5	PHY[5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control.
61	PMRXDV	Ipd/O	5	PHY[5] MII receive data valid.
66	PMRXER	Ipd/O	5	PHY[5] MII receive error. Strap option: PD (default) = packet size 1518/ 1522 bytes; PU = 1536 bytes.
57	PMTXC	O	5	PHY[5] MII transmit clock. PHY mode MII.
55	PMTXD0	Ipd	5	PHY[5] MII transmit bit 0.
54	PMTXD1	Ipd	5	PHY[5] MII transmit bit 1.
53	PMTXD2	Ipd	5	PHY[5] MII transmit bit 2.
52	PMTXD3	Ipd	5	PHY[5] MII transmit bit 3.
51	PMTXEN	Ipd	5	PHY[5] MII transmit enable.
56	PMTXER	Ipd	5	PHY[5] MII transmit error.
114	PS0	Ipd		No connect or pull down.
113	PS1	Ipd		No connect or pull down.

Notes:

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   Gnd = Ground.
   Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
47	PWRDN_N	Ipu		Full-chip power down. Active low.
48	RESERVE/NC			Reserved pin. No connect.
109	Reserved		All	No connect.
112	Reserved		All	No connect.
115	RST_N	Ipu		Reset the KS8995X. Active low.
5	RXM1	I	1	Physical receive signal - (differential).
11	RXM2	I	2	Physical receive signal - (differential).
20	RXM3	I	3	Physical receive signal - (differential).
26	RXM4	I	4	Physical receive signal - (differential).
33	RXM5	I	5	Physical receive signal - (differential).
4	RXP1	I	1	Physical receive signal + (differential).
10	RXP2	I	2	Physical receive signal + (differential).
19	RXP3	I	3	Physical receive signal + (differential).
25	RXP4	I	4	Physical receive signal + (differential).
32	RXP5	I	5	Physical receive signal + (differential).
119	SCANEN	Ipd		Factory test pin.
110	SCL	I/O	All	Output clock at 81kHz in I^2C master mode. See “Pin# 113.”
84	SCOL	Ipd/O		Switch MII collision detect.
87	SCONF0	Ipd		Dual MII configuration pin.
86	SCONF1	Ipd		Dual MII configuration pin.
85	SCRS	Ipd/O		Switch MII carrier sense.
111	SDA	I /O	All	Serial data input/output in I^2C master mode. See “Pin# 113.”
78	SMRXC	I/O		Switch MII receive clock. PHY or MAC mode MII.
83	SMRXD0	Ipd/O		Switch MII receive bit 0; strap option: see “Register 11[1].”

Pin# (91, 86, 87):	Switch MII	PHY [5] MII
000	Disable, Otri	Disable, Otri
001	PHY Mode MII	Disable, Otri
010	MAC Mode MII	Disable, Otri
011	PHY Mode SNI	Disable, Otri
100	Disable	Disable
101	PHY Mode MII	PHY Mode MII
110	MAC Mode MII	PHY Mode MII
111	PHY Mode SNI	PHY Mode MII

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   Gnd = Ground.
   Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
2. Otri = Output tristated.

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
82	SMRXD1	Ipd/O		Switch MII receive bit 1. Strap option: PD (default) = Switch MII in 100Mbps mode; PU = Switch MII in 10Mbps mode.
81	SMRXD2	Ipd/O		Switch MII receive bit 2. Strap option: PD (default) = Switch MII in full-duplex mode; PU = Switch MII in half-duplex mode.
80	SMRXD3	Ipd/O		Switch MII receive bit 3. Strap option: PD (default) = Disable Switch MII full-duplex flow control; PU = Enable Switch MII full-duplex flow control.
79	SMRXDV	Ipd/O		Switch MII receive data valid.
75	SMTXC	I/O		Switch MII transmit clock. PHY or MAC mode MII.
73	SMTXD0	Ipd		Switch MII transmit bit 0.
72	SMTXD1	Ipd		Switch MII transmit bit 1.
71	SMTXD2	Ipd		Switch MII transmit bit 2.
70	SMTXD3	Ipd		Switch MII transmit bit 3.
69	SMTXEN	Ipd		Switch MII transmit enable.
74	SMTXER	Ipd		Switch MII transmit error.
1	MDIXDIS	Ipd	1-5	Disable auto MDI/MDI-X.
128	TEST2			Factory test pin.
118	TESTEN	Ipd		Factory test pin.
7	TXP1	O	1	Physical transmit signal + (differential).
13	TXP2	O	2	Physical transmit signal + (differential).
22	TXP3	O	3	Physical transmit signal + (differential).
28	TXP4	O	4	Physical transmit signal + (differential).
35	TXP5	O	5	Physical transmit signal + (differential).
8	TXM1	O	1	Physical transmit signal – (differential).
14	TXM2	O	2	Physical transmit signal – (differential).
23	TXM3	O	3	Physical transmit signal – (differential).
29	TXM4	O	4	Physical transmit signal – (differential).
36	TXM5	O	5	Physical transmit signal – (differential).
123	VDDAP	P		1.8V analog V_{DD} for PLL.
3	VDDAR	P		1.8V analog V_{DD}.
15	VDDAR	P		1.8V analog V_{DD}.
31	VDDAR	P		1.8V analog V_{DD}.
41	VDDAR	P		1.8V analog V_{DD}.
43	VDDAR	P		1.8V analog V_{DD}.
125	VDDAR	P		1.8V analog V_{DD}.

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   Gnd = Ground.
   Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.

Pin Number	Pin Name	Type[1]	Port	Pin Function
9	VDDAT	P		2.5V or 3.3V analog V_{DD}.
18	VDDAT	P		2.5V or 3.3V analog V_{DD}.
24	VDDAT	P		2.5V or 3.3V analog V_{DD}.
37	VDDAT	P		2.5V or 3.3V analog V_{DD}.
50	VDDC	P		1.8V digital core V_{DD}.
89	VDDC	P		1.8V digital core V_{DD}.
117	VDDC	P		1.8V digital core V_{DD}.
59	VDDIO	P		3.3V digital V_{DD} for digital I/O circuitry.
77	VDDIO	P		3.3V digital V_{DD} for digital I/O circuitry.
100	VDDIO	P		3.3V digital V_{DD} for digital I/O circuitry.
121	X1	I		25MHz crystal clock connection/or 3.3V tolerant oscillator input. Oscillator should be ±100ppm.
122	X2	O		25MHz crystal clock connection.

Notes:
1. P = Power supply.
   I = Input.
   O = Output.

Introduction

The KS8995XA contains five 10/100 physical layer transceivers and five media access control (MAC) units with an integrated Layer 2 switch. The device runs in three modes. The first mode is as a five-port integrated switch. The second is as a five-port switch with the fifth port decoupled from the physical port. In this mode access to the fifth MAC is provided through a media independent interface (MII) . This is useful for implementing an integrated broadband router. The third mode uses the dual MII feature to recover the use of the fifth PHY. This allows the additional broadband gateway configuration, where the fifth PHY may be accessed through the MII-P5 port.

The KS8995XA is optimized for an unmanaged design in which the configuration is achieved through I/O strapping or EEPROM programming at system reset time.

On the media side, the KS8995XA supports IEEE 802.3 10BASE-T, 100BASE-TX on all ports, and 100BASE-FX on ports 4 and 5. The KS8995XA can be used as two separate media converters.

Physical signal transmission and reception are enhanced through the use of patented analog circuitry that makes the design more efficient and allows for lower power consumption and smaller chip die size.

The major enhancements from the KS8995E to the KS8995XA are support for programmable rate limiting, a dual MII interface, MDC/MDIO control interface for IEEE 802.3-defined register configuration (not all the registers), per-port broadcast storm protection, local loopback and lower power consumption.

The KS8995XA is pin-compatible to the managed switch, the KS8995M.

Functional Overview: Physical Layer Transceiver

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ to NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 3.01kΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then it tunes itself for optimization. This is an ongoing process and can self-adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

PLL Clock Synthesizer

The KS8995XA generates 125MHz, 42MHz, 25MHz, and 10MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal.

Scrambler/De-Scrambler (100BASE-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline

wander. The data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit nonrepetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

100BASE-FX Operation

100BASE-FX operation is very similar to 100BASE-TX operation except that the scrambler/de-scrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In this mode the auto-negotiation feature is bypassed since there is no standard that supports fiber auto-negotiation.

100BASE-FX Signal Detection

The physical port runs in 100BASE-FX mode if FXSDx >0.6V for ports 4 and 5 only. This signal is internally referenced to 1.25V.The fiber module interface should be set by a voltage divider such that FXSDx 'H' is above this 1.25V reference, indicating signal detect, and FXSDx 'L' is below the 1.25V reference to indicate no signal. When FXSDx is below 0.6V then 100BASE-FX mode is disabled.

100BASE-FX Far End Fault

Far end fault occurs when the signal detection is logically false from the receive fiber module. When this occurs, the transmission side signals the other end of the link by sending 84 1's followed by a zero in the idle period between frames. The far end fault may be disabled through register settings.

10BASE-T Transmit

The output 10BASE-T driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental when driven by an all-ones Manchester-encoded signal.

10BASE-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulsewidths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KS8995XA decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

Power Management

The KS8995XA features a per port power down mode. To save power the user can power down ports that are not in use by setting port control registers or MII control registers. In addition, it also supports full chip power down mode. When activated, the entire chip will be shutdown.

MDI/MDI-X Auto Crossover

The KS8995XA supports MDI/MDI-X auto crossover. This facilitates the use of either a straight connection CAT-5 cable or a crossover CAT-5 cable. The auto-sense function will detect remote transmit and receive pairs, and correctly assign the transmit and receive pairs from the Micrel device. This can be highly useful when end users are unaware of cable types and can also save on an additional uplink configuration connection. The auto crossover feature may be disabled through the port control registers.

Auto-Negotiation

The KS8995XA conforms to the auto-negotiation protocol as described by the 802.3 committee. Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto-negotiation the link partners advertise capabilities across the link to each other. If auto-negotiation is not supported or the link partner to the KS8995XA is forced to bypass auto-negotiation, then the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto-negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The flow for the link set up is depicted in Figure 4.

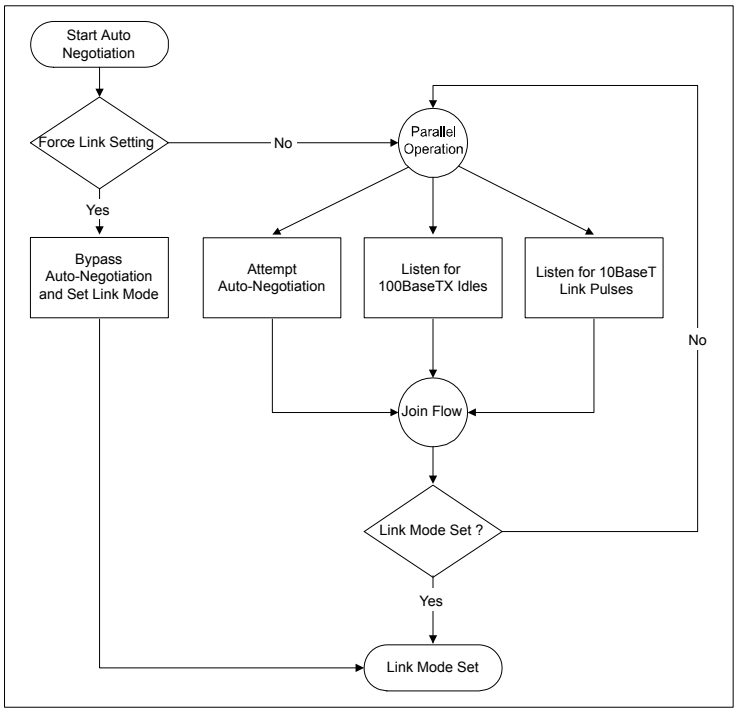


Figure 4. Auto-Negotiation

Functional Overview: Switch Core

Address Look-Up

The internal look-up table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information. The KS8995XA is guaranteed to learn 1K addresses and distinguishes itself from hash-based look-up tables which, depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

Learning

The internal look-up engine will update its table with a new entry if the following conditions are met:

- The received packet's source address (SA) does not exist in the look-up table.
- The received packet is good; the packet has no receiving errors, and is of legal length.

The look-up engine will insert the qualified SA into the table, along with the port number, time stamp. If the table is full, the last entry of the table will be deleted first to make room for the new entry.

Migration

The internal look-up engine also monitors whether a station is moved. If it happens, it will update the table accordingly.

Migration happens when the following conditions are met:

- The received packet's SA is in the table but the associated source port information is different.
- The received packet is good; the packet has no receiving errors, and is of legal length.

The look-up engine will update the existing record in the table with the new source port information.

Aging

The look-up engine will update the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look-up engine will remove the record from the table. The look-up engine constantly performs the aging process and will continuously remove aging records. The aging period is 300 ±75 seconds. This feature can be enabled or disabled through register 3 or by external pull-up or pull-down resistors on LED[5][2]. See "Register 3" section.

Switching Engine

The KS8995XA features a high performance switching engine to move data to and from the MAC's packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The KS8995XA has a 64kB internal frame buffer. This resource is shared between all five ports. The buffer sharing mode can be programmed through Register 2. See "Register 2." In one mode, ports are allowed to use any free buffers in the buffer pool.

In the second mode, each port is only allowed to use 1/5 of the total buffer pool. There are a total of 512 buffers available. Each buffer is sized at 128B.

Media Access Controller (MAC) Operation

The KS8995XA strictly abides by IEEE 802.3 standards to maximize compatibility.

Inter-Packet Gap (IPG)

If a frame is successfully transmitted, the 96-bit time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96-bit time IPG is measured from MCRS and the next MTXEN.

Backoff Algorithm

The KS8995XA implements the IEEE Std. 802.3 binary exponential back-off algorithm, and optional "aggressive mode" back off. After 16 collisions, the packet will be optionally dropped depending on the chip configuration in Register 3. See "Register 3."

Late Collision

If a transmit packet experiences collisions after 512-bit times of the transmission, the packet will be dropped.

Illegal Frames

The KS8995XA discards frames less than 64 bytes and can be programmed to accept frames up to 1536 bytes in Register 4. For special applications, the KS8995XA can also be programmed to accept frames up to 1916 bytes in Register 4. Since the KS8995XA supports VLAN tags, the maximum sizing is adjusted when these tags are present.

Flow Control

The KS8995XA supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KS8995XA receives a pause control frame, the KS8995XA will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (being flow controlled), only flow control packets from the KS8995XA will be transmitted.

On the transmit side, the KS8995XA has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The KS8995XA will flow control a port, which just received a packet, if the destination port resource is being used up. The KS8995XA will issue a flow control frame (XOFF), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KS8995XA will send out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being activated and deactivated too many times.

The KS8995XA will flow control all ports if the receive queue becomes full.

Half-Duplex Back Pressure

A half-duplex back pressure option (note: not in 802.3 standards) is also provided. The activation and deactivation conditions are the same as the above in full-duplex mode. If back pressure is required, the KS8995XA will send preambles to defer the other stations' transmission (carrier sense deference). To avoid jabber and excessive deference defined in 802.3 standard, after a certain time it will discontinue the carrier sense but it will raise the carrier sense quickly. This short silent time (no carrier sense) is to prevent other stations from sending out packets and keeps other stations in carrier sense deferred state. If the port has packets to send during a back pressure situation, the carrier-sense-type back pressure will be interrupted and those packets will be transmitted instead. If there are no

more packets to send, carrier-sense-type back pressure will be active again until switch resources are free. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, reducing the chance of further colliding and maintaining carrier sense to prevent reception of packets.

To ensure no packet loss in 10BASE-T or 100BASE-TX half-duplex modes, the user must enable the following:

- Aggressive backoff (register 3, bit 0)
- No excessive collision drop (register 4, bit 3)
- Back pressure (register 4, bit 5)

These bits are not set as the default because this is not the IEEE standard.

Broadcast Storm Protection

The KS8995XA has an intelligent option to protect the switch system from receiving too many broadcast packets. Broadcast packets will be forwarded to all ports except the source port, and thus use too many switch resources (bandwidth and available space in transmit queues). The KS8995XA has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally, and can be enabled or disabled on a per port basis. The rate is based on a 50ms interval for 100BT and a 500ms interval for 10BT. At the beginning of each interval, the counter is cleared to zero, and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in Register 6 and Register 7. The default setting for registers 6 and 7 is 0x4A, which is 74 decimal. This is equal to a rate of 1%, calculated as follows:

148,800 frames/sec × 50ms/interval × 1% = 74 frames/interval (approx.) = 0x4

MII Interface Operation

The media independent interface (MII) is specified by the IEEE 802.3 committee and provides a common interface between physical layer and MAC layer devices. The KS8995XA provides two such interfaces. The MII-P5 interface is used to connect to the fifth PHY, whereas the MII-SW interface is used to connect to the fifth MAC. Each of these MII interfaces contains two distinct groups of signals, one for transmission and the other for receiving. The table below describes the signals used in the MII-P5 interface.

The MII-P5 interface operates in PHY mode only, while the MII-SW interface operates in either MAC mode or PHY mode. These interfaces are nibble-wide data interfaces and therefore run at 1/4 the network bit rate (not encoded). Additional signals on the transmit side indicate when data is valid or when an error occurs during transmission. Likewise, the receive side has indicators that convey when the data is valid and without physical layer errors. For half-duplex operation, there is a signal that indicates a collision has occurred during transmission.

Note that the signal MRXER is not provided on the MII-SW interface for PHY mode operation and the signal MTXER is not provided on the MII-SW interface for MAC mode operation. Normally MRXER would indicate a receive error coming from the physical layer device. MTXER would indicate a transmit error from the MAC device. These signals are not appropriate for this configuration. For PHY mode operation, if the device interfacing with the KS8995XA has an MRXER pin, it should be tied low. For MAC mode operation, if the device interfacing with the KS8995XA has an MTXER pin, it should be tied low.

MII Signal	Description	KS8995XA Signal
MTXEN	Transmit enable	PMTXEN
MTXER	Transmit error	PMTXER
MTXD3	Transmit data bit 3	PMTXD[3]
MTXD2	Transmit data bit 2	PMTXD[2]
MTXD1	Transmit data bit 1	PMTXD[1]
MTXD0	Transmit data bit 0	PMTXD[0]
MTXC	Transmit clock	PMTXC
MCOL	Collision detection	PCOL
MCRS	Carrier sense	PCRS
MRXDV	Receive data valid	PMRXDV
MRXER	Receive error	PMRXER
MRXD3	Receive data bit 3	PMRXD[3]
MRXD2	Receive data bit 2	PMRXD[2]
MRXD1	Receive data bit 1	PMRXD[1]
MRXD0	Receive data bit 0	PMRXD[0]
MRXC	Receive clock	PMRXC
MDC	Management data clock	MDC
MDIO	Management data I/O	MDIO

Table 1. MII – P5 Signals (PHY Mode)

PHY Mode Connection			MAC Mode Connection	
External MAC	KS8995XA Signal	Description	External PHY	KS8995XA Signal
MTXEN	SMTXEN	Transmit enable	MTXEN	SMRXDV
MTXER	SMTXER	Transmit error	MTXER	Not used
MTXD3	SMTXD[3]	Transmit data bit 3	MTXD3	SMRXD[3]
MTXD2	SMTXD[2]	Transmit data bit 2	MTXD2	SMRXD[2]
MTXD1	SMTXD[1]	Transmit data bit 1	MTXD1	SMRXD[1]
MTXD0	SMTXD[0]	Transmit data bit 0	MTXD0	SMRXD[0]
MTXC	SMTXC	Transmit clock	MTXC	SMRXC
MCOL	SCOL	Collision detection	MCOL	SCOL
MCRS	SCRS	Carrier sense	MCRS	SCRS
MRXDV	SMRXDV	Receive data valid	MRXDV	SMTXEN
MRXER	Not used	Receive error	MRXER	SMTXER
MRXD3	SMRXD[3]	Receive data bit 3	MRXD3	SMTXD[3]
MRXD2	SMRXD[2]	Receive data bit 2	MRXD2	SMTXD[2]
MRXD1	SMRXD[1]	Receive data bit 1	MRXD1	SMTXD[1]
MRXD0	SMRXD[0]	Receive data bit 0	MRXD0	SMTXD[0]
MRXC	SMRXC	Receive clock	MRXC	SMTXC

Table 2. MII – SW Signals

SNI Interface Operation

The serial network interface (SNI) is compatible with some controllers used for network layer protocol processing. This interface can be directly connected to these types of devices. The signals are divided into two groups, one for transmission and the other for reception. The signals involved are described in the table below.

SNI Signal	Description	KS8995XA Signal
TXEN	Transmit Enable	SMTXEN
TXD	Serial Transmit Data	SMTXD[0]
TXC	Transmit Clock	SMTXC
COL	Collision Detection	SCOL
CRS	Carrier Sense	SMRXDV
RXD	Serial Receive Data	SMRXD[0]
RXC	Receive Clock	SMRXC

Table 3. SNI Signals

This interface is a bit-wide data interface and therefore runs at the network bit rate (not encoded). An additional signal on the transmit side indicates when data is valid. Likewise, the receive side has an indicator that conveys when the data is valid.

For half-duplex operation there is a signal that indicates a collision has occurred during transmission.

Advanced Functionality

QoS Support

The KS8995XA is a QoS switch, meaning that is it able to identify selected packets on its ingress ports, prioritize them, and service the packets according to their priority on the egress ports. In this way, the KS8995XA can provide statistically better service to the high priority packets that are latency sensitive, or require higher bandwidth. The KS8995XA supports ingress QoS classification using three different mechanisms: port-based priority, 802.1p tag-based priority, and DSCP priority for IPv4 packets.

Port-based priority is useful when the user wants to give a device on a given port high priority. For example in Figure 7, port 1 is given high priority because it is connected to an IP phone and port 4 is given lower priority because it is connected to a computer whose data traffic may be less sensitive to network congestion. Each port on the KS8995XA can be set as high or low priority with an EEPROM. The port priority is set in bit 4 of registers 0x10, 0x20, 0x30, 0x40, 0x50 for ports 1, 2, 3, 4 and 5, respectively. Port-based priority is overridden by the OR'ed result of the 802.1p and DSCP priorities if they are all enabled at the same time.

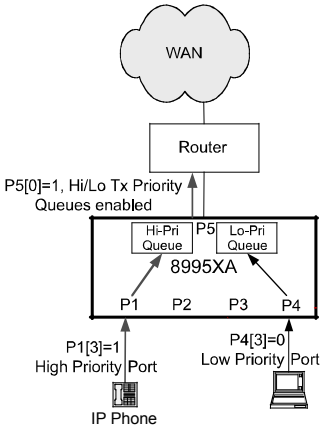


Figure 7. Port-Based Priority

The KS8995XA can classify tagged packets using the 802.1p tag-based priority. In this prioritization scheme, the user can enable the 802.1p classification on a per port basis in bit 5 of registers 0x10, 0x20, 0x30, 0x40 and 0x50 for ports 1, 2, 3, 4, and 5, respectively. Then the user specifies the 802.1p base priority in register 0x02, bits [6-4]. When a tagged packet is received, the KS8995XA examines the 3 bit 802.1p priority field shown in Figure 6. These 3 bits are compared against the base priority. The prioritization policy is as follows:

Comparison	Priority
802.1p Priority ≥Base Priority	High
802.1p Priority < Base Priority	Low

Table 4. 802.1p Priority

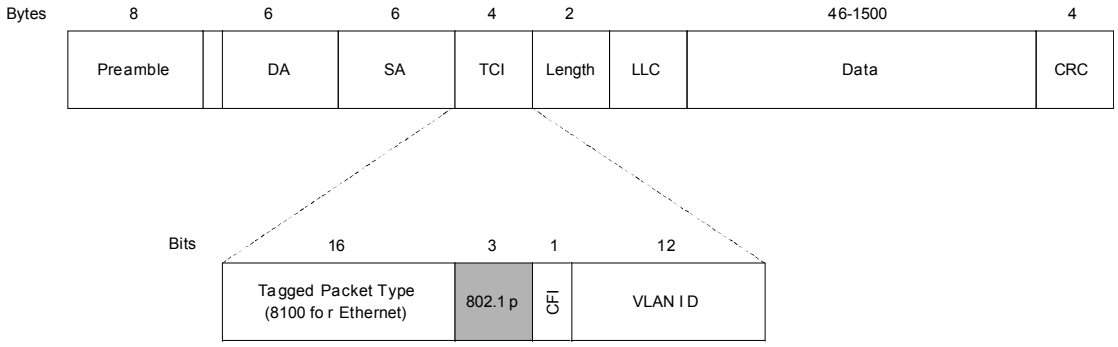


Figure 6. 802.3 Tagged Packet

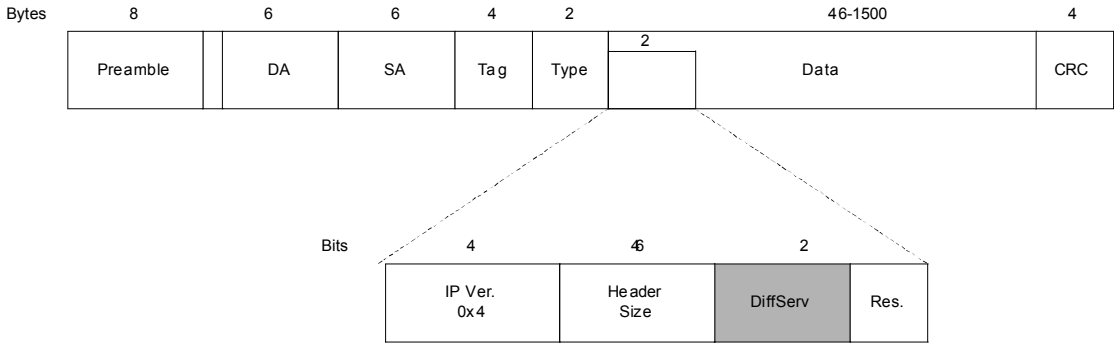


Figure 7. IPv4 Packet

In order to support QoS from end-to-end in a network, the KS8995XA can also classify packets based on the IPv4 DiffServ field shown in Figure 7.

The DiffServ field consists of 6 bits, which can be used to specify 64 code points. The KS8995XA provides 64 bits (DSCP[63:0]) in 8 registers (0x60 to 0x67), in which the user specifies the priority of each of the 64 code points. The DiffServ classification is enabled on a per port basis in bit 6 of registers 0x10, 0x20, 0x30, 0x40 and 0x50 for ports 1, 2, 3, 4, and 5, respectively. If the DiffServ classification is enabled on a port, the KS8995XA will decode the IPv4 DiffServ field and look at the user defined code point bit to determine if the packet is high priority or low priority. If the code point is a '1', the packet is high priority. If the code point is '0', the packet is low priority.

DiffServ Field (Binary)	Code Point	KS8995X (Reg. and Bit)
000000	DSCP[0]	0x67, bit 0
000001	DSCP[1]	0x67, bit 1
000010	DSCP[2]	0x67, bit 2
000011	DSCP[3]	0x67, bit 3
000100	DSCP[4]	0x67, bit 4
• • •	• • •	• • •
111011	DSCP[59]	0x60, bit 3
111100	DSCP[60]	0x60, bit 4
111101	DSCP[61]	0x60, bit 5
111110	DSCP[62]	0x60, bit 6
111111	DSCP[63]	0x60, bit 7

Table 5. DiffServ Code Point

Once classification of the packets has been determined either by port-based priority, 802.1p tag-based priority or DiffServ priority, they are placed in either the high or low priority queue on the egress port. The user can enable the egress priority queues on a per port basis by setting bit 0 of registers 0x10, 0x20, 0x30, 0x40, and 0x50 for ports 1, 2, 3, 4 and 5, respectively. If the egress priority queue for a given port is not set, the port will treat all packets as if they are the same priority, even though packets are classified on their ingress ports. If the egress priority queue for a given port is enabled, packets are serviced based on the user programmable egress policy. The priority scheme selection is set in register 0x05 bits[3-2] as shown in Table 6.

Register 0x05, bit 3	Register 0x05, bit 2	Egress Priority Scheme
0	0	Always deliver high priority packets first
0	1	Deliver high/low priority packets at a ratio of 10/1
1	0	Deliver high/low priority packets at a ratio of 5/1
1	1	Deliver high/low priority packets at a ratio of 2/1

Table 6. Transmit Priority Ratio

The KS8995XA offers support for port-based, 802.1p tag-based, and IPv4 DiffServ priority, as well as programmable egress policies. These KS8995XA QoS features enable identifying, classifying and forwarding packets based on their priority. The system designer is able to use this device to build network elements that give more control over system resources, priority service to mission critical applications, and can be integrated into the next generation of multimedia networks.

Rate Limit Support

KS8995XA supports hardware rate limiting on “receive” and “transmit” independently on a per port basis. It also supports rate limiting in a priority or non-priority environment. The rate limit starts from 0Kbps and goes up to the line rate in steps of 32Kbps. The KS8995XA uses one second as an interval. At the beginning of each interval, the counter is cleared to zero, and the rate limit mechanism starts to count the number of bytes during this interval.

For receive, if the number of bytes exceeds the programmed limit, the switch will stop receiving packets on the port until the “one second” interval expires. There is an option provided for flow control to prevent packet loss. If the rate limit is programmed greater than or equal to 128Kbps and the byte counter is 8K bytes below the limit, the flow control will be triggered. If the rate limit is programmed lower than 128Kbps and the byte counter is 2K bytes below the limit, the flow control will be triggered.

For transmit, if the number of bytes exceeds the programmed limit, the switch will stop transmitting packets on the port until the “one second” interval expires.

If priority is enabled, the KS8995XA can support different rate controls for both high priority and low priority packets. This can be programmed through Registers 21 – 27.

Configuration Interface

The KS8995XA functions as an unmanaged switch. If no EEPROM exists, the KS8995XA will operate from its default and strap-in settings.

I^2C Master Serial Bus Configuration

If a 2-wire EEPROM exists, the KS8995XA can perform more advanced features like broadcast storm protection and rate control. The EEPROM should have the entire valid configuration data from register 0 to register 109 defined in the memory map, except the status registers. The configuration access time (t_{prgm}) is less than 15ms as shown in Figure 8.

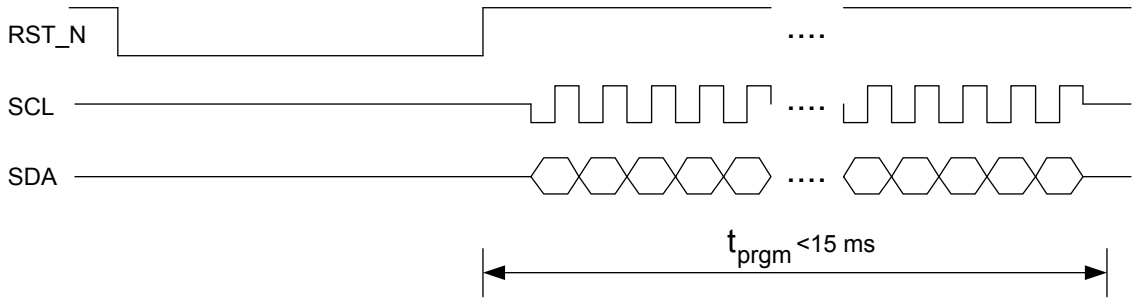


Figure 8. EEPROM Configuration Timing Diagram

To configure the KS8995XA with a pre-configured EEPROM use the following steps:

- At the board level, connect pin 110 on the KS8995XA to the SCL pin on the EEPROM. Connect pin 111 on the KS8995XA to the SDA pin on the EEPROM.
- Be sure the board-level reset signal is connected to the KS8995XA reset signal on pin 115 (RST_N).
- Program the contents of the EEPROM before placing it on the board with the desired configuration data. Note that the first byte in the EEPROM must be “95” for the loading to occur properly. If this value is not correct, all other data will be ignored.
- Place EEPROM on the board and power up the board. Assert the active-low board level reset to RST_N on the KS8995XA. After the reset is de-asserted, the KS8995XA will begin reading configuration data from the EEPROM. The configuration access time (tprgm) is less than 15ms.

Note: For proper operation, make sure pin 47 (PWRDN_N) is not asserted during the reset operation.

MII Management Interface (MIIM)

A standard MIIM interface is provided for all five PHY devices in the KS8995XA. An external device with MDC/MDIO capability is able to read PHY status or to configure PHY settings. For details on the MIIM interface standard, please reference the IEEE 802.3 specification (section 22.2.4.5). The MIIM interface does not have access to all the configuration registers in the KS8995XA. It can only access the standard MII registers. See “MIIM Registers” section.

Register Map

Offset		
Decimal	**Hex**	**Description**
0-1	0x00-0x01	Chip ID Registers
2-11	0x02-0x0B	Global Control Registers
12-15	0x0C-0x0F	Reserved
16-29	0x10-0x1D	Port 1 Control Registers
30-31	0x1E-0x2F	Port 1 Status Registers
32-45	0x20-0x2D	Port 2 Control Registers
46-47	0x2E-0x2F	Port 2 Status Registers
48-61	0x30-0x3D	Port 3 Control Registers
62-63	0x3E-0x3F	Port 3 Status Registers
64-77	0x40-0x4D	Port 4 Control Registers
78-79	0x4E-0x4F	Port 4 Status Registers
80-93	0x50-0x5D	Port 5 Control Registers
94-95	0x5E-0x5F	Port 5 Status Registers
96-103	0x60-0x67	TOS Priority Control Registers
104-109	0x68-0x6D	MAC Address Registers

Global Registers

Address	Name	Description	Mode	Default
Register 0 (0x00): Chip ID0				
7-0	Family ID	Chip family	RO	0x95
Register 1 (0x01): Chip ID1/Start Switch				
7-4	Chip ID	0x0 is assigned to 95 series. (95XA)	RO	0x0
3-1	Revision ID	Revision ID	RO	Based on real chip revision, 0x02=B2, 0x03=B3, 0x04=B4, 0x05=B5, etc.
0	Start switch	The chip starts automatically after trying to read the external EEPROM. If EEPROM does not exist, the chip will use default values for all internal registers. If EEPROM is present, the contents in the EEPROM will be checked. The switch will check: (1) Register 0 = 0x95, (2) Register 1 [7:4] = 0x0. If this check is OK, the contents in the EEPROM will override chip register default values.	RW	0x0
Register 2 (0x02): Global Control 0				
7	Reserved	Reserved	R/W	0x0
6-4	802.1p base priority	Used to classify priority for incoming 802.1q packets. “User priority” is compared against this value ≥: classified as high priority < : classified as low priority	R/W	0x4

Address	Name	Description	Mode	Default
3	Enable PHY MII	1, enable PHY MII interface (note: if not enabled, the switch will tri-state all outputs.)	R/W	Pin LED[5][1] strap option. Pull-down (0): isolate. Pull-up (1): Enable. *Note: LED[5][1] has internal pull-up.*
2	Buffer share mode	1, buffer pool is shared by all ports. A port can use more buffer when other ports are not busy. 0, a port is only allowed to use 1/5 of the buffer pool.	R/W	0x1
1	UNH mode	1, the switch will drop packets with 0x8808 in T/L filed, or DA=01-80-C2-00-00-01. 0, the switch will drop packets qualified as “flow control” packets.	R/W	0
0	Link change age	1, link change from “link” to “no link” will cause fast aging (<800µs) to age address table faster. After an age cycle is complete, the age logic will return to normal (300 ±75 seconds). *Note: If any port is unplugged, all addresses will be automatically aged out.*	R/W	0
Register 3 (0x03): Global Control 1				
7	Pass all frames	1, switch all packets including bad ones. Used solely for debugging purpose. Works in conjunction with sniffer mode.	R/W	0
6	Reserved	Reserved	R/W	0
5	IEEE 802.3x transmit flow control disable	0, will enable transmit flow control based on AN result 1, will not enable transmit flow control regardless of AN result.	R/W	Pin PMRXD3 strap option. Pull-down (0): Enable TX flow control. Pull-up (1): Disable TX/RX flow control. *Note: PMRXD3 has internal pull-down.*
4	IEEE 802.3x receive flow control disable	0, will enable receive flow control based on AN result 1, will not enable receive flow control regardless of AN result. *Note: Bit 5 and bit 4 default values are controlled by the same pin, but they can be programmed independently.*	R/W	Pin PMRXD3 strap option. Pull-down (0): Enable RX flow control. Pull-up (1): Disable TX/RX flow control. *Note: PMRXD3 has internal pull-down.*
3	Frame length field check	1, will check frame length field in the IEEE packets. If the actual length does not match, the packet will be dropped. (for L/T < 1500)	R/W	0
2	Aging enable	1, Enable age function in the chip 0, Disable aging function	R/W	Pin LED[5][2] strap option. Pull-down (0): Aging disable. Pull-up (1): Aging Enable. *Note: LED[5][2] has internal pull-up.*
1	Fast age enable	1, turn on fast age (800µs)	R/W	0

Address	Name	Description	Mode	Default
0	Aggressive back off enable	1, enable more aggressive back off algorithm in half duplex mode to enhance performance. This is not an IEEE standard.	R/W	Pin PMRXD0 strap option. Pull-down (0): Disable aggressive back off. Pull-up (1): Aggressive backoff. *Note: PMRXD0 has internal pull-down.*
Register 4 (0x04): Global Control 2				
7	Reserved	Reserved	R/W	1
6	Multicast storm protection disable	1, "Broadcast Storm Protection" does not include multicast packets. Only DA=FFFFFFFFFFFF packets will be regulated. 0, "Broadcast Storm Protection" includes DA = FFFFFFFFFFFF and DA[40] = 1 packets.	R/W	1
5	Reserved	Reserved	R/W	1
4	Flow control and back pressure fair mode	1, fair mode is selected. In this mode, if a flow control port and a non-flow control port talk to the same destination port, packets from the non-flow control port may be dropped. This is to prevent the flow control port from being flow controlled for an extended period of time. 0, in this mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port will be flow controlled. This may not be "fair" to the flow control port.	R/W	1
3	No excessive collision drop	1, the switch will not drop packets when 16 or more collisions occur. 0, the switch will drop packets when 16 or more collisions occur.	R/W	Pin PMRXD1 strap option. Pull-down (0): Drop excessive collision packets. Pull-up (1): Don't drop excessive collision packets. *Note: PMRXD1 has internal pull-down.*
2	Huge packet support	1, will accept packet sizes up to 1916 bytes (inclusive). This bit setting will override setting from bit 1 of the same register. 0, the max packet size will be determined by bit 1 of this register.	R/W	0
1	Legal maximum packet size check disable	1, will accept packet sizes up to 1536 bytes (inclusive). 0, 1522 bytes for tagged packets (not including packets with STPID from CPU to ports 1-4), 1518 bytes for untagged packets. Any packets larger than the specified value will be dropped.	R/W	Pin PMRXER strap option. Pull-down (0): 1518/1522 byte packets. Pull-up value will be dropped. (1): 1536 byte packets *Note: PMRXER has internal pull-down.*

Address	Name	Description	Mode	Default
0	Priority buffer reserve	1, each output queue is pre-allocated 48 buffers, used exclusively for high priority packets. It is recommended to enable this when priority queue feature is turned on. 0, no reserved buffers for high priority packets.	R/W	0
Register 5 (0x05): Global Control 3				
7	Reserved	Reserved	R/W	0
6	Reserved	Reserved	R/W	0
5	Reserved	Reserved	R/W	0
4	Reserved	Reserved	R/W	0
3-2	Priority scheme select	00 = always deliver high priority packets first. 01 = deliver high/low packets at ratio 10/1. 10 = deliver high/low packets at ratio 5/1. 11 = deliver high/low packets at ratio 2/1.	R/W	00
1	Reserved	Reserved	R/W	0
0	Sniff mode select	1, will do Rx AND Tx sniff (both source port and destination port need to match). 0, will do Rx OR Tx sniff (either source port or destination port needs to match). This is the mode used to implement Rx only sniff.	R/W	0
Register 6 (0x06): Global Control 4				
7	Switch MII back pressure enable	1, enable half-duplex back pressure on switch MII interface. 0, disable back pressure on switch MII interface.	R/W	0
6	Switch MII half duplex mode	1, enable MII interface half-duplex mode. 0, enable MII interface full-duplex mode.	R/W	Pin SMRXD2 strap option. Pull-down (0): Full-duplex mode. Pull-up (1): Half duplex mode. *Note: SMRXD2 has internal pull down.*
5	Switch MII flow control enable	1, enable full-duplex flow control on switch MII interface. 0, disable full-duplex flow control on switch MII interface.	R/W	Pin SMRXD3 strap option. Pull-down (0): disable flow control. Pull-up (1): enable flow control *Note: SMRXD3 has internal pull-down.*
4	Switch MII 10BT	1, the switch interface is in 10Mbps mode. 0, the switch interface is in 100Mbps mode.	R/W	Pin SMRXD1 strap option. Pull-down (0): Enable 100Mbps Pull-up (1): Enable 10Mpbs. *Note: SMRXD1 has internal pull-down.*
3	Null VID replacement	1, will replace null VID with port VID (12 bits). 0, no replacement for null VID.	R/W	0
2-0	Broadcast storm protection rate bit [10:8]	This along with the next register determines how many “64 byte blocks” of packet data allowed on an input port in a preset period. The period is 50ms for 100BT or 500ms for 10BT. The default is 1%.	R/W	000

Address	Name	Description	Mode	Default
Register 7 (0x07): Global Control 5				
7-0	Broadcast storm protection rate bit [7:0]	This along with the previous register determines how many “64 byte blocks” of packet data are allowed on an input port in a preset period. The period is 50ms for 100BT or 500ms for 10BT. The default is 1%.	R/W	0x4A(1)
Register 8 (0x08): Global Control 6				
7-0	Factory testing	Reserved	R/W	0x24
Register 9 (0x09): Global Control 7				
7-0	Factory testing	Reserved	R/W	0x28
Register 10 (0x0A): Global Control 8				
7-0	Factory testing	Reserved	R/W	0x24
Register 11 (0x0B): Global Control 9				
7-4	Reserved	N/A	0	
3	PHY power save	1, disable PHY power save mode. 0, enable PHY power save mode.	R/W	0
2	Factory setting	Reserved	R/W	0
1	LED mode	0, led mode 0 1, led mode 1 Mode 0, link up at 100/Full LEDx[2,1,0]=0,0,0 100/Half LEDx[2,1,0]=0,1,0 10/Full LEDx[2,1,0]=0,0,1 10/Half LEDx[2,1,0]=0,1,1 Mode 1, link up at 100/Full LEDx[2,1,0]=0,1,0 100/Half LEDx[2,1,0]=0,1,1 10/Full LEDx[2,1,0]=1,0,0 10/Half LEDx[2,1,0]=1,0,1 (0=LED on, 1=LED off)	R/W	Pin SMRXD0 strap option. Pull-down(0): Enabled led mode 0. Pull-up(1): Enabled. Led mode 1. Note: SMRXDO has internal pull-down 0.
		Mode 0 / **Mode 1**		
		LEDX_2: Lnk/Act / 100Lnk/Act		
		LEDX_1: Fulld/Col / 10Lnk/Act		
		LEDX_0: Speed / Fulld		
0	Reserved	Reserved	R/W	0

Note:

1. 148,800 frames/sec × 50ms/interval × 1% = 74 frames/interval (approx.) = 0x4A.

Port Registers

The following registers are used to enable features that are assigned on a per port basis. The register bit assignments are the same for all ports, but the address for each port is different, as indicated.

Register 16 (0x10): Port 1 Control 0
Register 32 (0x20): Port 2 Control 0
Register 48 (0x30): Port 3 Control 0
Register 64 (0x40): Port 4 Control 0
Register 80 (0x50): Port 5 Control 0

Address	Name	Description	Mode	Default
7	Broadcast storm protection enable	1, enable broadcast storm protection for ingress packets on the port. 0, disable broadcast storm protection.	R/W	0
6	DiffServ priority classification enable	1, enable DiffServ priority classification for ingress packets on port. 0, disable DiffServ function.	R/W	0
5	802.1p priority classification enable	1, enable 802.1p priority classification for ingress packets on port. 0, disable 802.1p.	R/W	0
4	Port-based priority classification enable	1, ingress packets on the port will be classified as high priority if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 0, ingress packets on port will be classified as low priority if “DiffServ” or “802.1p” classification is not enabled or fails to classify. *Note: “DiffServ”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.*	R/W	0
3	Reserved	Reserved	R/W	0
2	Tag insertion	1, when packets are output on the port, the switch will add 802.1q tags to packets without 802.1q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID.” 0, disable tag insertion.	R/W	0
1	Tag removal	1, when packets are output on the port, the switch will remove 802.1q tags from packets with 802.1q tags when received. The switch will not modify packets received without tags. 0, disable tag removal.	R/W	0
0	Priority enable	1, the port output queue is split into high and low priority queues. 0, single output queue on the port. There is no priority differentiation even though packets are classified into high or low priority.	R/W	0

Register 17 (0x11): Port 1 Control 1
Register 33 (0x21): Port 2 Control 1
Register 49 (0x31): Port 3 Control 1
Register 65 (0x41): Port 4 Control 1
Register 81 (0x51): Port 5 Control 1

Address	Name	Description	Mode	Default
7	Sniffer port	1, port is designated as sniffer port and will transmit packets that are monitored. 0, port is a normal port.	R/W	0
6	Receive sniff	1, all the packets received on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port.” 0, no receive monitoring.	R/W	0
5	Transmit sniff	1, all the packets transmitted on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port.” 0, no transmit monitoring.	R/W	0
4-0	Port VLAN membership	Define the port’s Port VLAN membership. Bit 4 stands for port 5, bit 3 for port 4...bit 0 for port 1. The port can only communicate within the membership. A ‘1’ includes a port in the membership, a ‘0’ excludes a port from membership.	R/W	0x1f

Register 18 (0x12): Port 1 Control 2
Register 34 (0x22): Port 2 Control 2
Register 50 (0x32): Port 3 Control 2
Register 66 (0x42): Port 4 Control 2
Register 82 (0x52): Port 5 Control 2

Address	Name	Description	Mode	Default
7	Reserved	Reserved		0x0
6	Reserved	Reserved	R/W	0
5	Discard non-PVID packets	1, the switch will discard packets whose VID does not match ingress port default VID. 0, no packets will be discarded.	R/W	0
4	Force flow control	1, will always enable Rx and Tx flow control on the port, regardless of AN result. 0, the flow control is enabled based on AN result. *Note: Setting a port for both half-duplex and forced flow control is an illegal configuration. For half-duplex enable back pressure.*	R/W	0 For port 4 only, there is a special configuration pin to set the default, Pin PCOL strap option. Pull-down (0): No force flow control. Pull-up (1): Force flow control. *Note: PCOL has internal pull-down*.
3	Back pressure enable	1, enable port half-duplex back pressure. 0, disable port half-duplex back pressure.	R/W	Pin PMRXD2 strap option. Pull-down (0): disable back pressure. Pull-up(1): enable back pressure. *Note: PMRXD2 has internal pull-down.*
2	Transmit enable	1, enable packet transmission on the port. 0, disable packet transmission on the port.	R/W	1
1	Receive enable	1, enable packet reception on the port. 0, disable packet reception on the port.	R/W	1

Address	Name	Description	Mode	Default
0	Learning disable	1, disable switch address learning capability. 0, enable switch address learning.	R/W	0

Register 19 (0x13): Port 1 Control 3
Register 35 (0x23): Port 2 Control 3
Register 51 (0x33): Port 3 Control 3
Register 67 (0x43): Port 4 Control 3
Register 83 (0x53): Port 5 Control 3

Address	Name	Description	Mode	Default
7-0	Default tag [15:8]	Port's default tag, containing: 7-5: user priority bits 4: CFI bit 3-0 : VID[11:8]	R/W	0

Register 20 (0x14): Port 1 Control 4
Register 36 (0x24): Port 2 Control 4
Register 52 (0x34): Port 3 Control 4
Register 68 (0x44): Port 4 Control 4
Register 84 (0x54): Port 5 Control 4

Address	Name	Description	Mode	Default
7-0	Default tag [7:0]	Default port 1's tag, containing: 7-0: VID[7:0]	R/W	1

Note:

Registers 19 and 20 (and those corresponding to other ports) serve two purposes: (1) Associated with the ingress untagged packets, and used for egress tagging; (2) Default VID for the ingress untagged or null-VID-tagged packets, and used for address look up.

Register 21 (0x15): Port 1 Control 5
Register 37 (0x25): Port 2 Control 5
Register 53 (0x35): Port 3 Control 5
Register 69 (0x45): Port 4 Control 5
Register 85 (0x55): Port 5 Control 5

Address	Name	Description	Mode	Default
7-0	Transmit high priority rate control [7:0]	This along with port control 7, bits [3:0] form a 12-bit field to determine how many "32Kbps" high priority blocks can be transmitted (in a unit of 4K bytes in a one second period).	R/W	0

Register 22 (0x16): Port 1 Control 6
Register 38 (0x26): Port 2 Control 6
Register 54 (0x36): Port 3 Control 6
Register 70 (0x46): Port 4 Control 6
Register 86 (0x56): Port 5 Control 6

Address	Name	Description	Mode	Default
7-0	Transmit low priority rate control [7:0]	This along with port control 7, bits [7:4] form a 12-bit field to determine how many “32Kbps” low priority blocks can be transmitted (in a unit of 4K bytes in a one second period).	R/W	0

Register 23 (0x17): Port 1 Control 7
Register 39 (0x27): Port 2 Control 7
Register 55 (0x37): Port 3 Control 7
Register 71 (0x47): Port 4 Control 7
Register 87 (0x57): Port 5 Control 7

Address	Name	Description	Mode	Default
7-4	Transmit low priority rate control [11:8]	This along with port control 6, bits [7:0] form a 12-bit field to determine how many “32Kbps” low priority blocks can be transmitted (in a unit of 4K bytes in a one second period).	R/W	0
3-0	Transmit high priority rate control [11:8]	This along with port control 5, bits [7:0] form a 12-bit field to determine how many “32Kbps” high priority blocks can be transmitted (in unit of 4K bytes in a one second period).	R/W	0

Register 24 (0x18): Port 1 Control 8
Register 40 (0x28): Port 2 Control 8
Register 56 (0x38): Port 3 Control 8
Register 72 (0x48): Port 4 Control 8
Register 88 (0x58): Port 5 Control 8

Address	Name	Description	Mode	Default
7-0	Receive high priority rate control [7:0]	This along with port control 10, bits [3:0] form a 12-bit field to determine how many “32Kbps” high priority blocks can be received (in a unit of 4K bytes in a one second period).	R/W	0

Register 25 (0x19): Port 1 Control 9
Register 41 (0x29): Port 2 Control 9
Register 57 (0x39): Port 3 Control 9
Register 73 (0x49): Port 4 Control 9
Register 89 (0x59): Port 5 Control 9

Address	Name	Description	Mode	Default
7-0	Receive low priority rate control [7:0]	This along with port control 10, bits [7:4] form a 12-bit field to determine how many “32Kbps” low priority blocks can be received (in a unit of 4K bytes in a one second period).	R/W	0

Register 26 (0x1A): Port 1 Control 10
Register 42 (0x2A): Port 2 Control 10
Register 58 (0x3A): Port 3 Control 10
Register 74 (0x4A): Port 4 Control 10
Register 90 (0x5A): Port 5 Control 10

Address	Name	Description	Mode	Default
7-4	Receive low priority rate control [11:8]	This along with port control 9, bits [7:0] form a 12-bit field to determine how many “32Kbps” low priority blocks can be received (in a unit of 4K bytes in a one second period).	R/W	0
3-0	Receive high priority rate control [11:8]	This along with port control 8, bits [7:0] form a 12-bit field to determine how many “32Kbps” high priority blocks can be received (in a unit of 4K bytes in a one second period).	R/W	0

Register 27 (0x1B): Port 1 Control 11
Register 43 (0x2B): Port 2 Control 11
Register 59 (0x3B): Port 3 Control 11
Register 75 (0x4B): Port 4 Control 11
Register 91 (0x5B): Port 5 Control 11

Address	Name	Description	Mode	Default
7	Receive differential priority rate control	1, If bit 6 is also ‘1’ this will enable receive rate control for this port on low priority packets at the low priority rate. If bit 5 is also ‘1’, this will enable receive rate control on high priority packets at the high priority rate. 0, receive rate control will be based on the low priority rate for all packets on this port.	R/W	0
6	Low priority receive rate control enable	1, enable port’s low priority receive rate control feature. 0, disable port’s low priority receive rate control.	R/W	0
5	High priority receive rate control enable	1, if bit 7 is also ‘1’ this will enable the port’s high priority receive rate control feature. If bit 7 is a ‘0’ and bit 6 is a ‘1’, all receive packets on this port will be rate controlled at the low priority rate. 0, disable port’s high priority receive rate control feature.	R/W	0
4	Low priority receive rate flow control enable	1, flow control may be asserted if the port’s low priority receive rate is exceeded. 0, flow control is not asserted if the port’s low priority receive rate is exceeded.	R/W	0
3	High priority receive rate flow control enable	1, flow control may be asserted if the port’s high priority receive rate is exceeded. To use this, differential receive rate control must be on. 0, flow control is not asserted if the port’s high priority receive rate is exceeded.	R/W	0
2	Transmit differential priority rate control	1, transmit rate control on both high and low priority packets based on the rate counters defined by the high and low priority packets respectively. 0, transmit rate control on any packets. The rate counters defined in low priority will be used.	R/W	0
1	Low priority transmit rate control enable	1, enable the port’s low priority transmit rate control feature. 0, disable the port’s low priority transmit rate control feature.	R/W	0

Address	Name	Description	Mode	Default
0	High priority transmit rate control enable	1, enable the port's high priority transmit rate control feature. 0, disable the port's high priority transmit rate control feature.	R/W	0

Register 28 (0x1C): Port 1 Control 12
Register 44 (0x2C): Port 2 Control 12
Register 60 (0x3C): Port 3 Control 12
Register 76 (0x4C): Port 4 Control 12
Register 92 (0x5C): Port 5 Control 12

Address	Name	Description	Mode	Default
7	Disable auto-negotiation	1, disable auto-negotiation, speed and duplex are decided by bit 6 and 5 of the same register. 0, auto-negotiation is on.	R/W	0
6	Forced speed	1, forced 100BT if AN is disabled (bit 7). 0, forced 10BT if AN is disabled (bit 7).	R/W	1
5	Forced duplex	1, forced full-duplex if (1) AN is disabled or (2) AN is enabled but failed. 0, forced half-duplex if (1) AN is disabled or (2) AN is enabled but failed.	R/W	0 For port 4 only, there is a special configure pin to set the default pin PCRS strap option. Pull-down (0): Force half-duplex. Pull-up (1): Force full-duplex. *Note: PCRS has internal pull down*.
4	Advertised flow control capability	1, advertise flow control capability. 0, suppress flow control capability from transmission to link partner.	R/W	1
3	Advertised 100BT full-duplex capability	1, advertise 100BT full-duplex capability. 0, suppress 100BT full-duplex capability from transmission to link partner.	R/W	1
2	Advertised 100BT half-duplex capability	1, advertise 100BT half-duplex capability. 0, suppress 100BT half-duplex capability from transmission to link partner.	R/W	1
1	Advertised 10BT full-duplex capability	1, advertise 10BT full-duplex capability. 0, suppress 10BT full-duplex capability from transmission to link partner.	R/W	1
0	Advertised 10BT half-duplex capability	1, advertise 10BT half-duplex capability. 0, suppress 10BT half-duplex capability from transmission to link partner.	R/W	1

Note:

Port Control 12 and 13, and Port Status 0 contents can be accessed by MIIM (MDC/MDIO) interface via the standard MIIM register definition.

Register 29 (0x1D): Port 1 Control 13
Register 45 (0x2D): Port 2 Control 13
Register 61 (0x3D): Port 3 Control 13
Register 77 (0x4D): Port 4 Control 13
Register 93 (0x5D): Port 5 Control 13

Address	Name	Description	Mode	Default
7	LED off	1, turn off all port's LEDs (LEDx_2, LEDx_1, LEDx_0, where "x" is the port number). These pins will be driven high if this bit is set to one. 0, normal operation.	R/W	0
6	Txids	1, disable port's transmitter. 0, normal operation.	R/W	0
5	Restart AN	1, restart auto-negotiation. 0, normal operation.	R/W	0
4	Disable far end fault	1, disable far end fault detection and pattern transmission. 0, enable far end fault detection and pattern transmission.	R/W	0
3	Power down	1, power down. 0, normal operation.	R/W	0
2	Disable auto MDI/MDI-X	1, disable auto MDI/MDI-X function. 0, enable auto MDI/MDI-X function.	R/W	0
1	Forced MDI	1, if auto MDI/MDI-X is disabled, force PHY into MDI mode. 0, MDIX mode.	R/W	0
0	MAC loopback	1, perform MAC loopback. 0, normal operation.	R/W	0

Register 30 (0x1E): Port 1 Status 0
Register 46 (0x2E): Port 2 Status 0
Register 62 (0x3E): Port 3 Status 0
Register 78 (0x4E): Port 4 Status 0
Register 94 (0x5E): Port 5 Status 0

Address	Name	Description	Mode	Default
7	MDIX status	1, MDI. 0, MDI-X.	RO	0
6	AN done	1, AN done. 0, AN not done.	RO	0
5	Link good	1, link good. 0, link not good.	RO	0
4	Partner flow control capability	1, link partner flow control capable. 0, link partner not flow control capable.	RO	0
3	Partner 100BT full-duplex capability	1, link partner 100BT full-duplex capable. 0, link partner not 100BT full-duplex capable.	RO	0
2	Partner 100BT half-duplex capability	1, link partner 100BT half-duplex capable. 0, link partner not 100BT half-duplex capable.	RO	0
1	Partner 10BT full-duplex capability	1, link partner 10BT full-duplex capable. 0, link partner not 10BT full-duplex capable.	RO	0
0	Partner 10BT half-duplex capability	1, link partner 10BT half-duplex capable. 0, link partner not 10BT half-duplex capable.	RO	0

Register 31 (0x1F): Port 1 Control 14
Register 47 (0x2F): Port 2 Control 14
Register 63 (0x3F): Port 3 Control 14
Register 79 (0x4F): Port 4 Control 14
Register 95 (0x5F): Port 5 Control 14

Address	Name	Description	Mode	Default
7	PHY loopback	1, perform PHY loopback, i.e. loopback MAC's Tx back to Rx. 0, normal operation.	R/W	0
6	Remote loopback	1, perform remote loopback, i.e. loopback PHY's Rx back to Tx. 0, normal operation.	R/W	0
5	PHY isolate	1, electrical isolation of PHY from MII and TX+/TX-. 0, normal operation.	R/W	0
4	Soft reset	1, PHY soft reset. 0, normal operation.	R/W	0
3	Force link	1, force link in the PHY. 0, normal operation.	R/W	0
2-1	Reserved	N/A	RO	0
0	Far end fault	1, far end fault status detected. 0, no far end fault status detected.	RO	0

Advanced Control Registers

The IPv4 TOS priority control registers implement a fully decoded 64 bit differentiated services code point (DSCP) register used to determine priority from the 6 bit TOS field in the IP header. The most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bit in the DSCP register. If the register bit is a 1, the priority is high; if it is a 0, the priority is low.

Address	Name	Description	Mode	Default
Register 96 (0x60): TOS Priority Control Register 0				
7-0	DSCP[63:56]		R/W	00000000
Register 97 (0x61): TOS Priority Control Register 1				
7-0	DSCP[55:48]		R/W	00000000
Register 98 (0x62): TOS Priority Control Register 2				
7-0	DSCP[47:40]		R/W	00000000
Register 99 (0x63): TOS Priority Control Register 3				
7-0	DSCP[39:32]		R/W	00000000
Register 100 (0x64): TOS Priority Control Register 4				
7-0	DSCP[31:24]		R/W	00000000
Register 101 (0x65): TOS Priority Control Register 5				
7-0	DSCP[23:16]		R/W	00000000
Register 102 (0x66): TOS Priority Control Register 6				
7-0	DSCP[15:8]		R/W	00000000
Register 103 (0x67): TOS Priority Control Register 7				
7-0	DSCP[7:0]		R/W	00000000

Registers 104 to 109 define the switching engine's MAC address. This 48-bit address is used as the source address in MAC pause control frames.

Register 104 (0x68): MAC Address Register 0				
7-0	MACA[47:40]		R/W	0x00
Register 105 (0x69): MAC Address Register 1				
7-0	MACA[39:32]		R/W	0x10
Register 106 (0x6A): MAC Address Register 2				
7-0	MACA[31:24]		R/W	0xA1
Register 107 (0x6B): MAC Address Register 3				
7-0	MACA[23:16]		R/W	0xff
Register 108 (0x6C): MAC Address Register 4				
7-0	MACA[15:8]		R/W	0xff
Register 109 (0X6D): MAC Address Register 5				
7-0	MACA[7:0]		R/W	0xff

MIIM Registers

The “PHYAD” defined by IEEE is assigned as “0x1” for port 1, “0x2” for port 2, “0x3” for port 3, “0x4” for port 4, “0x5” for port 5. The “REGAD” supported are 0,1,2,3,4,5.

Address	Name	Description	Mode	Default
Register 0: MII Control				
15	Soft reset	1, PHY soft reset. 0, normal operation.	RO	0
14	Loop back	1, loop back mode (loop back at MAC). 0, normal operation.	W	0
13	Force 100	1, 100Mbps. 0, 10Mbps.	R/W	1
12	AN enable	1, auto-negotiation enabled. 0, auto-negotiation disabled.	R/W	1
11	Power down	1, power down. 0, normal operation.	R/W	0
10	Isolate	Not supported.	RO	0
9	Restart AN	1, restart auto-negotiation. 0, normal operation.	R/W	0
8	Force full-duplex	1, full-duplex. 0, half-duplex.	R/W	0
7	Collision test	Not supported.	RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Force MDI	1, force MDI. 0, normal operation.	R/W	0
3	Disable auto MDIX	1, disable auto MDI-X. 0, normal operation.	R/W	0
2	Disable far end fault	1, disable far end fault detection. 0, normal operation.	R/W	0
1	Disable transmit	1, disable transmit. 0, normal operation.	R/W	0
0	Disable LED	1, disable LED. 0, normal operation.	R/W	0
Register 1: MII Status				
15	T4 capable	0, not 100 BASET4 capable.	RO	0
14	100 Full capable	1, 100BASE-TX full-duplex capable. 0, not capable of 100BASE-TX full-duplex.	RO	1
13	100 Half capable	1, 100BASE-TX half-duplex capable. 0, not 100BASE-TX half-duplex capable.	RO	1
12	10 Full capable	1, 10BASE-T full-duplex capable. 0, not 10BASE-T full-duplex capable.	RO	1
11	10 Half capable	1, 10BASE-T half-duplex capable. 0, not 10BASE-T half-duplex capable.	RO	1
10-7	Reserved		RO	0
6	Preamble suppressed	Not supported.	RO	0
5	AN complete	1, auto-negotiation complete. 0, auto-negotiation not completed.	RO	0
4	Far end fault	1, far end fault detected. 0, no far end fault detected.	RO	0
3	AN capable	1, auto-negotiation capable. 0, not auto-negotiation capable.	RO	1

Address	Name	Description	Mode	Default
2	Link status	1, link is up. 0, link is down.	RO	0
1	Jabber test	Not supported.	RO	0
0	Extended capable	0, not extended register capable.	RO	0
Register 2: PHYID HIGH				
15-0	Phyid high	High order PHYID bits.	RO	0x0022
Register 3: PHYID LOW				
15-0	Phyid low	Low order PHYID bits.	RO	0x1450
Register 4: Advertisement Ability				
15	Next page	Not supported.	RO	0
14	Reserved		RO	0
13	Remote fault	Not supported.	RO	0
12-11	Reserved		RO	0
10	Pause	1, advertise pause ability. 0, do not advertise pause ability.	R/W	1
9	Reserved		R/W	0
8	Adv 100 Full	1, advertise 100 full-duplex ability. 0, do not advertise 100 full-duplex ability.	R/W	1
7	Adv 100 Half	1, advertise 100 half-duplex ability. 0, do not advertise 100 half-duplex ability.	R/W	1
6	Adv 10 Full	1, advertise 10 full-duplex ability. 0, do not advertise 10 full-duplex ability.	R/W	1
5	Adv 10 Half	1, advertise 10 half-duplex ability. 0, do not advertise 10 half-duplex ability.	R/W	1
4-0	Selector field	802.3	RO	00001
Register 5: Link Partner Ability				
15	Next page	Not supported.	RO	0
14	LP ACK	Not supported.	RO	0
13	Remote fault	Not supported.	RO	0
12-11	Reserved		RO	0
10	Pause	Link partner pause capability.	RO	0
9	Reserved		RO	0
8	Adv 100 full	Link partner 100 full capability.	RO	0
7	Adv 100 half	Link partner 100 half capability.	RO	0
6	Adv 10 full	Link partner 10 full capability.	RO	0
5	Adv 10 half	Link partner 10 half capability.	RO	0
4-0	Reserved		RO	00000

Absolute Maximum Ratings[1]

Supply Voltage
(V_{DDAR}, V_{DDAP}, V_{DDC}) ..... –0.5V to +2.4V
(V_{DDAT}, V_{DDIO}) ..... –0.5V to +4.0V
Input Voltage (All Inputs) ..... –0.5V to +4.0V
Output Voltage (All Outputs) ..... –0.5V to +4.0V
Lead Temperature (soldering, 10 sec.) ..... 270°C
Storage Temperature (T_S) ..... –55°C to +150°C

Operating Ratings[2]

Supply Voltage
(V_{DDAR}, V_{DDAP}, V_{DDC}) ..... +1.7V to +1.9V
(V_{DDAT}) ..... +3.15V to +3.45V or +2.4V to +2.6V
(V_{DDIO}) ..... +3.15V to +3.45V
Ambient Temperature (T_A)
Commercial ..... –0°C to +70°C
Package Thermal Resistance[3]
PQFP (θ_{JA}) No Air Flow ..... 42.91°C/W
PQFP (θ_{JC}) No Air Flow ..... 19.6°C/W

Electrical Characteristics[4, 5]

Symbol	Parameter	Condition	Min	Typ	Max	Units
100BASE-TX Operation—All Ports 100% Utilization						
I_{DX}	100BASE-TX (Transmitter)	V_{DDAT}		20	28	mA
I_{DDC}	100BASE-TX (Digital Core/PLL+ Analog Rx)	V_{DDC}, V_{DDAP}, V_{DDAR}		157	230	mA
I_{DDIO}	100BASE-TX (Digital IO)	V_{DDIO}		17	30	mA
10BASE-TX Operation —All Ports 100% Utilization						
I_{DX}	10BASE-T (Transmitter)	V_{DDAT}		15	25	mA
I_{DDC}	10BASE-T (Digital Core + Analog Rx)	V_{DDC}, V_{DDAP}		102	180	mA
I_{DDIO}	10BASE-T (Digital IO)	V_{DDIO}		6	15	mA
Auto-Negotiation Mode						
I_{DX}	10BASE-T (Transmitter)	V_{DDAT}		25	40	mA
I_{DDC}	10BASE-T (Digital Core + Analog Rx)	V_{DDC}, V_{DDAP}		108	180	mA
I_{DDIO}	10BASE-T (Digital IO)	V_{DDIO}		17	20	mA
TTL Inputs						
V_{IH}	Input High Voltage		+2.0			V
V_{IL}	Input Low Voltage				+0.8	V
I_{IN}	Input Current (Excluding Pull-up/Pull-down)	V_{IN} = GND ~ V_{DDIO}	–10		10	µA
TTL Outputs						
V_{OH}	Output High Voltage	I_{OH} = –8mA	+2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA			+0.4	V
I_{OZ}	Output Tri-State Leakage	V_{IN} = GND ~ V_{DDIO}			10	µA
100BASE-TX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	100Ω termination on the differential output	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	100Ω termination on the differential output			2	%
t_r t_t	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance		0		0.5	ns
	Duty Cycle Distortion				±0.5	ns
	Overshoot				5	%
V_{SET}	Reference Voltage of I_{SET}			0.5		V
	Output Jitters	Peak-to-peak		0.7	1.4	ns

Symbol	Parameter	Condition	Min	Typ	Max	Units
10BASE-T Receive						
V_{SQ}	Squelch Threshold	5MHz square wave		400		mV
10BASE-T Transmit (measured differentially after 1:1 transformer) V_{DDAT} = 2.5V						
V_P	Peak Differential Output Voltage	100Ω termination on the differential output		2.3		V
	Jitters Added	100Ω termination on the differential output			16	ns
	Rise/Fall Times			28	30	ns

Notes:
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating. Unused inputs must always be tied to an appropriate logic voltage level (ground to V_{DD}).
3. No heat spreader in package. The thermal junction to ambient (θ_{JA}) and the thermal junction to case (θ_{JC}) are under air velocity 0m/s.
4. Specification for packaged product only. A single port's transformer consumes an additional about 40mA for 100Base-TX and 59mA for 10Bese-T.
5. Measurements were taken with operating ratings.

Timing Diagrams

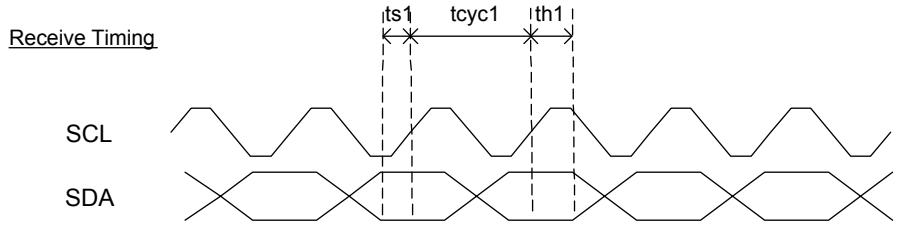


Figure 9. EEPROM Interface Input Receive Timing Diagram

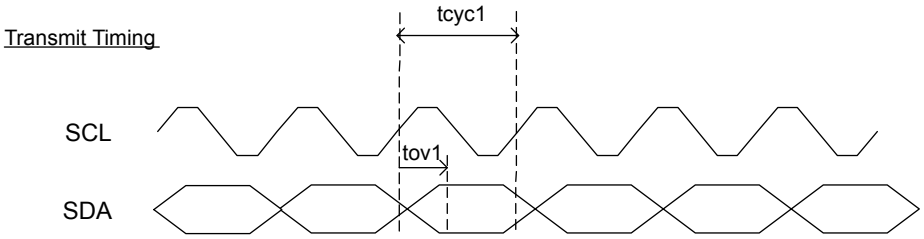


Figure 10. EEPROM Interface Output Transmit Timing Diagram

Symbol	Parameter	Min	Typ	Max	Units
t_{CYC1}	Clock Cycle		16384		ns
t_{S1}	Set-Up Time	20			ns
t_{H1}	Hold Time	20			ns
t_{OV1}	Output Valid	4096	4112	4128	ns

Table 7. EEPROM Timing Parameters

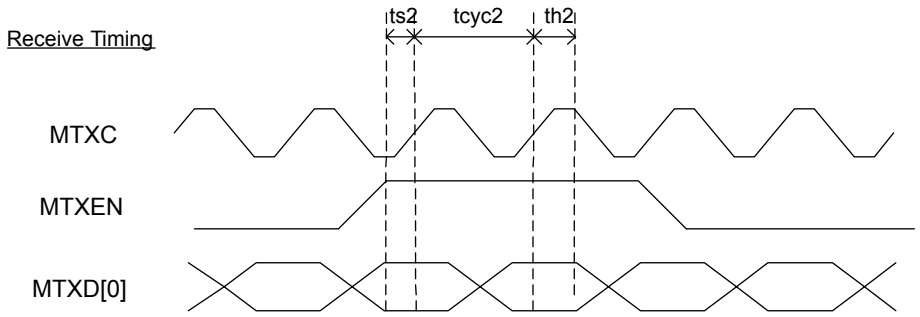


Figure 11. SNI Input Timing

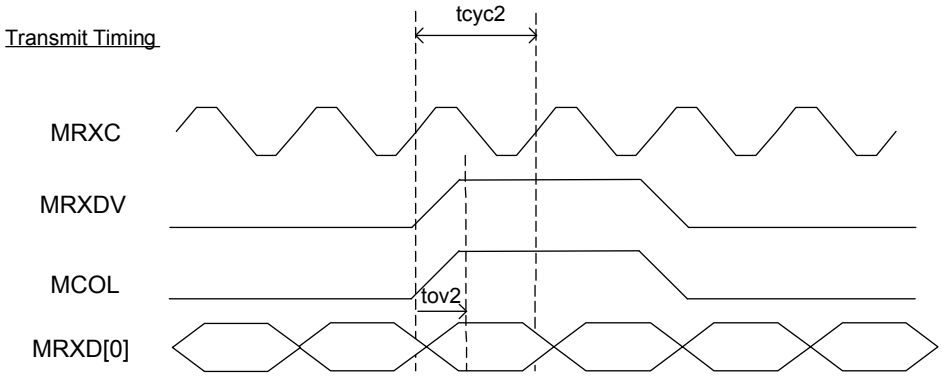


Figure 12. SNI Output Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{CYC2}	Clock Cycle		100		ns
t_{S2}	Set-Up Time	10			ns
t_{H2}	Hold Time	0			ns
t_{O2}	Output Valid	0	3	6	ns

Table 8. SNI Timing Parameters

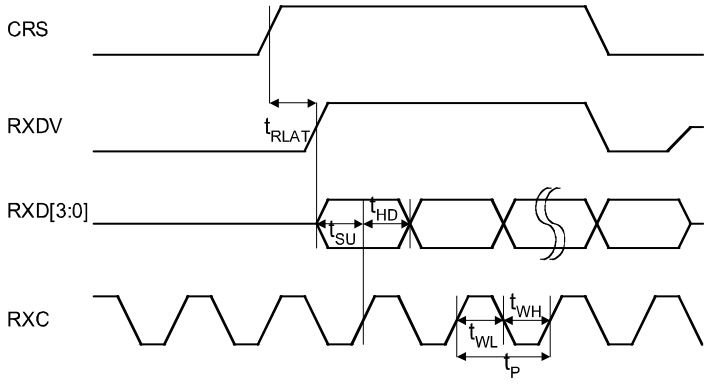


Figure 13. MII Received Timing – For 100BASE-T

Symbol	Parameter	Min	Typ	Max	Units
t_P	RXC Period		40		ns
t_{WL}	RXC Pulse Width	20			ns
t_{WH}	RXC Pulse Width	20			ns
t_{SU}	RXD [3:0], RXDV Set-up to Rising Edge of RXC		20		ns
t_{HD}	RXD [3:0], RXDV Hold from Rising Edge of RXC		20		ns
t_{RLAT}	CRS to RXD Latency, 4B or 5B Aligned		60		ns

Table 9. MII Received Timing Parameters

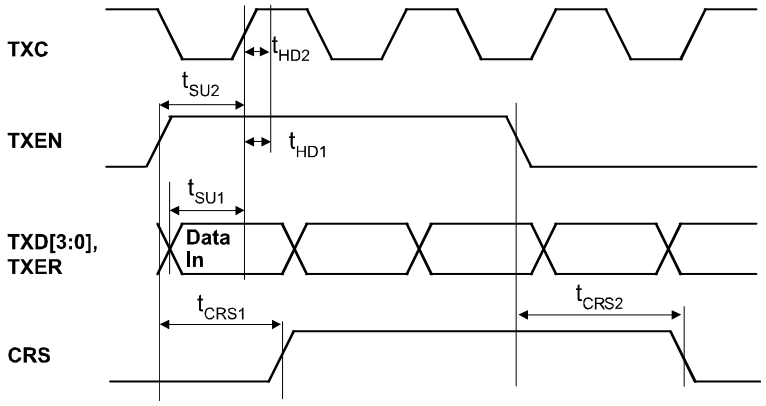


Figure 14. MII Transmitted Timing – For 100BASE-T

Symbol	Parameter	Min	Typ	Max	Units
t_{SU1}	TXD [3:0] Set-up to TXC High	10			ns
t_{SU2}	TXEN Set-up to TXC High	10			ns
t_{HD1}	TXD [3:0] Hold after TXC High	0			ns
t_{HD2}	TXER Hold after TXC High	0			ns
t_{CRS1}	TXEN High to CRS Asserted Latency		40		ns
t_{CRS2}	TXEN Low to CRS De-Asserted Latency		40		ns

Table 10. MII Transmitted Timing Parameters

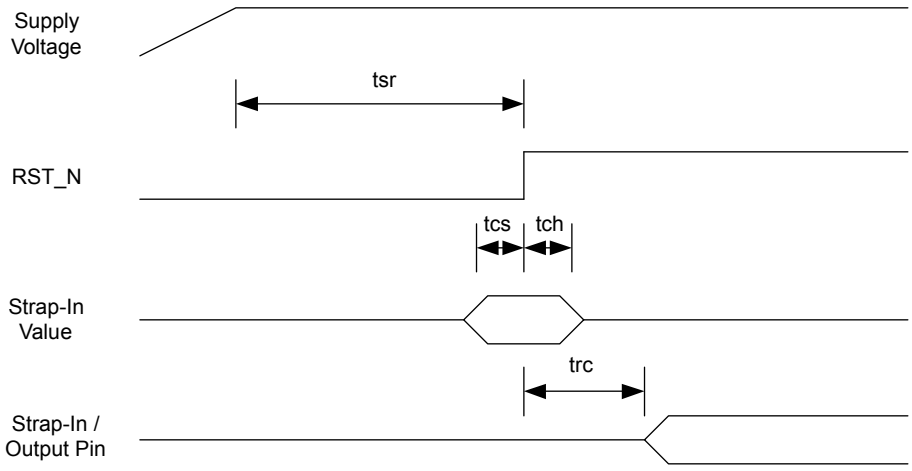


Figure 15. Reset Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{SR}	Stable Supply Voltages to Reset High	10			ms
t_{CS}	Configuration Set-Up Time	50			ns
t_{CH}	Configuration Hold Time	50			ns
t_{RC}	Reset to Strap-In Pin Output	50			ns

Table 11. Reset Timing Parameters

Reset Circuit Diagram

Micrel recommends the following discrete reset circuit as shown in Figure 16 when powering up the KS8895XA device. For the application where the reset circuit signal comes from another device (e.g., CPU, FPGA, etc), we recommend the reset circuit as shown in Figure 17.

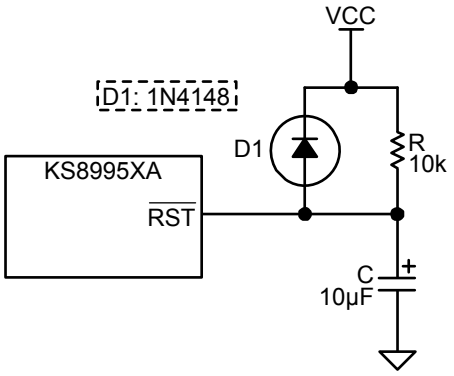


Figure 16. Recommended Reset Circuit

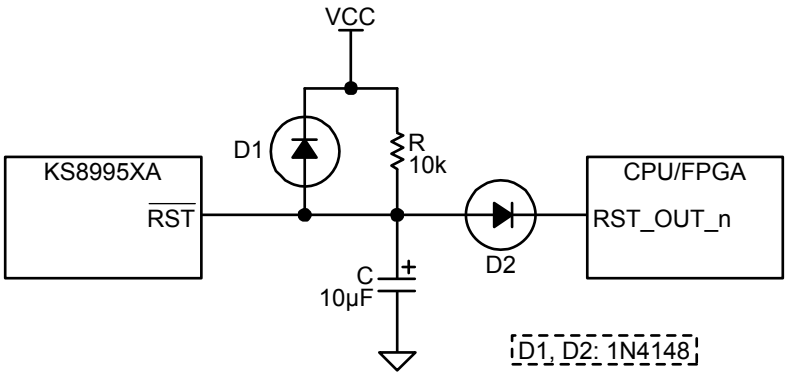


Figure 17. Recommended Circuit for Interfacing with CPU/FPGA Reset

At power-on-reset, R, C, and D1 provide the necessary ramp rise time to reset the Micrel device. The reset out from CPU/FPGA provides warm reset after power up. It is also recommended to power up the VDD core voltage earlier than VDDIO voltage. At worst case, the both VDD core and VDDIO voltages should come up at the same time.

Selection of Isolation Transformer(1)

One simple 1:1 isolation transformer is needed at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements. The following table gives recommended transformer characteristics.

Characteristics Name	Value	Test Condition
Turns Ratio	1 CT : 1 CT	
Open-Circuit Inductance (min.)	350µH	100mV, 100kHz, 8mA
Leakage Inductance (max.)	0.4µH	1MHz (min.)
Inter-Winding Capacitance (max.)	12pF	
D.C. Resistance (max.)	0.9Ω	
Insertion Loss (max.)	1.0dB	0MHz to 65MHz
HIPOT (min.)	1500Vrms	

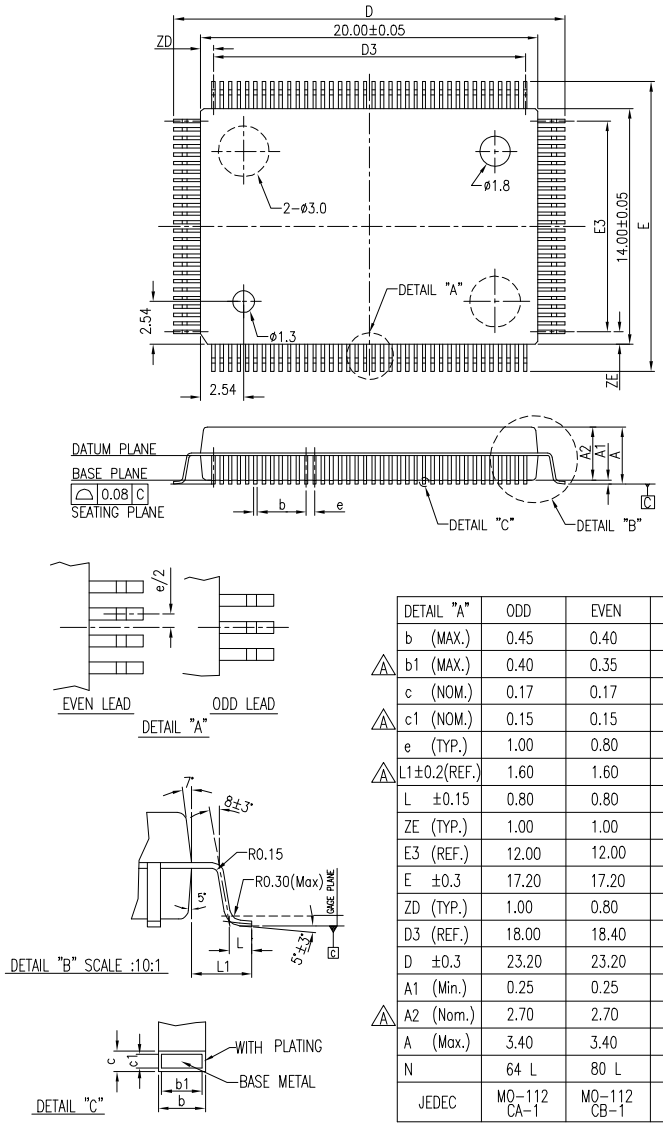
Note:
1. The IEEE 802.3u standard for 100BASE-TX assumes a transformer loss of 0.5dB. For the transmit line transformer, insertion loss of up to 1.3dB can be compensated by increasing the line drive current by means of reducing the ISET resistor value.

The following transformer vendors provide compatible magnetic parts for Micrel's device:

4-Port Integrated		Auto MDIX	Number of Ports	Single-Port		Auto MDIX	Number of Ports
Vendor	Part			Vendor	Part		
Pulse	H1164	Yes	4	Pulse	H1102	Yes	1
Bel Fuse	558-5999-Q9	Yes	4	Bel Fuse	S558-5999-U7	Yes	1
YCL	PH406466	Yes	4	YCL	PT163020	Yes	1
Transpower	HB826-2	Yes	4	Transpower	HB726	Yes	1
Delta	LF8731	Yes	4	Delta	LF8505	Yes	1
LanKom	SQ-H48W	Yes	4	LanKom	LF-H41S	Yes	1

Table 12. Qualified Magnetics Lists

Package Information



DETAIL "A"	ODD	EVEN	EVEN	EVEN
b (MAX.)	0.45	0.40	0.35	0.25
⚠A b1 (MAX.)	0.40	0.35	0.30	0.20
c (NOM.)	0.17	0.17	0.17	0.17
⚠A c1 (NOM.)	0.15	0.15	0.15	0.15
e (TYP.)	1.00	0.80	0.65	0.50
⚠A L1±0.2(REF.)	1.60	1.60	1.60	1.60
L ±0.15	0.80	0.80	0.80	0.80
ZE (TYP.)	1.00	1.00	0.83	0.75
E3 (REF.)	12.00	12.00	12.35	12.50
E ±0.3	17.20	17.20	17.20	17.20
ZD (TYP.)	1.00	0.80	0.58	0.75
D3 (REF.)	18.00	18.40	18.85	18.50
D ±0.3	23.20	23.20	23.20	23.20
A1 (Min.)	0.25	0.25	0.25	0.25
⚠A A2 (Nom.)	2.70	2.70	----	----
A (Max.)	3.40	3.40	3.40	3.40
N	64 L	80 L	100 L	128L
JEDEC	MO-112 CA-1	MO-112 CB-1	CC-1	----

128-Pin PQFP (PQ)

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