Low Input Voltage, Compact LCD Bias IC With VCOM Buffer

Check for Samples: TPS65150-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C6**
- **1.8-V to 6-V Input Voltage Range**
- **Integrated VCOM Buffer**
- **High Voltage Switch to Isolate VGH**
- **Gate Voltage Shaping of VGH**
- **2-A Internal MOSFET Switch**
- **Main Output V_S up to 15 V With < 1% Output Voltage Accuracy**
- **Virtual Synchronous Converter Technology**
- **Negative Regulated Charge Pump Driver VGL**
- **Positive Regulated Charge Pump Driver VGH**
- **Adjustable Power On Sequencing**
- **Adjustable Fault Detection Timing**
- **Gate Drive Signal for external isolation MOSFET**
- **Thermal Shutdown**
- **Available in TSSOP-24 Package**

APPLICATIONS

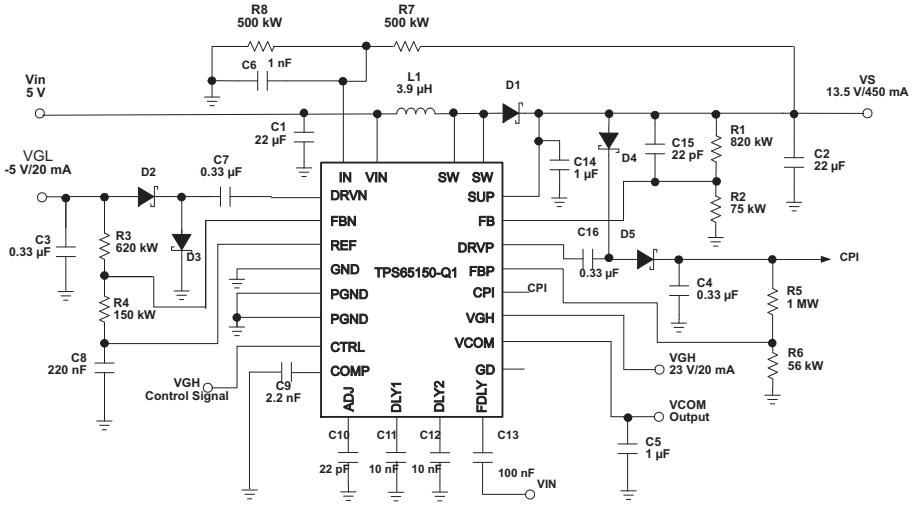
- **TFT LCD Displays for Notebooks**
- **TFT LCD Display for Monitor**
- **Car Navigation Display**

DESCRIPTION

The TPS65150-Q1 offers a very compact and small power-supply solution that provides all three voltages required by thin film transistor (TFT) LCD displays. With an input voltage range of 1.8 V to 6 V, the device is ideal for notebooks powered by a 2.5-V or 3.3-V input rail or monitor applications with a 5-V input-voltage rail. Additionally the TPS65150-Q1 provides an integrated high-current buffer to provide the VCOM voltage for the TFT backplane.

Two regulated adjustable charge-pump drivers provide the positive VGH and negative VGL bias voltages for the TFT. The device incorporates adjustable power-on sequencing for VGL as well as for VGH. This avoids any additional external components to implement application-specific sequencing. The device has an integrated high-voltage switch to isolate VGH. For the QFN package (RGE), contact TI sales.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

One can also use the same internal circuit to provide a gate-shaping signal of VGH for the LCD panel controlled by the signal applied to the CTRL input. For highest safety, the TPS65150-Q1 has an integrated adjustable shutdown latch feature to allow application-specific flexibility. The device monitors the outputs (V_S, VGL, VGH); and, as soon as one of the outputs falls below its power-good threshold, the device enters shutdown latch, after its adjustable delay time has passed by.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	UNIT
Voltages on pin VIN(2)	–0.3 V to 7 V
Voltages on pin SUP	–0.3 V to 15.5 V
Voltage on pin SW	20 V
Voltage on CTRL	–0.3 V to 7 V
Voltage on GD	15.5 V
Voltage on CPI	32 V
Operating junction temperature range	–40°C to 125°C
Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS65150-Q1 PWP 24 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	40.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	20.8	
θ_{JB}	Junction-to-board thermal resistance	18.4	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	18.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
VIN	Input voltage range	1.8		6	V
V_S	Output voltage range of the main boost converter V_S			15	V
L	Inductor(1)		4.7		µH
T_A	Operating ambient temperature	–40		125	°C

(1) Refer to application section for further information.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.3 V, V_S = 10 V, T_A = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_{IN}	Input voltage range			1.8		6	V
I_{QVIN}	No load quiescent current into V_{IN}	Device is not switching			14	25	µA
I_{QSUP}	No load quiescent current into SUP	Device is not switching			1.9	3	mA
I_{QVCOM}	VCOM quiescent current into SUP				750	1500	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling	–40°C < T_A < 85°C		1.6	1.8	V
			–40°C < T_A < 125°C		1.6	1.85	
V_{hys}	Undervoltage lockout threshold	V_{IN} rising	–40°C < T_A < 85°C		1.7	1.9	V
			–40°C < T_A < 125°C		1.7	1.95	
	Thermal shutdown	Temperature rising			155		°C
	Thermal shutdown hysteresis				10		°C
LOGIC SIGNALS CTRL							
V_{IH}	High level input voltage			1.6			V
V_{IL}	Low level input voltage					0.4	V
I_I	Input leakage current	CTRL = GND or V_{IN}			0.01	0.2	µA
MAIN BOOST CONVERTER							
V_S	Output voltage range					15	V
V_{FB}	Feedback regulation voltage	–40°C < T_A < 85°C		1.136	1.146	1.154	V
		–40°C < T_A < 125°C		1.132	1.146	1.160	
I_{FB}	Feedback input bias current				10	100	nA
$r_{DS(on)}$	N-MOSFET on-resistance (Q1)	V_S = 10 V; I_{SW} = 500 mA			200	300	mΩ
		V_S = 5 V; I_{SW} = 500 mA			305	450	
	P-MOSFET on-resistance (Q2)	V_S = 10 V; I_{SW} = 500 mA			8	15	Ω
		V_S = 5 V; I_{SW} = 500 mA			12	22	
I_{MAX}	Maximum P-MOSFET peak switch current					1	A
I_{LIM}	N-MOSFET switch current limit (Q1)			2	2.5	3.4	A
Ileak	Switch leakage current	V_{SW} = 15 V			1	10	µA
Vovp	Output overvoltage protection	V_{OUT} rising		16		20	V
f_{OSC}	Oscilator frequency			1.02	1.2	1.38	MHz
	Line regulation	V_{IN} = 1.8 V to 5 V, I_{load} = 1 mA			0.007		%/V
	Load regulation	V_{IN} = 5 V, I_{load} = 0 A to 400 mA			0.16		%/A
NEGATIVE CHARGE PUMP VGL							
VGL	Output voltage range					–2	V
V_{REF}	Reference voltage on pin REF	–40°C < T_A < 85°C		1.205	1.213	1.219	V
		–40°C < T_A < 125°C		1.203	1.213	1.223	
V_{FB}	Feedback regulation voltage			–36	0	36	mV
I_{FB}	Feedback input bias current				10	100	nA
$r_{DS(on)}$	Q4 P-channel switch $r_{DS(on)}$	I_{OUT} = 20 mA			4.4		Ω
V_{DropN}	Current sink voltage drop(1)	I_{DRN} = 50 mA, V_{FBN} = $V_{FBNNominal}$ –5%			130	300	mV
		I_{DRN} = 100 mA, V_{FBN} = $V_{FBNNominal}$ –5%			280	450	
	Load regulation	VGL = –5 V, I_{load} = 0 mA to 20 mA			0.016		%/mA
POSITIVE CHARGE PUMP OUTPUT							
V_{CPO}	Output voltage range	CTRL = GND, VGH = open				30	V

(1) The maximum charge-pump output current is half the drive current of the internal current source or sink.

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.3 V, V_S = 10 V, T_A = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

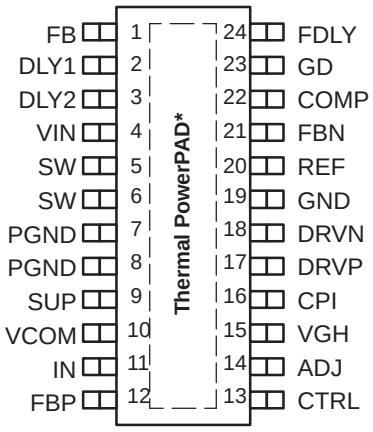
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback regulation voltage	CTRL = GND, VGH = open	1.187	1.214	1.238	V
I_{FB}	Feedback input bias current	CTRL = GND, VGH = open		10	100	nA
$r_{DS(on)}$	Q3 P-channel switch RDSon	I_{OUT} = 20 mA		1.1		Ω
V_{DropN}	Current sink voltage drop(1)	I_{DRP} = 50 mA, V_{FBP} = $V_{FBPNominal}$ –5%		420	650	mV
		I_{DRP}= 100 mA, V_{FBP} = $V_{FBPNominal}$ –5%		900	1400	
	Load regulation	VGH = 24 V, I_{load} = 0 mA to 20 mA		0.07		%/mA
VGH ISOLATION SWITCH, GATE-VOLTAGE FALL-TIME CONTROL						
$r_{DS(on)}$	Q5 - Pass MOSFET R_{DSon}	I_{OUT} = 20 mA		12	30	Ω
Iadj	Capacitor charge current	Vadj = 20 V, CPI = 30 V	160	200	240	µA
	Minimum output voltage	V_{adj} = 0 V, I_{VGH} = 10 mA		2		V
I_{VGH}	Maximum output current		20			mA
TIMING CIRCUITS DLY1, DLY2, FDLY						
I_{DLY1}	Drive current into delay capacitor DLY1	V_{DLY1} = 1.213 V	3	5	7	µA
I_{DLY2}	Drive current into delay capacitor DLY1	V_{DLY2} = 1.213 V	3	5	7	µA
R_{FDLY}	Fault time delay resistror(2)		250	450	650	kΩ
GATE DRIVE (GD)						
$V_{(GD, Vs)}$	Gate drive threshold(3)	V_S rising	–12% of V_S		–4% of V_S	V
V_{OL}	Gate-drive output low voltage	$I_{(sink)}$ = 500 µA			0.5	V
I_{LKG}	Gate drive output leakage current	V_{GD} = 15 V		0.001	1	µA
Vcom Buffer						
V_{CM}	Common-mode input range		2.25		(V_S) – 2 V	V
V_{os}	Input offset voltage	I_{OUT} = 0 mA	–25		25	mV
	DC load regulation	I_O = ±25 mA	–37		37	mV
		I_O = ±50 mA	–77		55	
		I_O = ±100 mA	–85		85	
		I_O = ±150 mA	–110		110	
I_B	VCOMIN Input bias current		–300	–30	300	nA
I_{peak}	Peak output current	V_S = 15 V	1.2			A
		V_S = 10 V	0.65			
		V_S = 5 V	0.15			

(2) Clculate the fault time as: t_F= C × R = C × 450 kΩ

(3) The main boost converter output V_S being within regulation causes the latching low of the GD signal. Cycling the input voltage or enable of the boost converter low resets the GD signal.

PIN ASSIGNMENT

TSSOP-24 Package
Top View



* The thermal die connects to GND.

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
ADJ	14	I/O	Gate voltage shaping circuit. Connecting a capacitor to this pin sets the fall time of the positive gate voltage (VGH).
COMP	22	O	This is the compensation pin for the main boost converter. A small capacitor and if required a series resistor is connected to this pin.
CPI	16	I	Input of the VGH isolation switch and gate voltage shaping circuit.
CTRL	13	I	Control signal for the gate voltage shaping signal. Apply the control signal for the gate voltage control. Usually the timing controller of the LCD panel generates this signal. If this function is not required, this pin needs to be connected to VIN. By doing this, the internal switch between CPI and VGH provides isolation for the positive charge pump output VGH. DLY2 sets the delay time for VGH to come up.
DLY1	2	I/O	Power-on sequencing adjust. Connecting a capacitor from this pin to GND allows to set the delay time between the boost converter output Vs and the negative charge pump VGL during startup.
DLY2	3	I/O	Power-on sequencing adjust. Connecting a capacitor from this pin to GND allows to set the delay time between the negative charge pump VGL and the positive charge pump during startup. Note that Q5 in the Gate Voltage Shaping block only turns on when the positive charge pump (FBP) is within regulation. (This provides input to output isolation of VGH).
DRVN	18	I/O	Charge pump driver to generate the negative voltage VGL.
DRVP	17	I/O	Charge pump driver to generate the positive output voltage VGH.
FB	1	I	Feedback of the main boost converter generating Vsource (V_S).
FBN	21	I	Feedback pin of the negative charge pump VGL.
FBP	12	I	Feedback pin of the positive charge pump.
FDLY	24	I/O	Fault delay. Connecting a capacitor from this pin to Vin allows to set the delay time from the point when one of the outputs (VS, VGH, VGL) drops below its power good threshold until the devices enters the shutdown latch. To re-start the device the input voltage has to be cycled to GND. This feature can be disabled by connecting the FDLY pin to Vin.
GD	23	I	Active low open drain output. This output is latched low when the boost converter Vs is in regulation. This signal can be used to drive an external MOSFET to provide isolation for V_S.
GND	19		Analog ground
IN	11	I	Input of the Vcom buffer. If this pin is connected to GND, the Vcom buffer is disabled.
PGND	7, 8		Power ground
REF	20	O	Internal reference output typically 1.213 V
SUP	9	I/O	Supply pin of the positive, negative charge pump and Boost Converter Gate Drive Circuit. This pin needs to be connected to the output of the main boost converter and can't be connected to any other voltage rail.
SW	5, 6	I	Switch pin of the boost converter

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VCOM	10	O	VCOM buffer output. Typically a 1-µF output capacitor is required on this pin.
VGH	15	O	Positive output voltage to drive the TFT gates with an adjustable fall time. This pin is internally connected with a MOSFET switch to the positive charge pump input CPI.
VIN	4	I	This is the input voltage pin of the device.
PowerPAD™ exposed thermal die	NA		The PowerPAD™ needs to be soldered to GND

TYPICAL CHARACTERISTICS

Table 1. TABLE OF GRAPHS

			FIGURES
Main Boost Converter			
η	Efficiency	versus Load current V_S = 10 V	Figure 1
η	Efficiency	versus Load current V_S = 13.5 V	Figure 2
η	Efficiency	versus Load current V_S = 15 V	Figure 3
f_{SW}	Switching frequency	versus Input voltage and temperature	Figure 4
	PWM operation	at nominal load current	Figure 5
	PWM operation	at light load current	Figure 6
	Load transient response		Figure 7
	Softstart boost converter		Figure 8
	Power-on sequencing		Figure 9
	Power-on sequencing	External MOSFET in series to V_S	Figure 10
	Gate voltage shaping of V_{GH}		Figure 11
	Adjustable Fault detection		Figure 12
Negative Charge-Pump Driver			
V_{GL}	V_{GL}	versus load current	Figure 13
Positive Charge-Pump Driver			
V_{GH}	V_{GH}	versus load current; Charge-pump doubler stage	Figure 14
V_{GH}	V_{GH}	versus load current; Charge-pump tripler stage	Figure 15
VCOM Buffer			
	VCOM Buffer transconductance		Figure 16

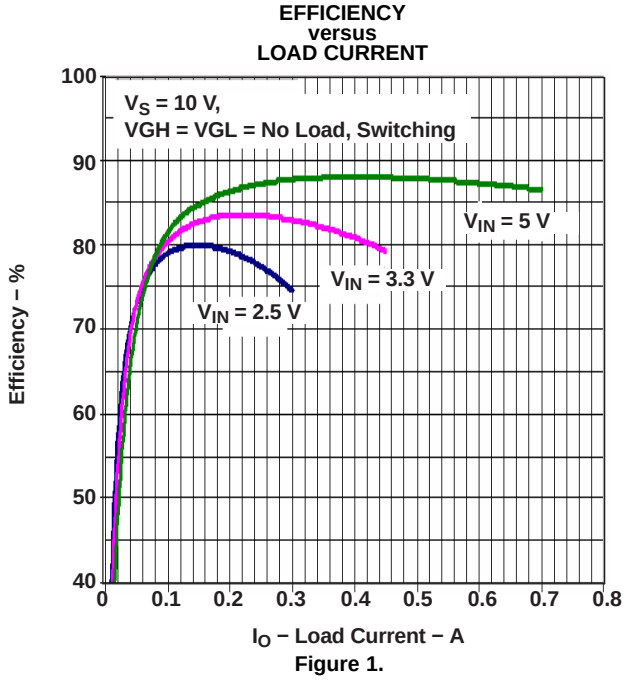


Figure 1.

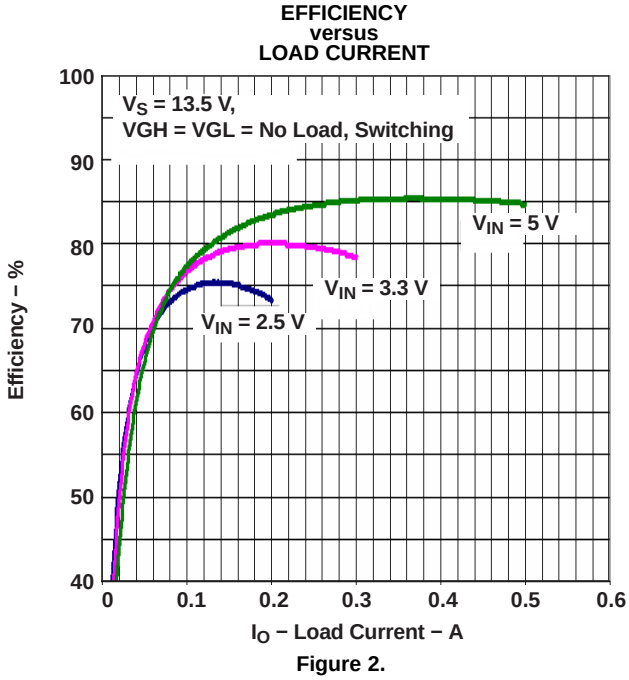


Figure 2.

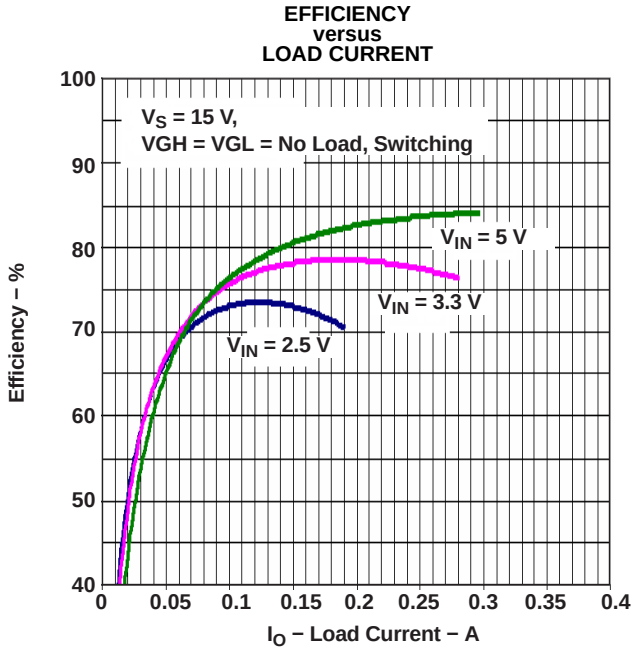


Figure 3.

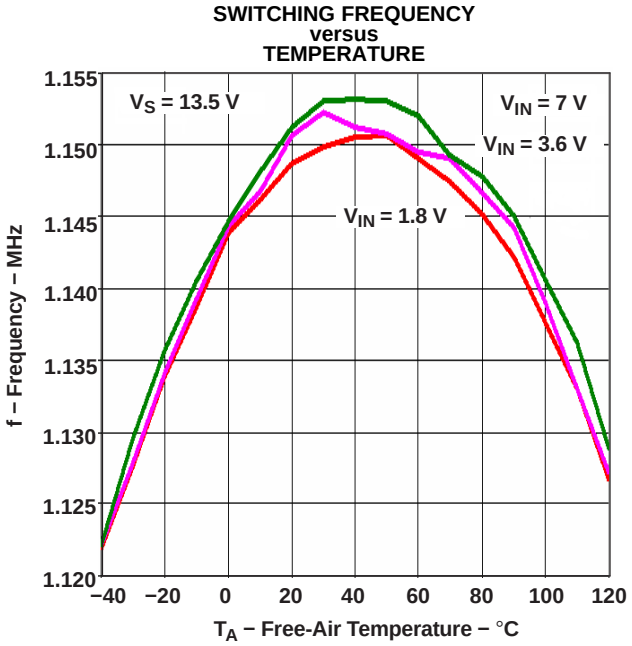


Figure 4.

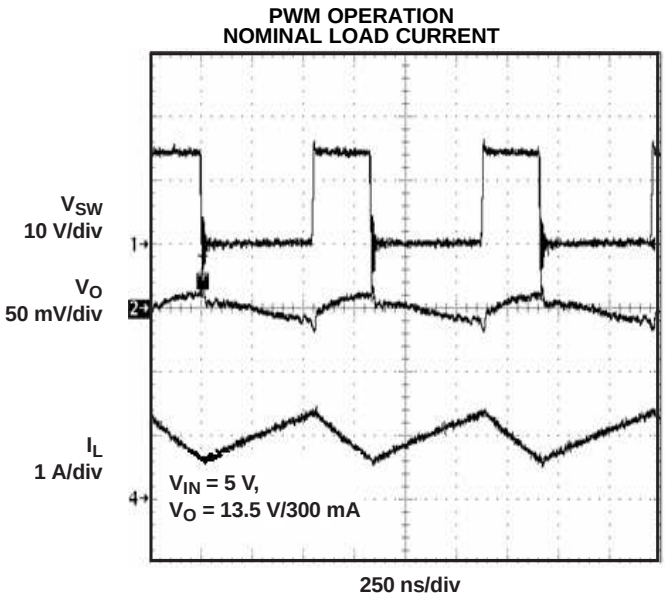


Figure 5.

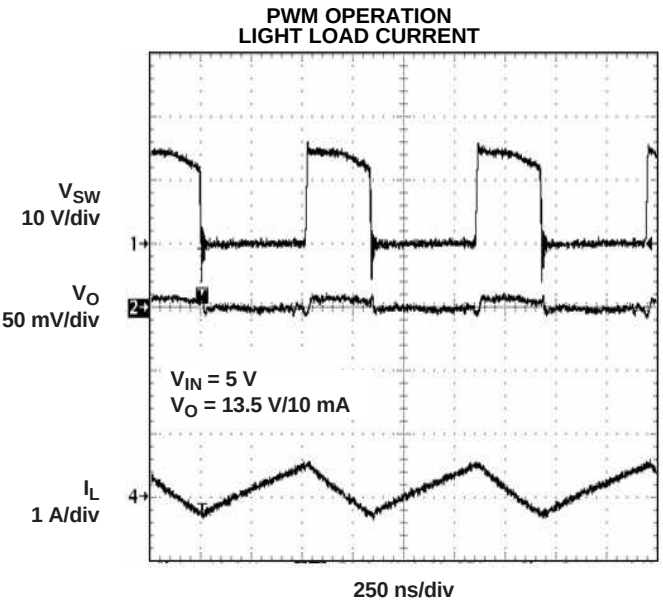


Figure 6.

LOAD TRANSIENT RESPONSE

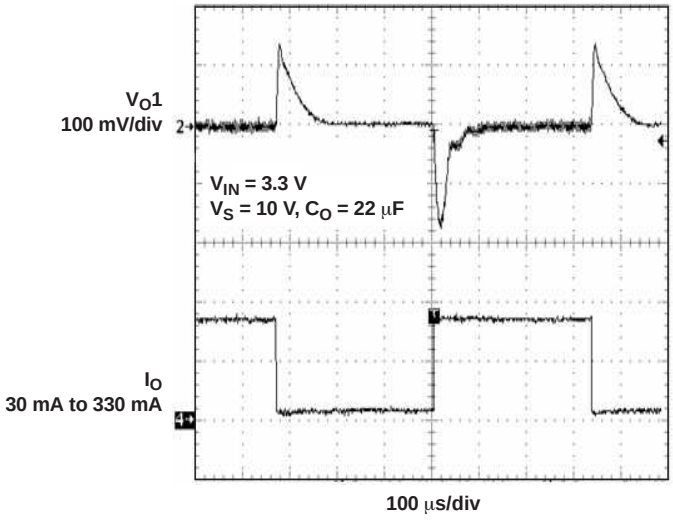


Figure 7.

SOFT START BOOST CONVERTER

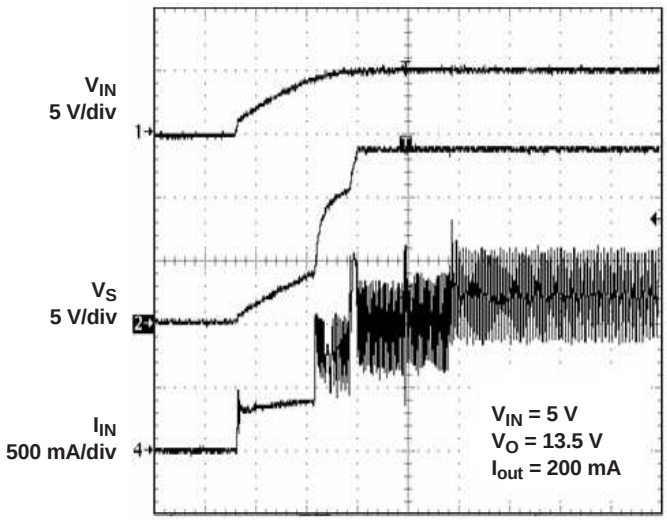


Figure 8.

POWER-ON SEQUENCING

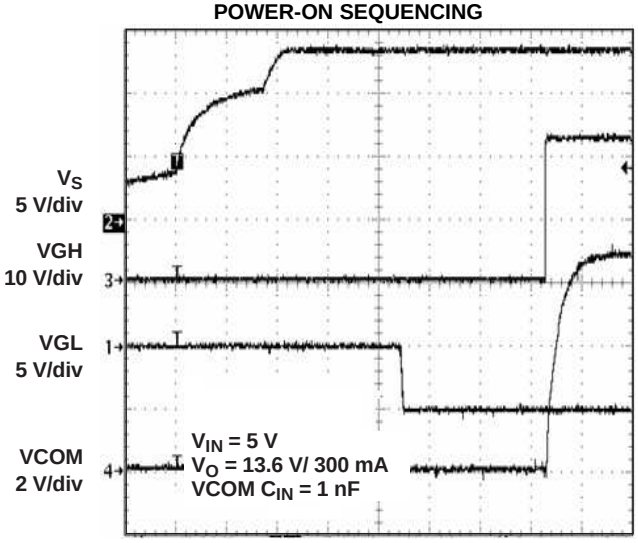


Figure 9.

POWER-ON SEQUENCING WITH EXTERNAL ISOLATION MOSFET AT V_S

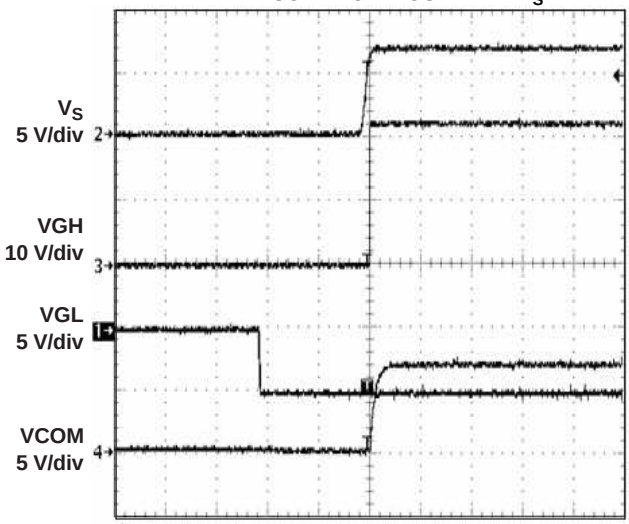
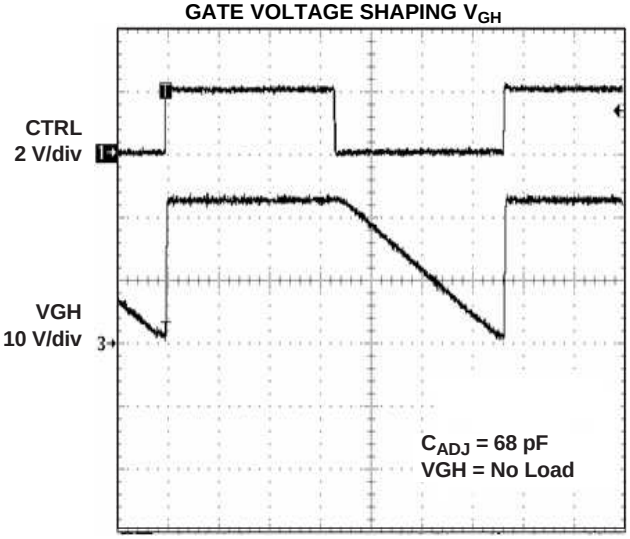


Figure 10.

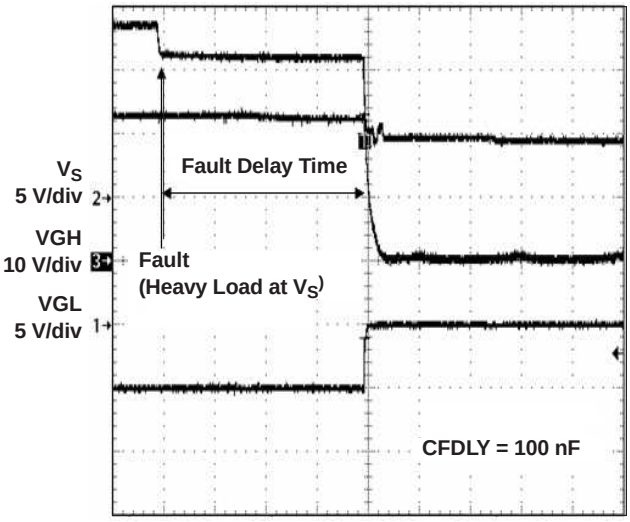
GATE VOLTAGE SHAPING V_{GH}



2.5 μs/div

Figure 11.

ADJUSTABLE FAULT DETECTION



10 ms/div

Figure 12.

V_{GL} – GATE VOLTAGE LOW versus LOAD CURRENT

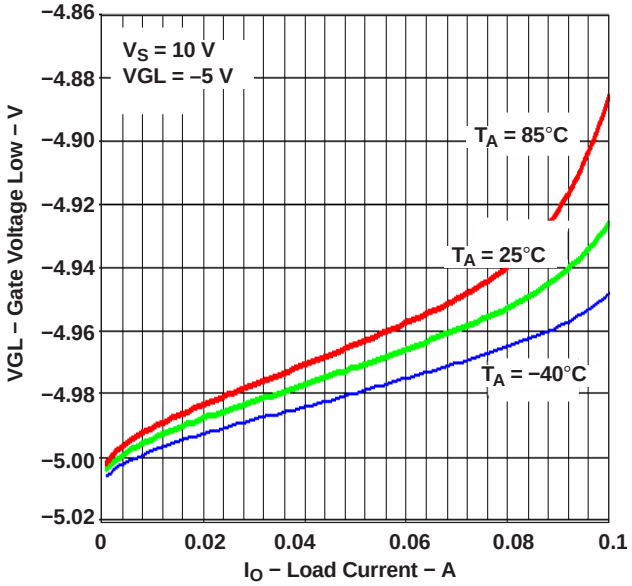


Figure 13.

V_{GH} – GATE VOLTAGE HIGH versus LOAD CURRENT –X2 STAGE

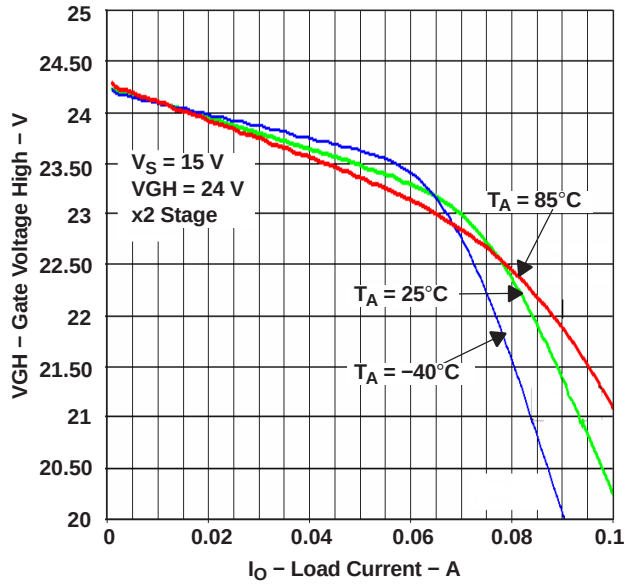
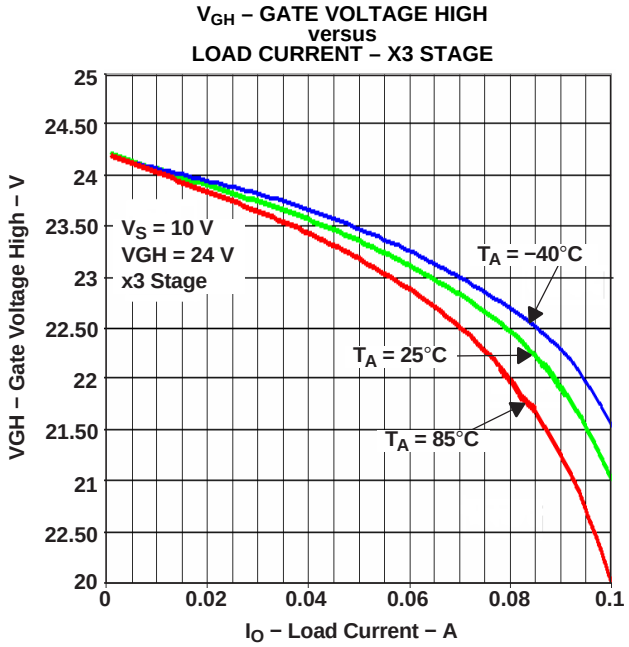
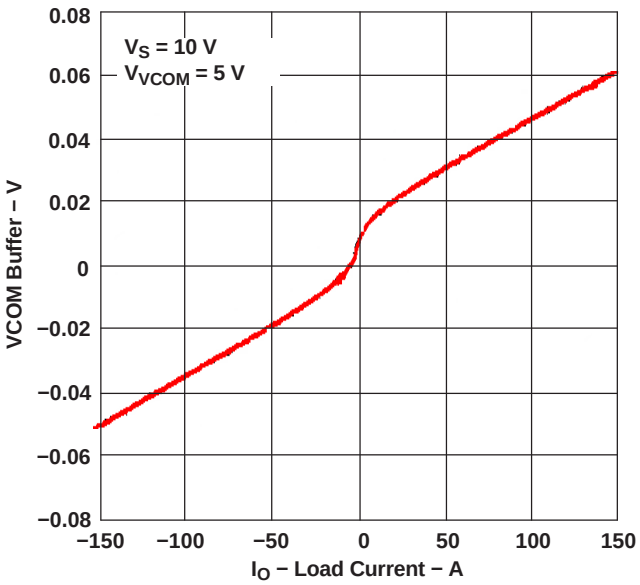


Figure 14.



V_{GH} – GATE VOLTAGE HIGH versus LOAD CURRENT – X3 STAGE

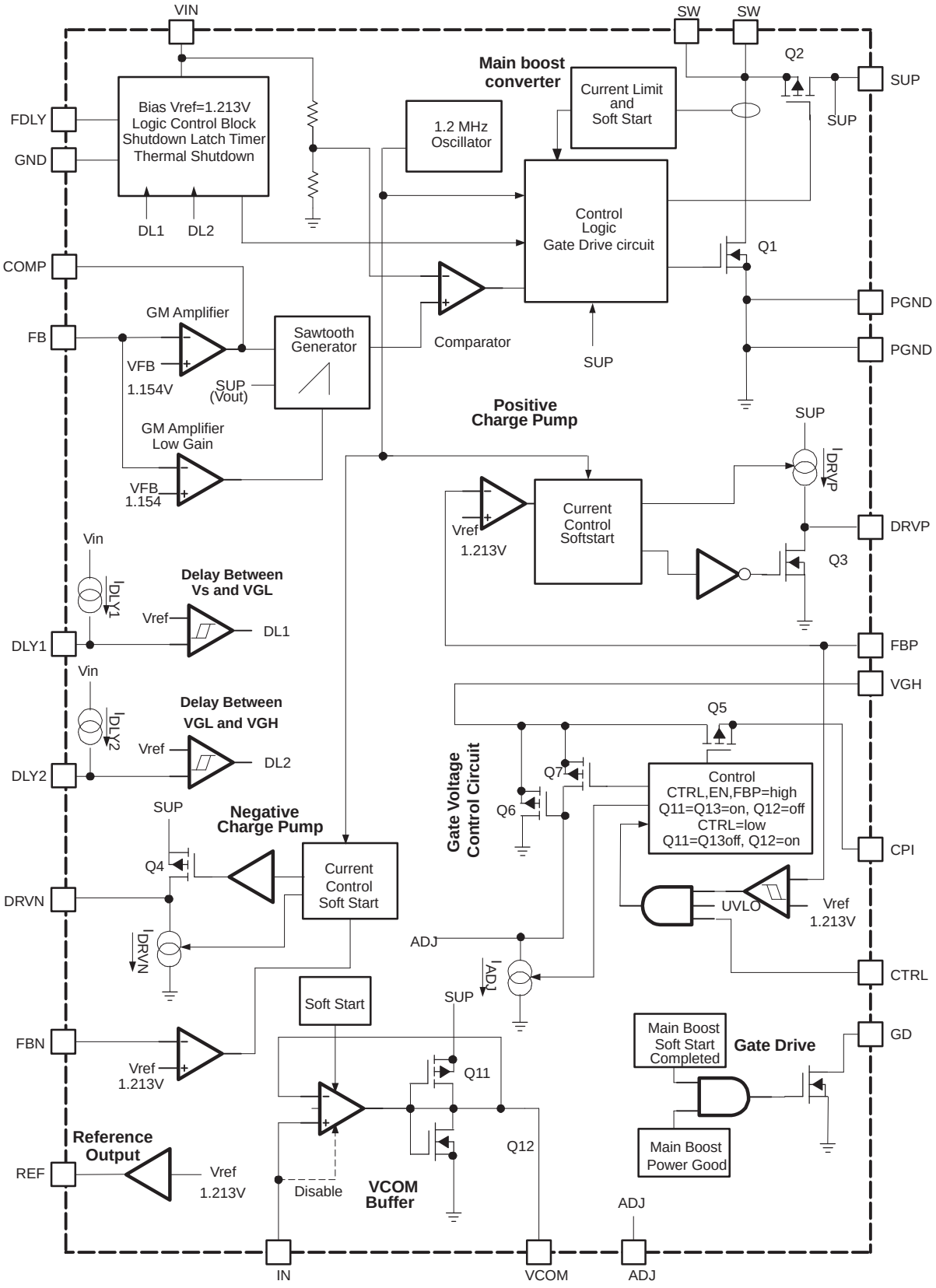
Figure 15.



VCOM BUFFER dV_{OUT} versus LOAD CURRENT

Figure 16.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

Main Boost Converter

The main boost converter operates with pulse-width modulation (PWM) and a fixed switching frequency of 1.2 MHz. The converter uses a unique fast-response, voltage-mode controller scheme with input-voltage feedforward. This achieves excellent line and load regulation (0.16%/A load regulation typical) and allows the use of small external components. To add higher flexibility to the selection of external component values, the device uses external loop compensation. Although the boost converter looks like a non-synchronous boost converter topology operating in discontinuous-conduction mode at light load current, the TPS65150-Q1 maintains continuous conduction even at light load currents. The device achieves continuous conduction by using the virtual synchronous converter technology having an external Schottky diode with an integrated MOSFET in parallel connected between the SW pin and the SUP pin. See *FUNCTIONAL BLOCK DIAGRAM*. The intention of this MOSFET is to allow the current to go below ground, which is the case at light load conditions. For this purpose, a small integrated P-Channel MOSFET, with typically 10-Ω $r_{DS(on)}$, is sufficient. When the inductor current is positive, the external Schottky diode with the lower forward voltage conducts the current. This causes the converter to operate with a fixed frequency in continuous-conduction mode over the entire load-current range. This avoids the ringing on the switch pin as seen with standard non-synchronous boost converters and allows a simpler compensation for the boost converter.

Soft Start

The main boost converter as well as the charge pump driver have an internal soft-start circuit. This avoids heavy voltage drops at the input voltage rail or at the output of the main boost converter versus during start-up caused by high inrush currents. As the main boost converter starts up, the internal current-limit threshold increases in three steps. The device starts with the first step, where the current-limit setting is 2/5 of the typical current limit (2/5 of 2.3 A) for 2048 clock cycles, then increases to 3/5 of the current limit for 2048 clock cycles, and the third step is the full current limit. This gives a typical start-up time around 5 ms.

Adjustable Fault Delay

The TPS65150-Q1 has an integrated adjustable-delay timer shutting down the entire device in case of a fault at the outputs. The fault timer is also active during startup. Connecting a capacitor from the FDLY pin to V_{IN} sets the delay time, from the point where one of the outputs (V_S, VGH, VGL) drops below its power-good threshold, until the device enters the shutdown latch. Because the fault delay timer is also active during startup, the device enters shutdown when the output voltage of the main boost converter, V_S, does not reach its power-good threshold after the fault delay time has passed. When an external isolation switch is used, as shown in Figure 24, then the device provides short-circuit protection even during start-up. To restart the device, cycle the input voltage to GND. The shutdown function can be disabled by connecting FDLY to V_{IN}. The fault delay time is calculated as:

$t_F = C \times R = C \times 450\ k\Omega = 100\ nF \times 450\ k\Omega \approx 40\ ms$

Positive Charge Pump

The positive charge pump provides a regulated output voltage, set by the external resistor divider. Figure 17 is an extract from the block diagram showing the positive charge-pump driver circuit . One can best understand the operation of the charge-pump driver by looking at Figure 17. During the first cycle, Q3 turns on and the flying capacitor, C_{fly}, charges to the source voltage, V_S. During the next clock cycle, Q3 turns off, and the current source charges the drive pin, DRVP, up to the supply voltage, VSUP. Because the flying capacitor voltage sits on top of the drive pin voltage, the maximum output voltage is VGH = V_{sup} + V_S – V_{drop}. V_{drop} is the voltage drop across the external diodes and internal charge-pump MOSFETs.

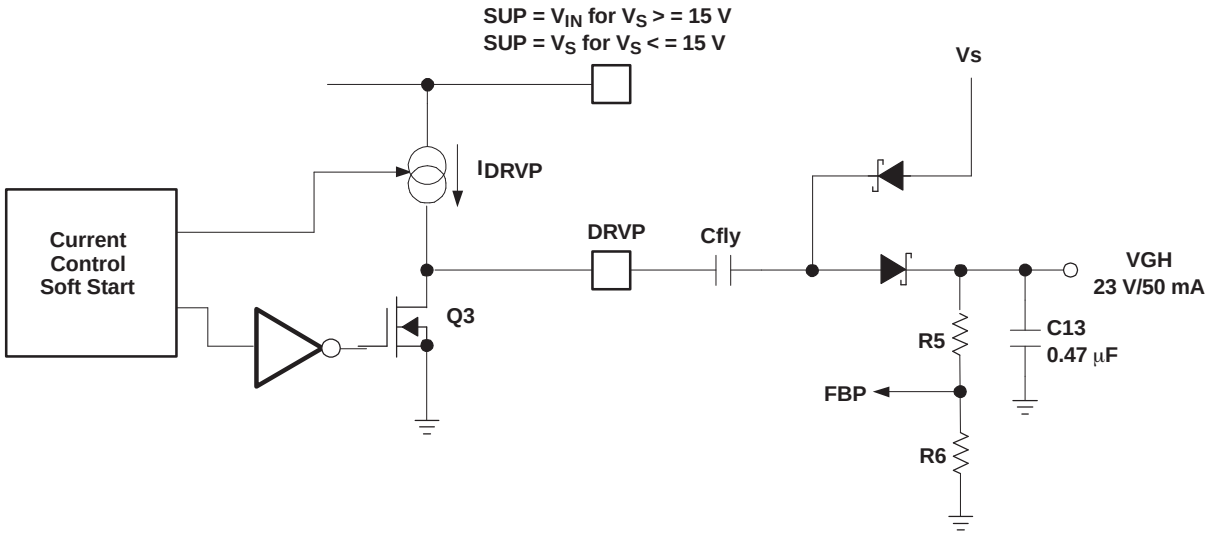


Figure 17. Positive Charge-Pump Driver

If higher output voltages are required, add another charge-pump stage to the output, as shown in Figure 21 at the end of the data sheet. To minimize quiescent current, use a high-impedance feedback divider. The top feedback-resistor selection should not be larger than 1 MΩ.

Setting the output voltage:

$$V_{out} = 1.213 \times \left(1 + \frac{R5}{R6}\right)$$

$$R5 = R6 \times \left(\frac{V_{out}}{V_{FB}} - 1\right) = R6 \times \left(\frac{V_{out}}{1.213} - 1\right) \quad (1)$$

Negative Charge Pump

The negative charge pump provides a regulated output voltage set by the external resistor divider. The negative charge pump operates very similar to the positive charge pump with the difference that the voltage on the supply pin SUP is inverted. The maximum output voltage for a single stage charge pump inverter is VGL = ($-V_{sup}$) + V_{drop}. V_{drop} is the voltage drop across the external diodes and internal charge-pump MOSFETs.

Setting the output voltage:

$$V_{out} = -V_{REF} \times \frac{R3}{R4} = -1.213\ V \times \frac{R3}{R4}$$

$$R3 = R4 \times \frac{|V_{out}|}{V_{REF}} = R4 \times \frac{|V_{out}|}{1.213} \quad (2)$$

The lower feedback resistor value, R4, should range between 40 kΩ and 120 kΩ; or, the overall feedback resistance should be from 500 kΩ to 1 MΩ. Smaller values load the reference too heavily; and larger values may cause stability problems. The negative charge pump requires two external Schottky diodes. The peak current rating of the Schottky diode must be twice the load current of the output. For a 20-mA output current, the BAT54 dual Schottky diode is a good choice.

Power-On Sequencing, DLY1, DLY2

As soon after application of the input voltage that it rises above the undervoltage lockout (UVLO) threshold, the device starts with the main boost converter, V_S, coming up first. Then the negative voltage, VGL, comes up, set by the delay time DLY1; and then the positive charge pump, VGH, set by the delay time DLY2. Finally, the VCOM buffer starts up. The capacitor values connected to these pins set the delay times, DLY1 and DLY2. An internal current source charges the capacitor with a constant current of typically 5 µA until the voltage reaches the internal comparator trip point of V_{REF} = 1.213 V.

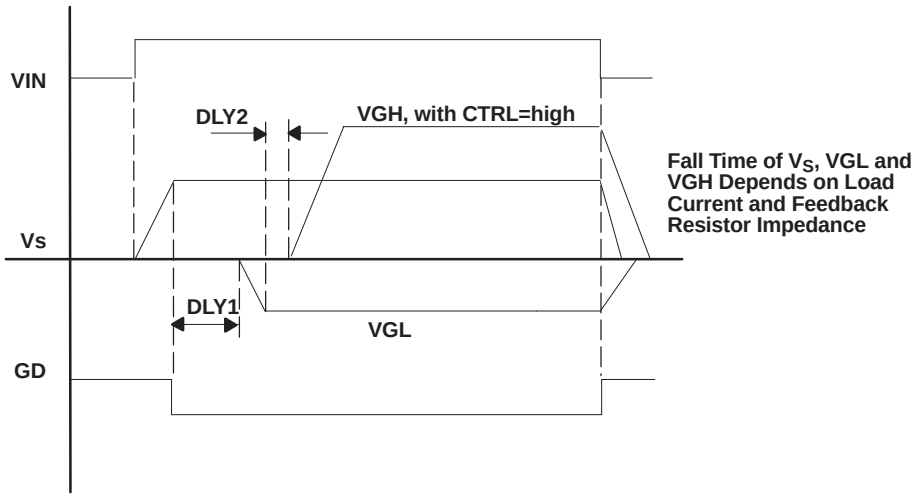


Figure 18. Power-On Sequencing With CTRL = High

Setting the Delay Times DLY1, DLY2

Connecting an external capacitor to the DLY1 and DLY2 pins sets the delay time. If no delay time is required, these pins can be left open. To set the delay time, a constant current source of typically 5 µA charges the external capacitor connected to DLY1 and DLY2. The delay time terminates when the capacitor voltage has reached the internal reference voltage of V_{REF} = 1.213 V. The calculation of the external delay capacitor is:

$$C_{dly} = \frac{5\ \mu A \times td}{V_{REF}} = \frac{5\ \mu A \times td}{1.213\ V} \quad \text{with td} = \text{Desired delay time} \tag{3}$$

Gate Drive, GD

A use of the gate drive pin can be to drive an external MOSFET, providing isolation for the main boost converter V_S. The gate drive is an open-drain output capable of sinking typically 500 µA. The gate drive latches low as soon as the main boost converter, V_S, reaches its power-good threshold. The gate drive signal goes high-impedance when the input voltage falls below the undervoltage lockout (UVLO) threshold or the device enters shutdown latch triggered by the fault delay.

VGH Switch and Gate Voltage Shaping, CPI – VGH

The gate-voltage shaping circuit reduces crosstalk between the LCD pixels by adjusting the fall time of the positive gate voltage, VGH. Connect the CTRL pin to V_{IN} if not using the gate-voltage shaping function. Implementation of this function is by adjusting the fall time of the gate voltage signal, VGH, generated by the positive charge pump. One can adjust the fall time with the external capacitor, C_{adj}, connected to the ADJ pin. The corresponding timing diagram is Figure 20.

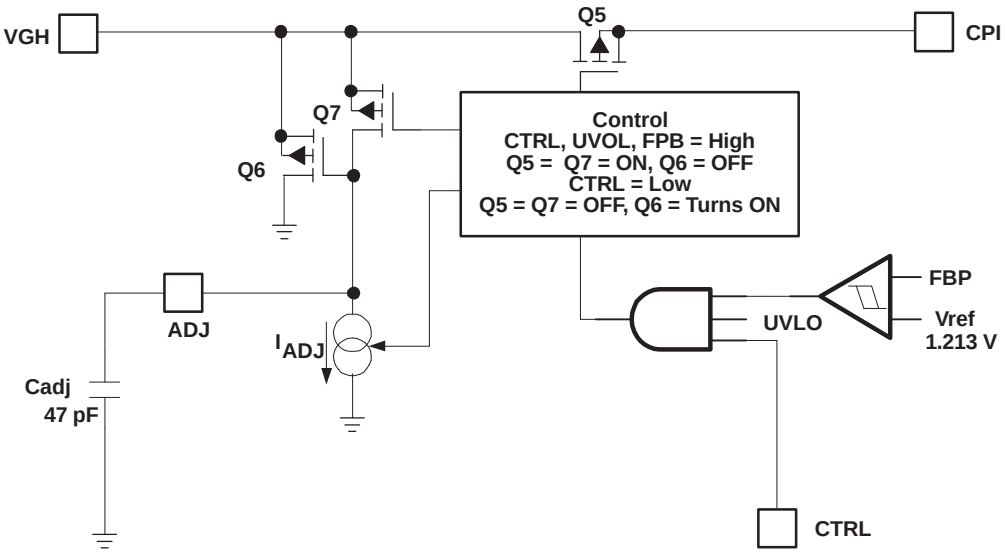


Figure 19. Implementation of the Gate-Voltage Shaping

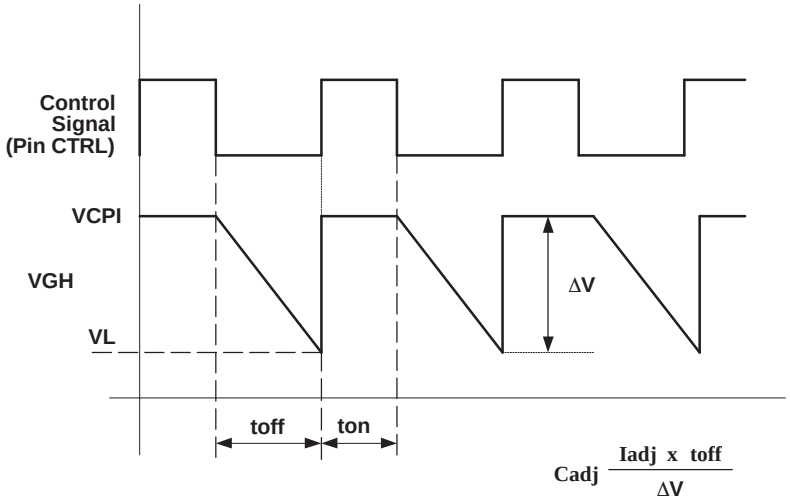


Figure 20. Timing Diagram of the Gate voltage shaping

The control signal applied to CTRL sets the timing of VGH. When CTRL is high, Q5 turns on and the positive charge pump voltage applied on CPI is present on VGH. At the same time, during the Q6 turnoff period, Q7 charges up the capacitor connected to ADJ to VGH. Taking CTRL low turns off Q5 and Q7, and Q6 slowly turns on as the discharge current I_{ADJ}, typically 200 µA, discharges the capacitor on ADJ. The capacitor value on C_{adj} determines the fall time of VGH. For a given off time (t_{off}), external capacitor C_{adj} determines the desired voltage drop, ΔV.

$$Cadj = \frac{Iadj \times toff}{\Delta V} \quad \text{with } Iadj = 200\ \mu A \tag{4}$$

When the input voltage falls below the undervoltage threshold (UVLO) or the device enters shutdown latch triggered by the fault delay timer, then Q5 disconnects VGH from CPI and is high-impedance.

Thermal Shutdown

A thermal shutdown prevents damage because of excessive heat and power dissipation. Typically, the thermal shutdown threshold is 155°C . On reaching this threshold, the device enters shutdown. One can enable the device enabled again by cycling the input voltage to GND.

VCOM Buffer

The VCOM buffer is a transconductance amplifier designed to drive capacitive loads. The IN pin is the input of the VCOM buffer. If there is no requirement for the VCOM buffer for certain applications, it is possible to shut down the VCOM buffer by connecting IN to ground, reducing the overall quiescent current. The VCOM buffer features a soft start, avoiding a large voltage drop at V_S during startup. Do not pull the VCOM buffer input, IN, dynamically to ground during operation.

Boost Converter Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency numbers from the provided efficiency curves, or use a worst-case assumption for the expected efficiency, for example 75%.

1. Duty Cycle : $$D = 1 - \frac{Vin \times \eta}{Vout} \quad (5)$$

2. Maximum output current : $$I_{out} = \left(Isw - \frac{Vin \times D}{2 \times fs \times L} \right) \times (1 - D) \quad (6)$$

3. Peak switch current : $$I_{swpeak} = \frac{Vin \times D}{2 \times fs \times L} + \frac{I_{out}}{1 - D} \quad (7)$$

with

I_{sw} = Converter switch current (minimum switch current limit = 2 A)

f_s = Converter switching frequency (typical 1.2 MHz)

L = Selected inductor value

η = Estimated converter efficiency (use the number from the efficiency plots, or 0.75 as an estimation)

The peak switch current is the steady-state peak switch current that the integrated switch, inductor, and external Schottky diode must be able to handle. Perform the calculation for the minimum input voltage, where the peak switch current is highest. For the calculation of the maximum current delivered by the boost converter, one must consider that the positive and negative charge pumps as well as the VCOM buffer run from the output of the boost converter.

Inductor Selection

Several inductors work with the TPS65150-Q1. Especially with external compensation, one can adjust the performance to the specific application requirements. The main parameter for the inductor selection is the inductor saturation current, which should be higher than the peak switch current as calculated previously, with additional margin to cover for heavy load transients. The alternative, more conservative approach, is to choose the inductor with a saturation current at least as high as the typical switch-current limit of 2.5 A. The second important parameter is the inductor dc resistance. Usually the lower the dc resistance the higher the efficiency. It is important to note that the inductor dc resistance is not the only parameter determining the efficiency. For a boost converter, where the inductor is the energy-storage element, the type and material of the inductor influences the efficiency as well. Especially at high switching frequencies of 1.2 MHz, inductor core losses, proximity effects, and skin effects become more important. Usually an inductor with a larger form factor gives higher efficiency. The efficiency difference between different inductors can vary between 2% to 10%. For the TPS65150-Q1, inductor values between 3.3 µH and 6.8 µH are a good choice, but other values can be used as well. Possible inductors are shown in Table 2.

Table 2. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	DIMENSIONS IN mm	Isat – DC Resistance
4.7 µH	Coilcraft DO1813P-472HC	8.89 × 6.1 × 5	2.6 A – 54 mΩ
4.2 µH	Sumida CDRH5D28 4R2	5.7 × 5.7 × 3	2.2 A – 23 mΩ
4.7 µH	Sumida CDC5D23 4R7	6 × 6 × 2.5	1.6 A – 48 mΩ
4.2 µH	Sumida CDRH6D12 4R2	6.5 × 6.5 × 1.5	1.8 A – 60 mΩ
3.9 µH	Sumida CDRH6D28 3R9	7 × 7 × 3	2.6 A – 20 mΩ

Table 2. Inductor Selection (continued)

INDUCTOR VALUE	COMPONENT SUPPLIER	DIMENSIONS IN mm	Isat – DC Resistance
3.3 µH	Sumida CDRH6D12 4R2	6.5 × 6.5 × 1.5	1.9 A – 50 mΩ

Output Capacitor Selection

For best output voltage filtering, TI recommends a low-ESR output capacitor. Ceramic capacitors have a low ESR value, but tantalum capacitors can be used as well, depending on the application. A 22-µF ceramic output capacitor works for most applications. Higher capacitor values can be used to improve the load transient regulation. See Table 3 for the selection of the output capacitor.

Input Capacitor Selection

For good input voltage filtering, low ESR ceramic capacitors are recommended. A 22-µF ceramic input capacitor is sufficient for most applications. For better input voltage filtering, this value can be increased. See Table 3, and *APPLICATION INFORMATION* for input capacitor recommendations.

Table 3. Input and Output Capacitor Selection

CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER	COMMENTS
22 µF, 1206	16 V	Taiyo Yuden EMK325BY226MM	C_{OUT}
22 µF, 1206	6.3 V	Taiyo Yuden JMK316BJ226	C_{IN}

Rectifier Diode Selection

To achieve high efficiency, use a Schottky diode. The reverse voltage rating should be higher than the maximum output voltage of the converter. Calculate the required average rectified forward current rating of the Schottky diode as the off-time of the converter times the maximum switch current of the TPS65150-Q1:

$$D = 1 - \frac{Vin}{Vout} \tag{8}$$

$$I_{avg} = (1 - D) \times Isw = \frac{Vin}{Vout} \times 2.0\ A \quad \text{with Isw = minimum switch current of the TPS65150 (2.0 A)} \tag{9}$$

Usually, a Schottky diode with 1-A maximum average rectified forward current rating is sufficient for most of the applications. Secondly, the Schottky rectifier must be able to dissipate the power. The dissipated power is the average rectified forward current times the diode forward voltage.

$P_D = I_{avg} \times VF = I_{sw} \times (1 - D) \times VF$ with I_{sw} = minimum switch current of the TPS65150-Q1 (2 A).

Typically, the diode should be able to dissipate 270 mW maximum depending on the load current and forward voltage. In terms of efficiency, the main parameters of the diode are the forward voltage and the reverse leakage current of the diode; both should be as low as possible.

Table 4. Rectifier Diode Selection

CURRENT RATING I_{avg}	Vr	$V_{forward}$	COMPONENT SUPPLIER
2 A	20 V	0.44 V at 2 A	SL22, Vishay Semiconductor
2 A	20 V	0.5 V at 2 A	SS22, Fairchild Semiconductor
1 A	30 V	0.44 V at 2 A	MBRS130L, Fairchild Semiconductor
1 A	20 V	0.45 V at 1 A	UPS120, Microsemi
1 A	20 V	0.45 V at 1 A	MBRM120, ON Semiconductor

Setting the Output Voltage

The external resistor divider sets the output voltage, calculated as:

$$V_{out} = 1.146\ V \times \left(1 + \frac{R1}{R2}\right) \tag{10}$$

To minimize quiescent current, use high-impedance feedback resistors. The upper feedback resistor R1 should not be larger than 1 MΩ. There is a requirement for a bypass capacitor across the upper resistor to speed up the circuit during load transients. Selection of the capacitor value is according to Table 5 and the Equation 11 as shown in the next section.

Compensation (COMP) and Feedforward Capacitor

One can compensate the regulator loop by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier. The compensation capacitor adjusts the low-frequency gain. Adding a resistor in series to it increases the high-frequency gain. The change in converter gain with the input voltage requires different compensation capacitors. Lower input voltages require a higher gain, and therefore a smaller compensation-capacitor value.

Table 5. Compensation Components for Different V_{IN} Voltages

V_{IN}	C_{COMP}	R_{COMP}	f_Z
2.5 V	470 pF	68 kΩ	8.8 kHz
3.3 V	470 pF	33 kΩ	7.8 kHz
5 V	2.2 nF	0 kΩ	11.2 kHz

The feedforward capacitor across the feedback resistor divider of the boost converter sets an additional zero at the frequency f_z to compensate the loop. Table 5 shows typical values for f_z , giving a feedforward capacitor value as calculated in Equation 11.

$$C_{FF} = \frac{1}{2 \times \pi \times f_Z \times R1} = \frac{1}{2 \times \pi \times 8.8\ kHz \times R1} \quad (11)$$

Please see the typical application circuits at the end of the datasheet for detailed circuit configurations and values.

Layout Consideration

The PCB layout is an important step in the power-supply design. An incorrect layout could cause converter instability, load regulation problems, noise, and EMI issues. Especially with a switching DC-DC converter at high load currents, too-thin PCB traces can cause significant voltage spikes. Good grounding becomes important as well. If possible, TI recommends a common ground plane to minimize ground shifts between analog (GND) and power ground (PGND). Additionally, the following PCB design layout guidelines are recommended for the TPS65150-Q1:

1. Boost converter output capacitor, input capacitor and power ground (PGND) should form a star ground or should be directly connected together on a common power ground plane.
2. Place the input capacitor directly from the input pin (VIN) to ground.
3. Use a bold PCB trace to connect SUP to the output V_S.
4. Place a small baypass capacitor from the SUP pin to ground.
5. Use short traces for the charge-pump drive pins (DRVN, DRVP) of VGH and VGL because these traces carry switching currents.
6. Place the charge pump flying capacitors as close as possible to the DRVP and DRVN pins, avoiding high voltage spikes at these pins.
7. Place the Schottky diodes as close as possible to the IC, respectively to the flying capacitors connected to DRVP and DRVN.
8. Carefully route the charge pump traces to avoid interference with other circuits, because they carry high voltage switching currents.
9. Place the output capacitor of the VCOM buffer as close as possible to the output pin (VCOM).
10. Solder the thermal pad of the TSSOP package to the PCB for improved thermal performance.

APPLICATION INFORMATION

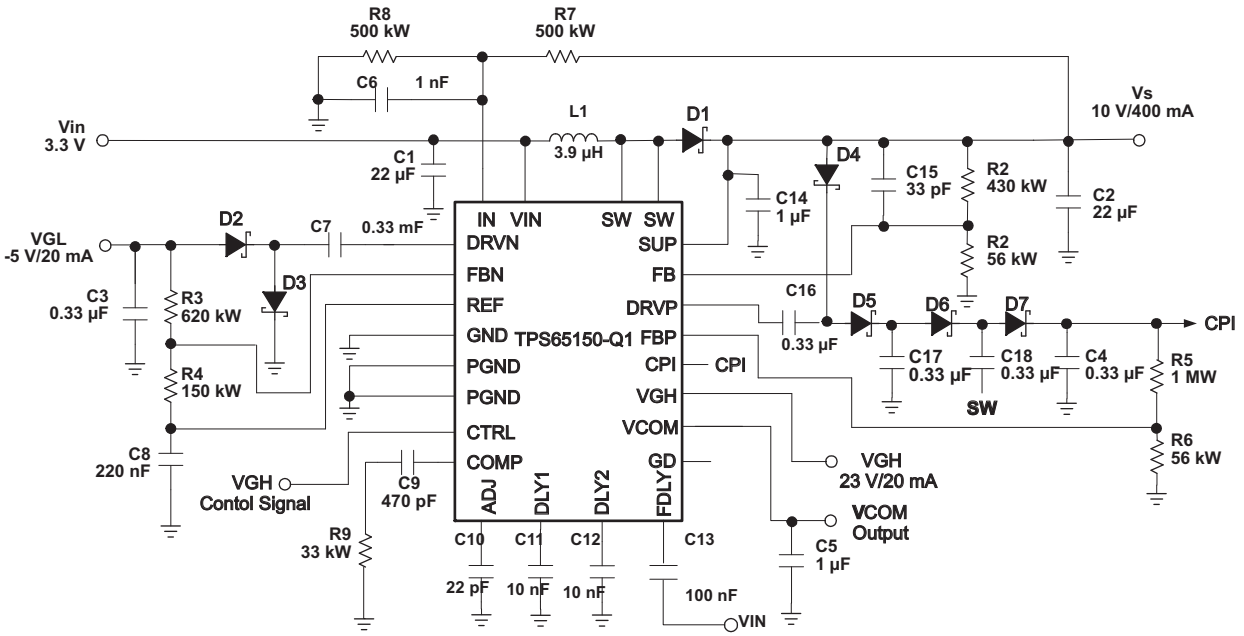


Figure 21. Notebook LCD Supply Powered From a 3.3-V Rail

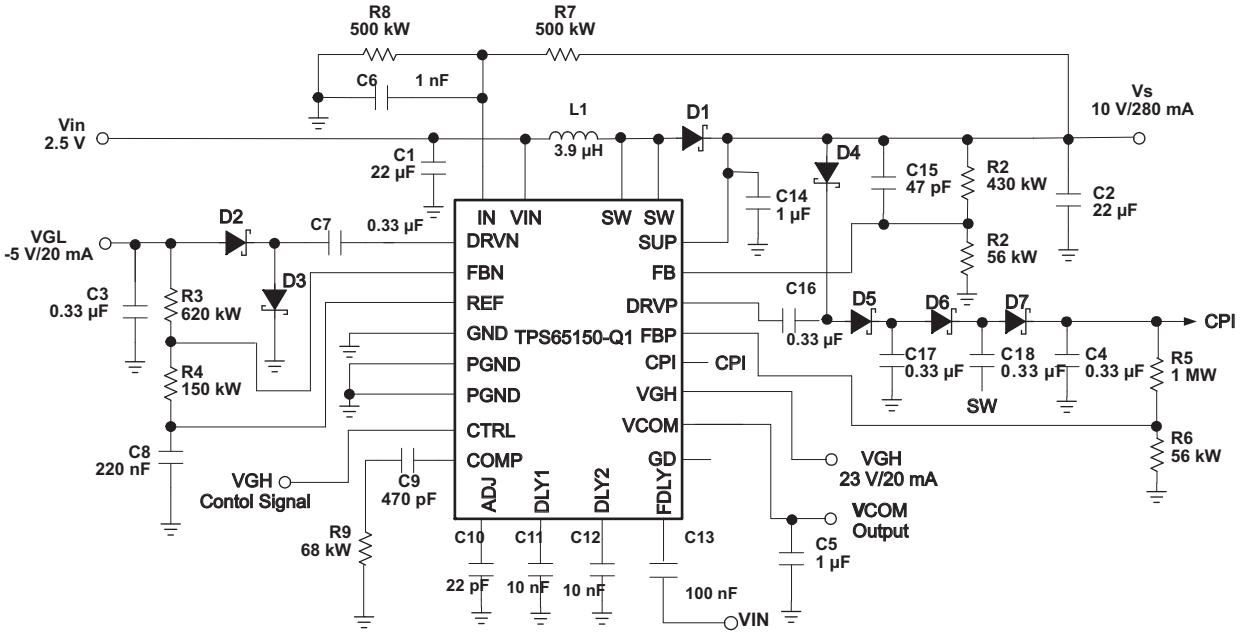


Figure 22. Notebook LCD Supply Powered From a 2.5-V Rail

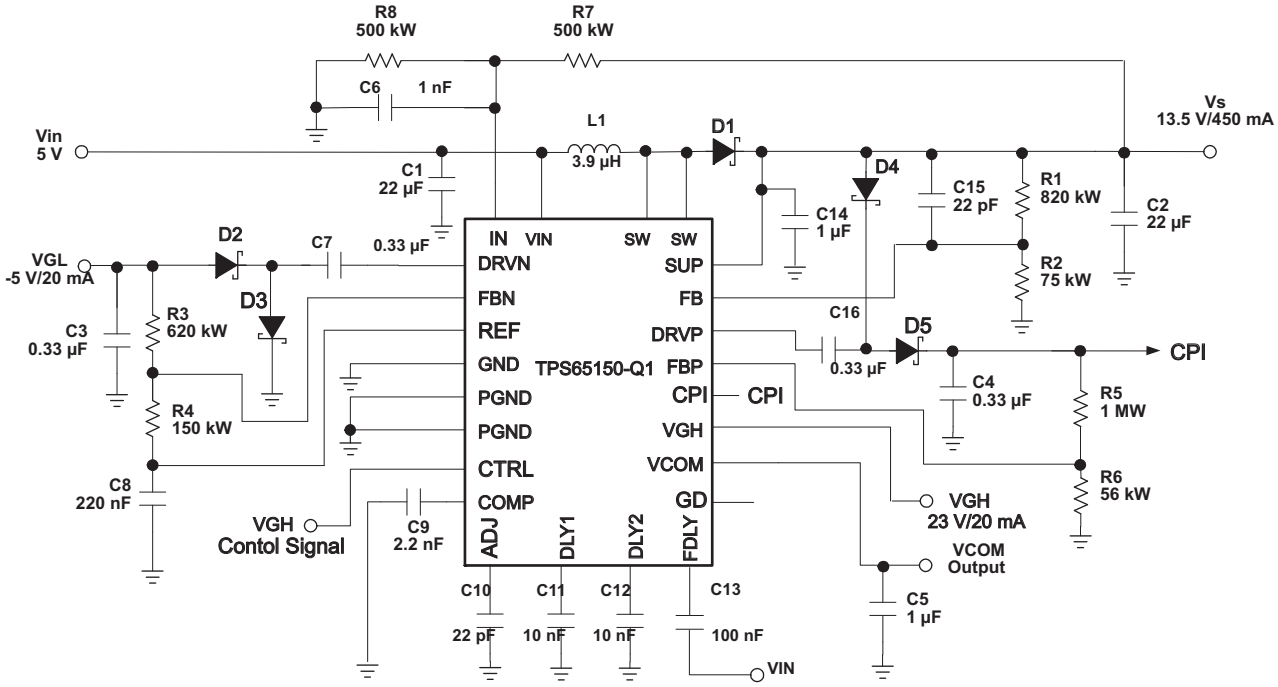


Figure 23. Monitor LCD Supply Powered From a 5-V Rail

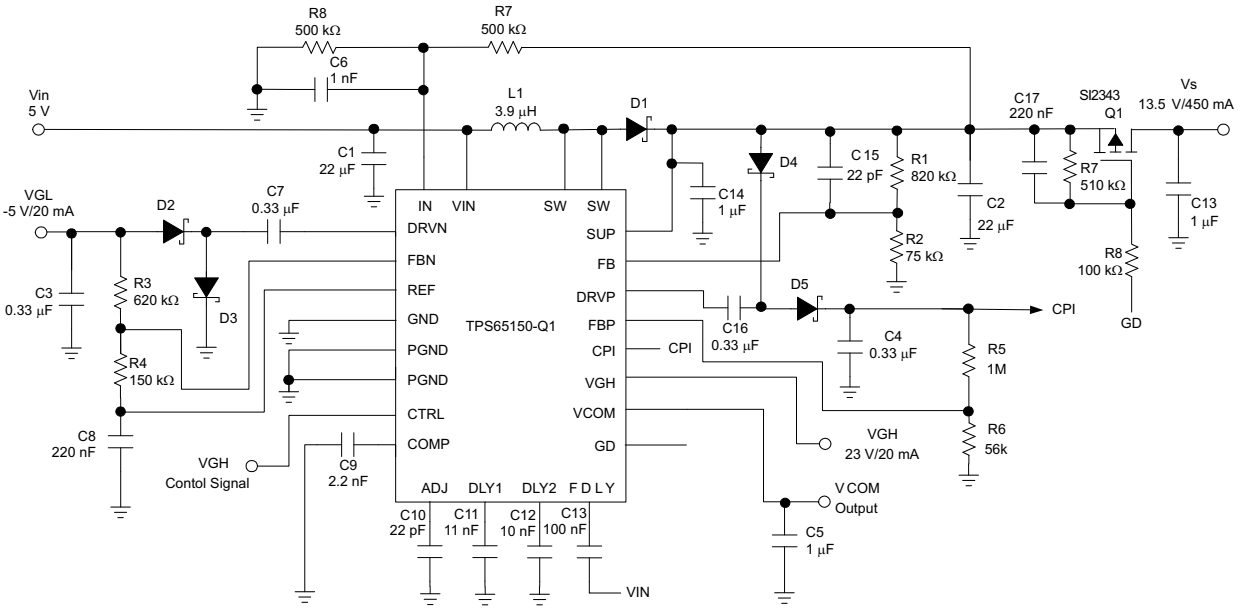


Figure 24. Typical Isolation and Short-Circuit Protection Switch for V_S Using Q1 and Gate Drive Signal (GD)

REVISION HISTORY

Changes from Original (June 2013) to Revision A	Page
• Changed document status from *Product Preview* to *Production Data*	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65150QPWPRQ1	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS65150Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

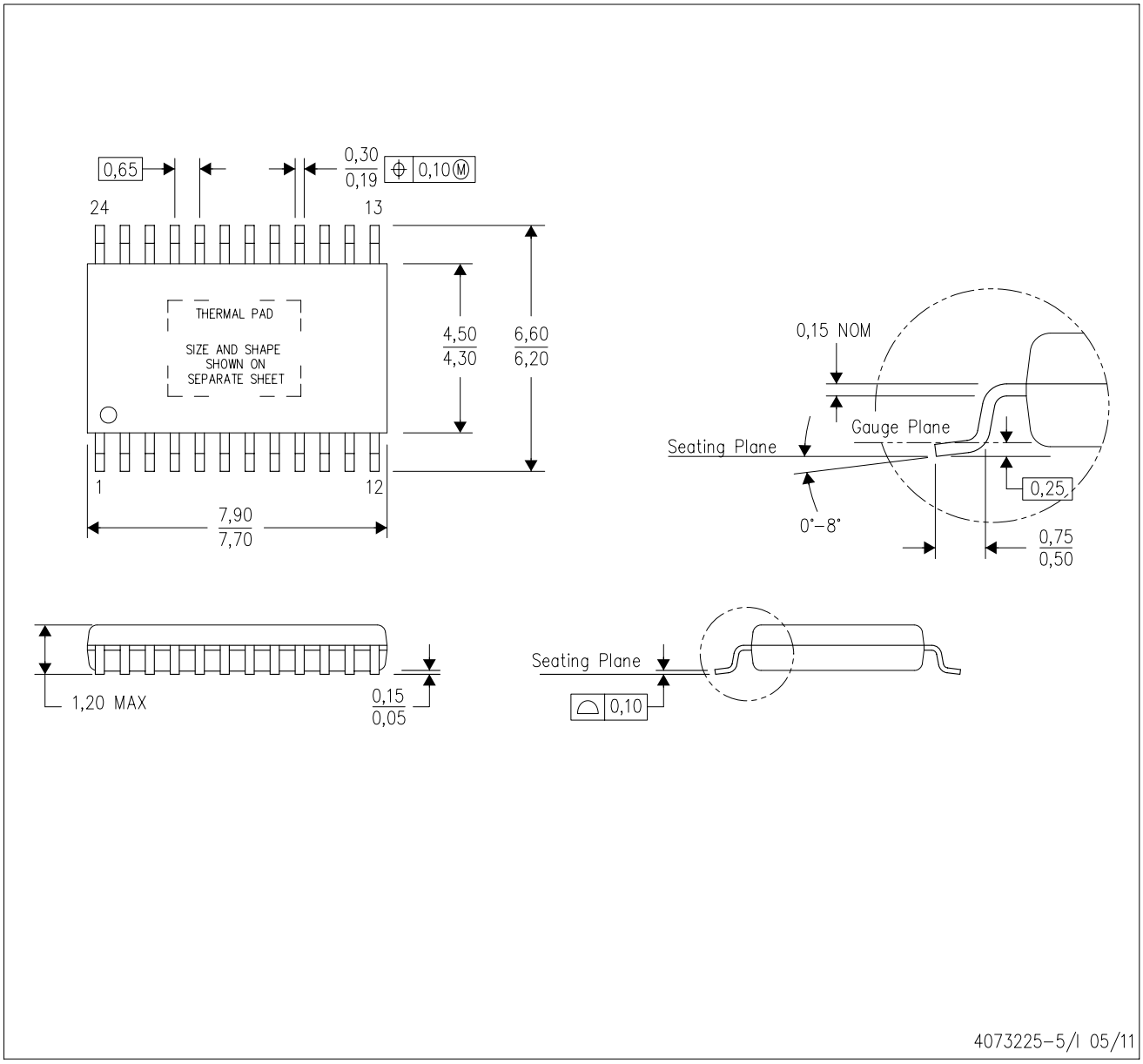
OTHER QUALIFIED VERSIONS OF TPS65150-Q1 :

- Catalog: TPS65150

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

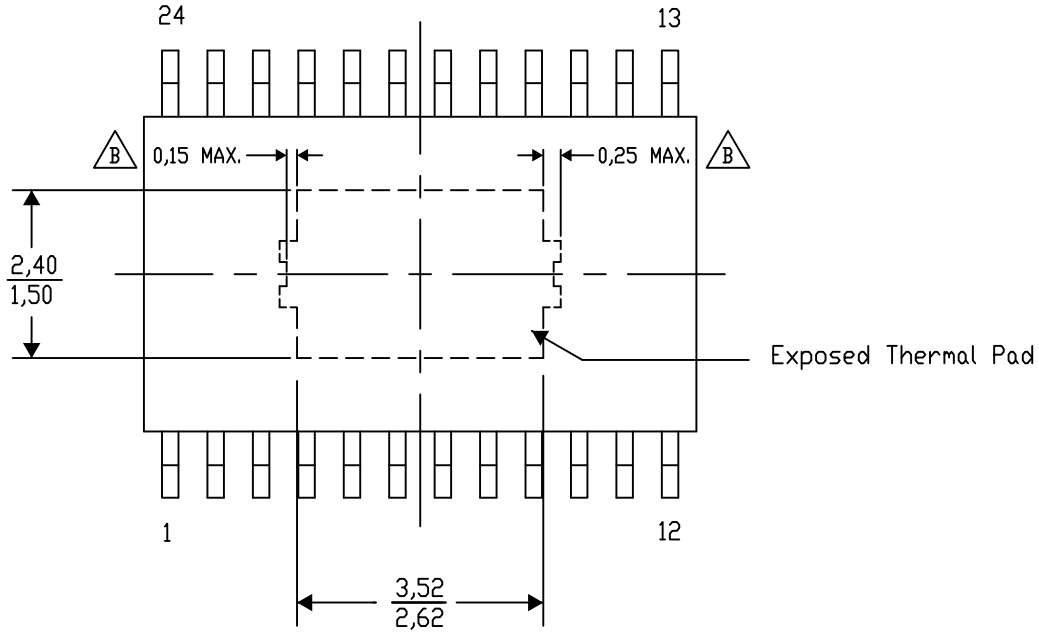
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–30/AG 08/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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