4 Ω, 360 MHz, Dual SPST Analog Switches

DESCRIPTION

The DG3537, DG3538, DG3539, DG3540 are dual SPST analog switches which operate from 1.8 V to 5.5 V single rail power supply. They are design for audio, video, and USB switching applications.

The devices have 4 Ω on-resistance and 360 MHz 3 dB bandwidth. 0.2 Ω on-resistance matching and 1 Ω flatness make the device high linearity. The devices are 1.6 V logic compatible within the full operation voltage range.

These switches are built on a sub-micron high density process that brings low power consumption and low voltage performance.

The switches are packaged in MICRO FOOT chip scale package of 3 x 3 bump array.

As a committed partner to the community and environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For MICRO FOOT analog switch products manufactured with tin/silver/copper (SnAgCu) device termination, the lead (Pb)-free "-E1" suffix is being used as a designator.

FEATURES

- 1.8 V to 5.5 V operation
- 3 Ω at 2.7 V R_{ON}
- 360 MHz - 3 dB bandwidth
- ESD method 3015.7 > 2 kV
- Latch-up current 0.300 mA (JESD 78)
- 1.6 V logic compatible

Pb-free
RoHS COMPLIANT

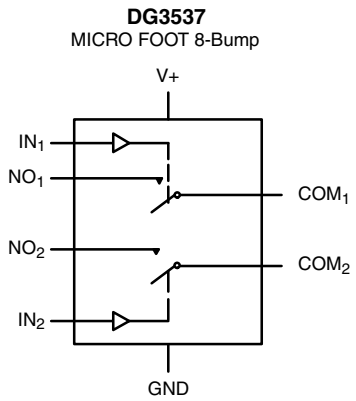
BENEFITS

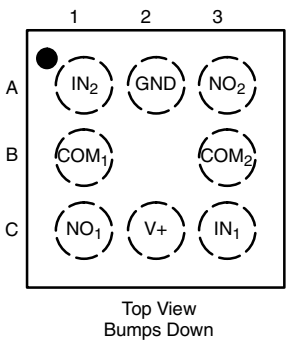
- Space saving MICRO FOOT® package
- High linearity
- Low power consumption
- High bandwidth
- Full rail Signal swing range

APPLICATIONS

- Cellular phones
- MP3
- Media players
- Modems
- Hard drives
- PCMCIA

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



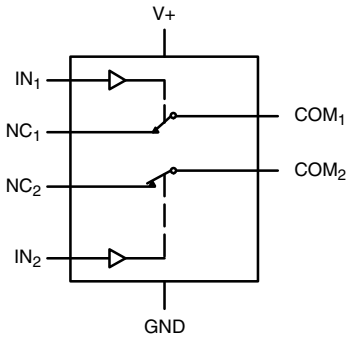


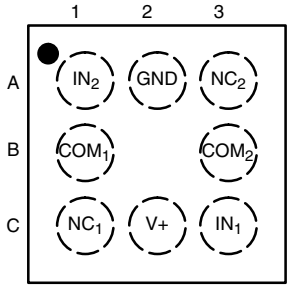
Top View
Bumps Down

3537 = Device Marking
xxx = Data/Lot Traceability Code

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

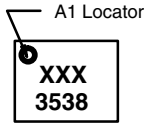
DG3538
MICRO FOOT 8-Bump





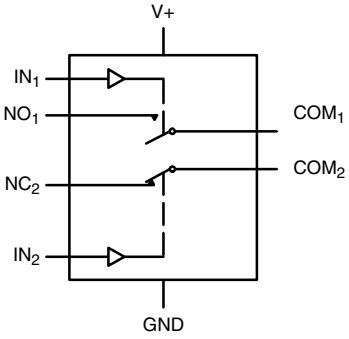
Top View
Bumps Down

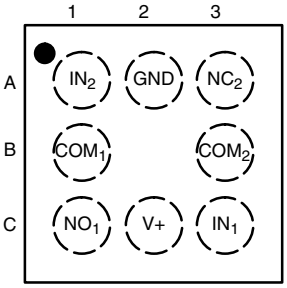
Device Marking



3538 = Device Marking
xxx = Data/Lot Traceability Code

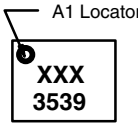
DG3539
MICRO FOOT 8-Bump





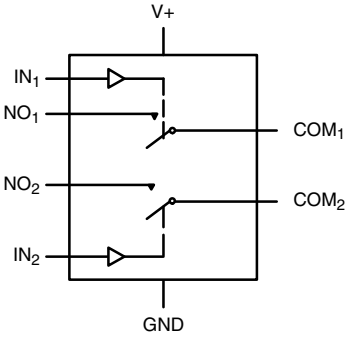
Top View
Bumps Down

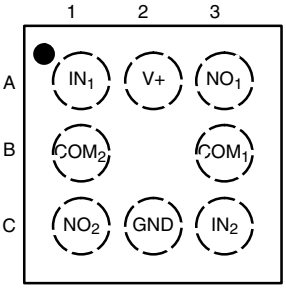
Device Marking



3539 = Device Marking
xxx = Data/Lot Traceability Code

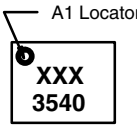
DG3540
MICRO FOOT 8-Bump





Top View
Bumps Down

Device Marking



3540 = Device Marking
xxx = Data/Lot Traceability Code

TRUTH TABLE

Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp. Range	Package	Part Number
- 40 °C to 85 °C	MICRO FOOT: 8 Bump (3 x 3, 0.5 mm Pitch, 238 µm Bump Height)	DG3537DB-T5-E1 DG3538DB-T5-E1 DG3539DB-T5-E1 DG3540DB-T1-E1

ABSOLUTE MAXIMUM RATINGS			
Parameter		**Limit**	**Unit**
Reference V+ to GND		- 0.3 to + 6	V
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3 V)	
Continuous Current (NO, NC, COM)		± 100	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage Temperature	(D Suffix)	- 65 to 150	°C
Package Solder Reflow Conditions[b]	IR/Convection	250	
ESD per Method 3015.7		> 2	kV
Power Dissipation (Packages)[c]	MICRO FOOT: 8 Bump (3 x 3 mm)[d]	400	mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. Refer to IPC/JEDEC (J-STD-020B)
c. All bumps welded or soldered to PC Board.
d. Derate 5.0 mW/°C above 70 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

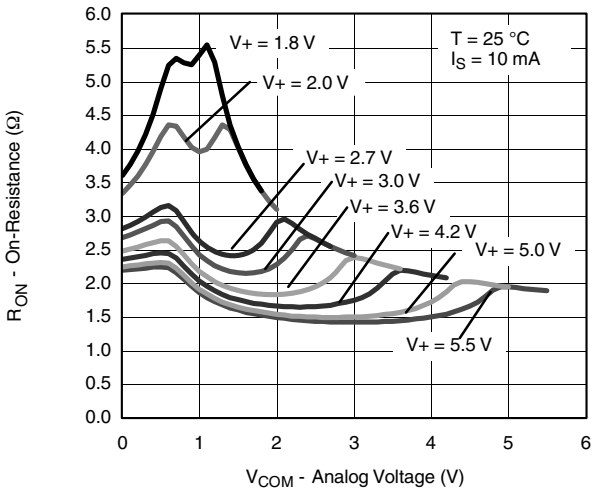
SPECIFICATIONS (V+ = 3 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 2.7 to 3.6 V, V_{IN} = 0.5 V or 1.4 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance[d]	R_{ON}	V+ = 2.7 V, V_{COM} = 0.2/1.5 V, I_{NO}, I_{NC} = 10 mA	Room Full		3	4 4.3	Ω
R_{ON} Flatness[d]	R_{ON} Flatness		Room		0.75	1.2	
On-Resistance Match Between Channels[d]	$\Delta R_{DS(on)}$		Room			0.25	
Switch Off Leakage Current[f]	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.6 V, V_{NO}, V_{NC} = 0.3 V/3.3 V, V_{COM} = 3.3 V/0.3 V	Room Full	- 2 - 20		2 20	nA
	$I_{COM(off)}$		Room Full	- 2 - 20		2 20	
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 3.6 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3.3 V	Room Full	- 2 - 20		2 20	
Digital Control							
Input High Voltage[d]	V_{INH}		Full	1.4			V
Input Low Voltage	V_{INL}		Full			0.5	
Input Capacitance	C_{in}		Full		8		pF
Input Current[f]	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	1		1	µA

SPECIFICATIONS (V+ = 3 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 2.7 to 3.6 V, V_{IN} = 0.5 V or 1.4 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Dynamic Characteristics							
Turn-On Time	t_{ON}	V+ = 2.7 V, V_{NO} or V_{NC} = 1.5 V R_L = 300 Ω, C_L = 35 pF	Room Full		16	46 48	ns
Turn-Off Time	t_{OFF}		Room Full		7	37 39	
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 2 V, R_{GEN} = 0 Ω	Room		1		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 78.5		dB
Crosstalk[d]	X_{TALK}		Room		- 113		
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz	Room		- 58		
Crosstalk[d]	X_{TALK}		Room		- 66		
Off Capacitance[d]	$C_{NO/NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		8		pF
	$C_{COM(off)}$		Room		14		
Channel-On Capacitance[d]	$C_{NO/NC(on)}$		Room		27		
	$C_{COM(on)}$		Room		27		
Power Supply							
Power Supply Current	I+	V_{IN} = 0 or V+	Room Full		0.001	1.0 1.0	µA

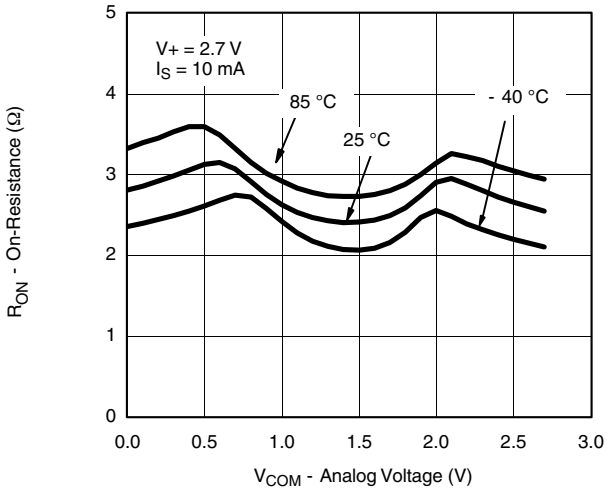
SPECIFICATIONS (V+ = 5 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 4.2 to 5.5 V, V_{IN} = 0.8 V or 2.0 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C** Min.[b]	Typ.[c]	Max.[b]	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance[d]	R_{ON}	V+ = 4.2 V, V_{COM} = 0.5/3.5 V, I_{NO}, I_{NC} = 10 mA	Room Full		2.6	3.5 3.7	Ω
r_{ON} Flatness[d]	R_{ON} Flatness		Room		0.8	1.2	
On-Resistance Match Between Channels[d]	$\Delta R_{DS(on)}$		Room			0.2	
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 5.5 V, V_{NO}, V_{NC} = 1.0 V/4.5 V, V_{COM} = 4.5 V/1.0 V	Room Full	- 2 - 20		2 20	nA
	$I_{COM(off)}$		Room Full	- 2 - 20		2 20	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 5.5 V, V_{NO}, V_{NC} = V_{COM} = 1.0 V/4.5 V	Room Full	- 2 - 20		2 20	
Digital Control							
Input High Voltage[d]	V_{INH}		Full	2.0			V
Input Low Voltage	V_{INL}		Full			0.8	
Input Capacitance	C_{in}		Full		8		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V+ = 4.2 V, V_{NO} or V_{NC} = 3.0 V, R_L = 300 Ω, C_L = 35 pF	Room Full		11	41 43	ns
Turn-Off Time	t_{OFF}		Room Full		7	37 39	
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 2 V, R_{GEN} = 0 Ω	Room		1		pC
Off Capacitance[d]	$C_{NO/NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		8		pF
	$C_{COM(off)}$		Room		14		
Channel-On Capacitance[d]	$C_{NO/NC(on)}$		Room		28		
	$C_{COM(on)}$		Room		28		
Power Supply							
Power Supply Current	I+	V_{IN} = 0 or V+	Room Full		0.001	1.0 1.0	µA

Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5 V leakage testing, not production tested.

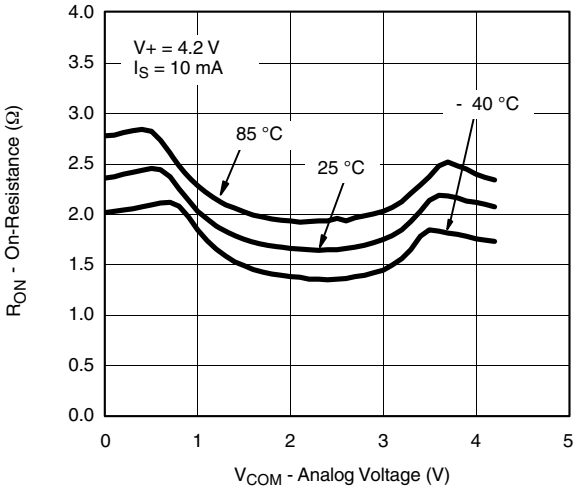
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



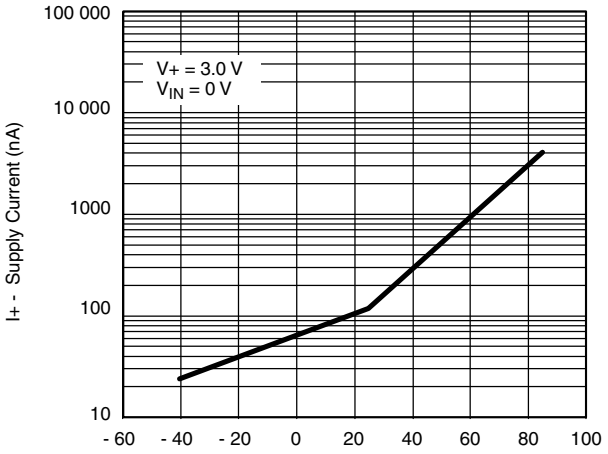
R_{ON} vs. V_{COM} and Supply Voltage



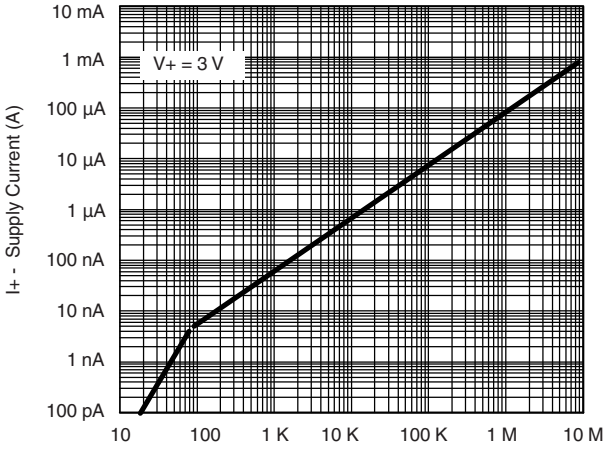
R_{ON} vs. Analog Voltage and Temperature



R_{ON} vs. Analog Voltage and Temperature

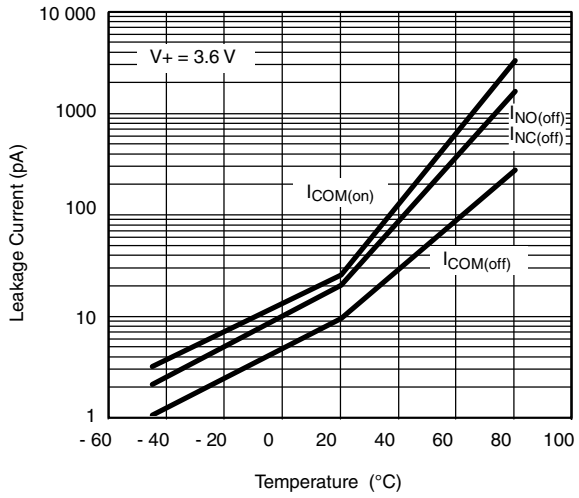


Supply Current vs. Temperature

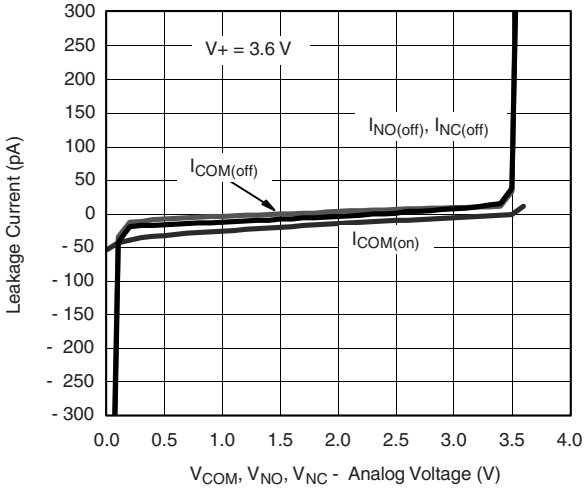


Supply Current vs. Input Switching Frequency

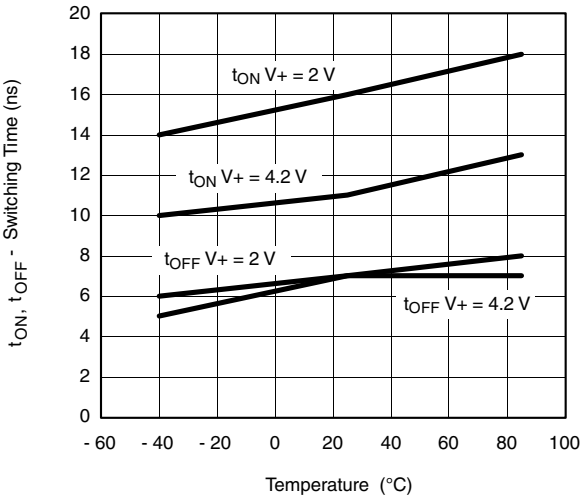
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



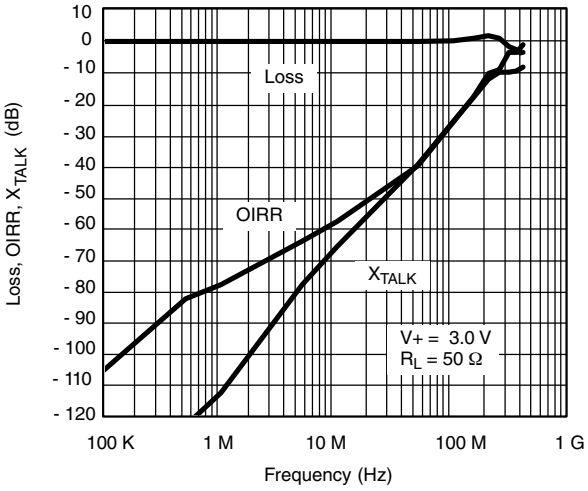
Leakage Current vs. Temperature



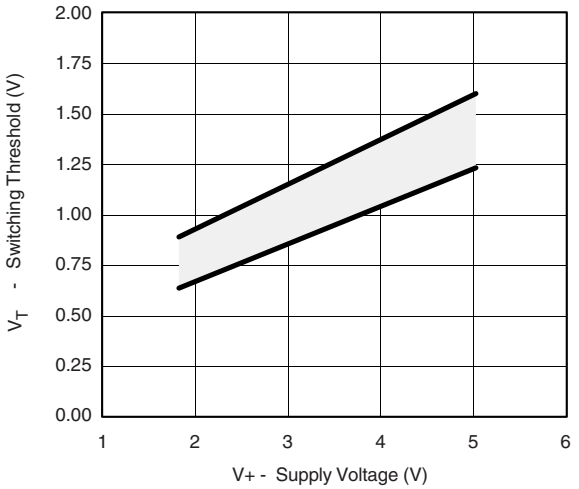
Leakage vs. Analog Voltage



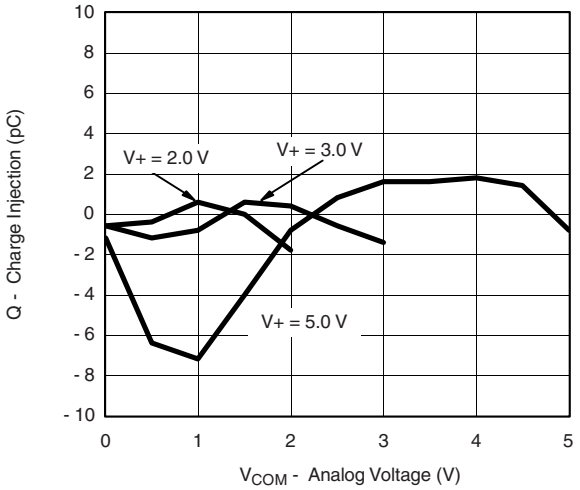
Switching Time vs. Temperature



Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

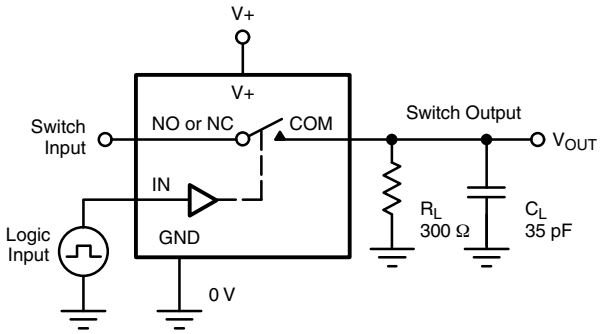


Switching Threshold vs. Supply Voltage



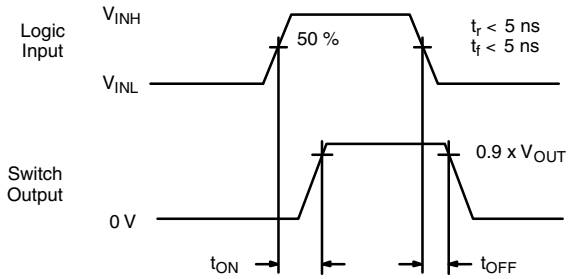
Charge Injection vs. Analog Voltage

TEST CIRCUITS



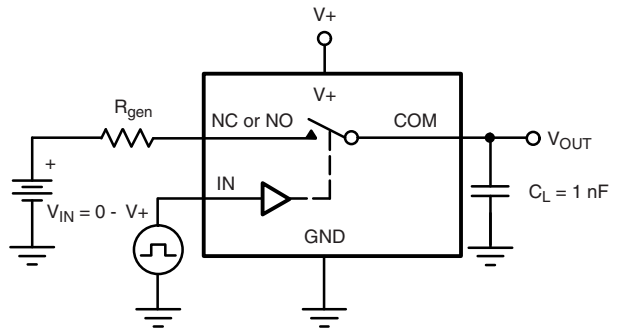
C_L (includes fixture and stray capacitance)

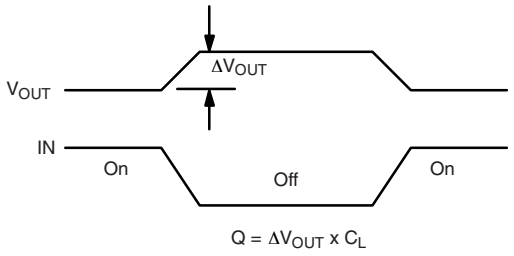
$$V_{OUT} = V_{NOorNC}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

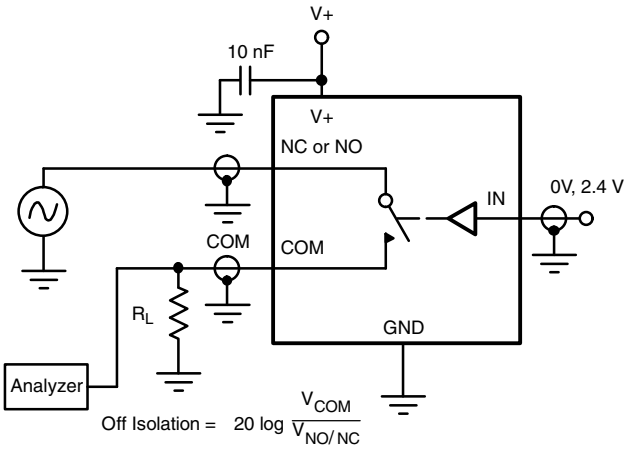




$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 2. Charge Injection



Off Isolation = $20 \log \frac{V_{COM}}{V_{NO/NC}}$

Figure 3. Off-Isolation

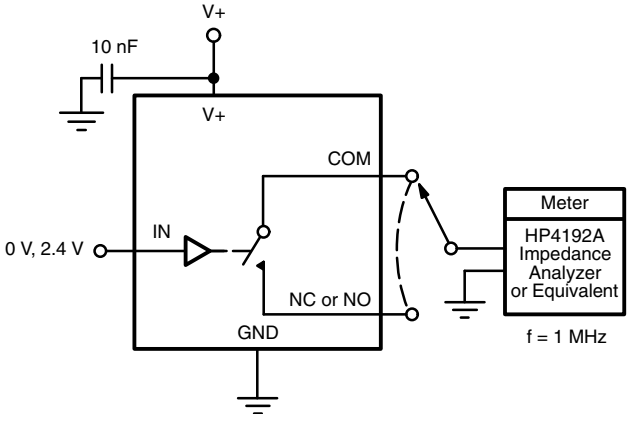
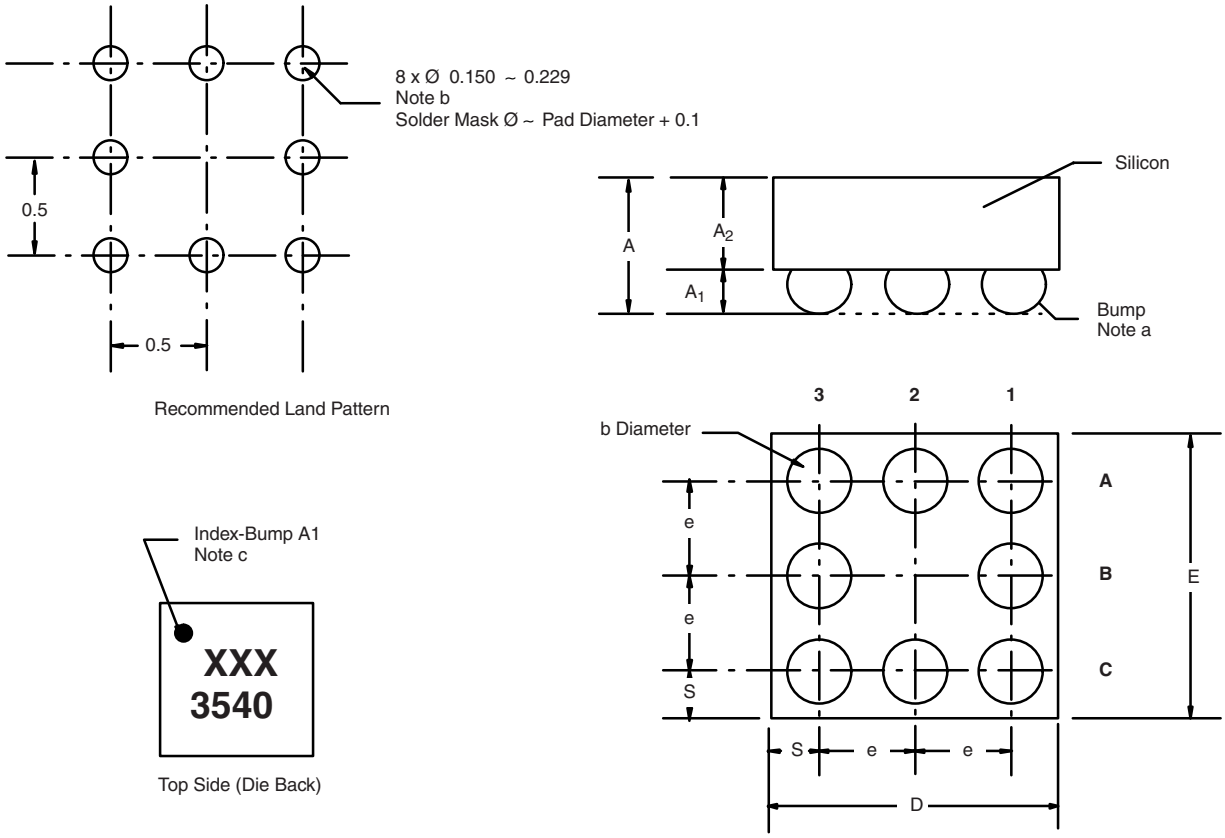


Figure 4. Channel Off/On Capacitance

PACKAGE OUTLINE

MICRO FOOT: 8 BUMP (3 x 3, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)



Notes (Unless Otherwise Specified):
a. Bump is Lead (Pb)-free Sn/Ag/Cu.
b. Non-solder mask defined copper landing pad.
c. Laser Mark on silicon die back; back-lapped, no coating. Shown is not actual marking; sample only.

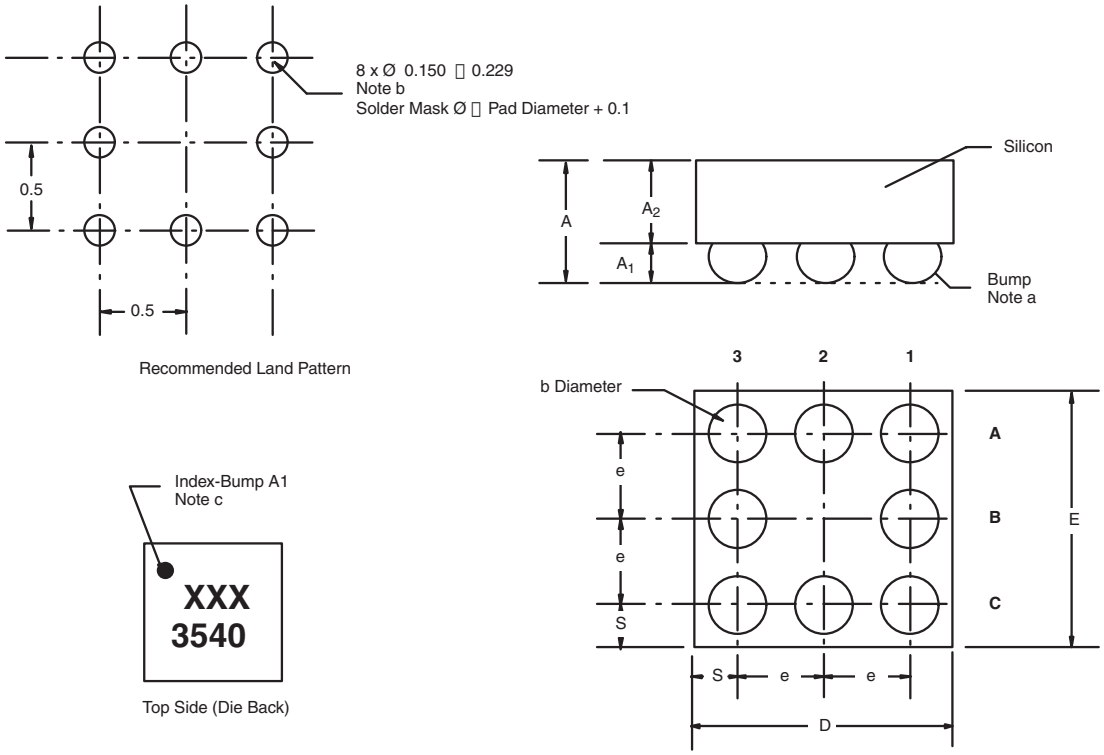
Dim.	Millimeters[a]		Inches	
	Min.	Max.	Min.	Max.
A	0.688	0.753	0.0271	0.0296
A_1	0.218	0.258	0.0086	0.0102
A_2	0.470	0.495	0.0185	0.0195
b	0.306	0.346	0.0120	0.0136
D	1.480	1.520	0.0583	0.0598
E	1.480	1.520	0.0583	0.0598
e	0.5 BASIC		0.0197 BASIC	
S	0.230	0.270	0.0091	0.0106

Notes:

a. Use millimeters as the primary measurement.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73320.

MICRO FOOT: 8-BUMP (3 mm x 3 mm, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)



Notes

(unless otherwise specified)

a. Bump is lead (Pb)-free Sn/Ag/Cu.

b. Non-solder mask defined copper landing pad.

c. Laser mark on silicon die back; back-lapped, no coating. Shown is not actual marking; sample only.

DIM.	MILLIMETERS[a]		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.688	0.753	0.0271	0.0296
A_1	0.218	0.258	0.0086	0.0102
A_2	0.470	0.495	0.0185	0.0195
b	0.306	0.346	0.0120	0.0136
D	1.480	1.520	0.0583	0.0598
E	1.480	1.520	0.0583	0.0598
e	0.5 BASIC		0.0197 BASIC	
S	0.230	0.270	0.0091	0.0106

Note

a. Use millimeters as the primary measurement.

ECN: S11-1065-Rev. A, 13-Jun-11
DWG: 6002

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AMEYA360
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Website :

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Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com