

TMS320C6474

Mezzanine EVM Board

***Technical
Reference***

**TMS320C6474
Mezzanine EVM Board
Technical Reference**

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About This Manual

This document describes the board level operations of the TMS320C6474 DSP Mezzanine EVM Board. The board is based on the Texas Instruments TMS320C6474 Digital Signal Processor.

The TMS320C6474 Mezzanine EVM Board is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320C6474 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320C6474 Mezzanine Board will sometimes be referred to as the EVM, C6474 EVM, or TMS320C6474 EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320C64xx DSP CPU Reference Guide
Texas Instruments TMS320C64xx DSP Peripherals Reference Guide

Table 1: Manual History

Revision	History
A	Initial Release

Chapter 1

Overview of the TMS320C6474 Evaluation Module

Chapter One provides an overview description of the TMS320C6474 Evaluation Module along with the key features and a block diagram of the evaluation platform.

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1.1 Key Features

The C6474 Evaluation Module (EVM) is a high performance standalone development platform that enables users to evaluate and develop applications for the TI C64xx DSP family. The EVM also serves as a hardware reference design for the TMS320C6474 DSP. The EVM is an AMCC type double width Mezzanine board.

The dual DSPs on the C6474 Mezzanine Board interface to on-board peripherals dedicated I/O pins or SRIO interface connector. The DDR2 memory is on its own dedicated EMIF.

The EVM has a 100/1000 mbit Phy which is connected to the DSP's on board EMAC.

The board is powered by +12 volts delivered via the AMCC connector. On-board switching voltage regulators provide the DSP core voltage, 1.1V for I/O, 1.5V for RGMII, 1.8V for DDR, and 3.3V I/O supplies. The board is held in reset until these supplies are within operating specifications.

Code Composer communicates with the Mezzanine Board via the mini-USB connector to the embedded JTAG emulator on the EVM. The Mezzanine board can also be used with an external emulator through the external 14 or 60 pin JTAG connectors.

Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

The key features of the of the C6474 EVM include:

- Two (2) Texas Instruments TMS320C6474 DSPs operating at 1 Ghz. (6 cores, 3 per device)
- 128 Mbytes of DDR2 memory for each processor
- 10/100/1000 MBPs multi-channel ethernet interface
- I²C Serial ROM for boot loading each processor
- 4 user accessible LEDs per processor
- Software board configuration through registers implemented in CPLD and I²C ROM
- Auto-Configured boot options and clock input selection
- Standard AMCC expansion connectors for use as a daughter card
- On-board JTAG emulator with USB host interface
- Single voltage power supply (+12V)

1.2 Functional Overview of the TMS320C6474 EVM

The EVM Platform is a double wide AMCC expansion board. The board has two Texas Instruments C6474 DSPs running at 1 Ghz. The figure below is a block diagram of the TMS320C6474 EVM.

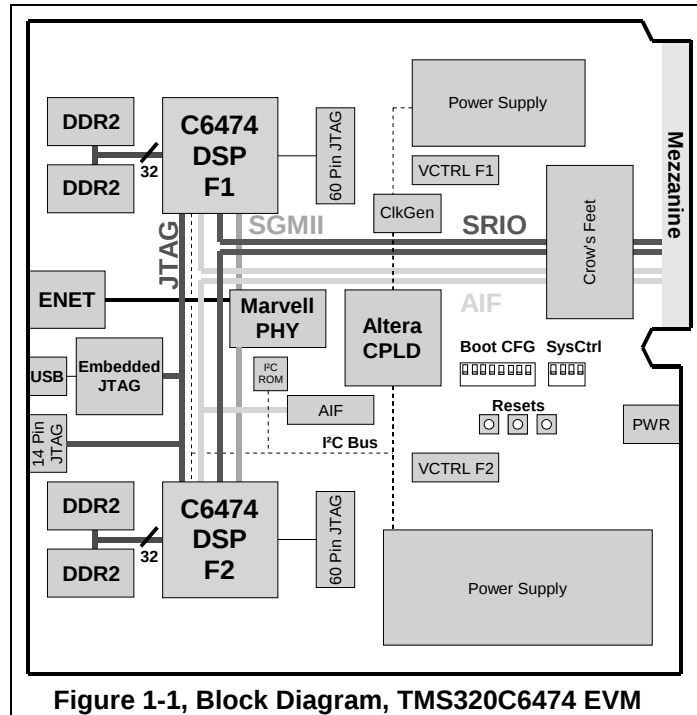


Figure 1-1, Block Diagram, TMS320C6474 EVM

1.3 Basic Operation

The EVM Platform is designed to work with TI's Code Composer Studio development environment and ships with a version specifically tailored to work with the board. Code Composer communicates with the board through the on-board JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

After the install is complete, follow these steps to run Code Composer. The EVM board must be fully connected to launch the EVM version of Code Composer.

- 1) Connect the included power supply to the EVM board.
- 2) Connect the EVM to your PC with a standard USB cable (also included).
- 3) Launch Code Composer from its icon on your desktop.

Detailed information about the EVM including examples and reference material is available on the EVM's included compact disc.

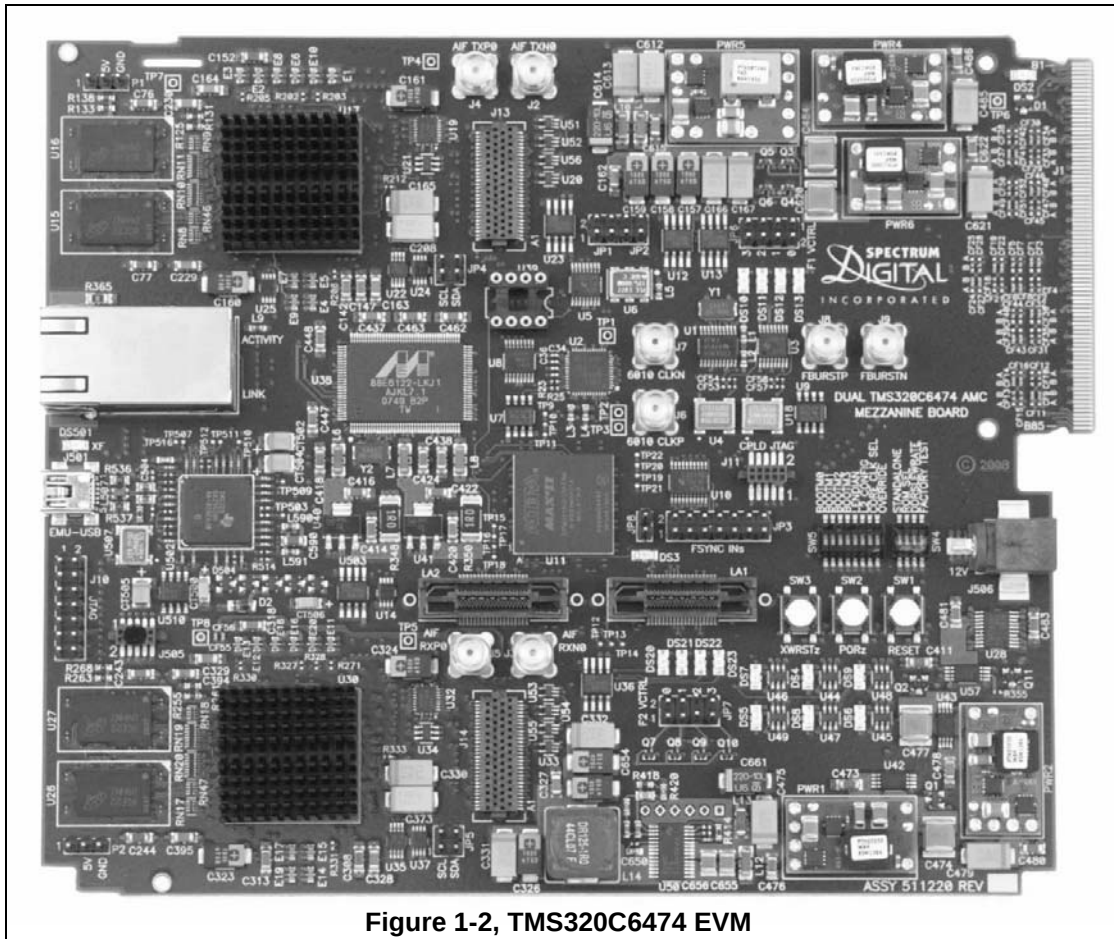


Figure 1-2, TMS320C6474 EVM

1.4 Configuration Switch Settings

The configuration switch settings for the EVM platform are discussed in chapter 2. The EVM has one set of 8 and one set of 4 configuration switches that allow users to control the operational state of the DSP when it is released from reset. The configuration switch blocks are labeled SW4 and SW5 on the EVM board. These switches are located next to the reset switch.

1.5 Power Supply

The EVM operates from a single +12V external power supply connected to the main power input (J5). Internally, the +12V input is converted into +5V, +3.3V, +2.5V, +1.8V, +1.1V and 2 core voltages for the DSPs using multiple voltage regulators. The core voltage supply incorporates smart reflex technology and is used for the DSP core while the +3.3V supply is used for the support circuitry and other chips on the board. The +2.5 volts is used to operate the Maxell ethernet Phy. The +1.1 volt supply operates DSP peripherals. The +1.8 volt supply is used to support DDR2 memories. The power connector is a 2.5mm barrel-type plug.

Chapter 2

Introduction to the TMS320C6474 EVM Mezzanine Board

Chapter five provides a description of the TMS320C6474 Mezzanine EVM Board along with the key features and a block diagram of the circuit board.

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2.1 Memory Map

The C64xx family of DSPs has a large byte addressable address space. Program code and data can be placed anywhere in the unified address space. Addresses are always 32-bits wide.

The memory map shows the address space of a C6474 EVM. By default, the internal memory sits at the lower section of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

Note that each device has 3 cores and can access the on chip peripherals.

Address	
0x00000000	
0x00800000	L2 SRAM
0x00900000	Reserved Space or Peripheral Regs or L2 SRAM
0x80000000	DDR2 RAM
0xA0000000	AIF Data
0xB0000000	Reserved
0xF0000000	

Figure 2-1, Memory Map, C6474 Mezzanine EVM Board

2.2 EVM Configuration and Configuration Switch Settings

Note

Both C6474 devices operate in the same boot mode configuration on the EVM.

The C6474 EVM has two I²C configuration EEPROMs and two configuration switches, SW4, and SW5.

The two I²C configuration EEPROMs known as factory I²C configuration EEPROM and user I²C configuration EEPROM.

The factory I²C configuration EEPROM is write protected and can not be changed, the user I²C configuration EEPROM is mapped to C6474 CPU1 and can be over written.

At RESET the embedded control processor samples the configuration switches SW4, and SW5 and determines if the factory I²C configuration EEPROM in conjunction with configuration switches are used to configure the on board C6474 devices, or if the user I²C configuration EEPROM in conjunction with configuration switches configures the EVM.

Switch SW5 controls general boot parameters, whereas SW4 determines general control parameters such as if the board is used in stand alone mode or which I²C configuration EEPROM is used.

If SW4 ROMSEL is ON the user configuration EEPROM is selected. If the SW4 ROMSEL is OFF the factory configuration switch is selected.

The user I²C configuration EEPROM as shipped, contains the exact same defaults as the factory I²C configuration EEPROM. The factory shipped configuration uses the factory configuration EEPROM with the defaults over written via SW5, (OVERRIDE=OFF). The exact same configuration could be duplicated by enabling the user I²C configuration on SW4, ROM_SEL switch.

Anytime a parameter on SW5 is selected the override position MUST be selected to the OFF position for the parameters to be active at boot. Furthermore when the OVERRIDE position is active all the configuration switches on SW5 must be set appropriately as they are all over written at boot.

For more detailed information on the available configurations for SW4 and SW5 are defined in chapter 3, sections 3.3.4 and 3.3.5.

The following tables describe switches SW4 and SW5.

Table 1: SW4 Configuration Switch

SW4 Switch Position	Description	Function
1	AMCC/Standalone Select	Off = Operating in AMCC mode On = Operating in stand alone mode *
2	ROM_SEL Select	Off = Select factory I ² C configuration default EEPROM * On = Select the user I ² C configuration EEPROM
3	DDRSRATE Select	Off = DSP DDRSLRATE is 1 (full memory speed) * On = DSP DDRSLRATE is 0 (reduce slew rate by 33%)
4	Use Mode select	Off = Factory test mode On = Standard Mode *
Note: For SW4 ON position is a logic low or "0", OFF position is a logic high or "1"		

* Default position as shipped

When in AMCC mode the AMCC_ENABLEn signal from the AMCC connector acts as an additional power on reset. When the AMCC_ENABLEn signal is high both the PORz and XWMRSTz resets to the DSP are asserted along with boot configuration. If the AMCC_ENABLEn signal is low and the boot configuration process is complete then PORz and XWMRSTz are released.

Table 2: SW5 Configuration Switch

SW5 Switch Position	Description	Function	Default *
1	BOOTM0	DSP Boot Mode 0	OFF
2	BOOTM1	DSP Boot Mode 1	ON
3	BOOTM2	DSP Boot Mode 2	ON
4	BOOTM3	DSP Boot Mode 3	ON
5	LENDIAN	DSP LENDIAN	OFF
6	L2CONFIG	DSP L2CONFIG	OFF
7	CORECLK	DSP CORECLK	OFF
8	OVERRIDE	Off = use boot mode setting from switches On = use boot mode setting from EEPROM	ON
Note: For SW5 ON position is a logic low or "0", OFF position is a logic high or "1"			

* Default position as shipped

2.3 JTAG Overview

The EVM incorporates Spectrum Digital's embedded JTAG emulation, a 14 pin JTAG interface and 2 - 60 pin TI JTAG/Trace headers. A CPLD is used for routing the various JTAG paths so that no user switches or hardware configuration is required.

The board supports both C6474 devices in the JTAG scan chain when used with the on-board emulation or 14 pin JTAG header J10. When the 60 pin JTAG header is used only one C6474 device is connected to that header. There is a 60 pin JTAG header for each cpu. If only one 60 pin JTAG header is used, the other C6474 device is accessible via its 14 pin or 60 pin JTAG emulation connector.

2.4 EVM Power Domains

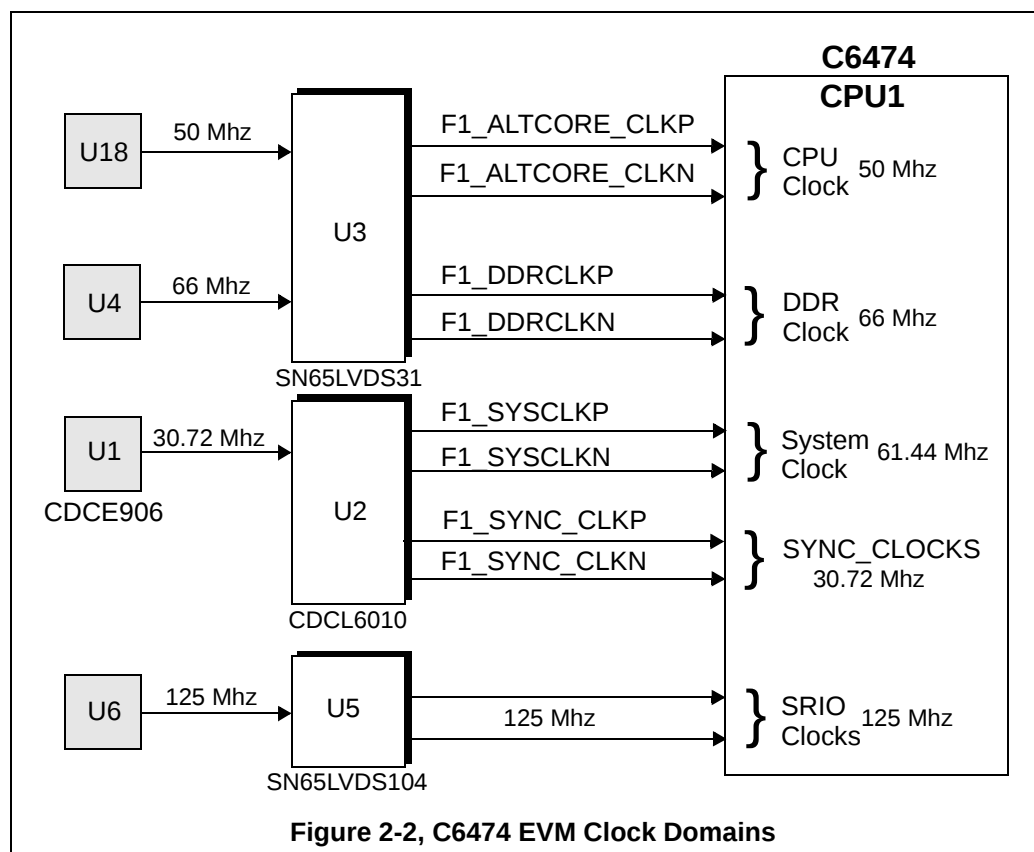
The EVM incorporates a power domain controller via the on board CPLD and on board emulation/configuration processor. The board is powered by 12 volt input supplied by connector J506 or the AMC interface connector. This 12 volts is down converted to +5 volts to operate the on-board 3.3 volt, 2.5 volt, 1.8 volt, 1.1 volt and 2 DSP core regulators.

At power up, the 3.3 volt domain EVM_3V3, the 2.5 volt domain EMU_2V5 and 1.8 volt domain EVM_1V8 are enabled. The configuration processor then enables the EVM_2V5 domain, the F_DVDD_18 domain, the F_VDDD_11 domain, and the F1_CVDD domain and the F2_CVDD domain. All these domains are monitored by separate power monitors. As the domains are enabled the power feedback LEDs from the CPLD are illuminated. When the power domains are present the configuration processor then enables the clock domains, sets the boot mode parameters and then releases the reset and power on reset signals to the C6474 devices. If the configuration is successful the RED configuration LED is turned off.

This configuration is all handled automatically via the CPLD and configuration processor.

2.5 Clock Domains

The EVM incorporates a wide variety of clocks to the C6474 devices. These clocks are configured automatically during the power up configuration sequence. The figure below illustrates the clocking for the CPU #1 on the EVM module. CPU #2 uses a similar technique.



2.6 I²C Boot Configuration EEPROM

The C6474 EVM supports 2 boot configuration EEPROMS, one is programmed with factory defaults which the user cannot modify. The other is the user configuration EEPROM that can be used to override factory defaults. The user configuration EEPROM is programmed with factory defaults for production test purposes. The EEPROMS are broken into 5 configuration sections and occupy either 1 or 2 32-byte blocks of EEPROM. The following tables describe the contents of the EEPROMs.

Table 3: I²C Boot Configuration EEPROM

EEPROM Address	Name	Function
0x00 - 0x1F	EEPROM Version	EEPROM Version string
0x20 - 0x3F	C6474 Boot and Configuration	DSP Boot mode configuration settings
0x60 - 0x7F	CDCL6010 Configuration	CDCL6010 Settings
0x80 - 0xBF	CDCE906 Configuration	CDCE906 Settings
0xC0 - 0xFF	Unused	

During the boot process the EEPROM is read section by section and used to configure the C6474 EVM. The firmware makes the following simple checks before configuring the C6474 EVM:

- Verifies factory EEPROM exists. If not then configuration aborts.
- Verifies that factory EEPROM version and firmware version match. If not then configuration aborts.
- Verifies that user EEPROM exists. If user EEPROM is selected as the configuration source and does not exist then configuration aborts.
- Verifies that CDCE906 exists and has a valid EEPROM section header, if true then configure the CDCE906.
- Verifies that CDCE906 exists and has a valid EEPROM section header, if true then configure the CDCE906.

2.6.1 EEPROM Version

The EEPROM version string occupies 1 32-byte block of EEPROM. The version string as defined as "C6474 V00.00.01" for Major.Minor.Build format. During the boot sequence the factory programmed EEPROM version string is read and compared to that of the embedded firmware. If they do not match then the boot sequence is aborted.

2.6.2 C6474 Boot and Configuration

The C6474 Boot and Configuration section occupies 3 bytes with the following definitions:

Table 4: Byte 0: Default 0xF0

Bit #	Name	Function
0	BOOTM0	DSP BOOTM0
1	BOOTM1	DSP BOOTM1
2	BOOTM2	DSP BOOTM2
3	BOOTM3	DSP BOOTM3
4	LENDIAN	DSP LENDIAN
5	L2CONFIG	DSP L2CONFIG
6	CORECLK	DSP CORECLK
7	DDRSLRATE	DSP DDRSLRATE

Table 5: Byte 1: Default 0x21

Bit #	Name	Function
3 - 0	DEVNUM - F1	DSP F1 Device Number
7 - 4	DEVNUM - F2	DSP F2 Device Number

Table 6: Byte 2: Default 0x00

Bit #	Name	Function
0	FRAME_SYNC_SELECT	0 - Select GPIO9 (default) 1 - Select EXT_CPLD_FSYNC_BURST
1	FRAME_SYNC_DISABLE	0 - Enable frame clocks (default) 1 - disable frame clocks
2 - 7	Not used	

2.6.3 CDCL6010 Configuration

The CDCL6010 is an 11 output clock multiplier, distributor, jitter cleaner and buffer. This programmable device generates 10 clock signals. These clock signals are defined in the table below.

Table 7: CDCL6010 Generated Clocks

Pin #	Pin Name	Clock Signal Generated
6	YP0	F1.SYSCLK.P
7	YPN	F1.SYSCLK.N
9	YP1	F2.SYSCLK.P
10	YN1	F2.SYSCLK.N
27	YP5	F1.FSYNC_CLKP
28	YN5	F1.FSYNC_CLKN
30	YP6	F2.FSYNC_CLKP
31	YN6	F2.FSYNC_CLKN
33	YP7	CPLD_FSYNC_CLKP
34	YN7	CPLD_FSYNC_CLKN

The CDCL6010 Configuration section occupies 32 bytes. The section ID is 3. During boot process if the CDCL6010 section ID is read as 3 and the number of address/data pairs is greater than 0 then the CDCL6010 will be configured.

Table 8: CDCL6010 - Base Address - 0x60

Byte #	Value	Function
0	0x03	Section ID
1	N	Number of Address: Data pairs
2	Address 1	CDCL6010 - Register address
3	Data 1	CDCL6010 - Register data
4 - 31	Reserved	

2.6.4 CDCE906 Configuration

The CDCE906 is a programmable 3-PLL 6 output clock synthesizer. This device generates 6 clock signals on the EVM. Two of the six clocks are fed into 2 sets of inputs to U3, SN65LVD31 which generates 4 differential clock domains. The clock signals generated by the CDCE906 are defined in the table below.

Table 9: CDCE906 Generated Clocks

Pin #	Pin Name	Clock Signal Generated
11	Y0	CLK 30.72MHZ
12	Y1	CPLD_CLK
15	Y2	Input to 1A U3, SN65LVDS31
16	Y3	Input to 2A U3, SN65LVDS31
19	Y4	Input to 3A U3, SN65LVDS31
20	Y5	Input to 4A U3, SN65LVDS31

Of the 2 sets of 2 inputs (4 total) to U3, each of them have an option to use the CDCE906 output or fixed oscillators as inputs. currently the EVM uses fixed oscillators.

The clock signals generated by the SN65LVD31 are defined in the table below.

Table 10: SN65LVD31 Generated Clocks

Pin #	Pin Name	Clock Signal Generated
2	1Y	F1_ALTCORE_CLKP
3	1Z	F1_ALTCORE_CLKN
5	2Z	F1_DDRCLK_N
6	2Y	F1_DDRCLK_P
10	3Y	F2_ALTCORE_CLKP
11	3Z	F2_ALTCORE_CLKN
13	4Z	F2_DDRCLK_N
14	4Y	F2_DDRCLK_P

The CDCE906 Configuration section occupies 64 bytes. The section ID is 4. During boot process if the CDE906 section ID is read as 4 and the number of address/data pairs is greater then 0 then the CDE906 will be configured.

Table 11: CDCE906 - Base Address - 0x80

Byte #	Value	Function
0	0x04	Section ID
1	N	Number of Address: Data pairs
2	Address 1	CDC906 - Register address
3	Data 1	CDC906 - Register data
4 - 31	Reserved	

2.7 I²C Device Address Mapping

The following table specifies the I²C device mappings for the C6474 EVM:

Table 12: I²C Device Address Mapping

Device	Device Address	Reference
CPU1 BOOT EEPROM	0b1010000_rw 0xA0	U23
CPU1 FACTORY CONFIG EEPROM	0b1010001_rw 0xA2	U13
CPU1 USER CONFIG EEPROM	0b1010010_rw 0xA4	U12
CPU1 CDCL6010	0b1101000_rw 0xD0	U2
F1 CDCE906	0b1101001_rw 0xD1	U1
CPU2 BOOT EEPROM	0b1010000_rw 0xA0	U36

2.8 CPLD

NOTE

This is to be used at the factory only.

The CPLD registers on the C6474 EVM are accessed from the embedded emulation processor. On EVM power up both C6474 devices are powered down. Once the embedded emulation processor has booted it will then configure the C6474 boot modes and configuration pins, sequence the power supplies and then release the C6474 resets. There are three boot mode options on the C6474:

- Factory Default Mode: Boot mode options are configured from factory default I²C configuration EEPROM.
- User Boot Mode: Boot mode options are configured from user I²C configuration EEPROM.
- Switch Mode: Boot mode and selected configuration options driven from boot/configuration switches.

The following tables describe the contents of the CPLD registers.

2.8.1 Version Register (read/write)

The default CPLD version is 0x21.

Table 13: Version Register

Bit #	Name
0	VER - Minor:0
1	VER - Minor:1
2	VER - Minor:2
3	VER - Minor:3
4	VER - Major:0
5	VER - Major:1
6	VER - Major:2
7	VER - Major:3

2.8.2 Optional Configuration Switches (read/write)

Bits 0-3 map to SW4. The DSP_CFG0_ADDR and DSP_CFG1_ADDR are used during the boot configuration process to address the boot configuration shadow registers. The boot modes, boot configuration and device numbers are read from one of the I²C EEPROMS and written into 3 shadow configuration registers. The shadow registers are mapped to the same address as the VERSION register.

Table 14: Optional configuration Switches

Bit #	Name	Function
0	SW_STANDALONE	0 : Operating in stand alone mode 1 : Operating in AMCC mode
1	SW_ROM_SEL	0 : Use settings from factory default EEPROM 1 : Use settings from user config EEPROM
2	DDRSRATE	Switch DDRSLRATE Select
3	SW_FACTORY_TEST	Internal use for Emulation development
4	DSP_CFG0_ADDR	DSP Config shadow register address 0
5	DSP_CFG1_ADDR	DSP Config shadow register address 1
6	Reserved	
7	Reserved	

2.8.3 NMI (read/write)

Table 15: NMI

Bit #	Name	Function
0	F1 - NMI0	F1 NMI0 Pin
1	F1 - NMI1	F1 NMI1 Pin
2	F1 - NMI2	F1 NMI2 Pin
3	F2 - NMI0	F2 NMI0 Pin
4	F2 - NMI1	F2 NMI1 Pin
5	F2 - NMI2	F2 NMI2 Pin
6	ENET_RESETh	Drives ENET_RESETh Pin
7	Not used	

2.8.4 Power Main Control (read/write)

Default power configuration is for all supplies except for the 2.5v to be off on startup and the DSP resets forced to reset. The 2.5V supply must be active as it is shared by the embedded emulation block.

Table 16: Power Main Control

Bit #	Name	Function
0	EN_DUT_2V5	Enable 2.5 volt supply
1	EN_DUT_1V2	Enable 1.1/1.2 volt supply
2	EN_DUT_3V3	Enable 3.3 volt supply
3	EN_DUT_1V8	Enable 1.8 volt supply
4	EN_F1_CORE	Enable F1 core supply
5	EN_F2_CORE	Enable F2 core supply
6	DSP_RELEASE	1 : Release DSP reset 0 : Force DSP reset
7	I ² C_WP	

2.8.5 Power Domain Status (read only)

This read only register provides the status of the various power levels.

Table 17: Power Domain Status

Bit #	Name	Function
0	STAT_2V5	2.5 volt power good
1	STAT_1V2	1.2 volt power good
2	STAT_3V3	3.3 volt power good
3	STAT_1V8	1.8 volt power good
4	STAT_F1_CORE	F1 power good
5	STAT_F2_CORE	F2 power good
6	F1_RSTAT	F1 Reset status
7	F2_RSTAT	F2 Reset status

2.8.6 Thermal and BOOT Status (read only)

Table 18: Thermal and BOOT Status

Bit #	Name	Function
0	F1_ALERT1Z	F1 TMP411 ALERT1Z
1	F1_CRIT1Z	F1 TMP411 CRIT1Z
2	F1_BOOT_PIN_RELEASE	0 : Boot mode pins are active to F1 1 : Boot mode pins are high-Z to F1
3	F2_ALERT1Z	F2 TMP411 ALERT1Z
4	F2_CRIT1Z	F2 TMP411 CRIT1Z
5	F2_BOOT_PIN_RELEASE	0 : Boot mode pins are active to F2 1 : Boot mode pins are high-Z to F2
6	Reserved	
7	AMCC_ENABLE	0 : AMCC enabled 1 : AMCC disabled

2.8.7 Register 6

This register is reserved for future use.

Table 19: Register 6

Bit #	Name	Function
0	Not used	Reserved
1	Not used	Reserved
2	Not used	Reserved
3	Not used	Reserved
4	Not used	Reserved
5	Not used	Reserved
6	Not used	Reserved
7	Not used	Reserved

2.8.8 BOOT Mode Switches (read only)

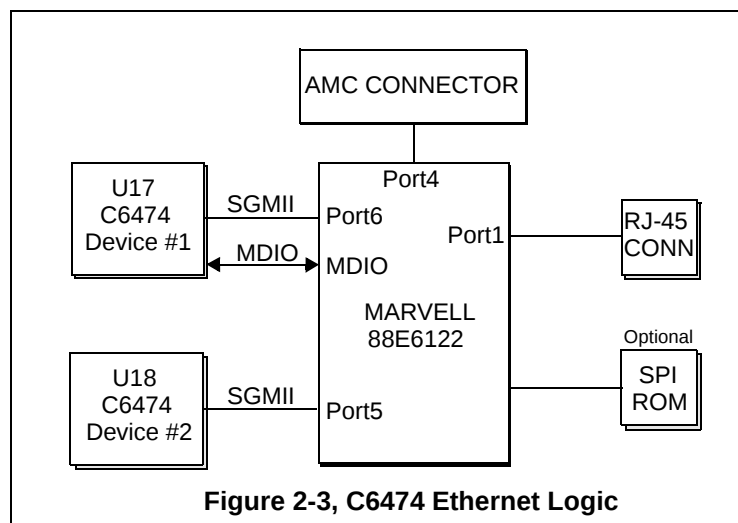
Bits 0 - 7 of this register are mapped to switch SW5.

Table 20: Boot Mode Switches

Bit #	Name	Function
0	SW_MODE0	Switch Boot Mode 0
1	SW_MODE1	Switch Boot Mode 1
2	SW_MODE2	Switch Boot Mode 2
3	SW_MODE3	Switch Boot Mode 3
4	SW_LENDIAN	Switch LENDIAN Select
5	SW_L2CONFIG	Switch L2CONFIG Select
6	SW_CORECLK	Switch CORECLK Select
7	SW_OVERRIDE	1 = use boot mode setting from switches 0 = user boot mode setting from EEPROM

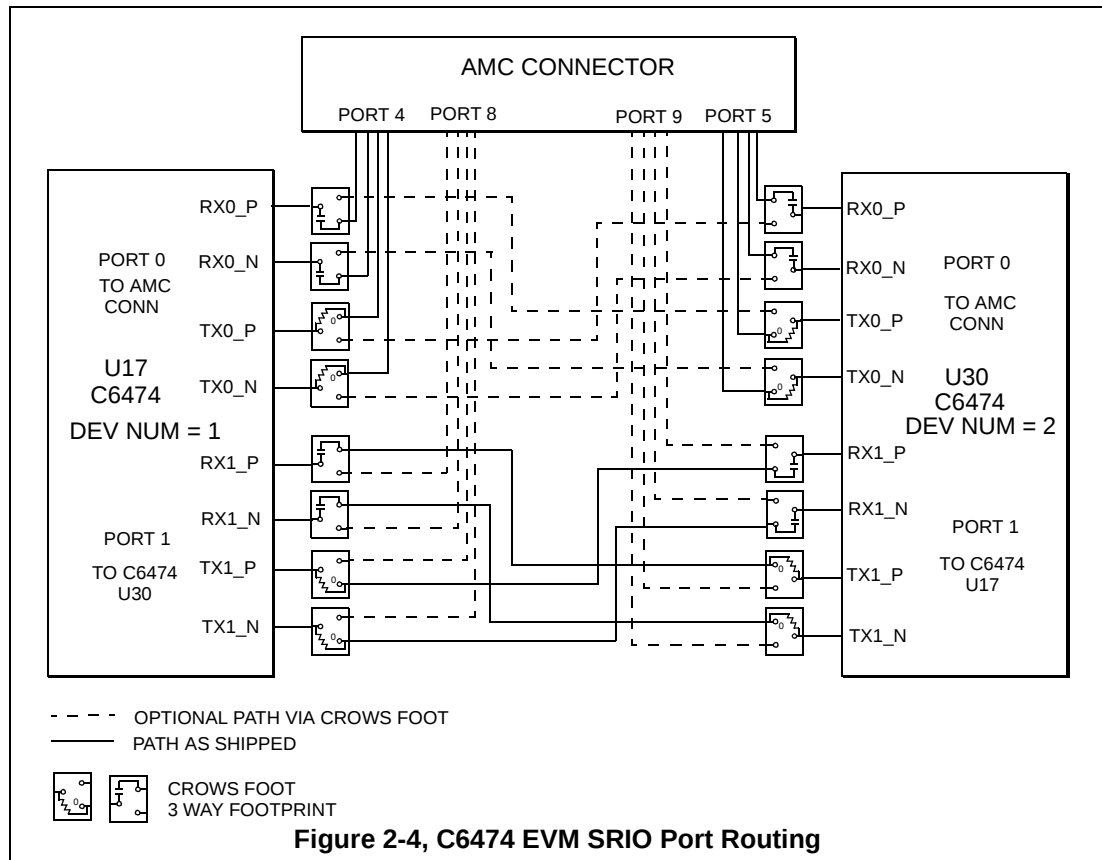
2.9 Ethernet Phy

The C6474 EVM incorporates a multi-port Marvell 88E6122 ethernet switch. The C6474 (U17) is the master device which configures this switch via the MDIO interface. Both C6474 devices have access to this switch as shown in the figure below.



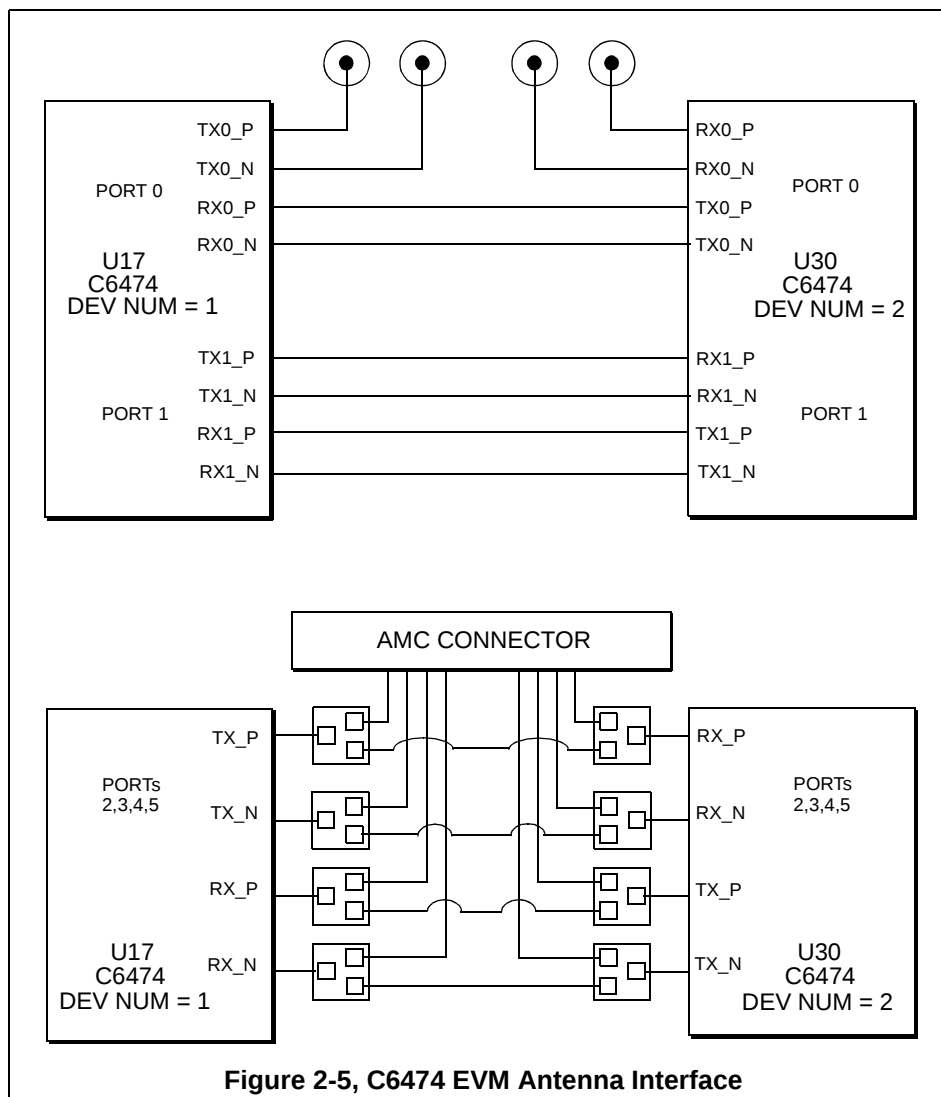
2.10 Serial Rapid I/O (SRIO) Interfaces

The C6474 EVM uses Serial Rapid I/O to communicate between the 2 CPU devices and the AMC connector. This versatile high speed interface allows the user to effectively communicate between on board and off board systems. The figure below illustrates the as shipped configuration of the SRIO.



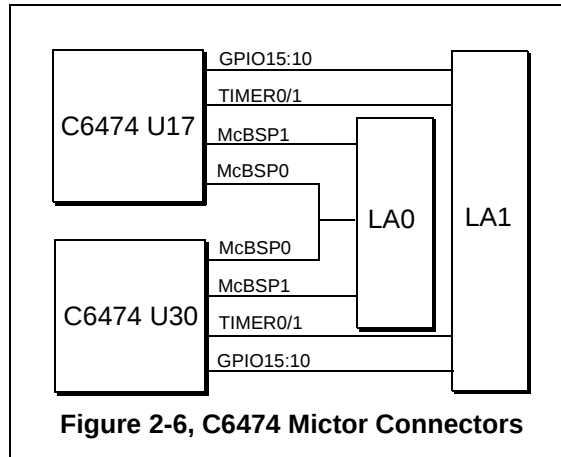
2.11 Antenna Interface (AIF)

The antenna interface uses high speed serial interface to communicate between the two on board C6474 devices and external interfaces. Port 0 on the EVM supports one incoming stream and one outgoing stream via DSP interconnection. Port 1 supports direct full DSP to DSP interconnection. Ports 2-5 default configuration supports 1 full link to the AMC connector (port 5) and 3 full DSP to DSP links (ports 2-4). The figure below illustrates the antenna configuration on the the C6474 EVM.



2.12 Mictor Connectors

The C6474 EVM provides 2 Mictor connectors (LA0 and LA1) for expansion interfaces for Timer 0/1 and GPIO[15:10] pins for each processor. Furthermore McASP1 on both processors are available on these Mictors. McASP0 provides a direct DSP to DSP connection. All the signals present on the Mictor connectors are described in sections 3.2.17 and 3.2.18 of chapter 3. The figure below illustrates a brief description of the Mictor connector interface on the C6474 EVM.



Chapter 3

Physical Description

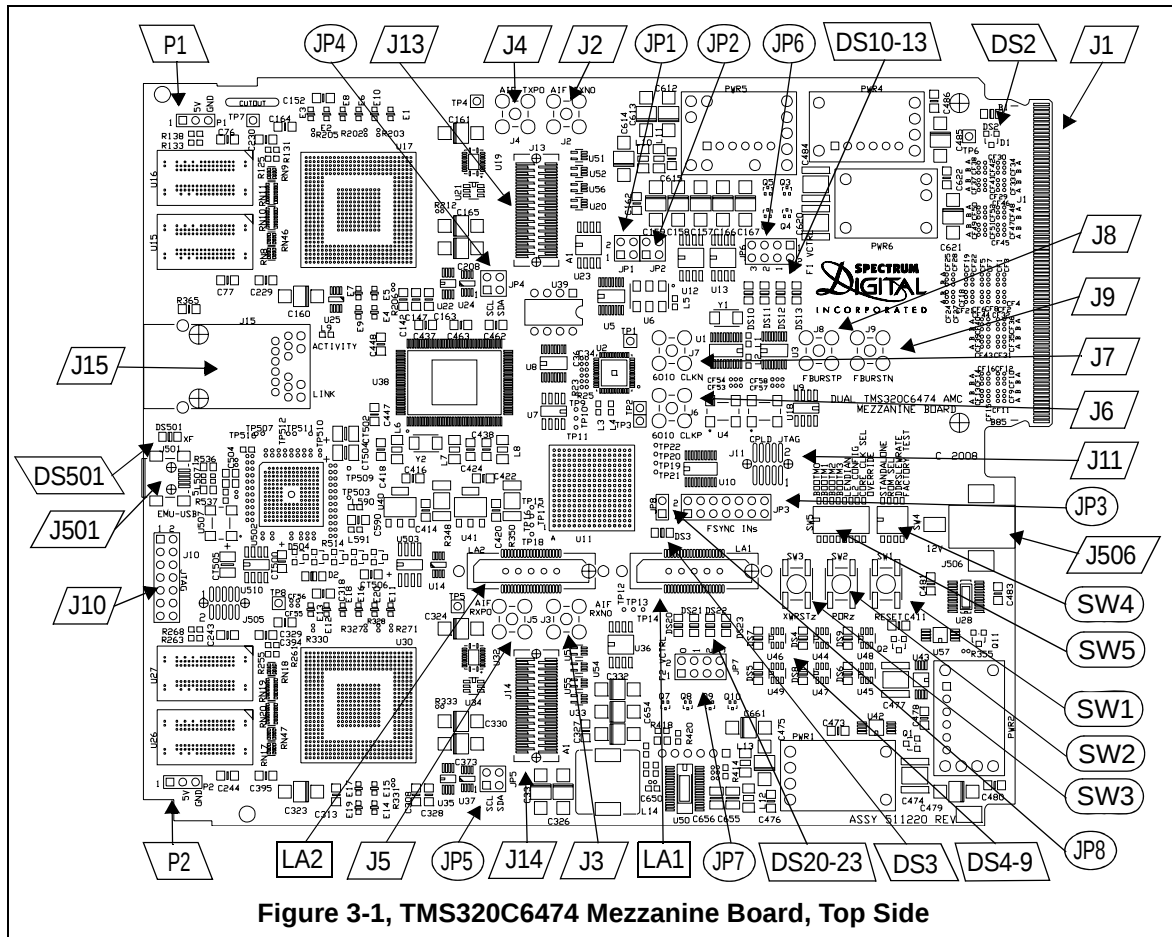
This chapter describes the physical layout of the TMS320C6474 Mezzanine Board and its connectors.

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3.1 Board Layout

The C6474 Mezzanine Board is a 7.107 x 5.848 inch (180.52 x 148.54 mm.) multi-layer board which is powered through connector J506. Figure 3-1 shows the layout of the C6474 Mezzanine Board.



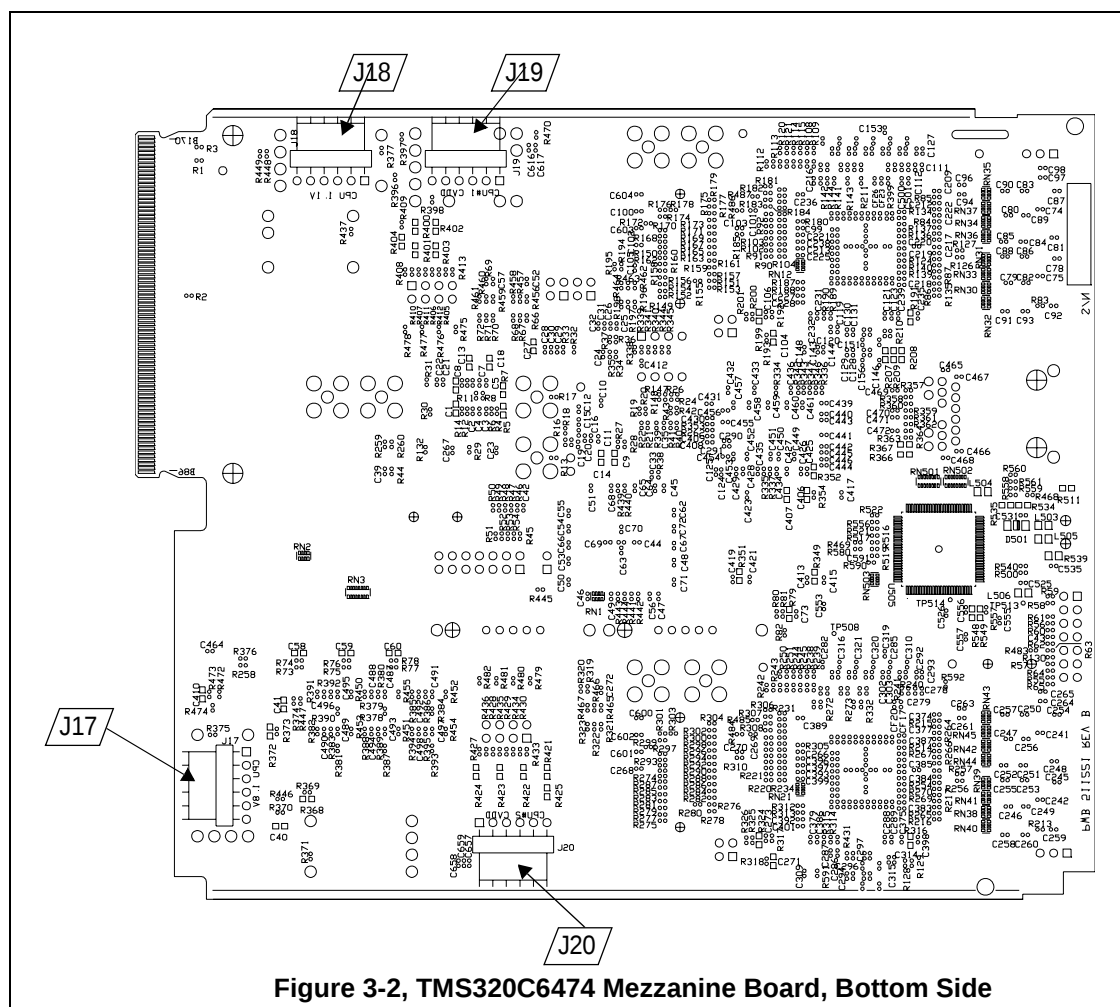


Figure 3-2, TMS320C6474 Mezzanine Board, Bottom Side

3.2 Connector Index

The TMS320C6474 Mezzanine Board has several connectors which provide the user access to the various signals on the board.

Table 1: TMS320C6474 Mezzanine Board Connectors

Connector	# Pins	Function
J1		AMC Interface
J2	SMA	CPU 1 AIFTXN0 Output
J4	SMA	CPU 1 AIFTXP0 Output
J3	SMA	CPU 2 AIFTXN0 Input
J5	SMA	CPU 2 AIFTXP0 Input
J6	SMA *	Alternate Input CLK To CDCL60IO Positive
J7	SMA *	Alternate Input CLK To CDCL60IO Negative
J8	SMA	External FYSNC Burst Input Positive
J9	SMA	External FYSNC Burst Input Negative
J10	14	TI JTAG (+3.3 Volt Compatible)
J11	10	CPLD Programming header
J13	60	CPU 1 Trace Interface
J14	60	CPU 2 Trace Interface
J15		Ethernet Interface
J17	6	Socket for PW2 Supply
J18	6	Socket for PW4 Supply
J19	6	Socket for PW5 Supply
J20	6	Socket For Spare Supply
J501		USB Connection to Embedded JTAG controller
J506		+12 Volt Input
LA1		CPU 1, CPU2 McBSP Expansion
LA2		CPU 1, CPU2 Timer, GPIO Expansion
P1		Fan Connector for CPU 1
P2		Fan Connector for CPU 2

* Must disable on board logic to use this feature

3.2.1 J1, AMCC Interface Connector

The J1 card edge connector plugs into the J1 connector on the DSK circuit board. This connector provides a high speed Serial Rapid I/O to the DSK board. This connector has 170 pins. Pin 1 is across from pin 170, and pin 85 is across from pin 86. The signals on this connector are shown in the tables below.

Table 2: J1, AMCC Connector, Pins 1-42, 170-129

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	170	GND	Ground
2	+12V	12 Volt Power	169	NC	Reserved
3	PS1	AMC_PS1	168	NC	Reserved
4	ALT +3.3V	Not Used	167	NC	Reserved
5	GND	Ground	166	NC	Reserved
6			165	NC	Reserved
7	GND	Ground	164	GND	Ground
8			163	NC	Reserved
9	+12V	12 Volt Power	162	NC	Reserved
10	GND	Ground	161	GND	Ground
11			160	NC	
12			159	NC	
13	GND	Ground	158	GND	Ground
14			157		SRIO Channel 19 TXMT+
15			156		SRIO Channel 19 TXMT-
16	GND	Ground	155	GND	Ground
17			154		SRIO Channel 19 RCV+
18	+12V	12 Volt Power	153		SRIO Channel 19 RCV-
19	GND	Ground	152	GND	Ground
20			151		SRIO Channel 18 TXMT+
21			150		SRIO Channel 18 TXMT-
22	GND	Ground	149	GND	Ground
23			148		SRIO Channel 18 RCV+
24			147		SRIO Channel 18 RCV-
25	GND	Ground	146	GND	Ground
26			145		SRIO Channel 17 TXMT+
27	+12V	12 Volt Power	144		SRIO Channel 17 TXMT-
28	GND	Ground	143	GND	Ground
29			142		SRIO Channel 17 RCV+
30			141		SRIO Channel 17 RCV-
31	GND	Ground	140	GND	Ground
32			139		SRIO Channel 16 TXMT+
33			138		SRIO Channel 16 TXMT-
34	GND	Ground	137	GND	Ground
35			136		SRIO Channel 16 RCV+
36			135		SRIO Channel 16 RCV-
37	GND	Ground	134	GND	Ground
38			133		SRIO Channel 15 TXMT+
39			132		SRIO Channel 15 TXMT-
40	GND	Ground	131	GND	Ground
41	ENABLE	AMC ENABLE	130		SRIO Channel 15 RCV+
42	+12V	12 Volt Power	129		SRIO Channel 15 RCV-

Table 3: J1, AMCC Connector, Pins 43-128-86

Pin	Signal	Description	Pin	Signal	Description
43	GND	Ground	128	GND	Ground
44	DSPB.RIOTXP0	SRIO Channel 0 TXMT+	127		SRIO Channel 14 TXMT+
45	DSPB.RIOTXN0	SRIO Channel 0 TXMT-	126		SRIO Channel 14 TXMT-
46	GND	Ground	125	GND	Ground
47	DSPB.RIORXP0	SRIO Channel 0 RCV+	124		SRIO Channel 14 RCV+
48	DSPB.RIORXP0	SRIO Channel 0 RCV-	123		SRIO Channel 14 RCV-
49	GND	Ground	122	GND	Ground
50	DSPB.RIOTXP1	SRIO Channel 1 TXMT+	121		SRIO Channel 13 TXMT+
51	DSPB.RIOTXN1	SRIO Channel 1 TXMT-	120		SRIO Channel 13 TXMT-
52	GND	Ground	119	GND	Ground
53	DSPB.RIORXP1	SRIO Channel 1 RCV+	118		SRIO Channel 13 RCV+
54	DSPB.RIORXN1	SRIO Channel 1 RCV-	117		SRIO Channel 13 RCV-
55	GND	Ground	116	GND	Ground
56	NC	I ² C Clock	115		SRIO Channel 12 TXMT+
57	+12V	12 Volt Power	114		SRIO Channel 12 TXMT-
58	GND	Ground	113	GND	Ground
59	NC	SRIO Channel 2 TXMT+	112		SRIO Channel 12 RCV+
60	NC	SRIO Channel 2 TXMT+	111		SRIO Channel 12 RCV-
61	GND	Ground	110	GND	Ground
62	NC	SRIO Channel 2 RCV+	109	NC	
63	NC	SRIO Channel 2 RCV-	108	NC	
64	GND	Ground	107	GND	Ground
65	NC	SRIO Channel 3 TXMT+	106	NC	
66	NC	SRIO Channel 3 TXMT-	105	NC	
67	GND	Ground	104	GND	Ground
68	NC	SRIO Channel 3 RCV+	103	NC	
69	NC	SRIO Channel 3 RCV-	102	NC	
70	GND	Ground	101	GND	Ground
71	NC	I ² C Data	100	NC	
72	+12V	12 Volt Power	99	NC	
73	GND	Ground	98	GND	Ground
74	NC		97		SRIO Channel 9 TXMT+
75	NC		96		SRIO Channel 9 TXMT-
76	GND	Ground	95	GND	Ground
77	NC		94		SRIO Channel 9 RCV+
78	NC		93		SRIO Channel 9 RCV-
79	GND	Ground	92	GND	Ground
80	NC		91		SRIO Channel 8 TXMT+
81	NC		90		SRIO Channel 8 TXMT-
82	GND	Ground	89	GND	Ground
83	PST PS0	AMC Present0	88		SRIO Channel 8 RCV+
84	+12V	12 Volt Power	87		SRIO Channel 8 RCV-
85	GND	Ground	86	GND	Ground

3.2.2 J2, J4 CPU2 AIFTX SMA Interface Connectors

Connectors J2 and J4 provide an optional SMA connection to CPU2. These SMA's connect to the CPU2 AIFTXN0 and AIFTXP0 outputs respectively.

3.2.3 J3, J5, CPU1 AIFRX SMA Interface Connectors

Connectors J3 and J5 provide an optional SMA connection to CPU1. These SMA's connect to the CPU1 AIFRXN0 and AIFRXP0 inputs respectively.

3.2.4 J6,J7, Optional Clock Input SMA's

Connectors J6 and J7 provide an optional SMA connection to the CDCL6010 clock generator. The onboard generator must be disabled to use these inputs. This generator is used to provide the sysclk and fsync clocks to CPU1 and CPU2. J6 is the positive differential input for this alternate clock source and J7 is the negative differential input for this alternate clock source.

3.2.5 J8, J9, Optional External FSYNC Burst SMA Inputs

Connectors J8 and J9 provide an optional SMA connection to generate fsync bursts to CPU1 and CPU2. J8 is the positive differential input, J9 is the negative differential input. These inputs generate a pulse to the onboard CPLD which generates burst pulses to the corresponding CPU inputs.

3.2.6 J10, 14 Pin TI JTAG Interface

J10 is a standard TI 14 pin JTAG connector. The onboard CPLD multiplexes this interface with the onboard emulation logic and the 60 pin interface connectors for each CPU. When an emulator is plugged into J10 both CPU1 and CPU2 are in the scan chain unless one of the 60 pin interface connectors is also plugged in. The CPLD provides 3.3 Volt to 1.8 Volt conversion on this interface so any 3.3Volt compatible emulator can be used to interface to the C6474 devices. Note, that when an emulator is plugged into this connector the onboard emulation is disabled. The pinout for the connector is shown in the figure below.

TMS	1	2	TRST-	Header Dimensions Pin-to-Pin spacing, 0.100 in. (X,Y) Pin width, 0.025-in. square post Pin length, 0.235-in. nominal
TDI	3	4	GND	
PD (+3.3V)	5	6	no pin (key)	
TDO	7	8	GND	
TCK-RET	9	10	GND	
TCK	11	12	GND	
EMU0	13	14	EMU1	

Figure 3-2, J10, 14 Pin JTAG Interface

The signal names for each pin are shown in the table below.

Table 4: J10, 14 Pin JTAG Interface

Pin #	Signal Name
1	TMS
2	TRST-
3	TDI
4	GND
5	PD
6	no pin
7	TDO
8	GND
9	TCK-RET
10	GND
11	TCK
12	GND
13	EMU0
14	EMU1

3.2.7 J11, CPLD Programming Header

J11 is used in the factory to program the onboard CPLD. It is not intended to be used under normal operation.

3.2.8 J13, 60 Pin Emulation Interface for CPU1

The 60 pin emulation connector for CPU1 is for advanced emulation capability. The signals on this connector are 4 columns by 15 rows as shown in the table below

Table 5: J13, 60 Pin Emulation Connector

Row #	Column A Signal Name	Column B Signal Name	Column C Signal Name	Column D Signal Name
1	Ground	IDO	ID2	Ground
2	Ground	TMS	EMU18	Ground
3	Ground	EMU17	TRSTn	Ground
4	Ground	TDI	EMU16	Ground
5	Ground	EMU14	EMU15	Ground
6	Ground	EMU12	EMU13	Ground
7	Ground	TDO	EMU11	Ground
8	TYPE0	TVD	TCLKRTN	TYPE1
9	Ground	EMU9	EMU10	Ground
10	Ground	EMU7	EMU8	Ground
11	Ground	EMU5	EMU6	Ground
12	Ground	TCLK	EMU4	Ground
13	Ground	EMU2	EMU3	Ground
14	Ground	EMU0	EMU1	Ground
15	Ground	ID1	ID3	Ground

3.2.9 J14, 60 Pin Emulation Interface for CPU2

The 60 pin emulation connector for CPU2 is for advanced emulation capability. The signals on this connector are 4 columns by 15 rows as shown in the table below

Table 6: J13, 60 Pin Emulation Connector

Row #	Column A Signal Name	Column B Signal Name	Column C Signal Name	Column D Signal Name
1	Ground	IDO	ID2	Ground
2	Ground	TMS	EMU18	Ground
3	Ground	EMU17	TRSTn	Ground
4	Ground	TDI	EMU16	Ground
5	Ground	EMU14	EMU15	Ground
6	Ground	EMU12	EMU13	Ground
7	Ground	TDO	EMU11	Ground
8	TYPE0	TVD	TCLKRTN	TYPE1
9	Ground	EMU9	EMU10	Ground
10	Ground	EMU7	EMU8	Ground
11	Ground	EMU5	EMU6	Ground
12	Ground	TCLK	EMU4	Ground
13	Ground	EMU2	EMU3	Ground
14	Ground	EMU0	EMU1	Ground
15	Ground	ID1	ID3	Ground

3.2.10 J15, Ethernet Connector

J15 is an integrated 1 gigabit Ethernet interface connector. It is driven from the 88E6122Marvell Phy P1 port. The output connections are shown in the table below.

Table 7: J15, Ethernet Connector Pin Out

Pin #	Signal Name
1	TX1+
2	TX1-
3	TX2+
4	TX3+
5	TX3-
6	TX2-
7	TX4+
8	TX4-

3.2.11 J17, PWR2 Converter Interface

Connector J17 provides the interface for output of the PWR2 DC-DC converter that generates +1.8 volts. The signals on this connector are shown in the table below.

Table 8: J17, PWR2 Converter Interface

Pin #	Signal Name
1	F_DVDD_18
2	F_DVDD_18
3	GND
4	GND
5	GND
6	F_DVDD_18_MON

3.2.12 J18, PWR4 Converter Interface

Connector J18 provides the interface for output of the PWR4 DC-DC converter that generates +1.1 volts. The signals on this connector are shown in the table below.

Table 9: J17, PWR2 Converter Interface

Pin #	Signal Name
1	F_DVDD_11
2	F_DVDD_11
3	GND
4	GND
5	GND
6	F_DVDD_11_MON

3.2.13 J19, PWR5 Converter Interface

Connector J19 provides the interface for output of the PWR5 DC-DC converter that generates the F1_CVDD voltage. The signals on this connector are shown in the table below.

Table 10: J17, PWR2 Converter Interface

Pin #	Signal Name
1	F1_CVDD
2	F1_CVDD
3	GND
4	GND
5	GND
6	F1_CVDD_MON

3.2.14 J20, TPS54010PWP Converter Interface

Connector J20 provides the interface for output of the TPS54010PWP DC-DC converter that generates the F2_CVDD voltage. The signals on this connector are shown in the table below.

Table 11: J17, TPS54010WP Converter Interface

Pin #	Signal Name
1	F2_CVDD
2	F2_CVDD
3	GND
4	GND
5	GND
6	F2_CVDD_MON

3.2.15 J501, Embedded Emulation USB Connector

J501 is a Mini USB connector which is the primary interface to the embedded USB emulation controller. The pin outs for this connector are shown in the table below.

Table 12: J501, Embedded Emulation USB Connector

Pin #	Signal Name
1	Power Input
2	Data Minus
3	Data Plus
4	ID, not used
5	Ground

3.2.16 J506, +12 Volt Input

Connector J506 is used to provide +12 volts to the board. Do **not** use the connector if powering the board from the AMCC connector.

3.2.17 LA1, Logic Analyzer 1 Connector

LA1 is a standard 38 pin mictor connector used to interface to the McBSP ports on the C6474 CPU1 and CPU2 devices. This connector is used for expansion and visibility interfaces. The signal on the pins are shown in the table below.

Table 13: LA1, Logic Analyzer 1 Connector

Pin	Signal	Pin	Signal
1	Not Used	38	Not Used
2	Not Used	37	Not Used
3	Not Used	36	Not Used
4	CPU1-TIMI0	35	CPU2-TIMI0
5	CPU1-TIMI1	34	CPU2-TIMI1
6	CPU1-TIMO0	33	CPU2-TIMO0
7	CPU1-TIMO1	32	CPU2-TIMO1
8	Not Used	31	Not Used
9	Not Used	30	Not Used
10	Not Used	29	Not Used
11	Not Used	28	Not Used
12	CPU1-GPIO10	27	CPU2-GPIO10
13	CPU1-GPIO11	26	CPU2-GPIO11
14	CPU1-GPIO12	25	CPU2-GPIO12
15	CPU1-GPIO13	24	CPU2-GPIO13
16	CPU1-GPIO14	23	CPU2-GPIO14
17	CPU1-GPIO15	22	CPU2-GPIO15
18	Not Used	21	Not Used
19	Not Used	20	Not Used

3.2.18 LA2, Logic Analyzer 2 Connector

LA2 is a standard 38 pin mictor connector used to interface to the Timer and GPIO pins on the C6474 CPU1 and CPU2 devices. This connector is used for expansion and visibility interfaces. The signal on the pins are shown in the table below.

Table 14: LA2, Logic Analyzer 2 Connector

Pin	Signal	Pin	Signal
1	Not Used	38	Not Used
2	Not Used	37	Not Used
3	Not Used	36	Not Used
4	CPU1 CLKS0	35	CPU2 CLKS0
5	Not Used	34	Not Used
6	CPU1-CLKR0 CPU2-CLKX0	33	Not Used
7	CPU1-FSR0 CPU2-FSX0	32	Not Used
8	CPU1-DR0 CPU2-DX0	31	Not Used
9	CPU1-CLX0 CPU2-CLRK0	30	Not Used
10	CPU1-FSX0 CPU2-FSR0	29	Not Used
11	CPU1-DX0 CPU2-DR0	28	Not Used
12	CPU1-CLKS1	27	CPU2-CLKS1
13	Not Used	26	Not Used
14	CPU1-CLRK1	25	CPU2-CLKX1
15	CPU1-FSR1	24	CPU2-FSX1
16	CPU1-DR1	23	CPU2-DX1
17	CPU1-CLKX1	22	CPU2-CLRK1
18	CPU1-FSX1	21	CPU2-FSR1
19	CPU1-DX1	20	CPU2-DR1

3.2.19 P1, Optional Fanpower Connector

P1 provides +5 volts for an optional Fan connection for CPU1.

3.2.20 P2, Optional Fanpower Connector

P2 provides +5 volts for an optional Fan connection for CPU2.

3.3 Switches

The TMS320C6474 Mezzanine Board has three push button switches, SW1-SW3. Their positions on the board are indicated in Figure 3-1. The functions of each switch are listed in the table below.

Table 15: Mezzanine Board Switches

Switch	Function
SW1	Reset
SW2	Power On Reset
SW3	XWRSTz

3.3.1 SW1, Reset Pushbutton

When pushed SW1 drives a full board reset. This is equivalent to a power cycle and will have the following effects:

- Turns off power to both DSPs.
- Resets the CPLD.
- Resets the embedded emulation block including USB port.
- Turns on power to DSPs but holds them in reset with both PORz and XWMRSTz asserted low.
- Reloads board configuration from EEPROMs and/or switches.
- Releases reset to Ethernet controller then releases DSPs.

If you are running Code Composer Studio (CCS) via the embedded emulation block then you will lose your CCS connection when SW1 is pressed as it does a full reset of the embedded emulation block. In this case you will have to exit and reenter CCS to reload the emulation application.

If you are running CCS via an external emulator then you will still lose your CCS connection but can recover with a CCS disconnect/connect sequence.

3.3.2 SW2, PORz Pushbutton

Switch SW2 drives the DSP PORz pin low when pressed. If the DSP asserts RSTAT low then boot mode configuration pins will be re-asserted. If RSTAT is not asserted then boot mode configuration pins are high-z.

This switch is digitally debounced and will drive PORz low for a minimum of 10 ms.

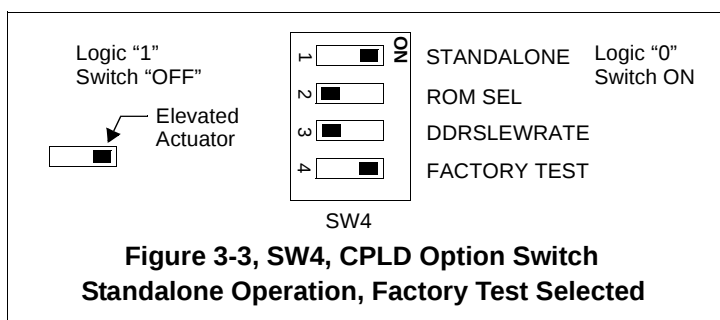
3.3.3 SW3, XWMRSTz Pushbutton

SW3 drives the DSP XWMRSTz pin low when pressed. The DSP boot configuration pins are NOT asserted for XWMRSTz.

This switch is digitally debounced and will drive XWMRSTz low for minimum of 10ms.

3.3.4 SW4, CPLD Option Switch

SW4 is a 4 position DIP switch that is used to pull down the CPLD lines CPLD.OPTSW0-3 to ground. A diagram of the SW4 switch is shown below.



The following table describes the positions on switch SW4.

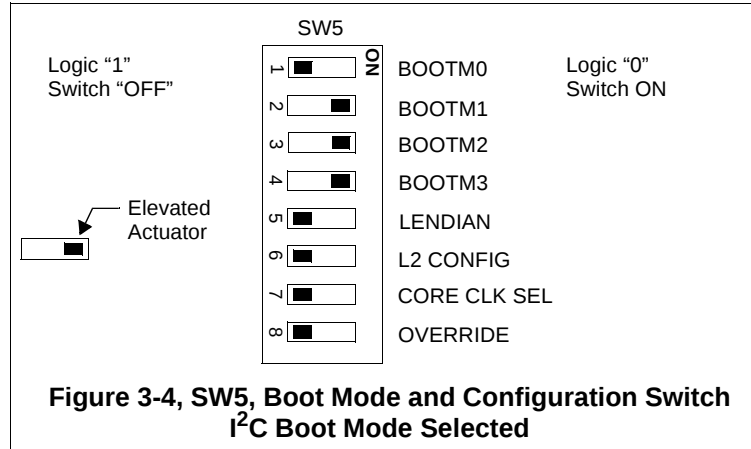
Table 16: SW4, CPLD Option Switch

SW4 Switch Position	Description	Function
1	AMCC/Standalone Select	Off = Operating in AMCC mode On =Operating in stand alone mode *
2	ROM_SEL Select	Off =Select factory I ² C configuration default EEPROM * On =Select the user I ² C configuration EEPROM
3	DDRSLEWRATE Select	Off =DSP DDRSLRATE is 1 (full memory speed) * On =DSP DDRSLRATE is 0 (reduce slew rate by 33%)
4	Use Mode select	Off = Factory test mode On =Standard Mode *
Note: For SW4 ON position is a logic low or "0", OFF position is a logic high or "1"		

* Default position as shipped

3.3.5 SW5, Boot Mode and Configuration Switch

SW5 is a 8 position DIP switch that is used to configure boot options when the override switch, (SW5, position 8), is in the “OFF” position. A diagram of switch SW5 is shown below. See section 2.2 for configuration information.



The following table describes the positions on switch SW5.

Table 17: SW5, Boot Mode and Configuration Switch Settings

Position	Function	
1	BOOTM0	Boot Mode Options See next table
2	BOOTM1	
3	BOOTM2	
4	BOOTM3	
5	LENDIAN	Off = Little endian * On = Big endian
6	L2 CONFIG	On = Asymmetric L2 Configuration * Off = Symmetric L2 Configuration
7	CORE CLK SEL	On = Use SYSCLKIN for CPU Core Clock Off = Use ALT CORECLK for CPU Core Clock *
8	OVERRIDE	On = Ignore all options on SW5 Off = Overrides I ² C Config EEPROM 7 above parameters *

* default

The table below shows the signals on each switch position.

Table 18: SW5, Boot Mode Options

M3	M2	M1	M0	Boot Mode
On	On	On	On	No Boot
On	On	On	Off	I ² C Master Boot A *
On	On	Off	On	I ² C master Boot B
On	On	Off	Off	I ² C Slave Boot
On	Off	On	On	EMAC Master Boot
On	Off	On	Off	EMAC Slave Boot
On	Off	Off	On	EMAC Forced-Mode Boot
On	Off	Off	Off	Reserved
Off	On	On	On	Serial RapidIO Boot (Config 0)
Off	On	On	Off	Serial RapidIO Boot (Config 1)
Off	On	Off	On	Serial RapidIO Boot (Config 2)
Off	On	Off	Off	Serial RapidIO Boot (Config 3)

* default

For more information on the boot modes refer to TI document SPRS552.

3.4 Jumpers

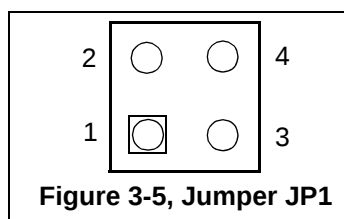
The TMS320C6474 Mezzanine Board has eight jumper blocks, JP1-JP8. Their positions on the board are indicated in Figure 3-1. The functions of each switch are listed in the table below.

Table 19: C6474 Mezzanine Board Switches

Switch	Function
JP1	CLKS0 Header
JP2	CLKS1 Header
JP3	User FSYNC Inputs
JP4	C6474 CPU1 Alternate I ² C Access Header
JP5	C6474 CPU2 Alternate I ² C Access Header
JP6	C6474 CPU11 Power Reflex Overrides
JP7	C6474 CPU2 Power Reflex Overrides
JP8	C6474 CPU1 to CPU2 Sync Burst Connection

3.4.1 Jumper JP1, CLKS0 Header

Jumper JP1 is a 4 position jumper used to access the CLKS0 signals on the C6474 CPU1 and CPU2. The layout of the header is shown in the figure below.



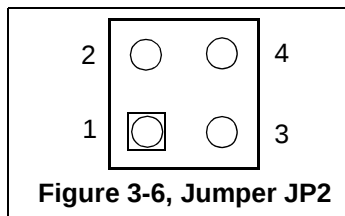
The signals on each pin are shown in the table.

Table 20: Jumper JP1, CLKS0 Header

Position	Signal	Position	Signal
1	GND	2	CPU1 CLKS0
3	GND	4	CPU2 CLKS0

3.4.2 Jumper JP2, CLKS1 Header

Jumper JP2 is a 4 position jumper to access the CLKS1 signals on the C6474 CPU1 and CPU2. The layout of the header is shown in the figure below.



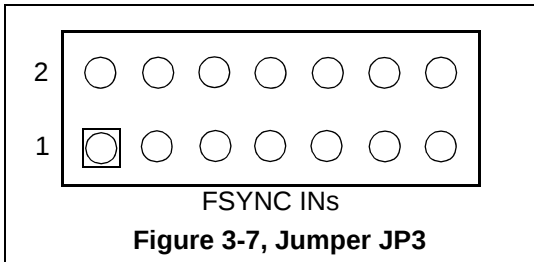
The signals on each pin are shown in the table.

Table 21: Jumper JP2, CLKS1 Header

Position	Signal	Position	Signal
1	GND	2	CPU1 CLKS1
3	GND	4	CPU2 CLKS1

3.4.3 Jumper JP3, User FSYNC Inputs

Jumper JP3 is a 14 position jumper used to drive optional burst signals to the C6474 devices. The signals are buffered by U10. The buffer needs to be enabled when these optional inputs are used. The layout of the jumper is shown below.



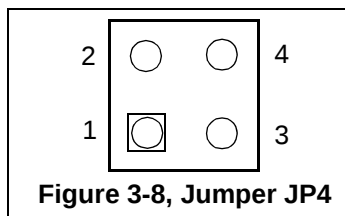
The function of each jumper setting is shown in the table below.

Table 22: Jumper JP3, User FSYNC Inputs

Position	Signal	Position	Signal
1	GND	2	CPU1, CPU2 FSYNC_CLK
3	GND	4	CPU1, CPU2 SYNC_BURST
5	GND	6	CPU1, CPU2 TRTCLK
7	GND	8	CPU1, CPU2 TRT
9	GND	10	CPU1 SMFRAME CLK
11	GND	12	CPU2 SMFRAME CLK
13	GND	14	BUFFER ENABLE

3.4.4 Jumper JP4, CPU1 I²C Header

Jumper JP4 is an access point to the CPU1's I²C signals. The mapping of the header is shown in the figure below.



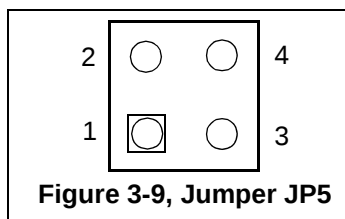
The signals on each pin are shown in the table.

Table 23: Jumper JP4, CPU1 I²C Header

Position	Signal	Position	Signal
1	GND	3	SCL (+3.3 Volts)
2	GND	4	SDA (+3.3 Volts)

3.4.5 Jumper JP5, CPU2 I²C Header

Jumper JP4 is an access point to the CPU2's I²C signals. The mapping of the header is shown in the figure below.



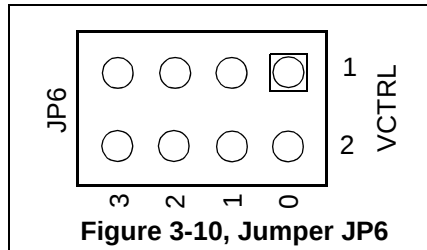
The signals on each pin are shown in the table.

Table 24: Jumper JP4, CPU2 I²C Header

Position	Signal	Position	Signal
1	GND	3	SCL (+3.3 Volts)
2	GND	4	SDA (+3.3 Volts)

3.4.6 Jumper JP6, Voltage Control Override CPU1

The C6474 device incorporates smart reflex power supply circuitry to adjust the core voltage on the device. JP6 is an override jumper that allows the user to force the pins off. Shorting positions 1-2, 3-4, 5-6, 7-8 forces that control position off. The jumper can be used in any combination of the above sequence to vary the core voltage. This is not recommended in general practice. In general practice the C6474 device itself will set these voltage control pins. The layout of the jumper is shown below.



The function of each jumper setting is shown in the table below.

Table 25: Jumper JP6, Voltage Control Override CPU1

Position	Signal	Position	Signal
2	GND	1	CPU1 VCNTL0
4	GND	3	CPU1 VCNTL1
6	GND	5	CPU1 VCNTL2
8	GND	7	CPU1 VCNTL3

Table 26: Jumper JP6, Voltage Selection

VCNTL #	VCNTL[3:0]	CV _{DD}
0	0000	0.900
1	0001	0.920
2	0010	0.940
3	0011	0.960
4	0100	0.980
5	0101	1.00
6	0110	1.02
7	0111	1.04
8	1000	1.06
9	1001	1.08
10	1010	1.10
11	1011	1.12
12	1100	1.14
13	1101	1.16
14	1110	1.18
15	1111	1.20

3.4.7 Jumper JP7, Voltage Control Override CPU2

The C6474 device incorporates smart reflex power supply circuitry to adjust the core voltage on the device. JP7 is an override jumper that allows the user to force the pins off. Shorting positions 1-2, 3-4, 5-6, 7-8 forces that control position off. The jumper can be used in any combination of the above sequence to vary the core voltage. This is not recommended in general practice. In general practice the C6474 device itself will set these voltage control pins. The layout of the jumper is shown below.

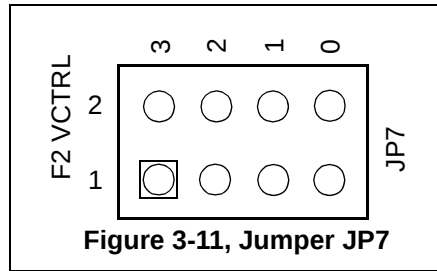


Figure 3-11, Jumper JP7

The function of each jumper setting is shown in the table below.

Table 27: Jumper JP7, Voltage Control Override CPU2

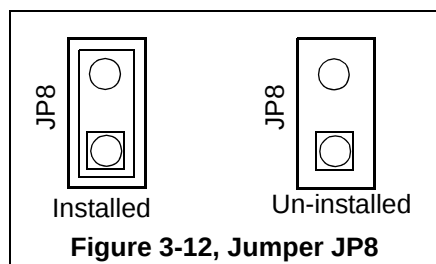
Position	Signal	Position	Signal
2	GND	1	CPU2 VCNTL0
4	GND	3	CPU2 VCNTL1
6	GND	5	CPU2 VCNTL2
8	GND	7	CPU2 VCNTL3

Table 28: Jumper JP7, Voltage Selection

VCNTL #	VCNTL[3:0]	CV _{DD}
0	0000	0.900
1	0001	0.920
2	0010	0.940
3	0011	0.960
4	0100	0.980
5	0101	1.00
6	0110	1.02
7	0111	1.04
8	1000	1.06
9	1001	1.08
10	1010	1.10
11	1011	1.12
12	1100	1.14
13	1101	1.16
14	1110	1.18
15	1111	1.20

3.4.8 Jumper JP8, SYNC Burst

Jumper JP8 is a 2 position jumper which allows the Sync burst pin of the C6474 CPU1 to be connected to the Sync Burst pin of CPU2. The normal configuration is to short this jumper. The jumper is shown in the figure below.



3.5 Test Points

The TMS320C6474 Mezzanine Board has 28 test points. The position of each test point is shown in the figure below.

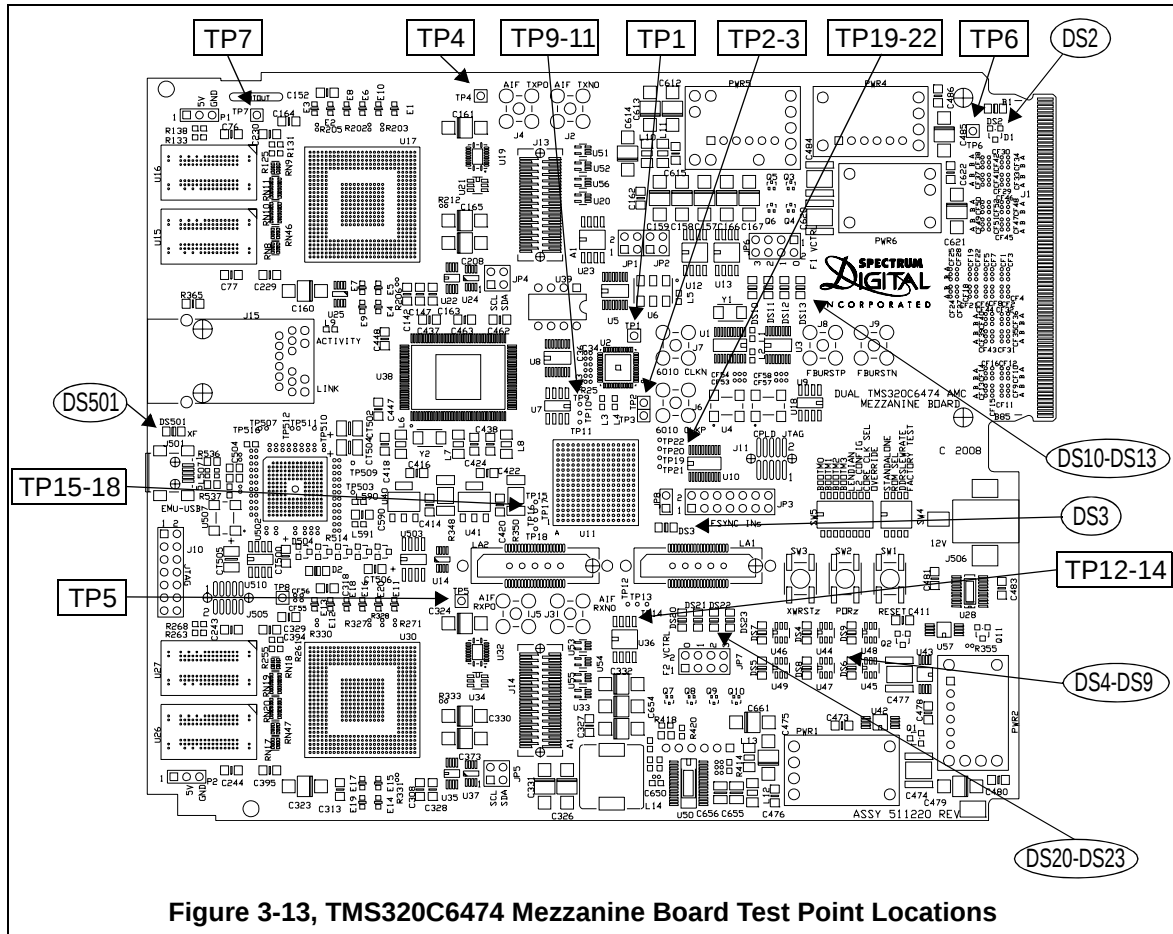


Figure 3-13, TMS320C6474 Mezzanine Board Test Point Locations

Table 29: TMS320C6474 Mezzanine Board Test Points

Test Point	Signal	Test Point	Signal
TP1	CDCL6010, Status, U2, Pin 13	TP13	F2_PORz, U11A, N3
TP2	CDCL6010, YP10, U2, Pin 46	TP14	F2_XWRSTz, U11A, P2
TP3	CDCL6010, YN10, U2, Pin 45	TP15	SRIO_CLK_EN, U11B, D6
TP4	F1_SYSCLKOUT, U17C, AD6	TP16	BURST_CLK_EN, U11B, C5
TP5	F2_SYSCLKOUT, U30C, AD6	TP17	CPU_CLKS_EN, U11B, D5
TP6	3.3V_ALT, J1, B4	TP18	U11B, A2
TP7	DVDD18MON, U17I, AG7	TP19	U11D, M12, B4.IO_49
TP9	F1_RESETSTAT, U11C, E13	TP20	U11D, R13, B4.IO_50
TP10	F1_PORz, U11C, E14	TP21	U11D, N12, B4.IO_51
TP11	F1_XWRSTz, U11C, D13	TP22	U11D, R14, B4.IO_52
TP12	F2_RESETSTAT, U11A, M4		

3.6 System LEDs

The TMS320C6474 Mezzanine Board has seventeen LEDs. Their positions on the board are indicated in Figure 3-1. The meaning of each switch are listed in the table below.

Table 30: Mezzanine Board LEDs

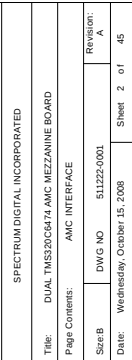
Switch	Color	Meaning
DS2	Green	12 Volt Power
DS3	Red	Board Config Status
DS4	Green	+3.3 Volts Okay
DS5	Green	+2.5 Volts Okay
DS6	Green	+1.8 Volts Okay
DS7	Green	+1.1 Volts Okay
DS8	Green	CPU 1 Core Voltage Okay
DS9	Green	CPU 2 Core Voltage Okay
DS10	Green	CPU 1 User LED 0, controlled by GPO0
DS11	Green	CPU 1 User LED 1, controlled by GPO1
DS12	Green	CPU 1 User LED 2, controlled by GPO2
DS13	Green	CPU 1 User LED 3, controlled by GPO3
DS20	Green	CPU 2 User LED 0, controlled by GPO0
DS21	Green	CPU 2 User LED 1, controlled by GPO1
DS22	Green	CPU 2 User LED 2, controlled by GPO2
DS23	Green	CPU 2 User LED 3, controlled by GPO3
DS501	Green	Embedded JTAG USB Link Status

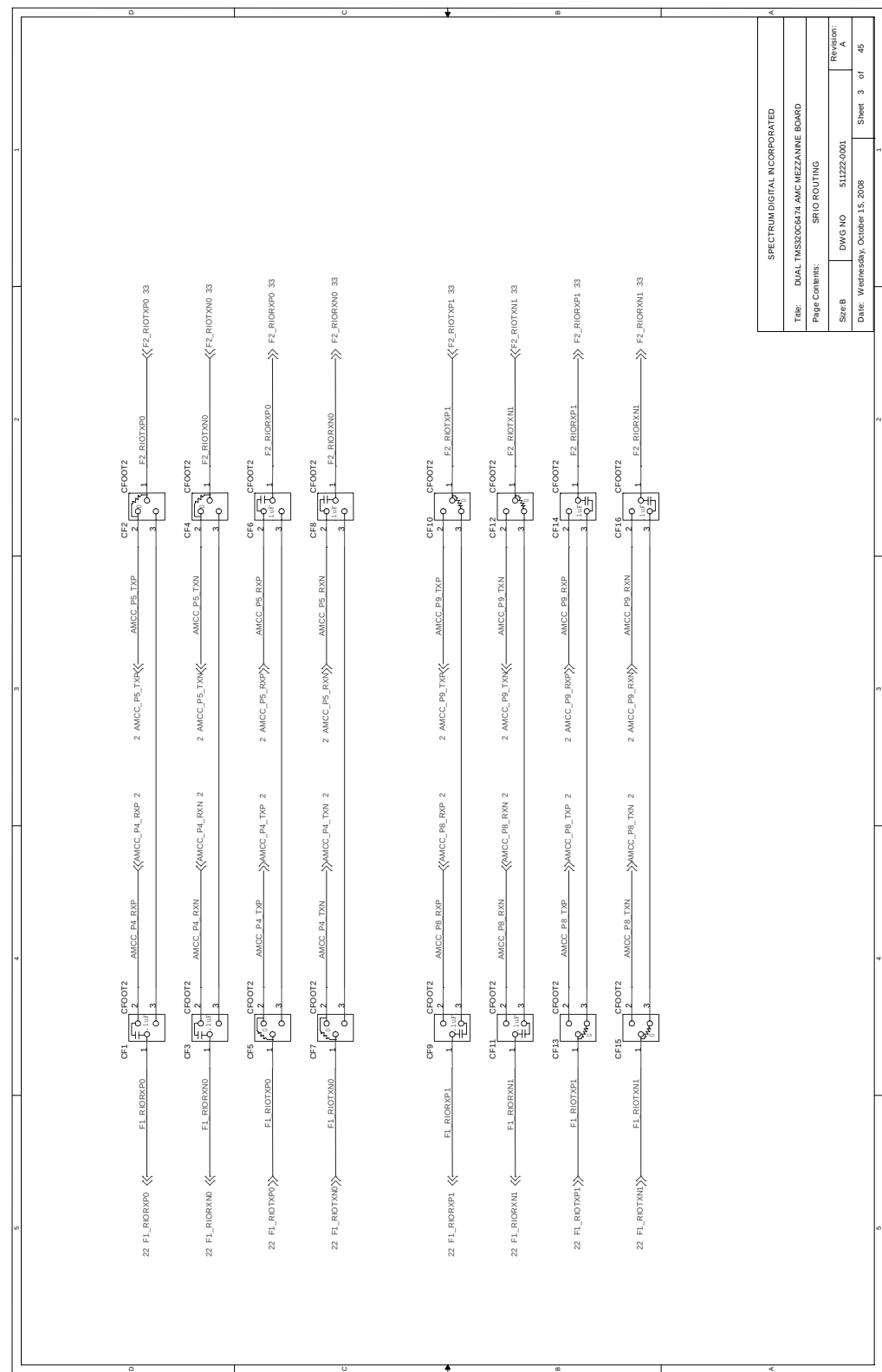
Appendix A

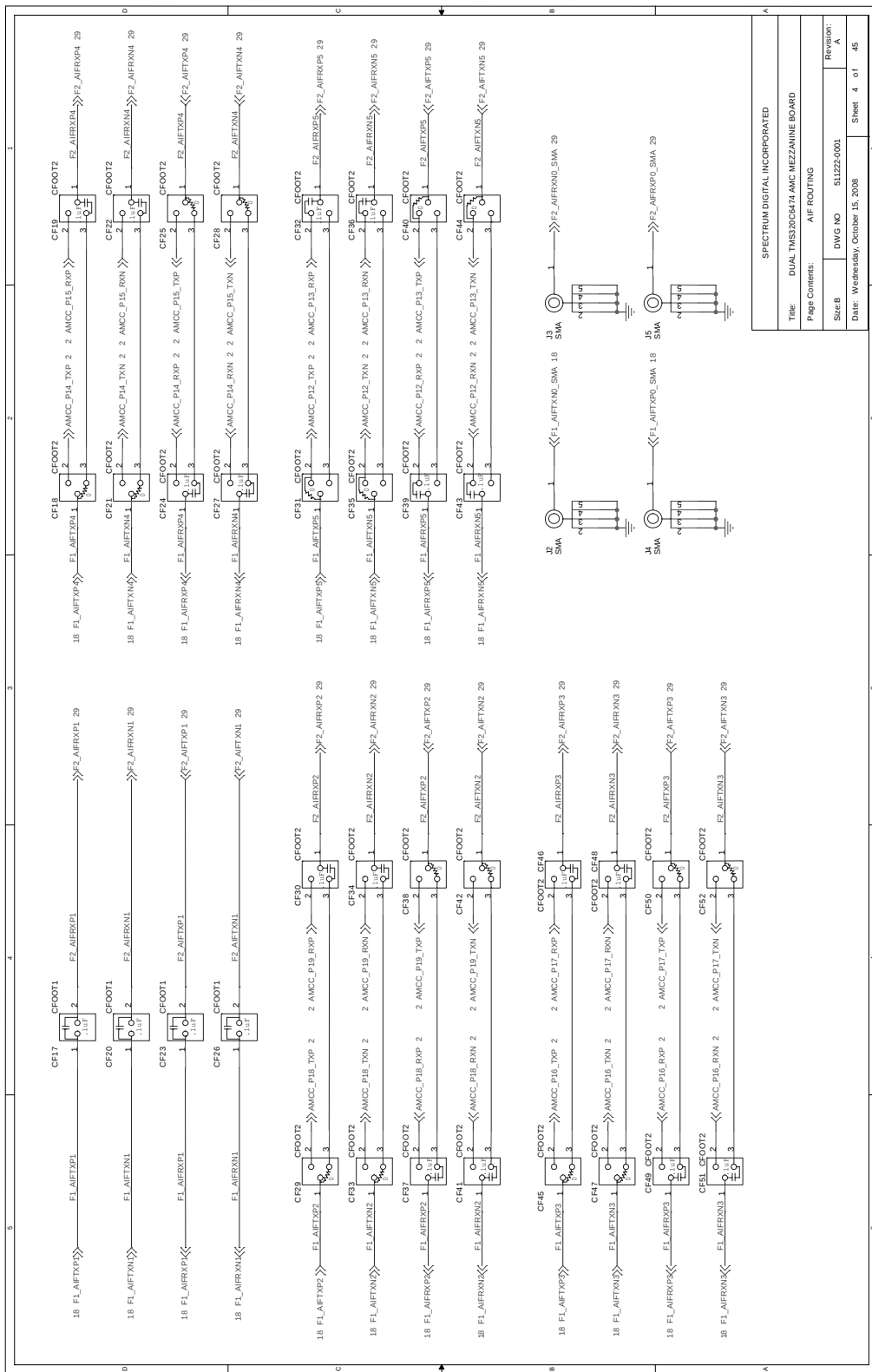
Schematics

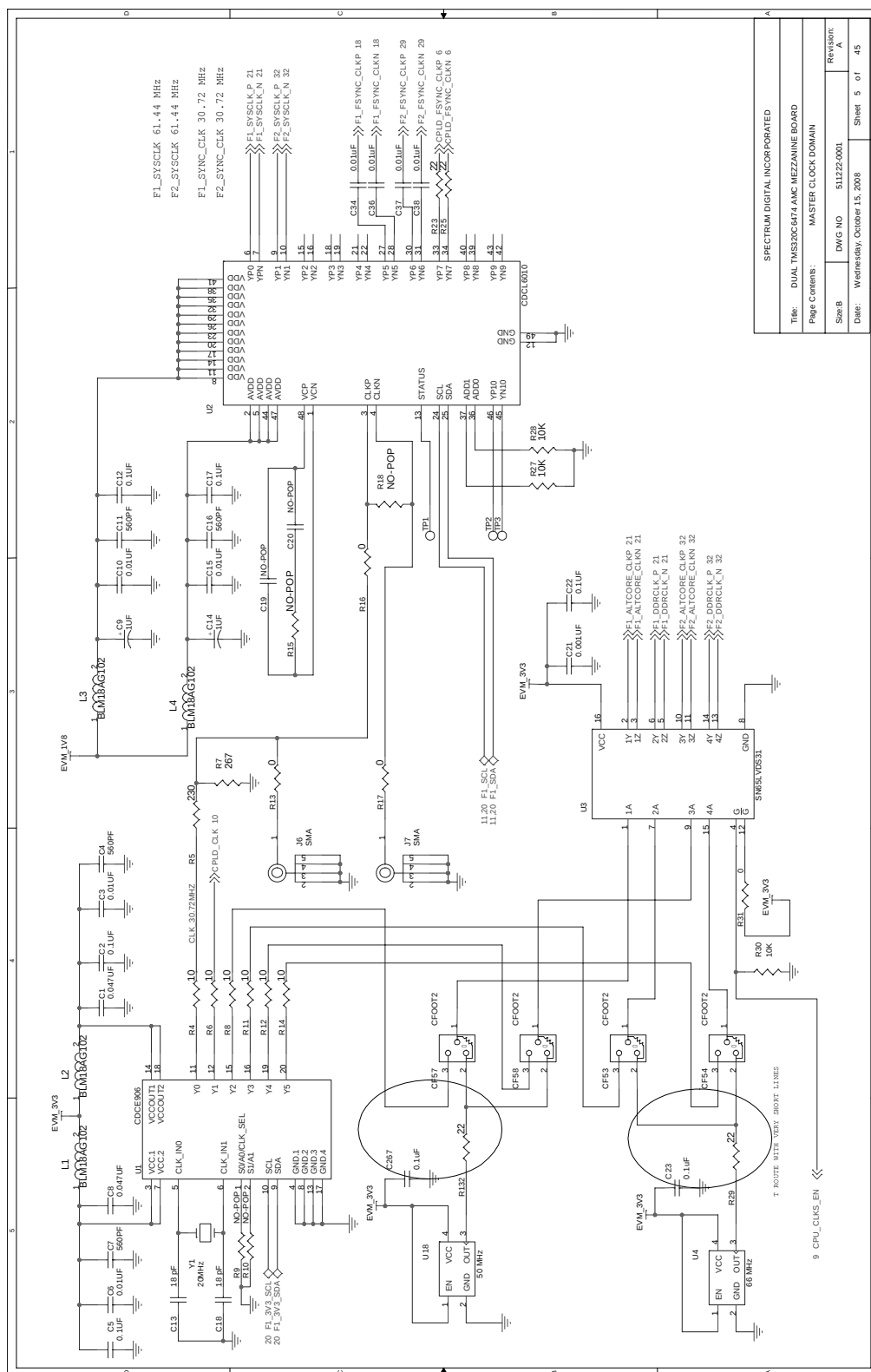
This appendix contains the schematics for the TMS320C6474 Mezzanine Board.

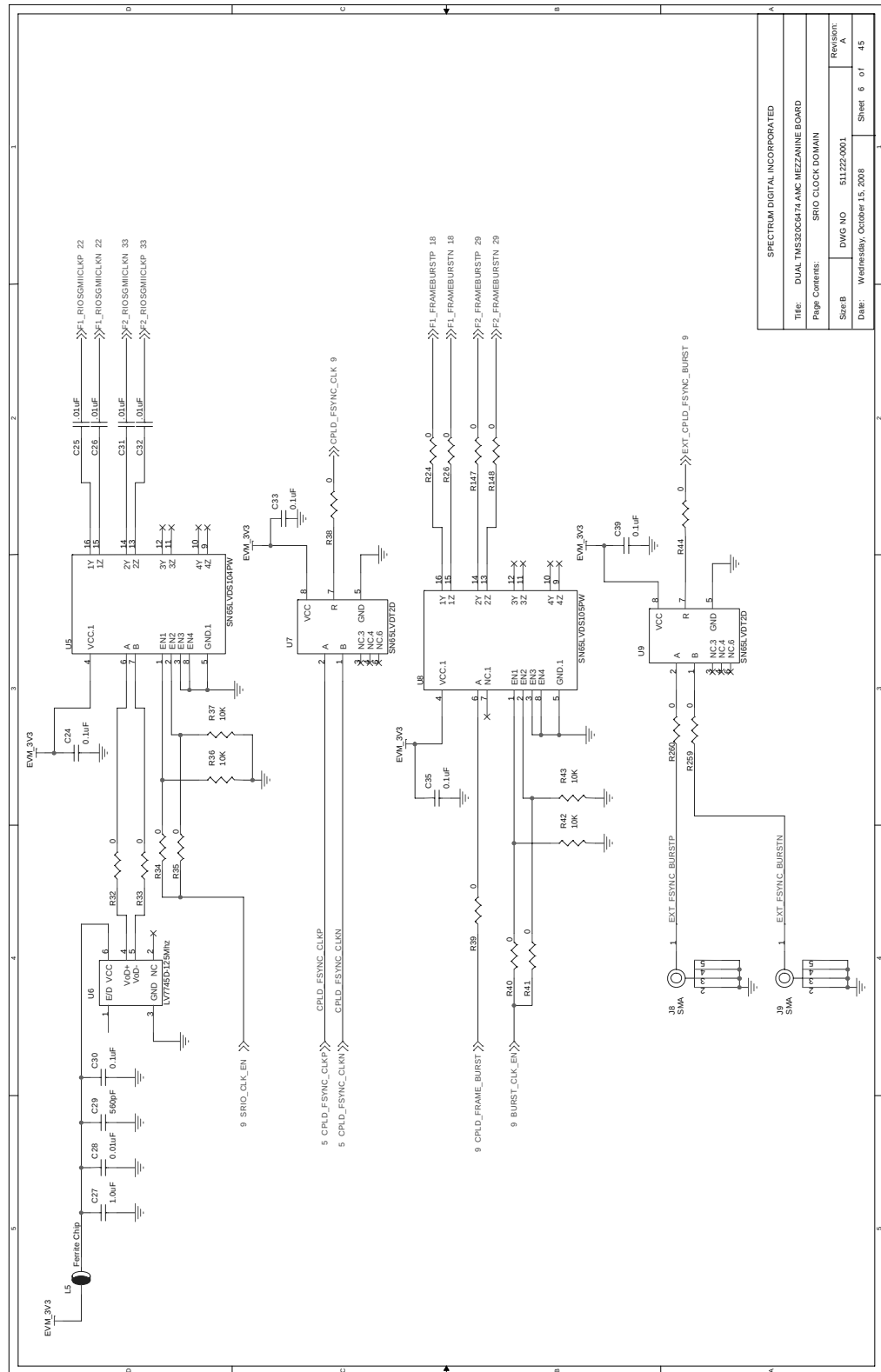
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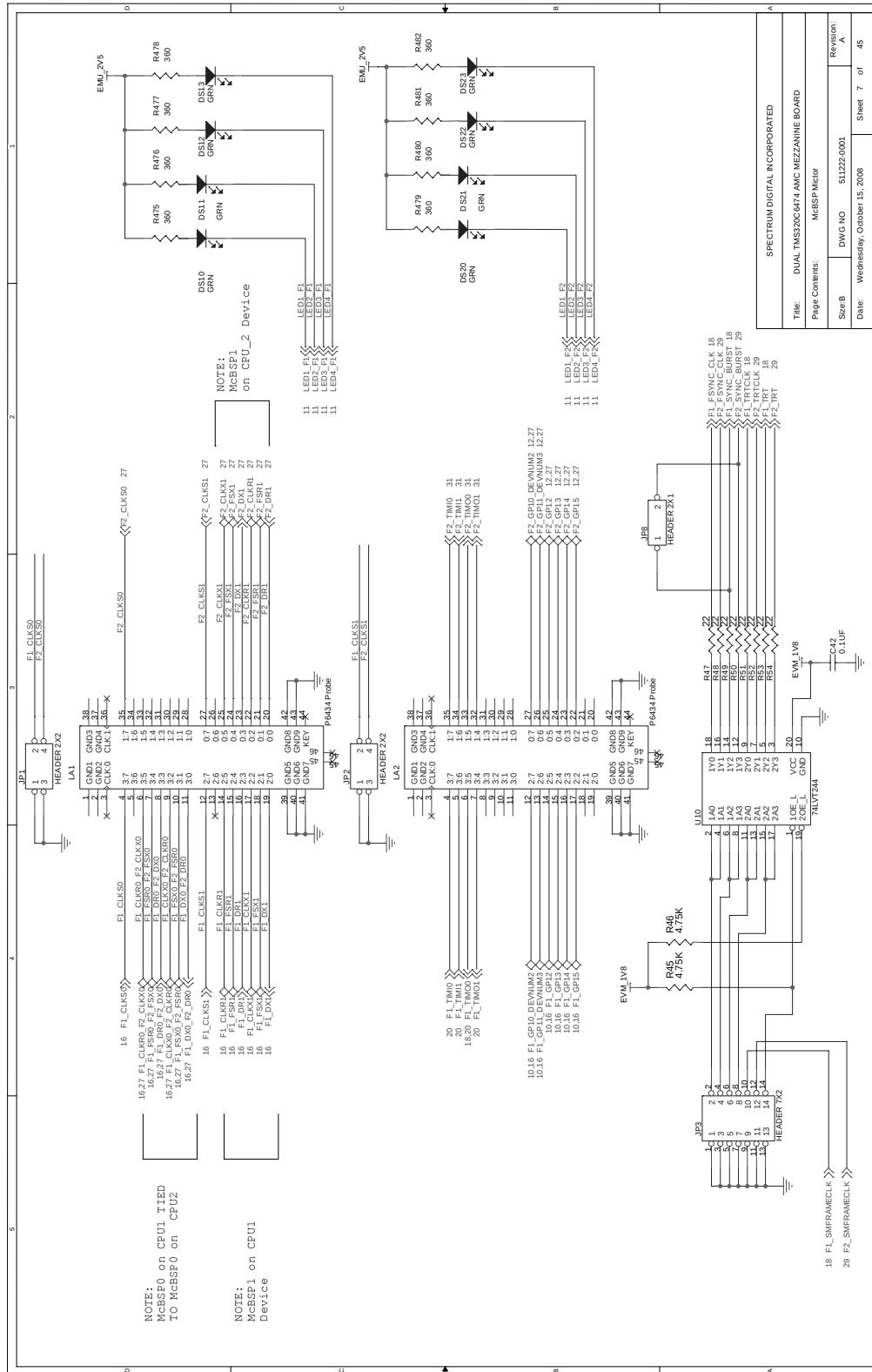


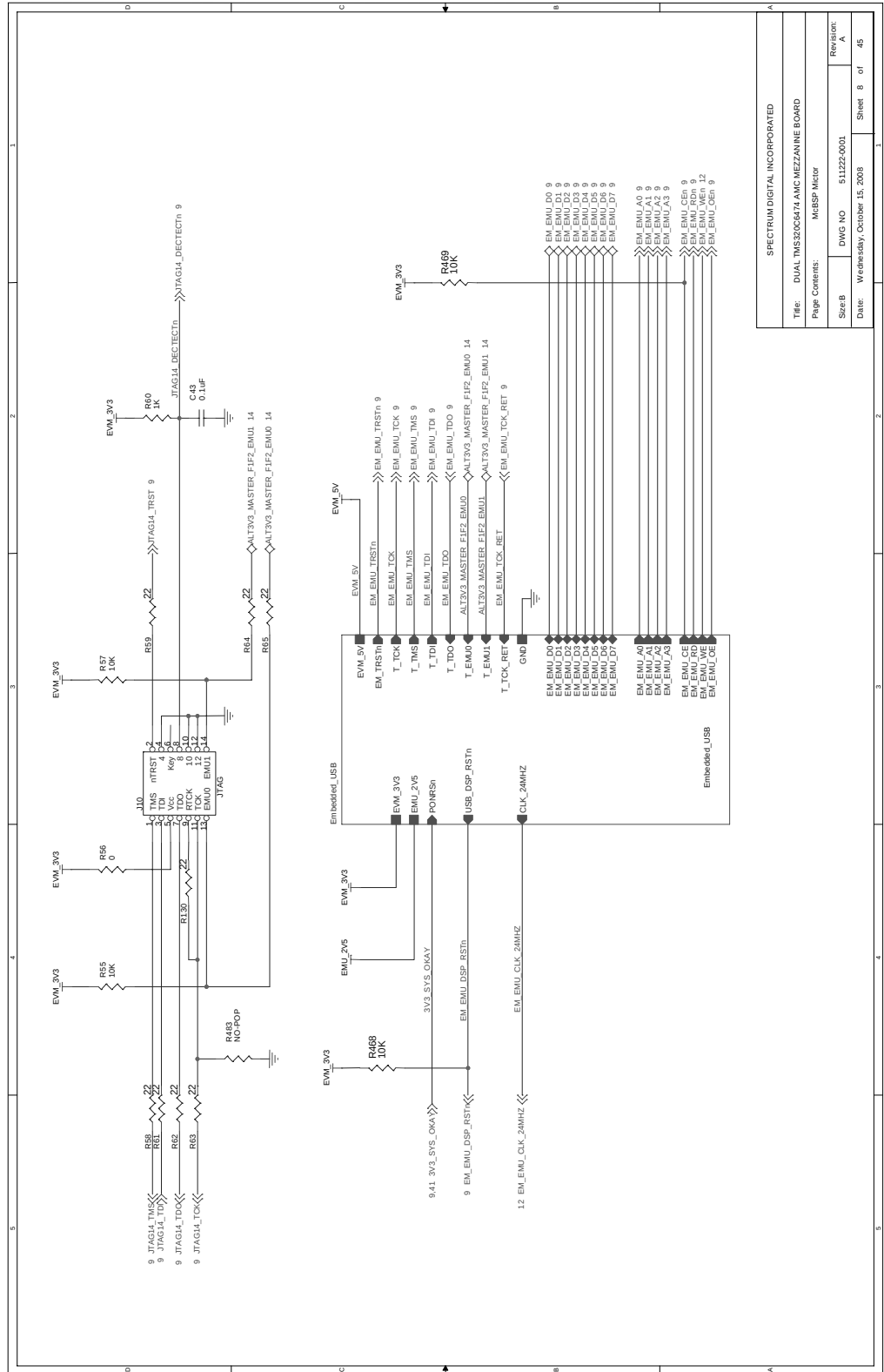


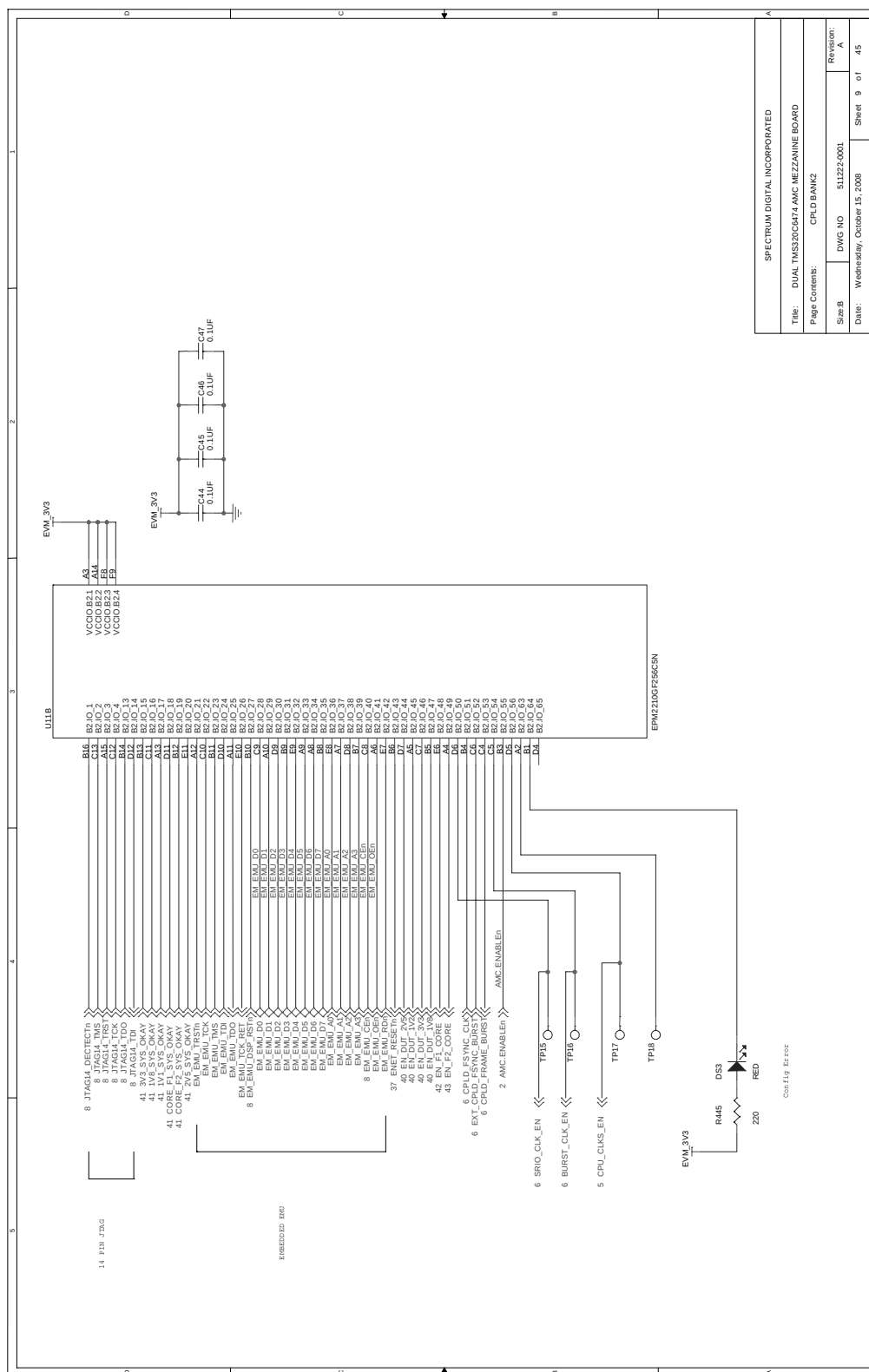




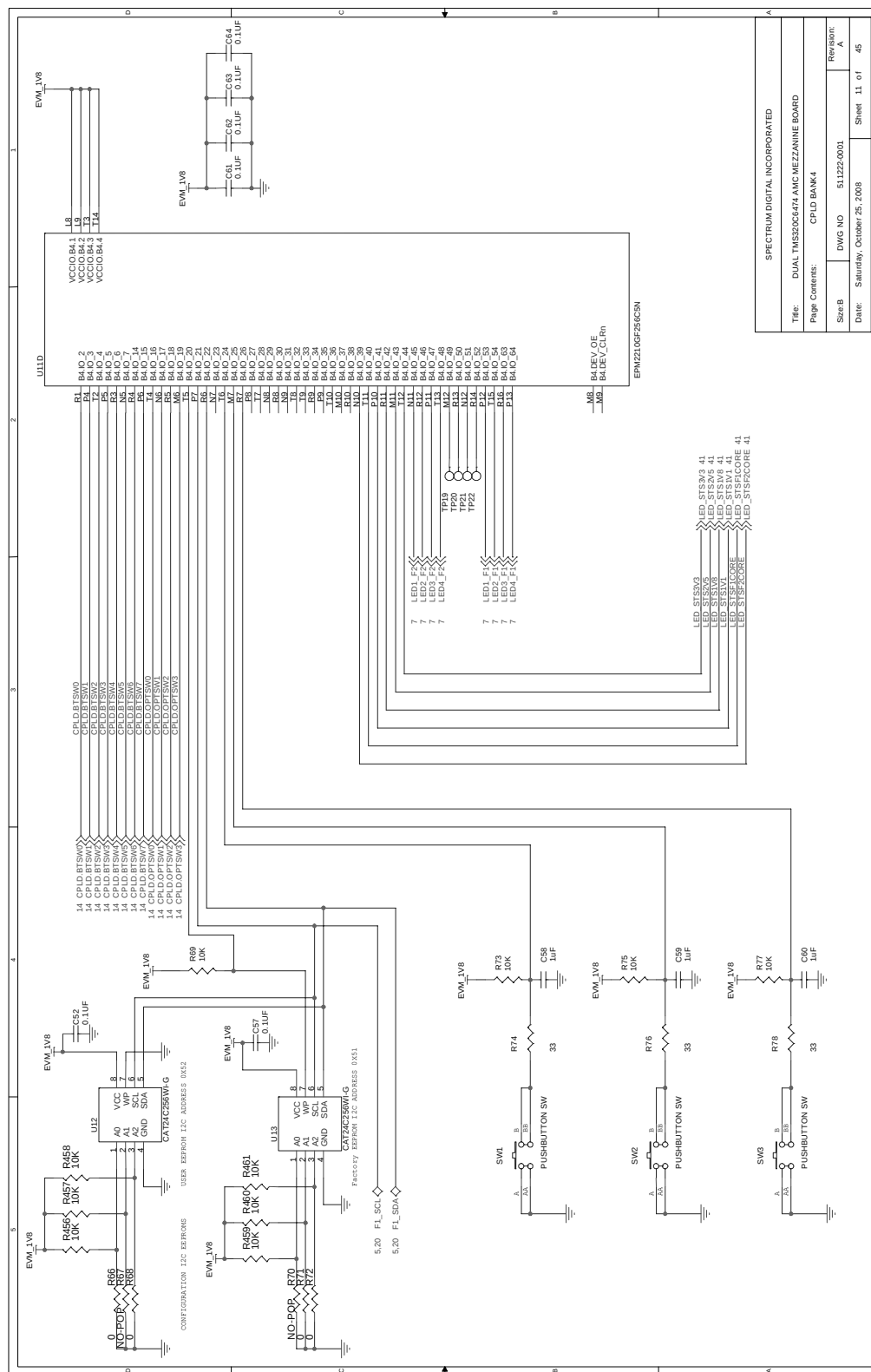
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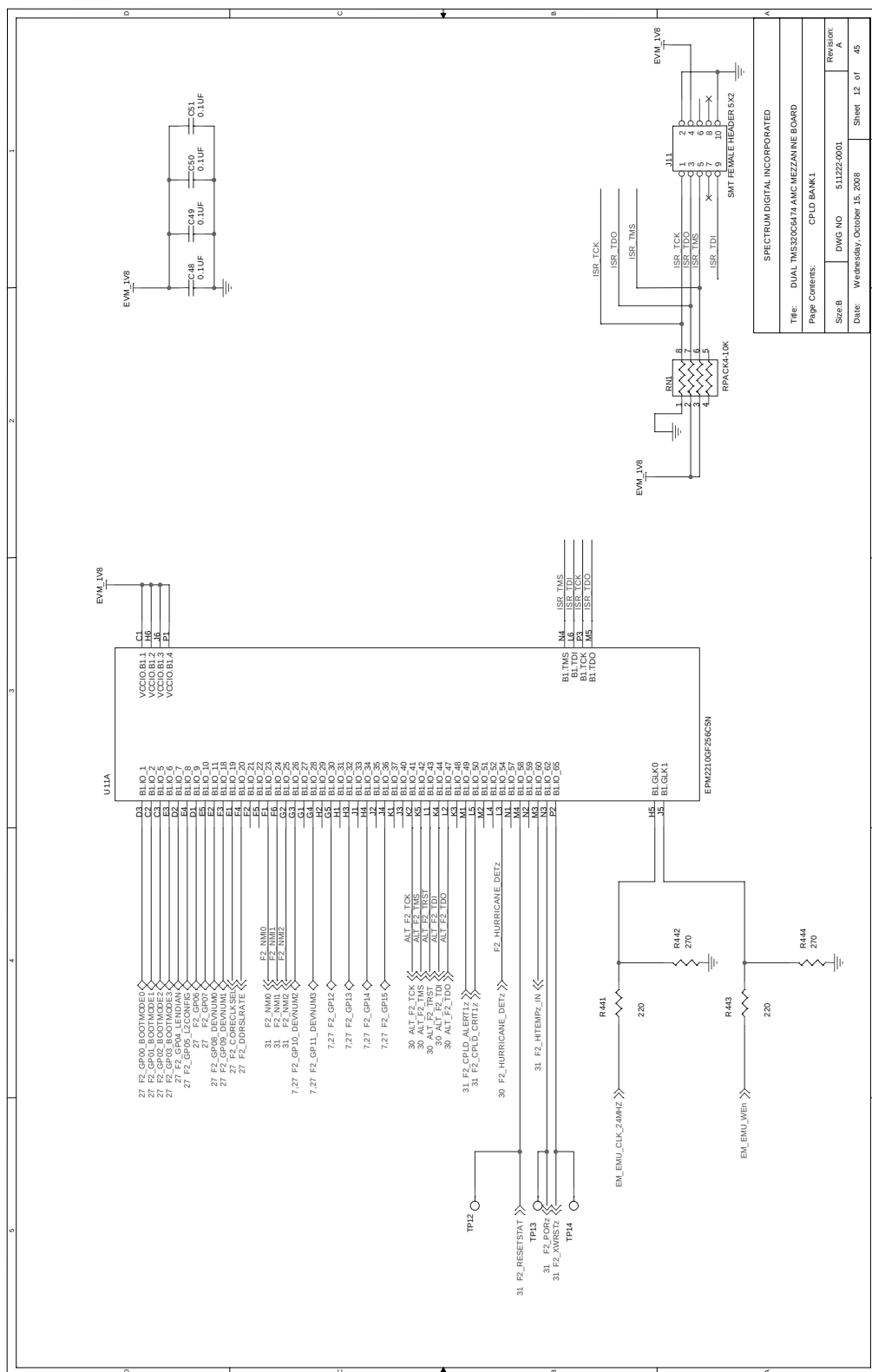


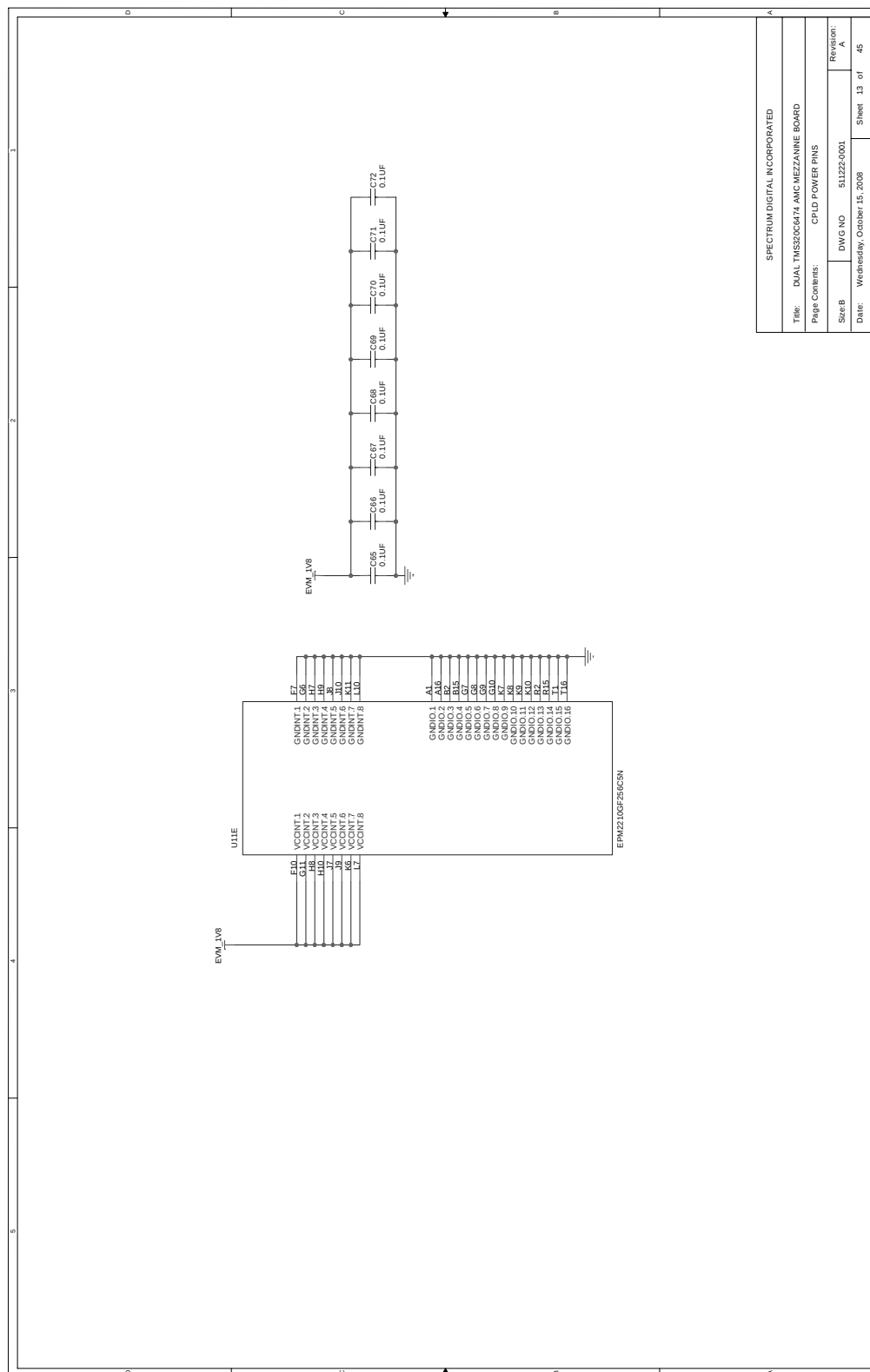


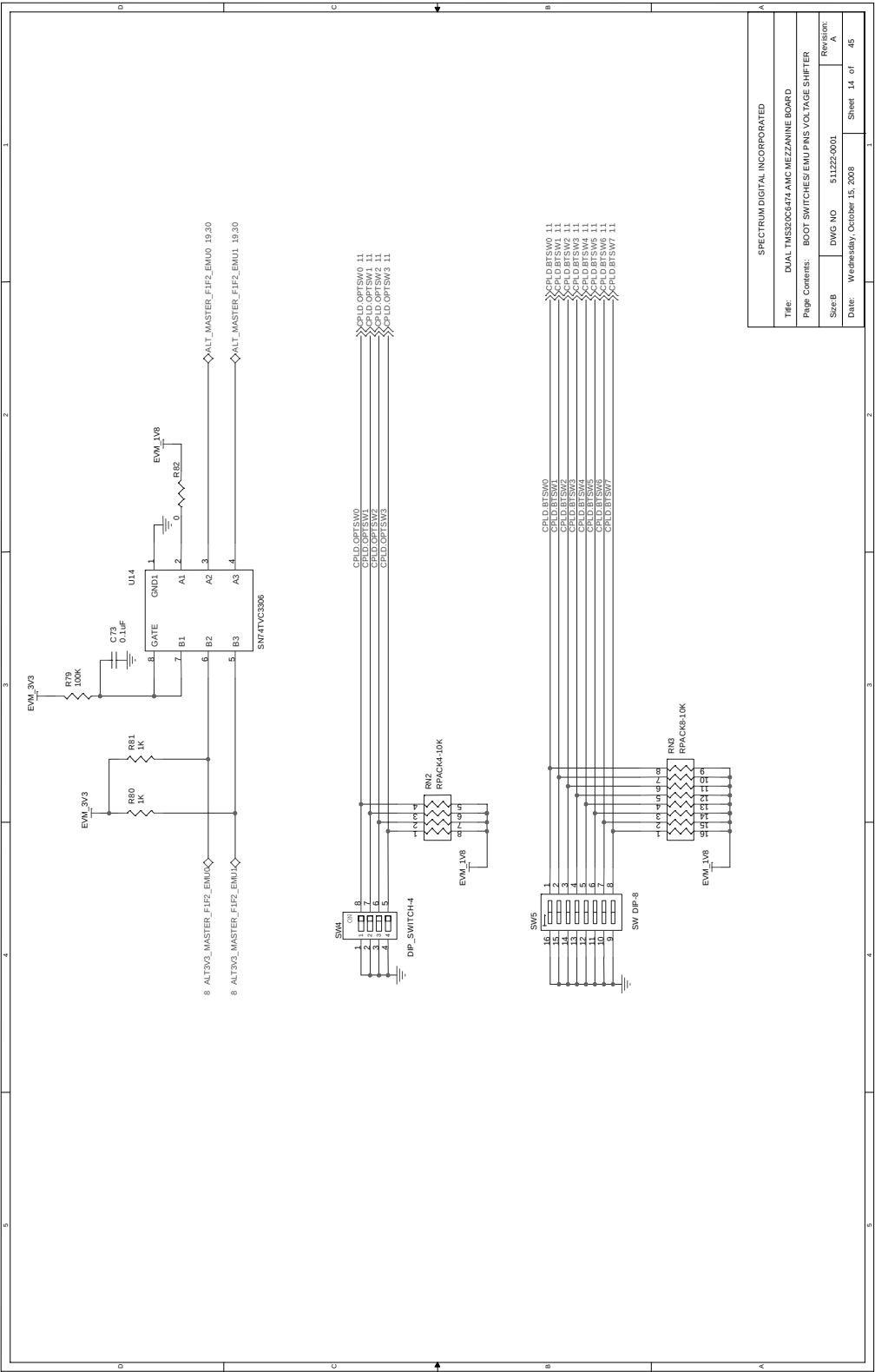


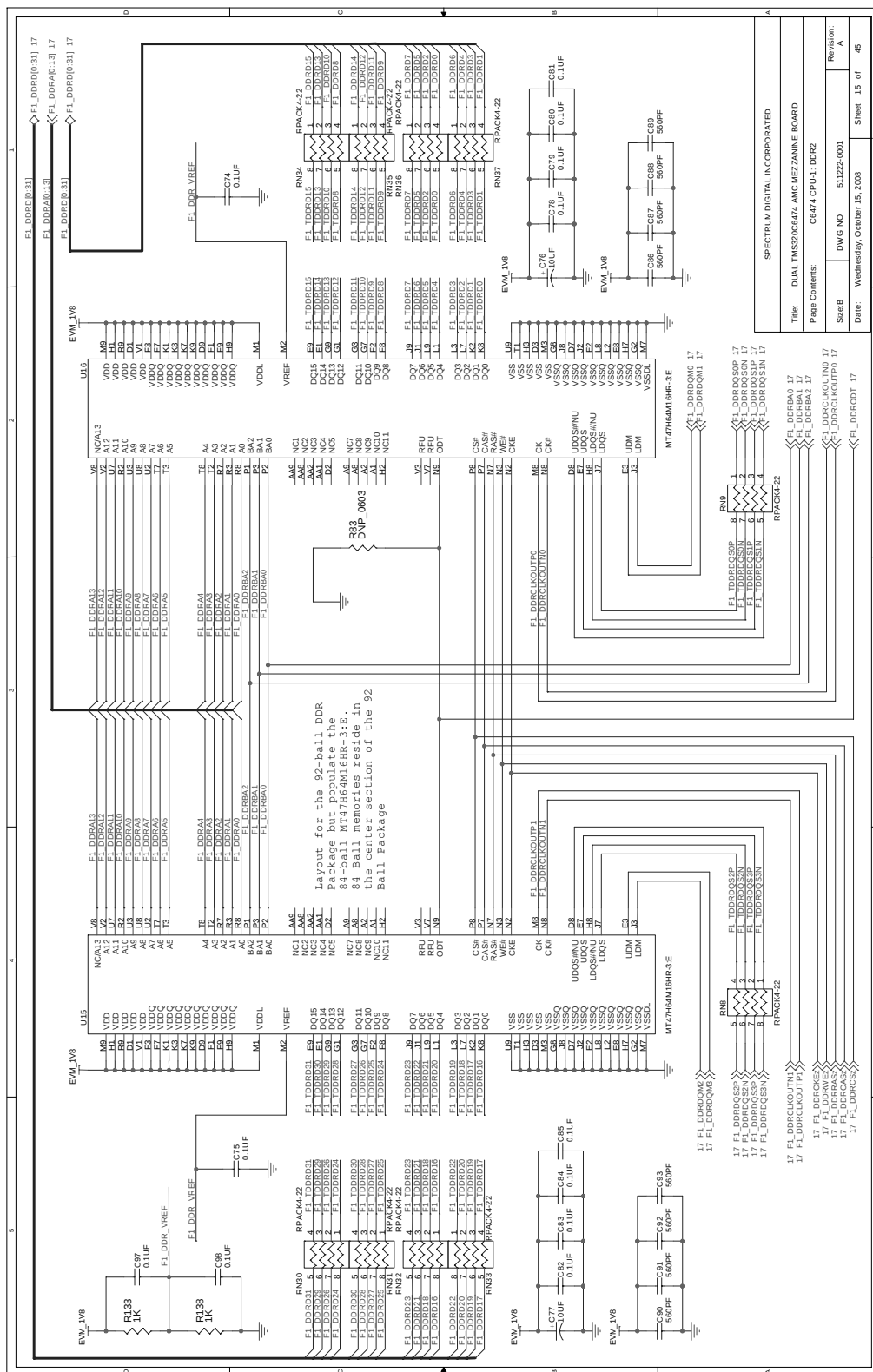


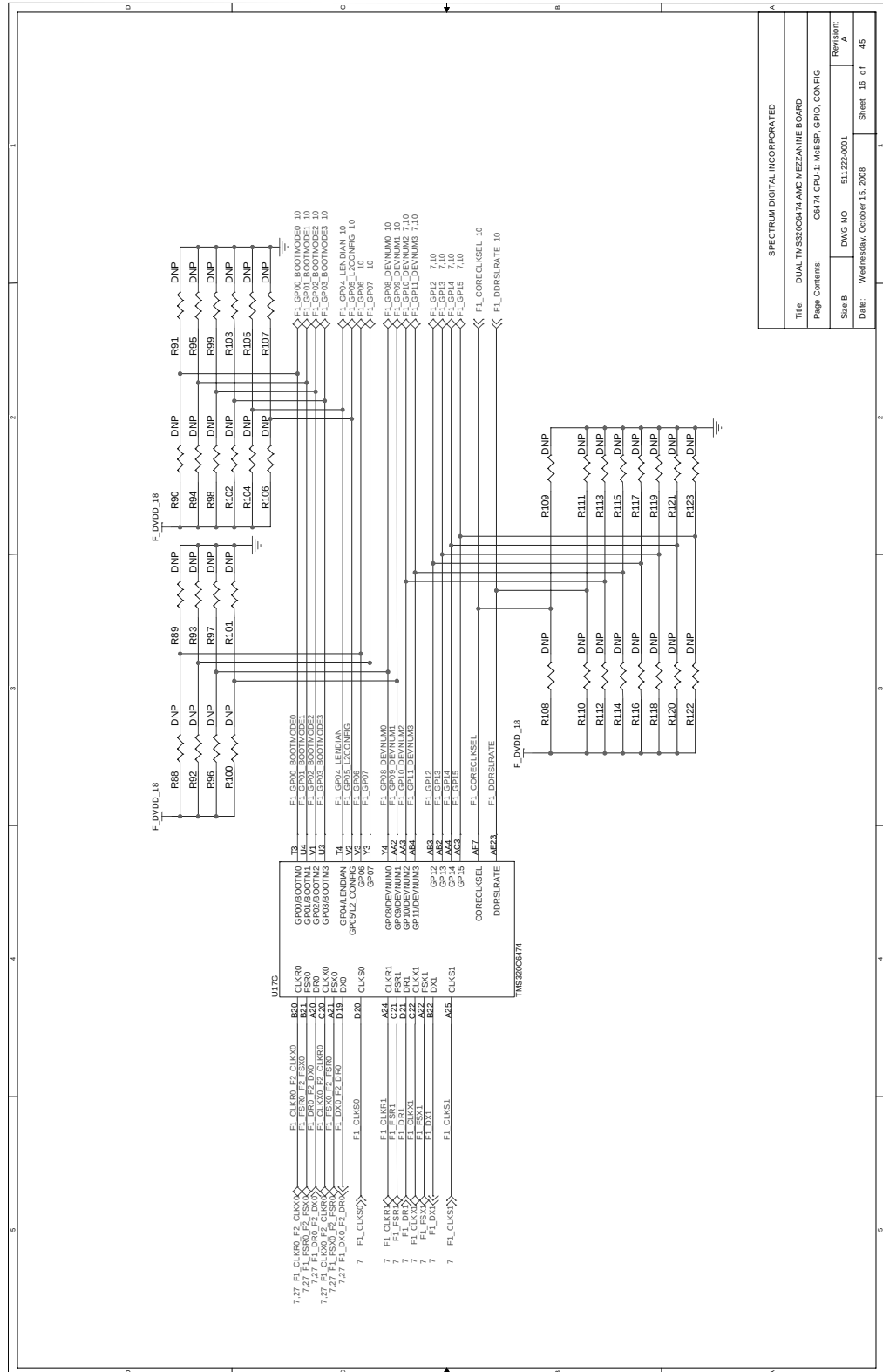


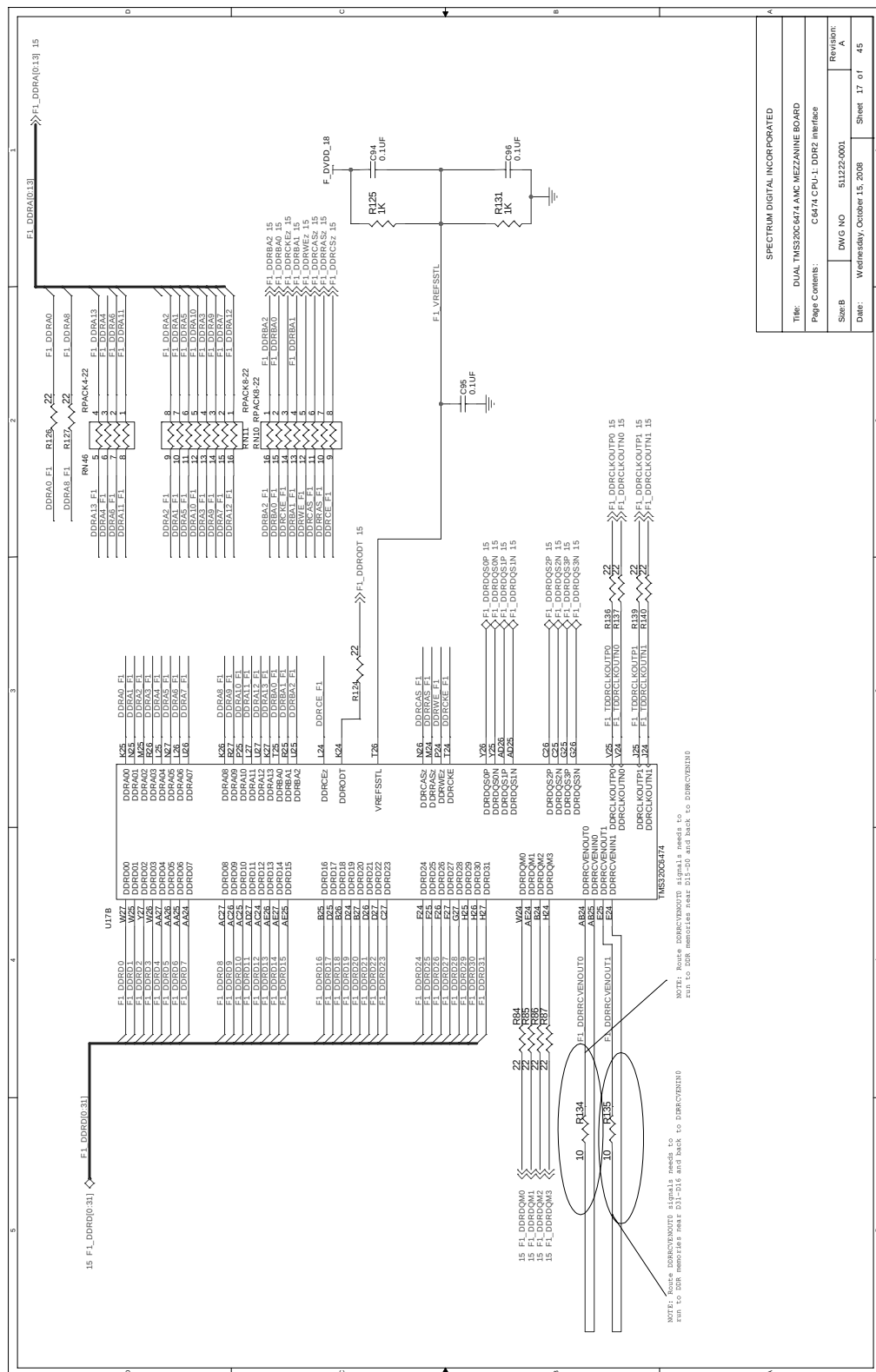


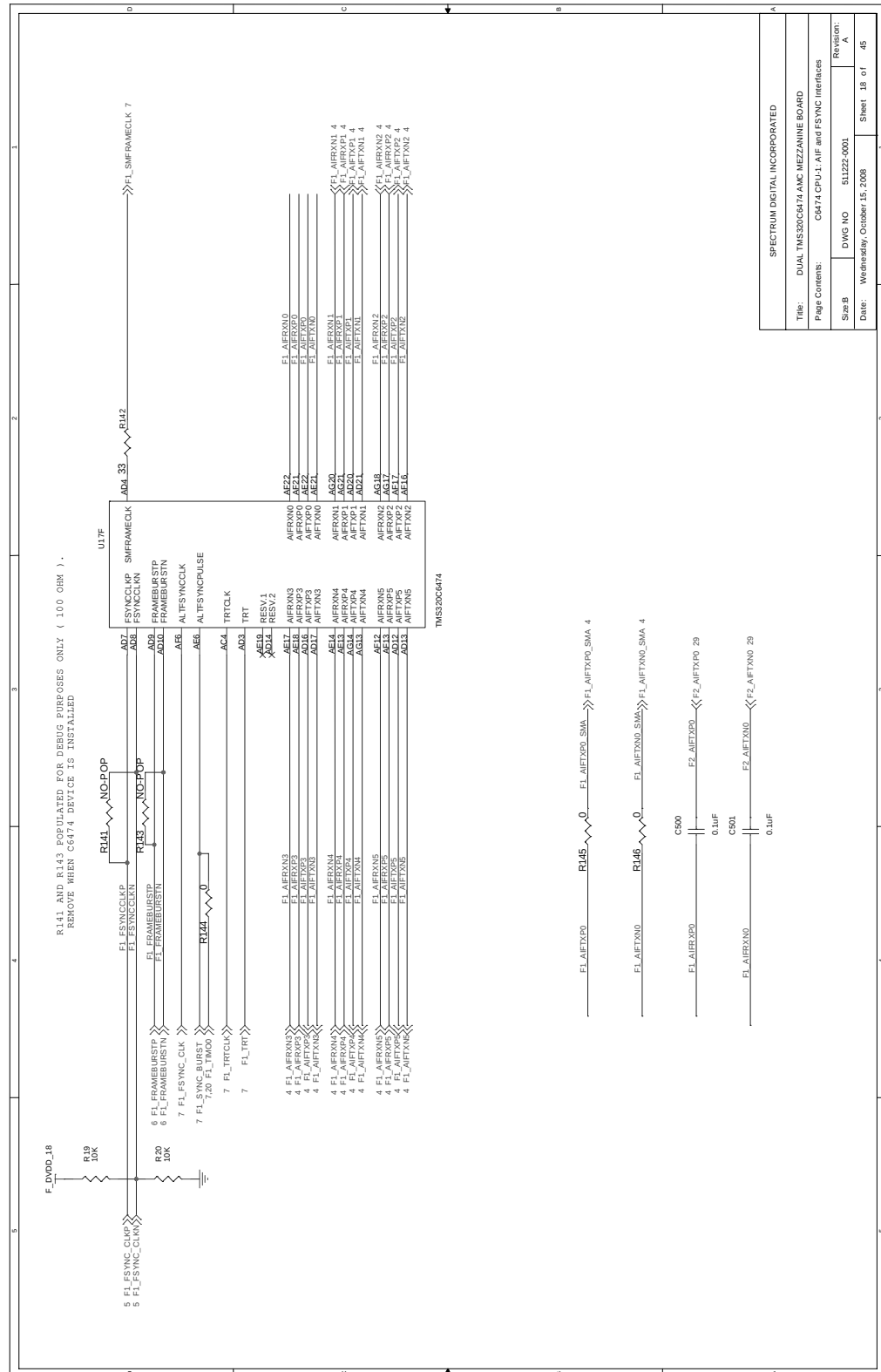


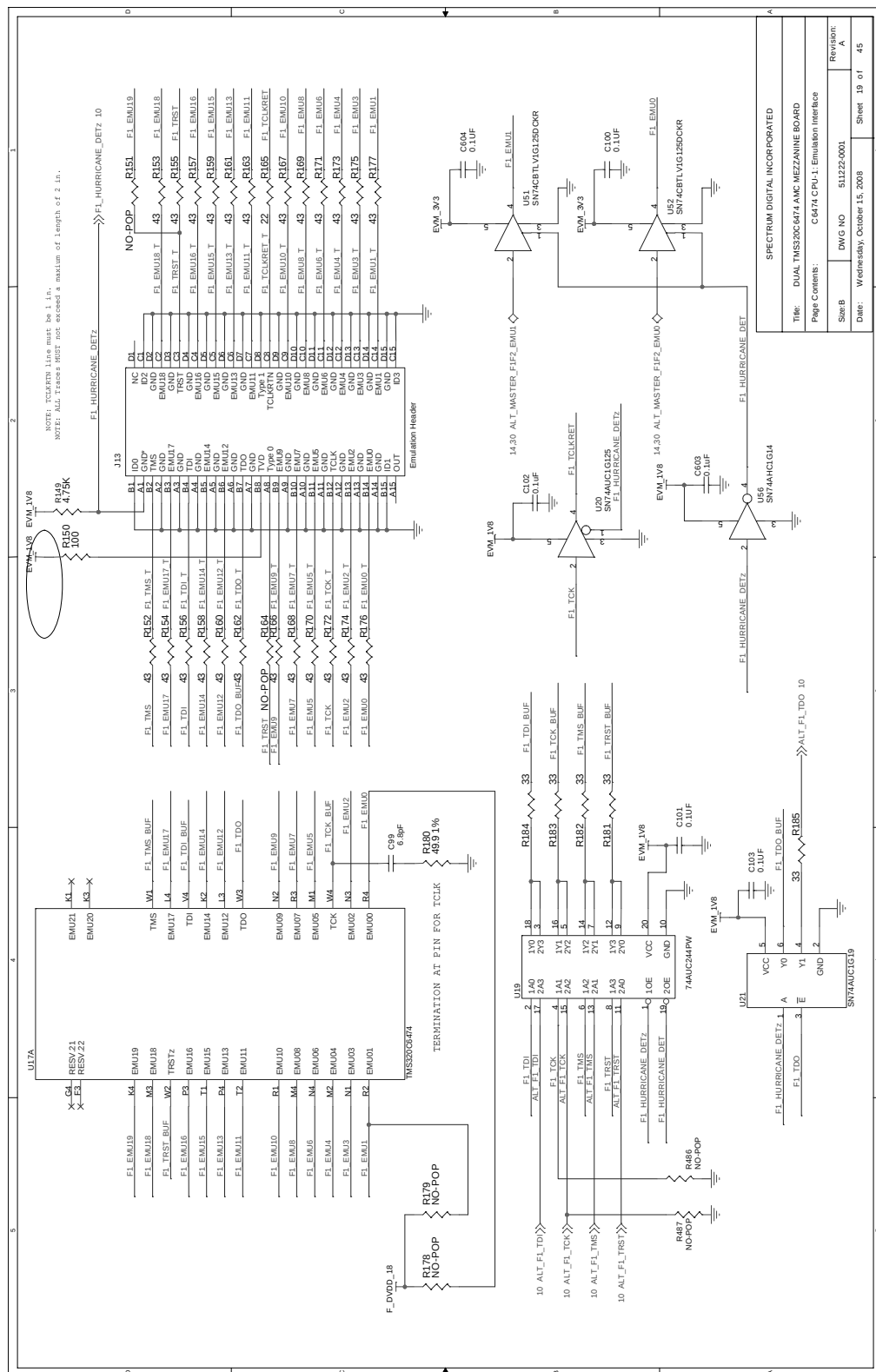


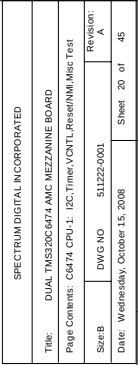




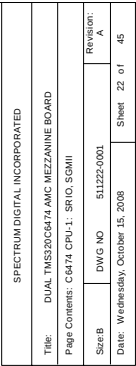


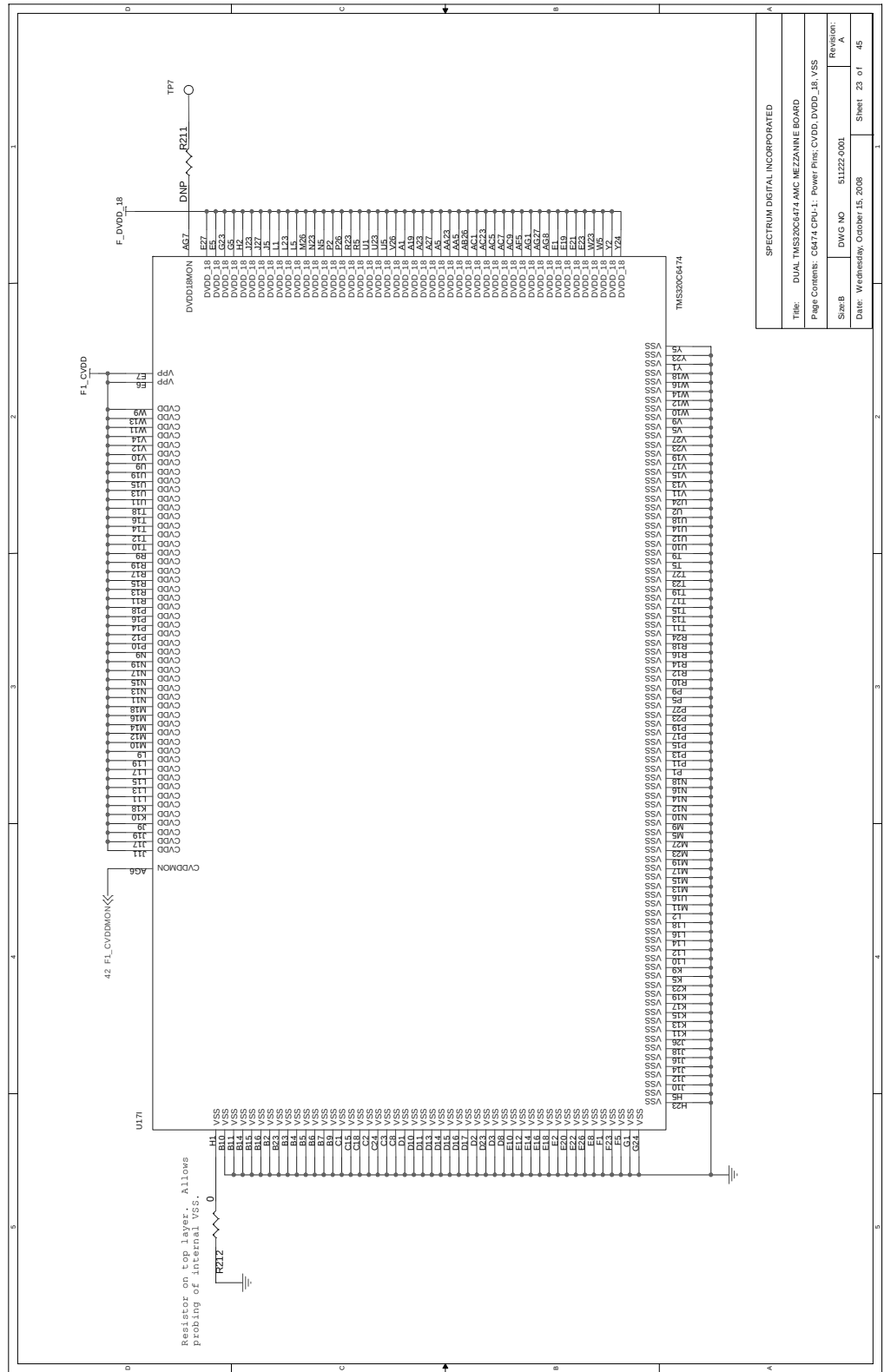


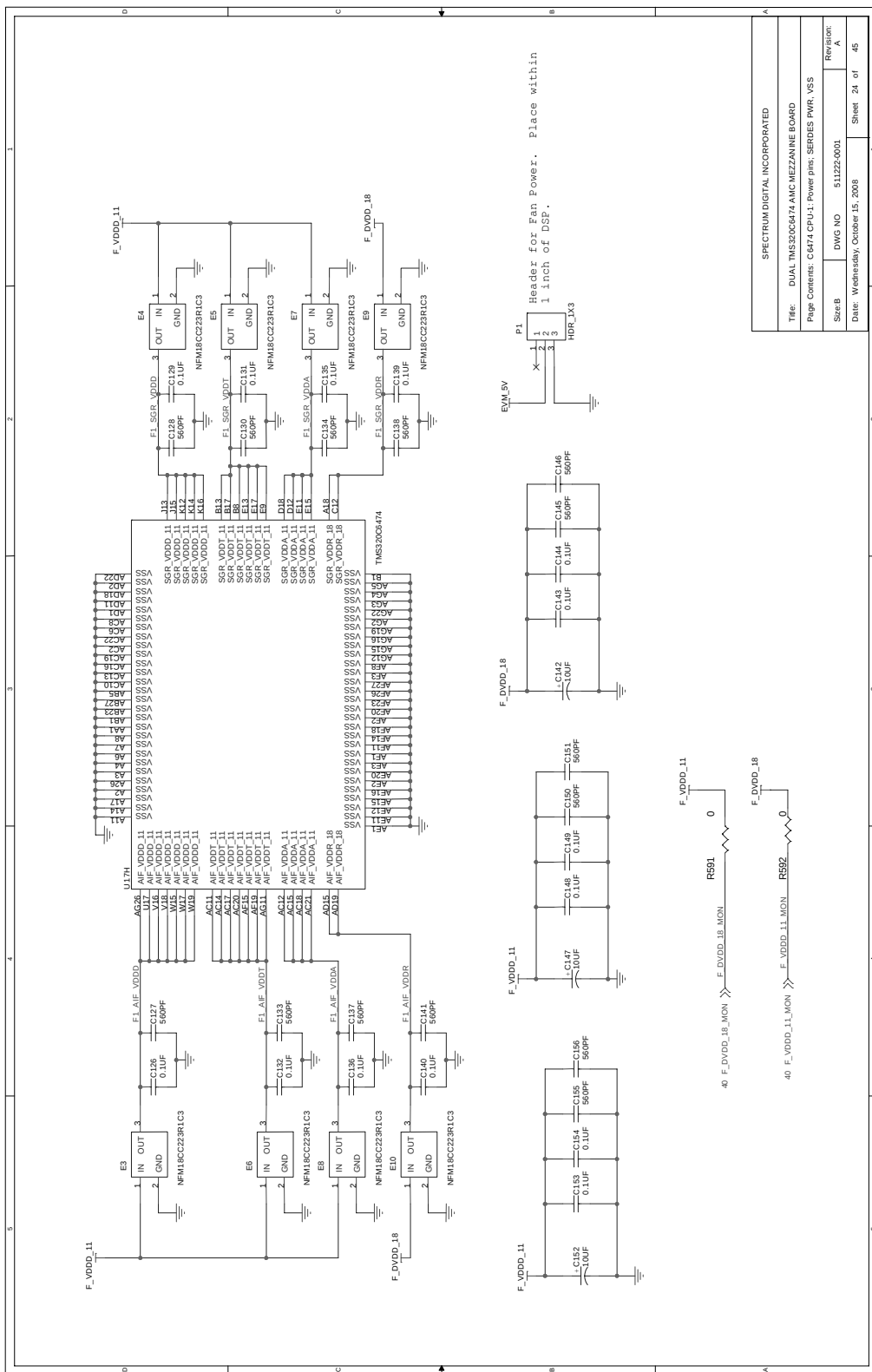


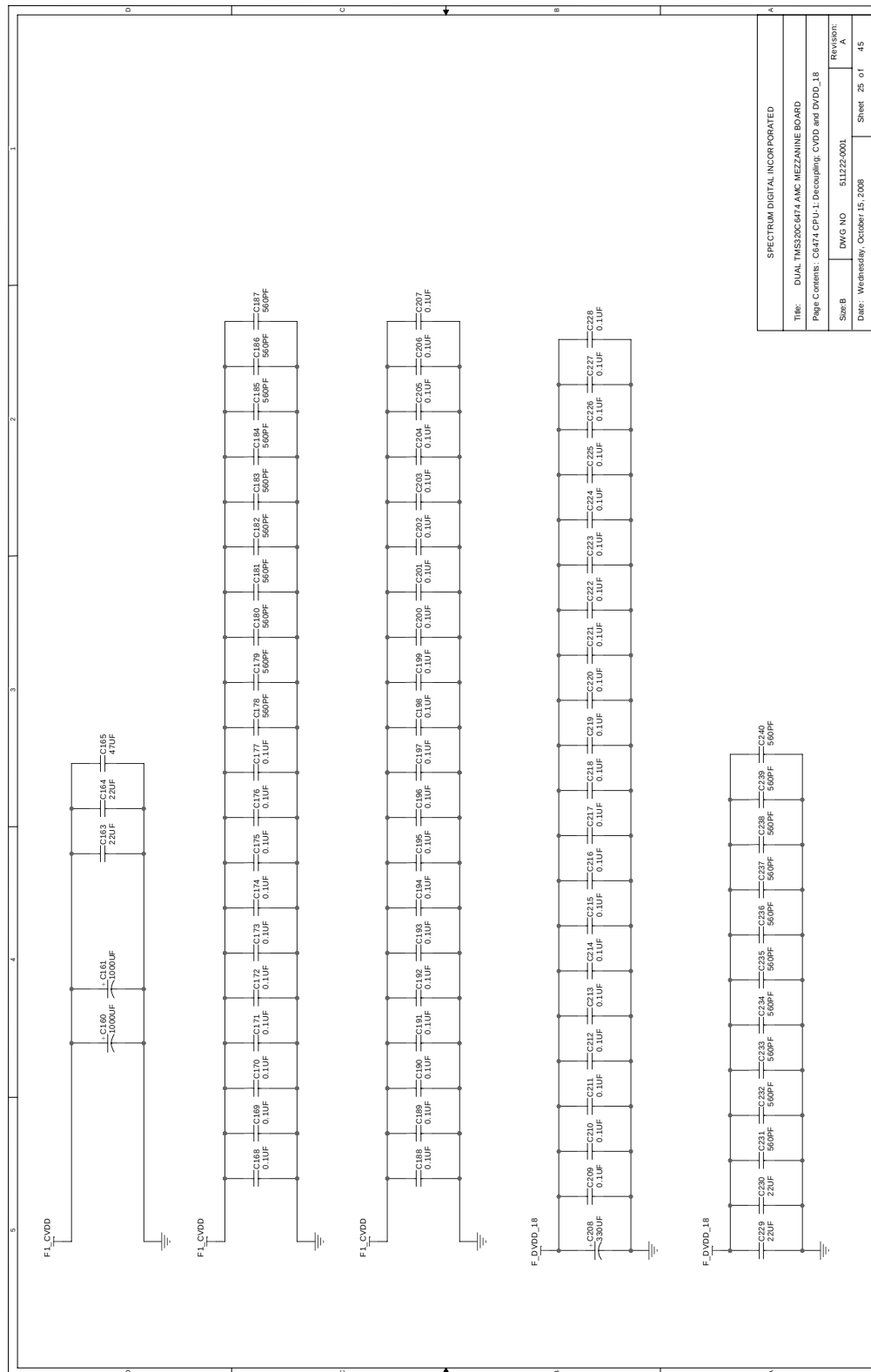


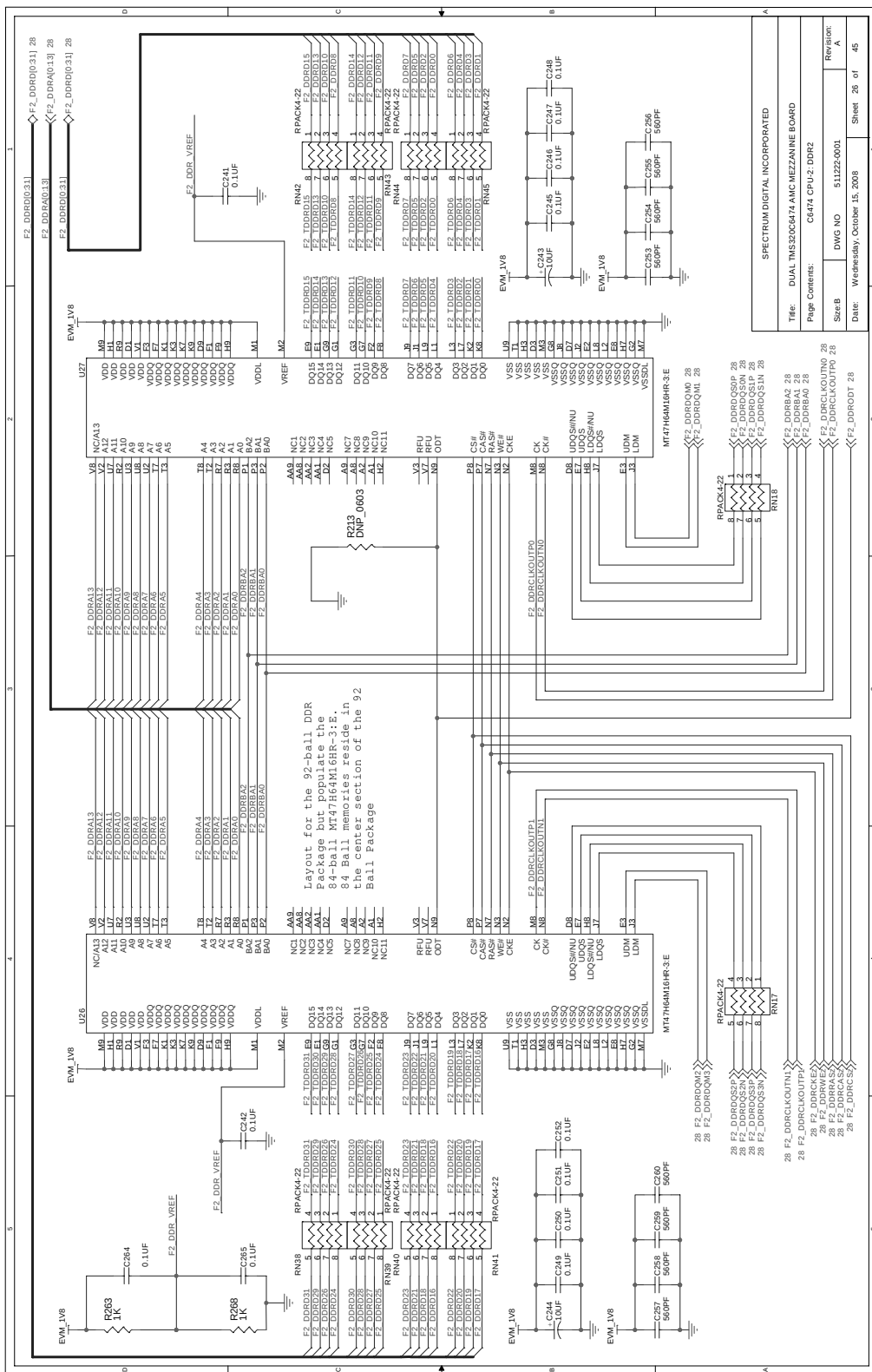


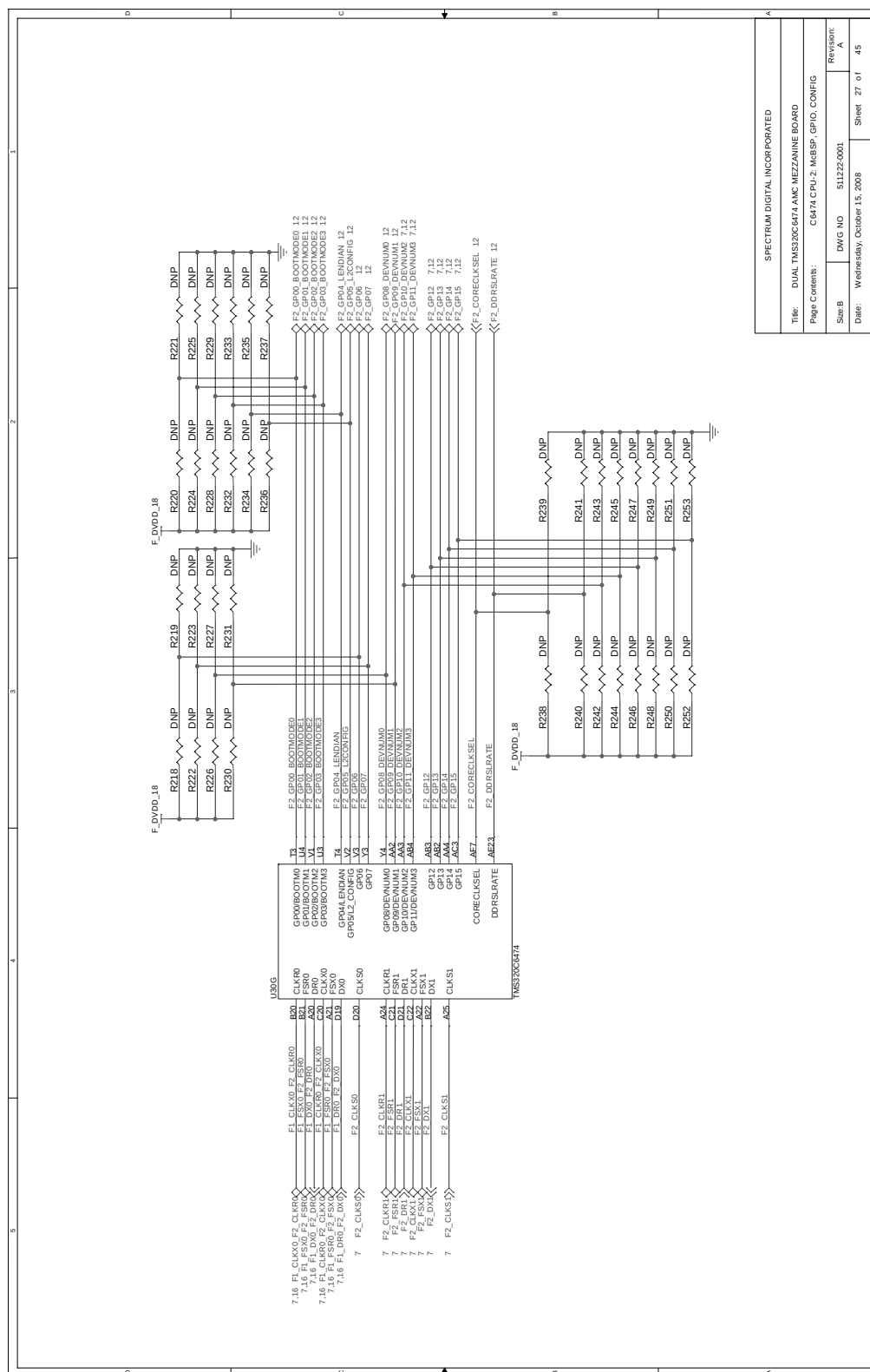


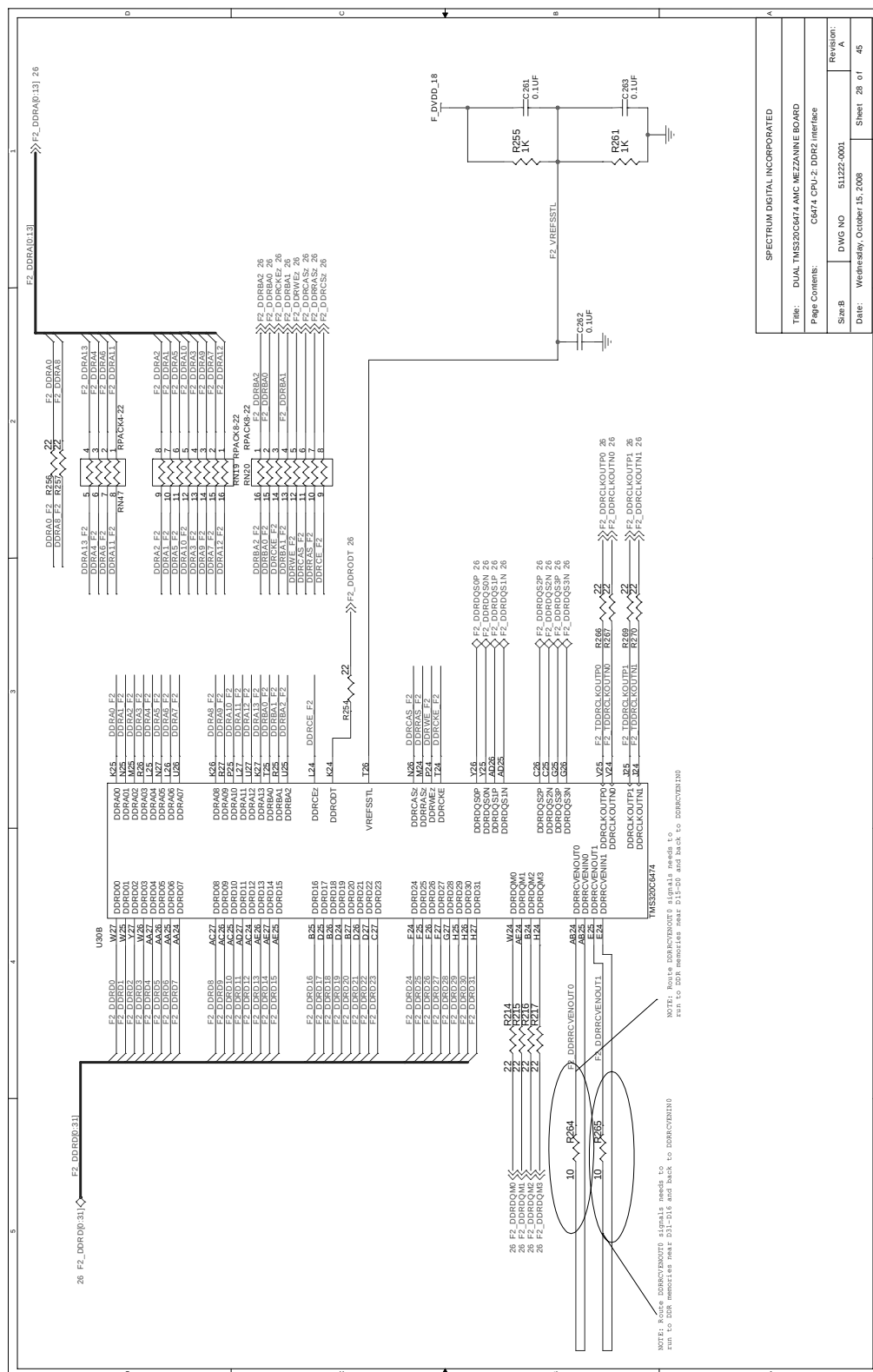


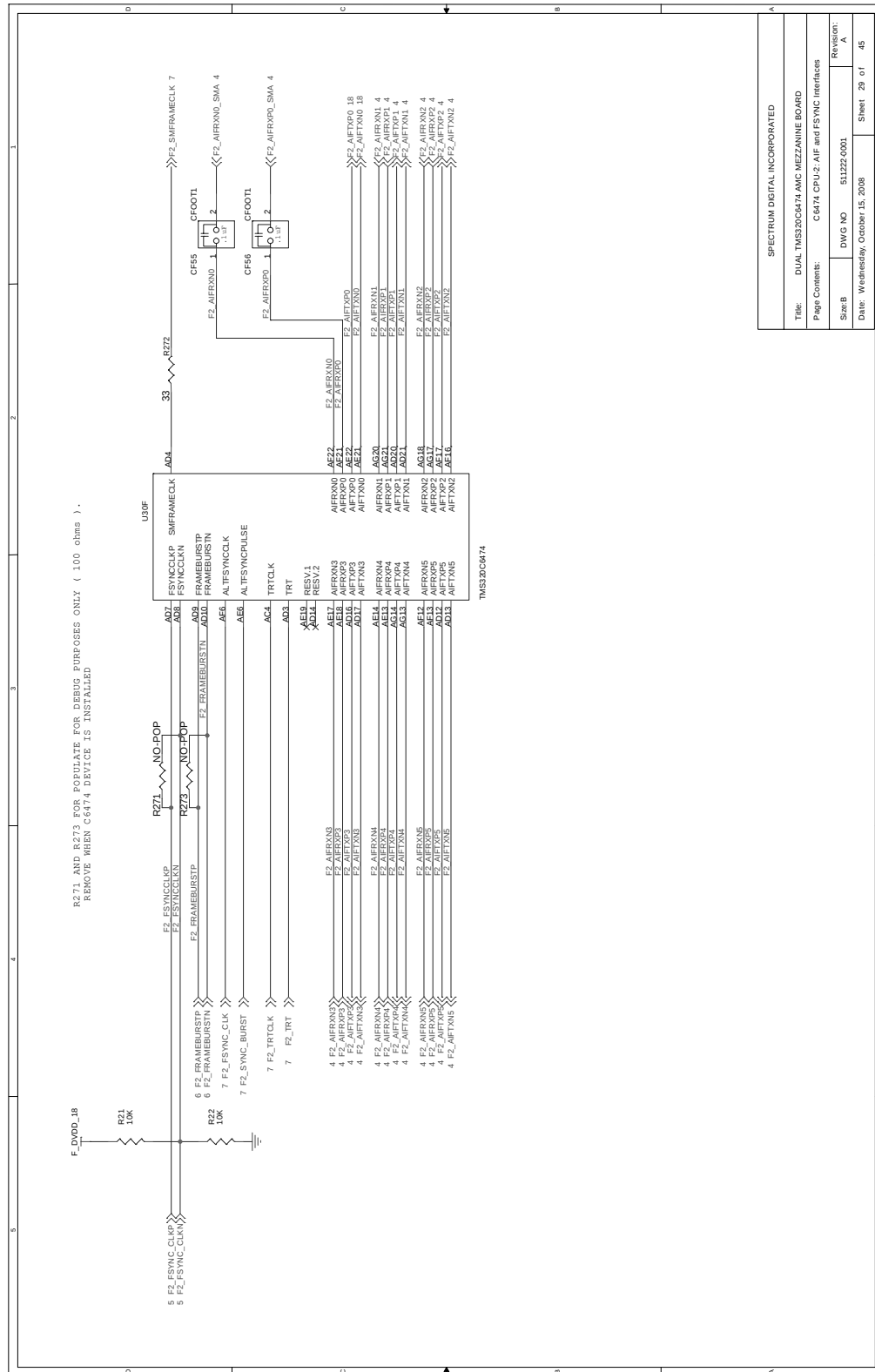


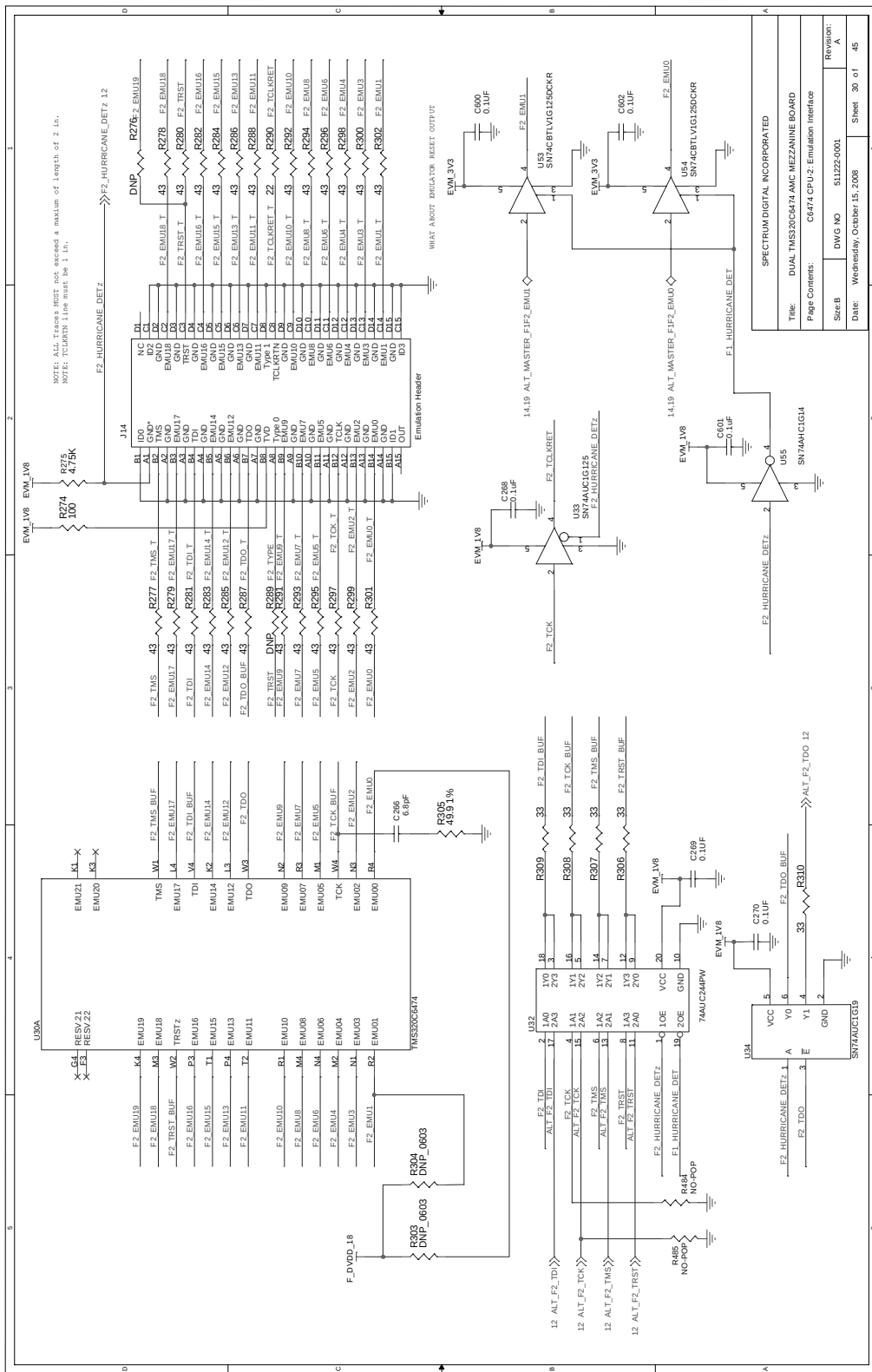


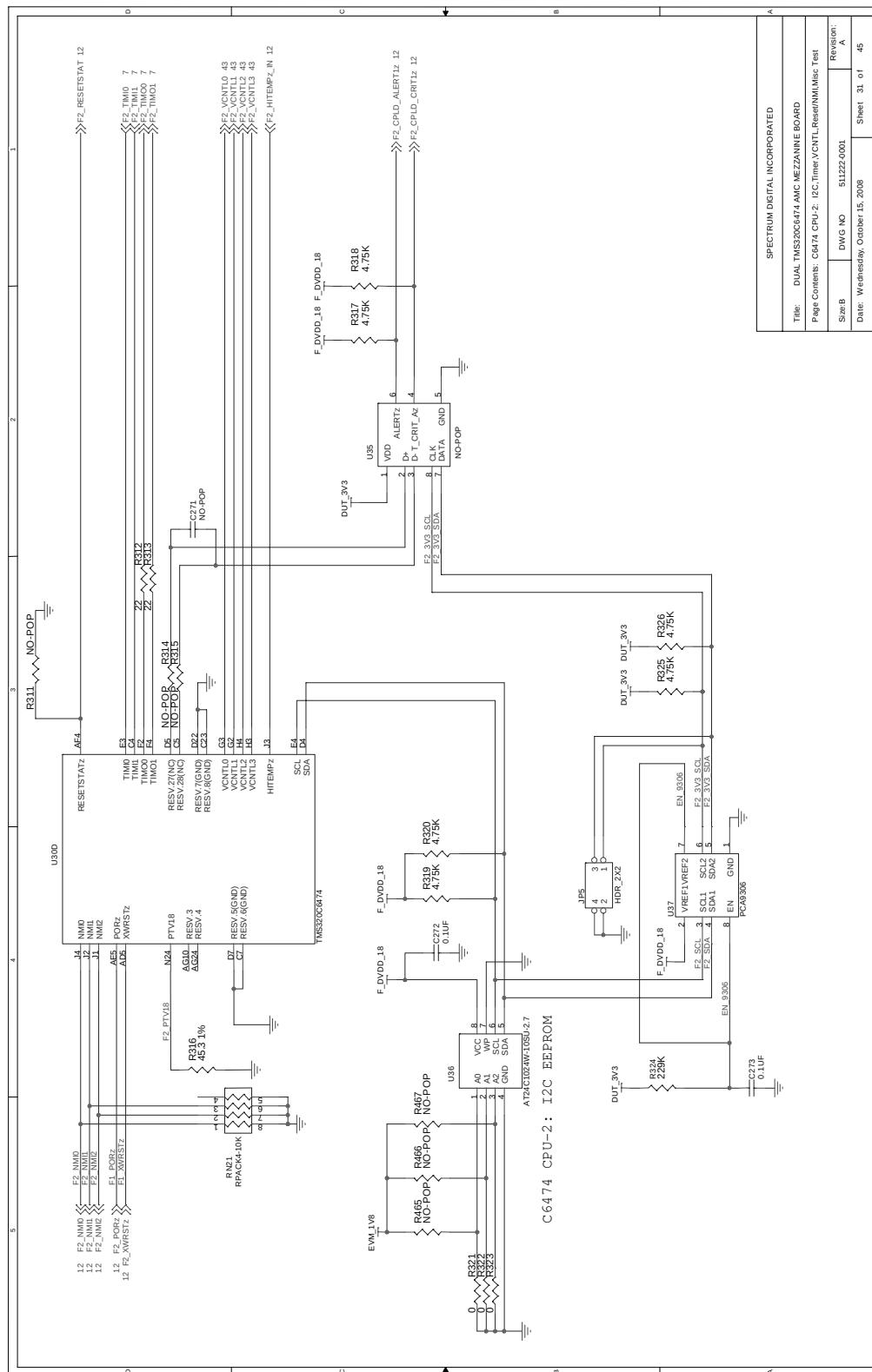


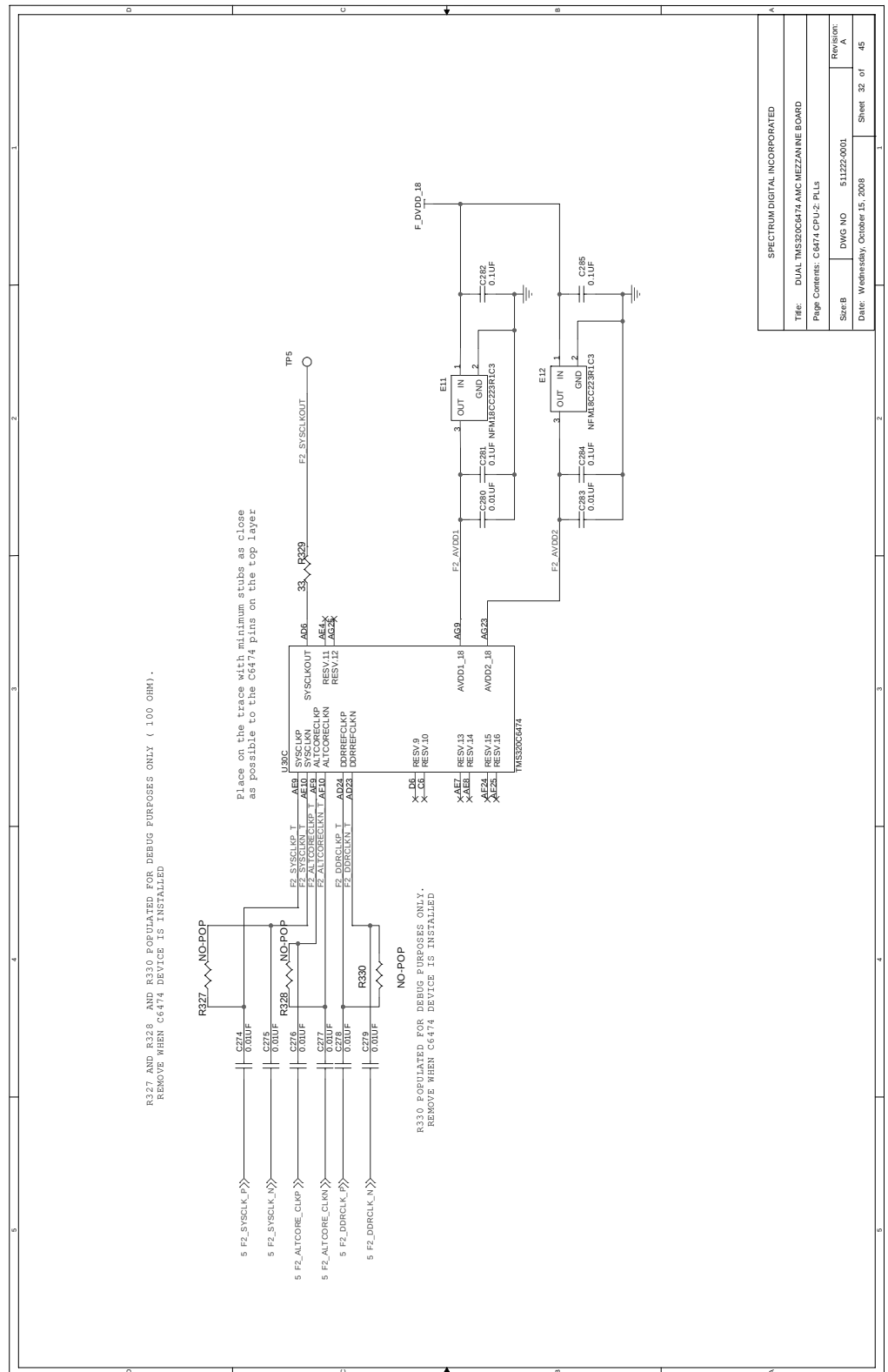


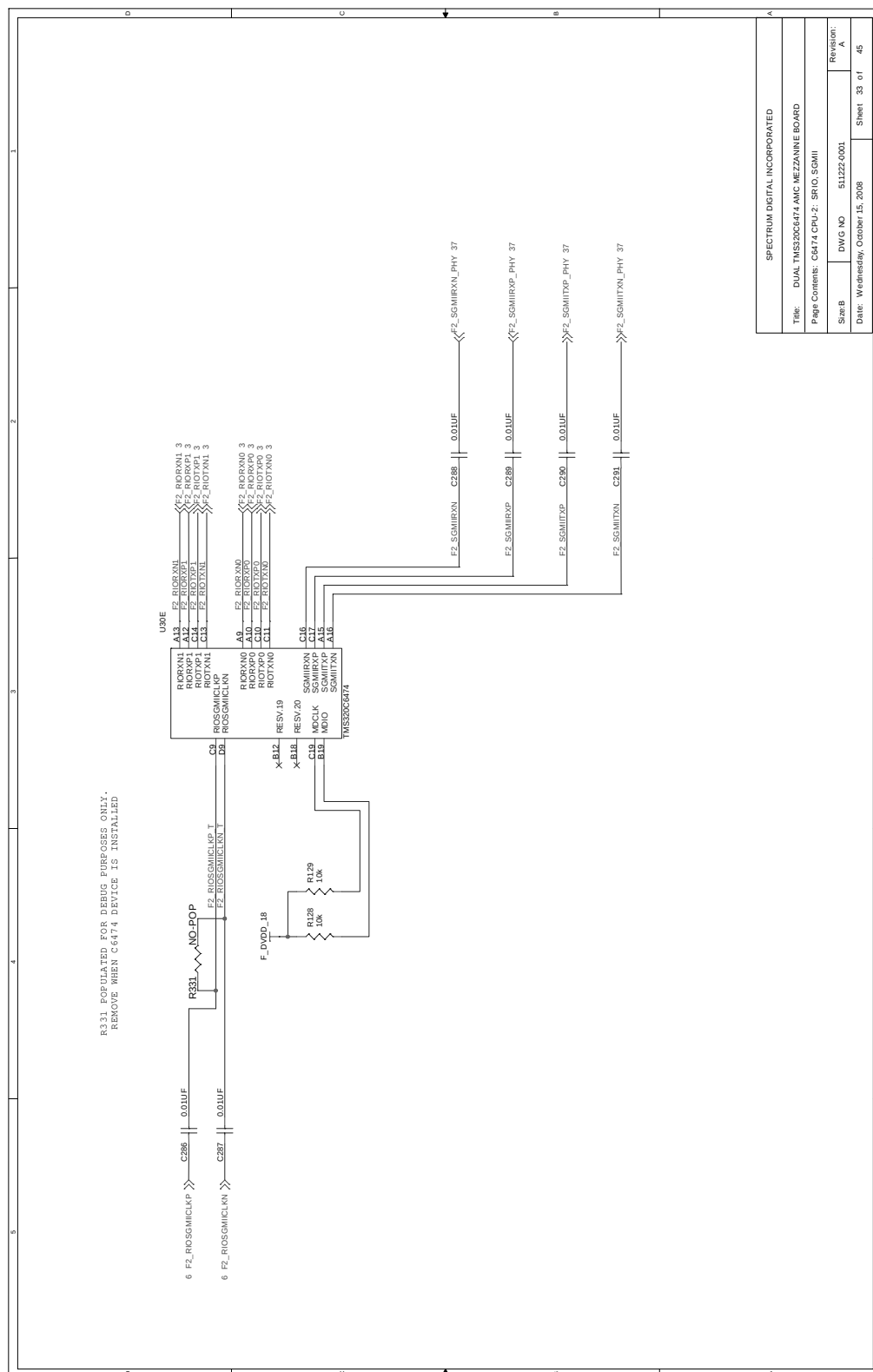


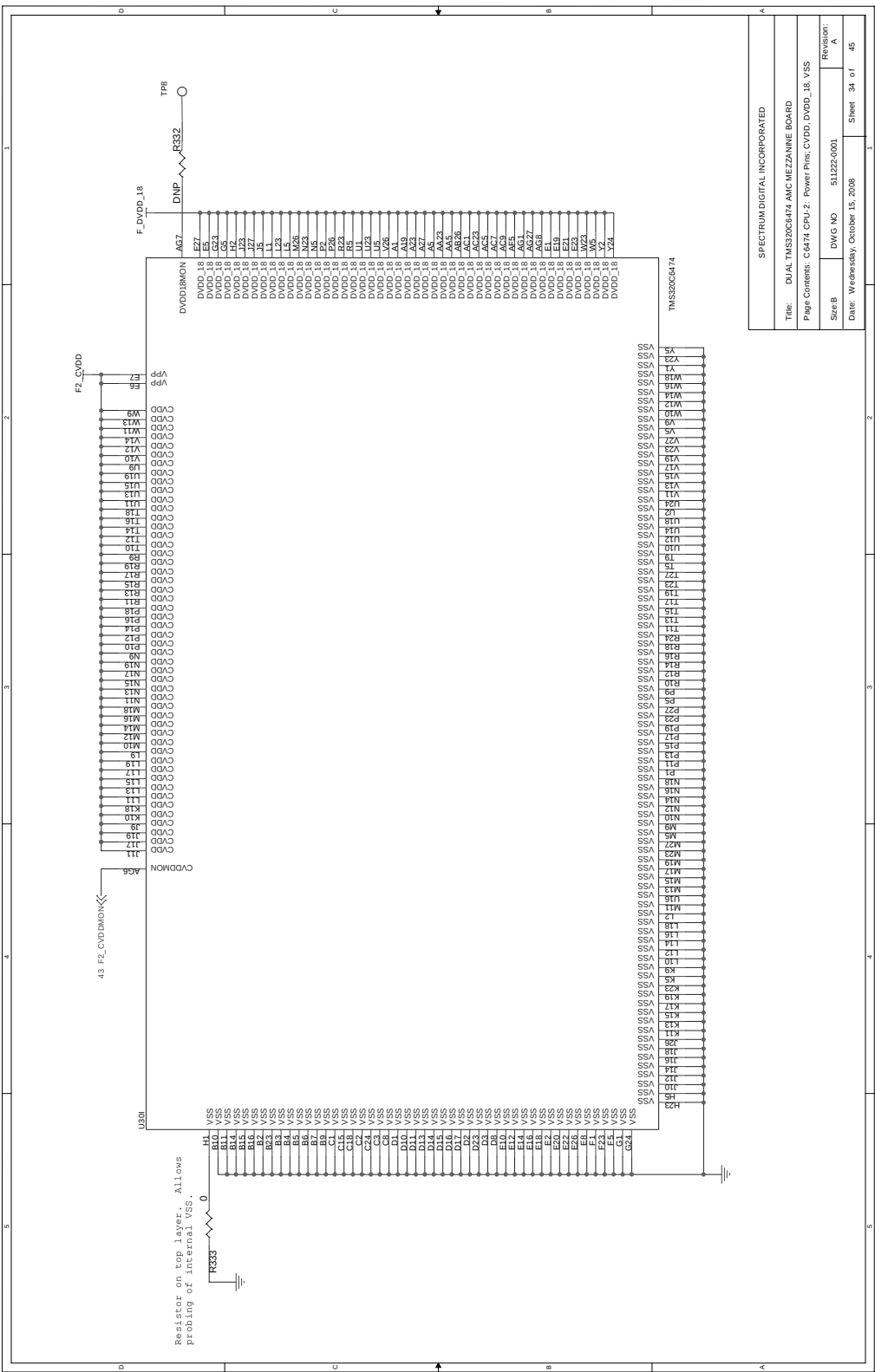


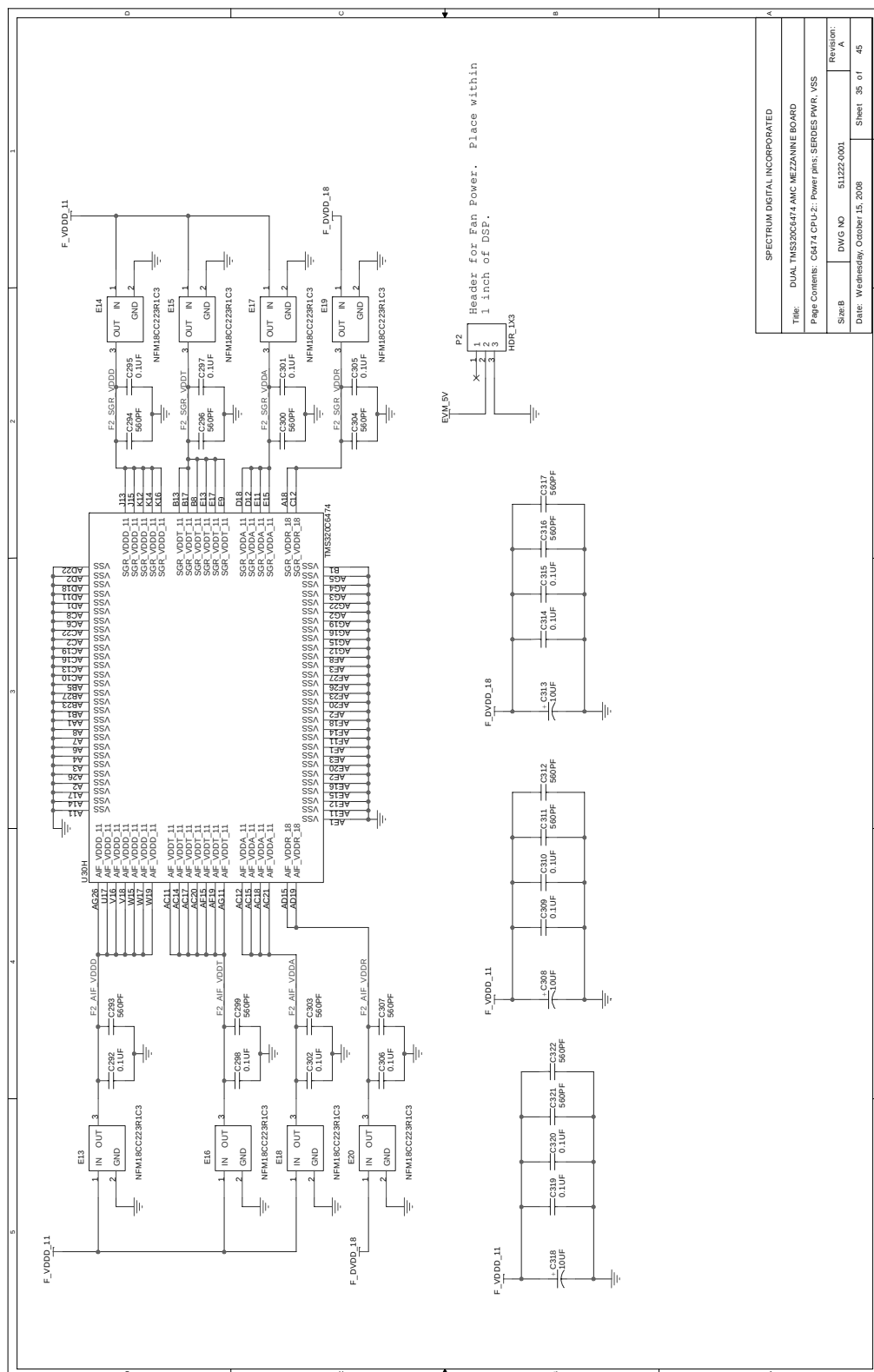


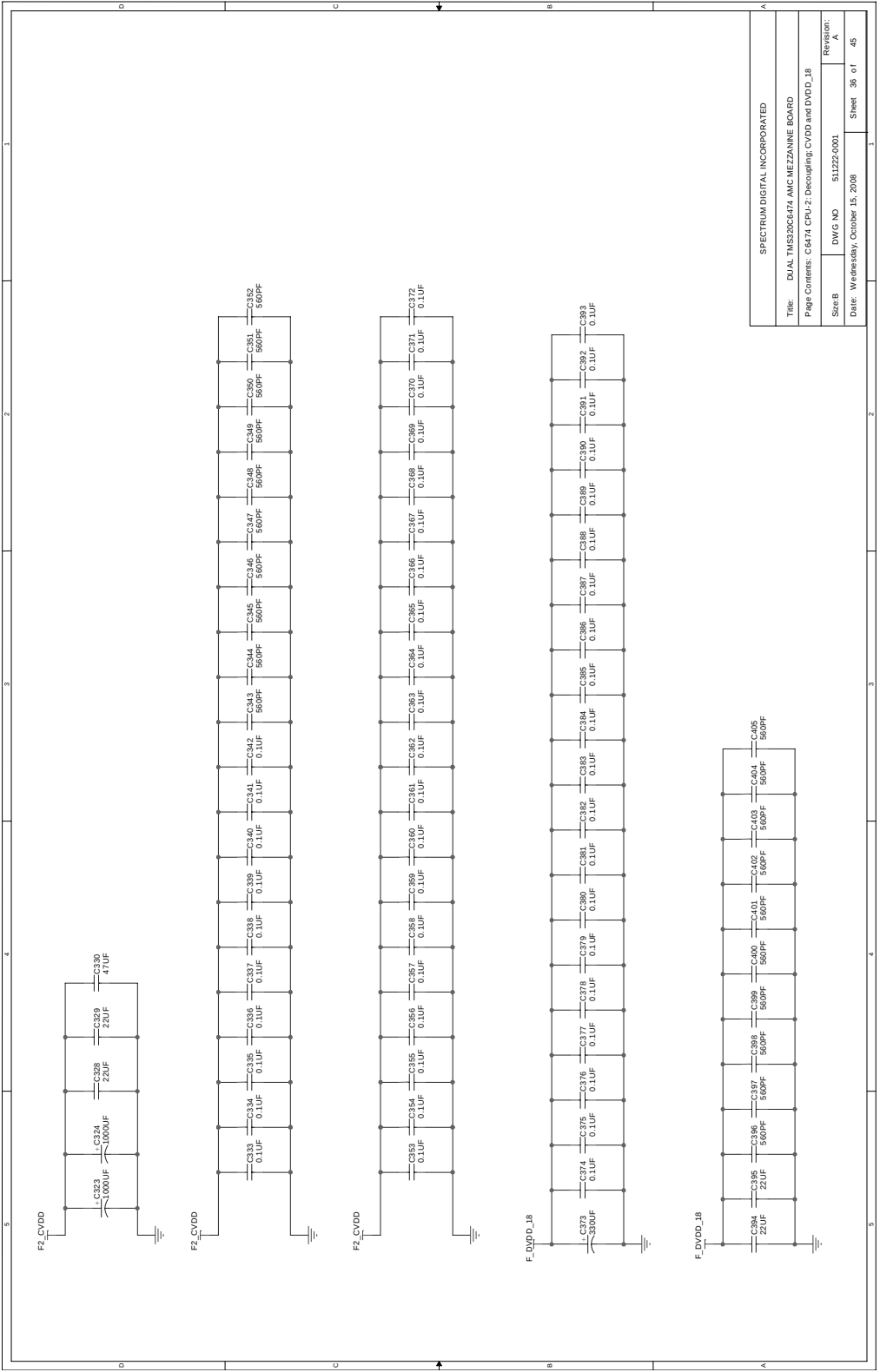




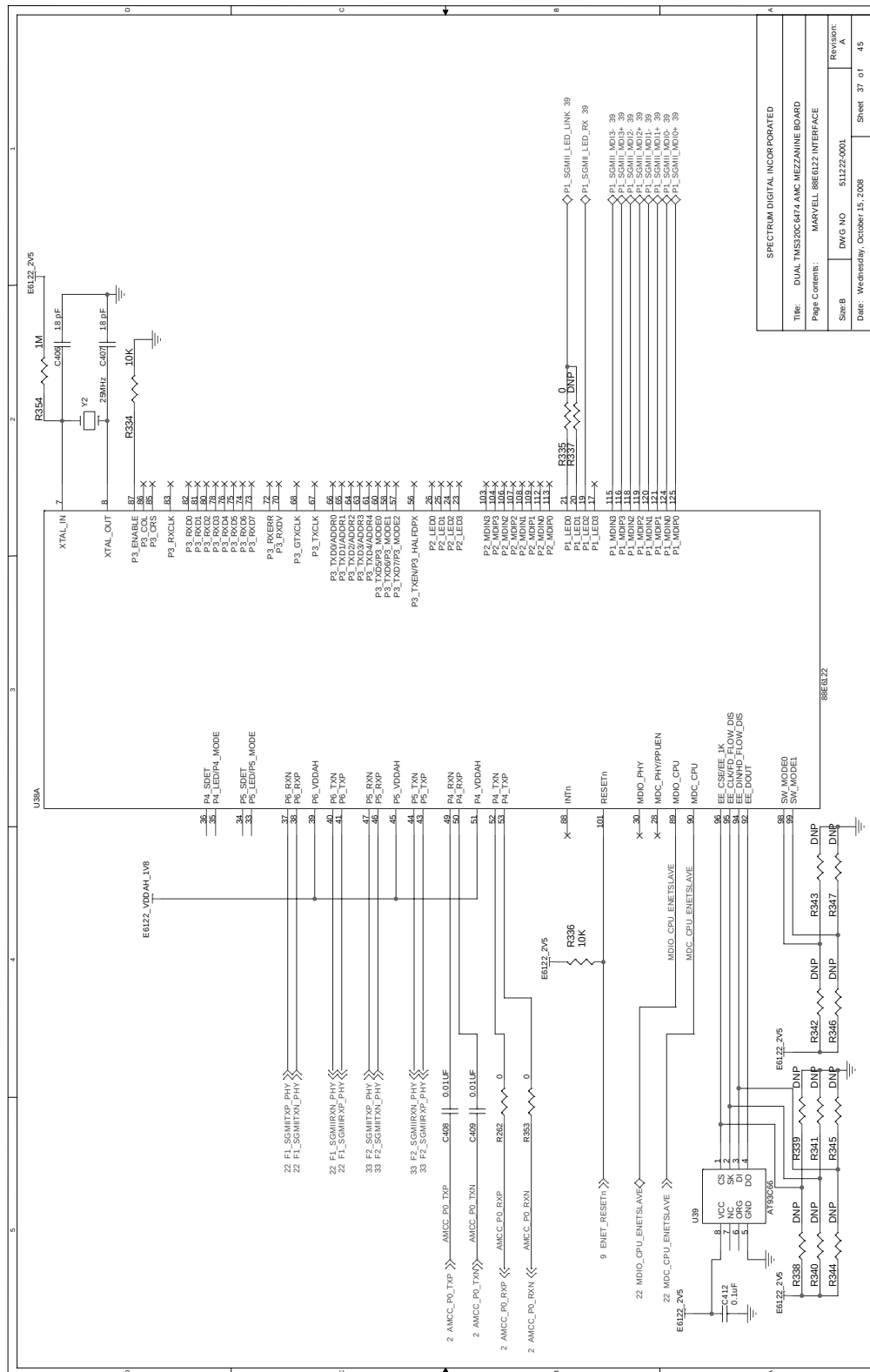


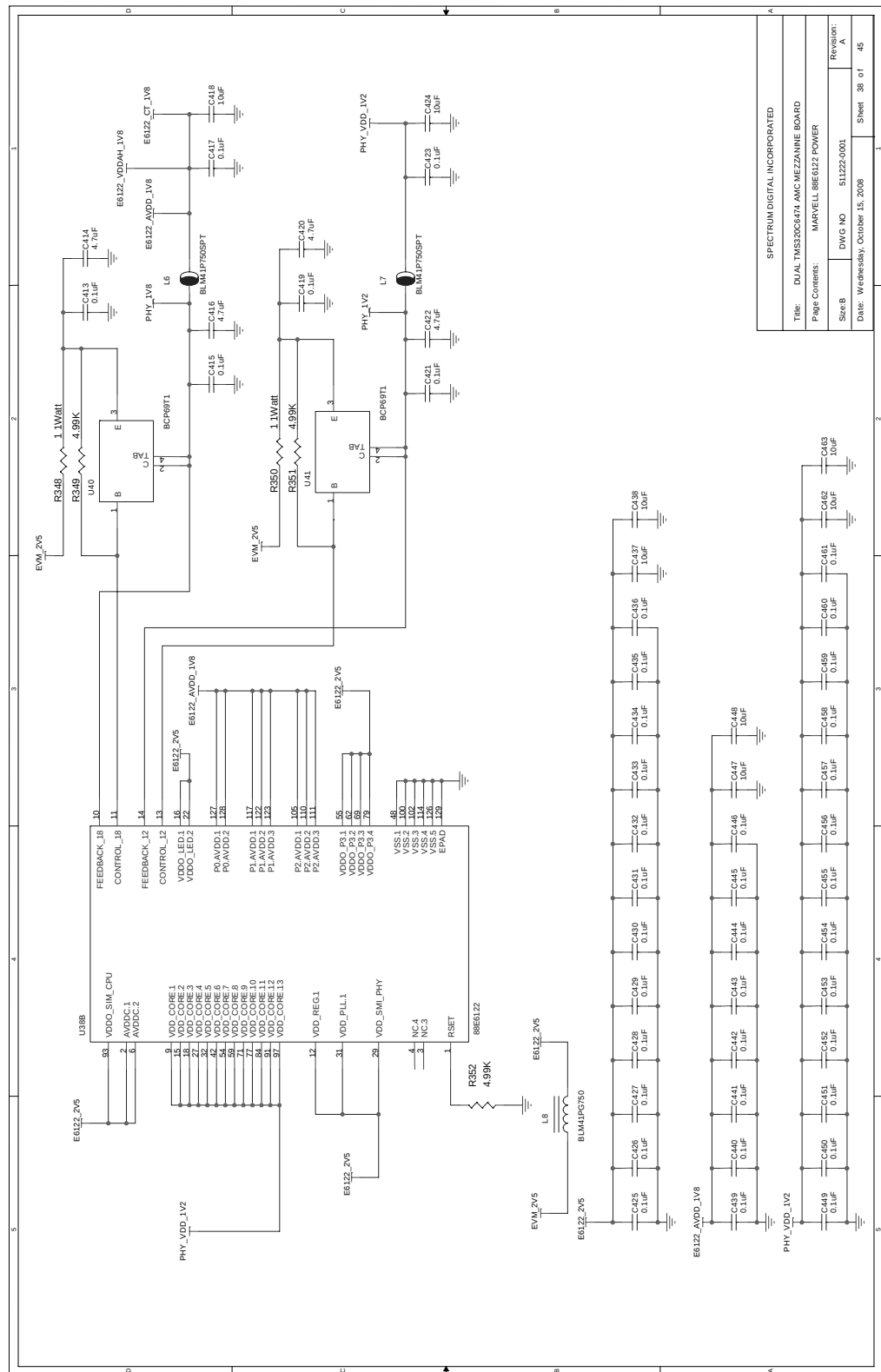


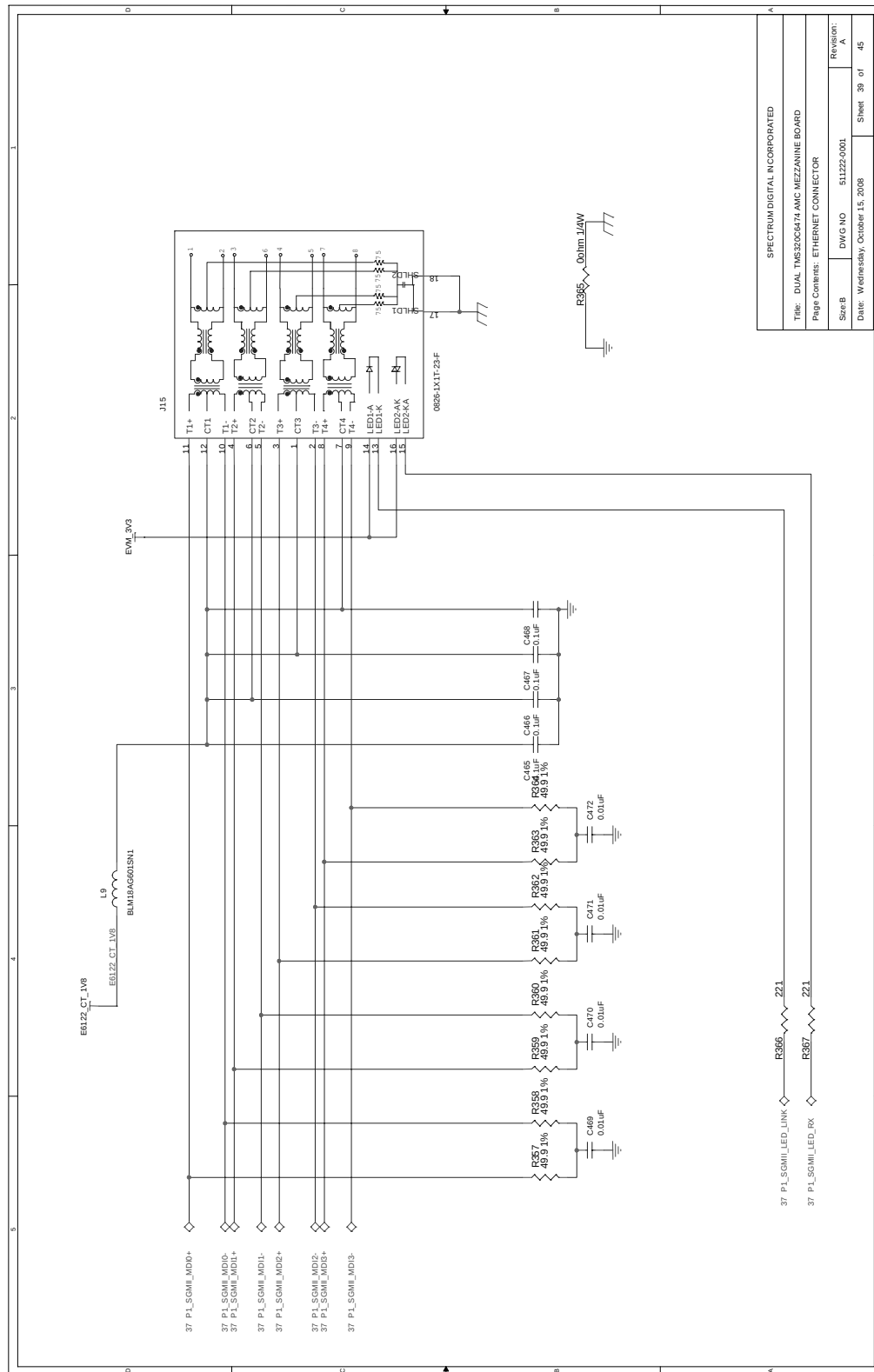


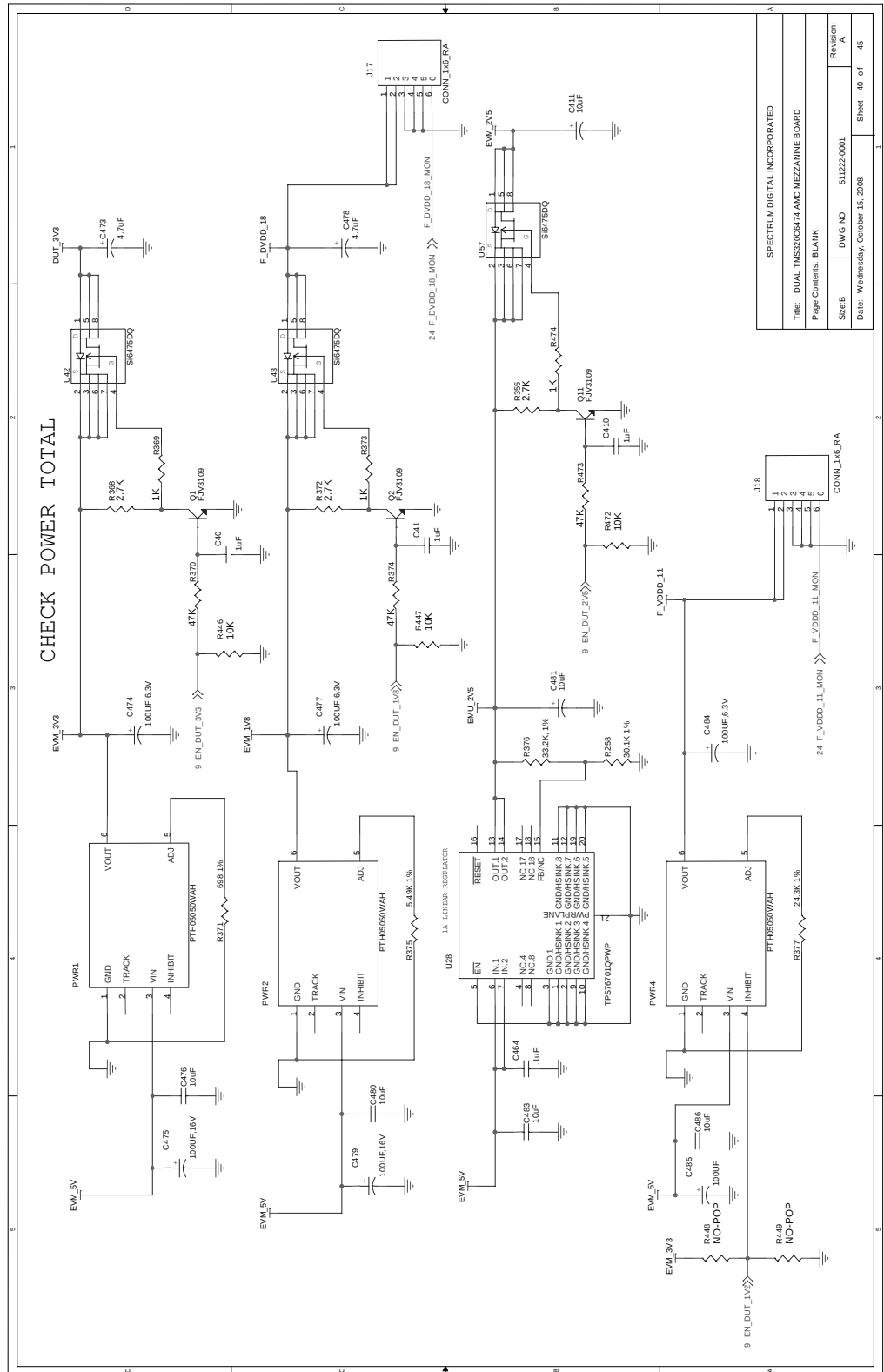


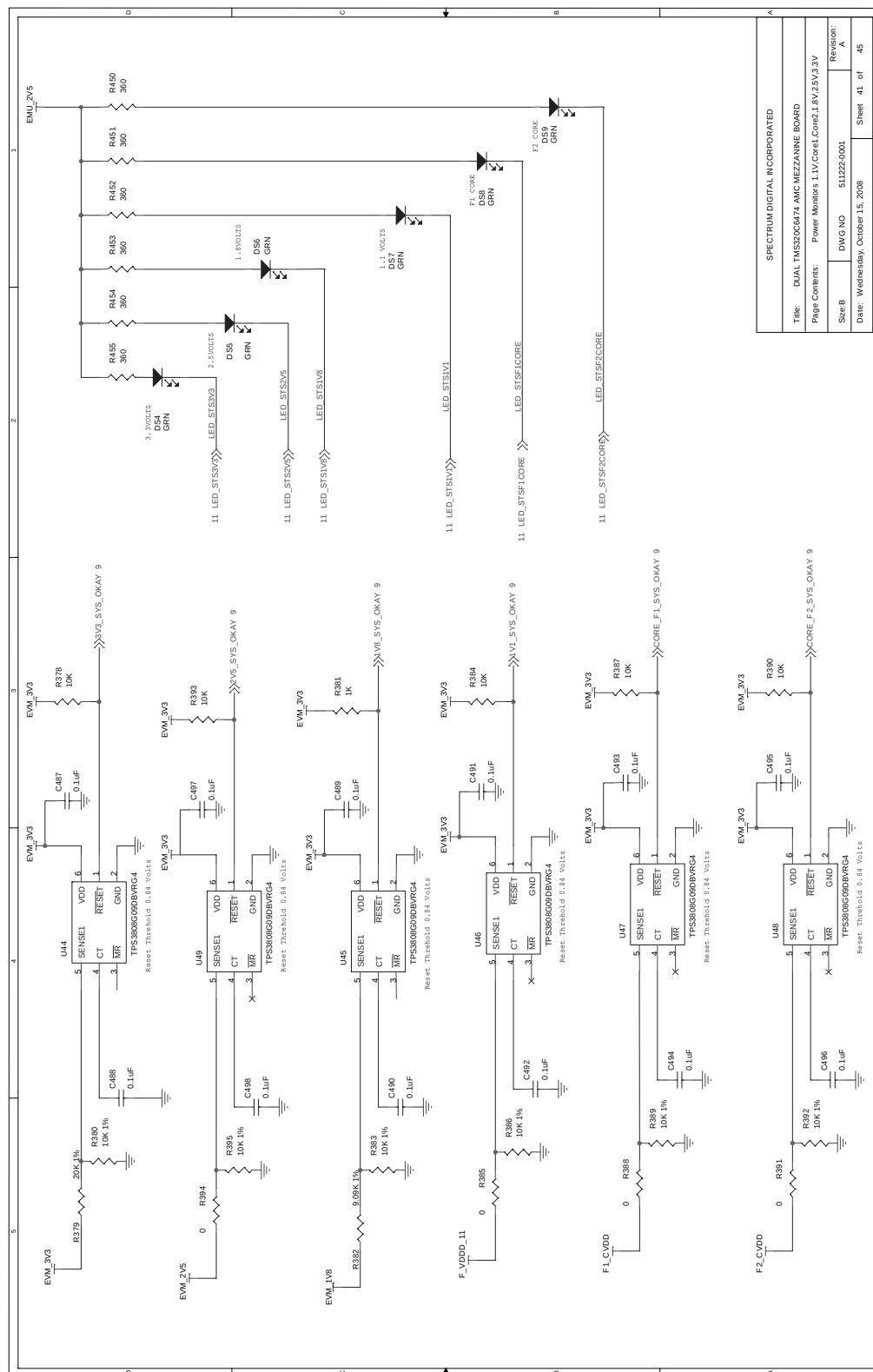
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Size B	DWG NO	Revision:	
	511222-0001	A	
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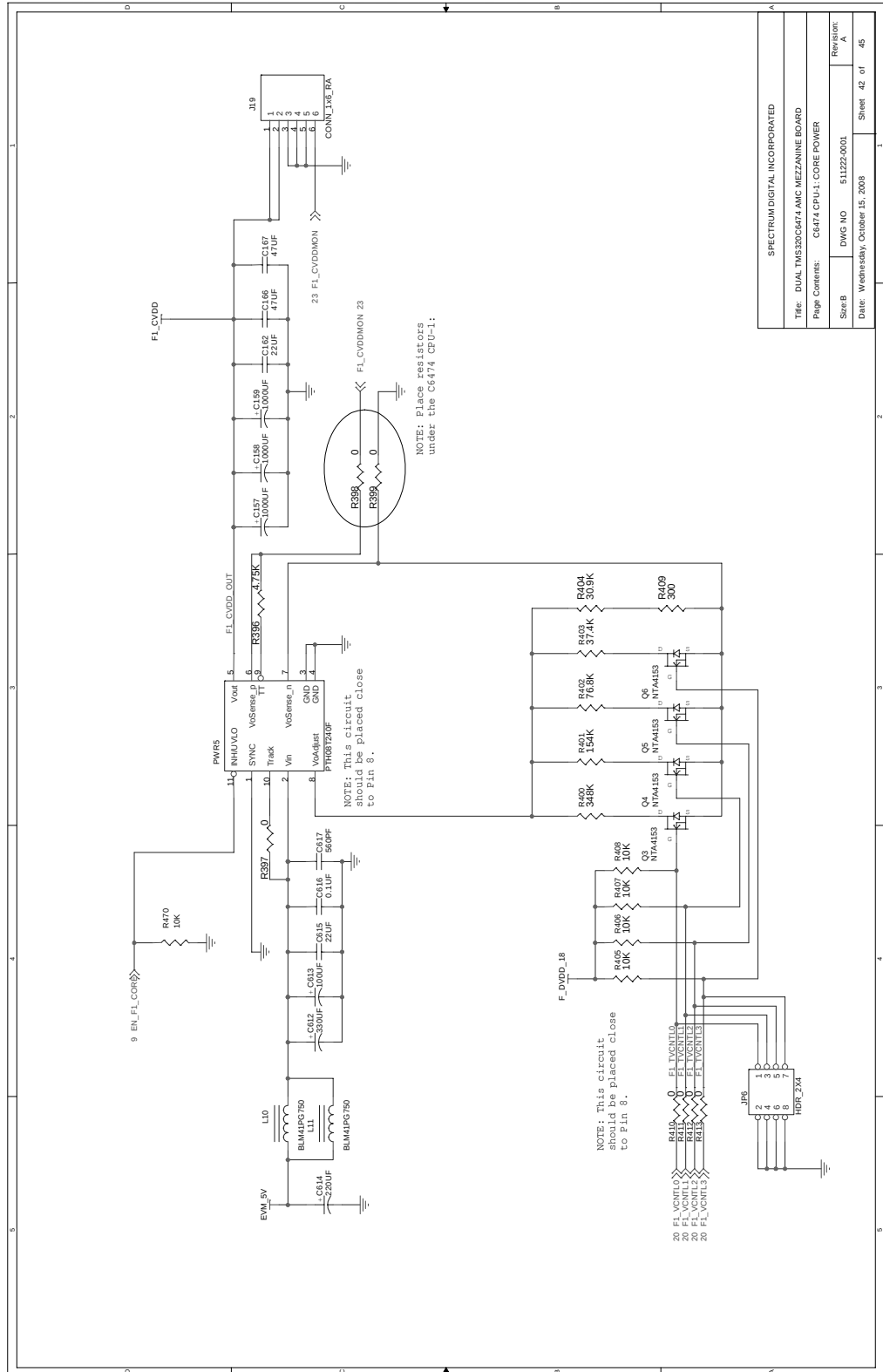


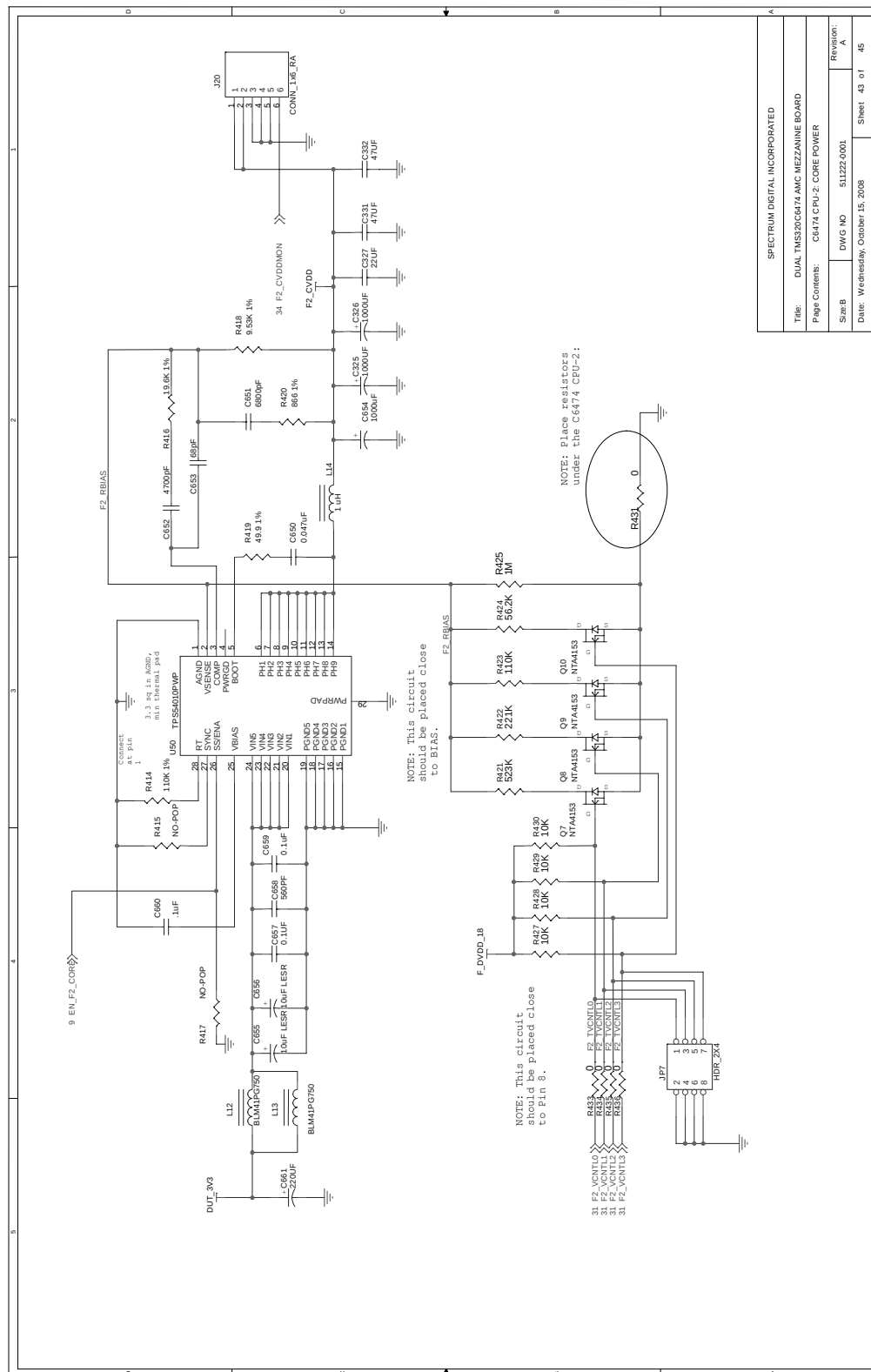


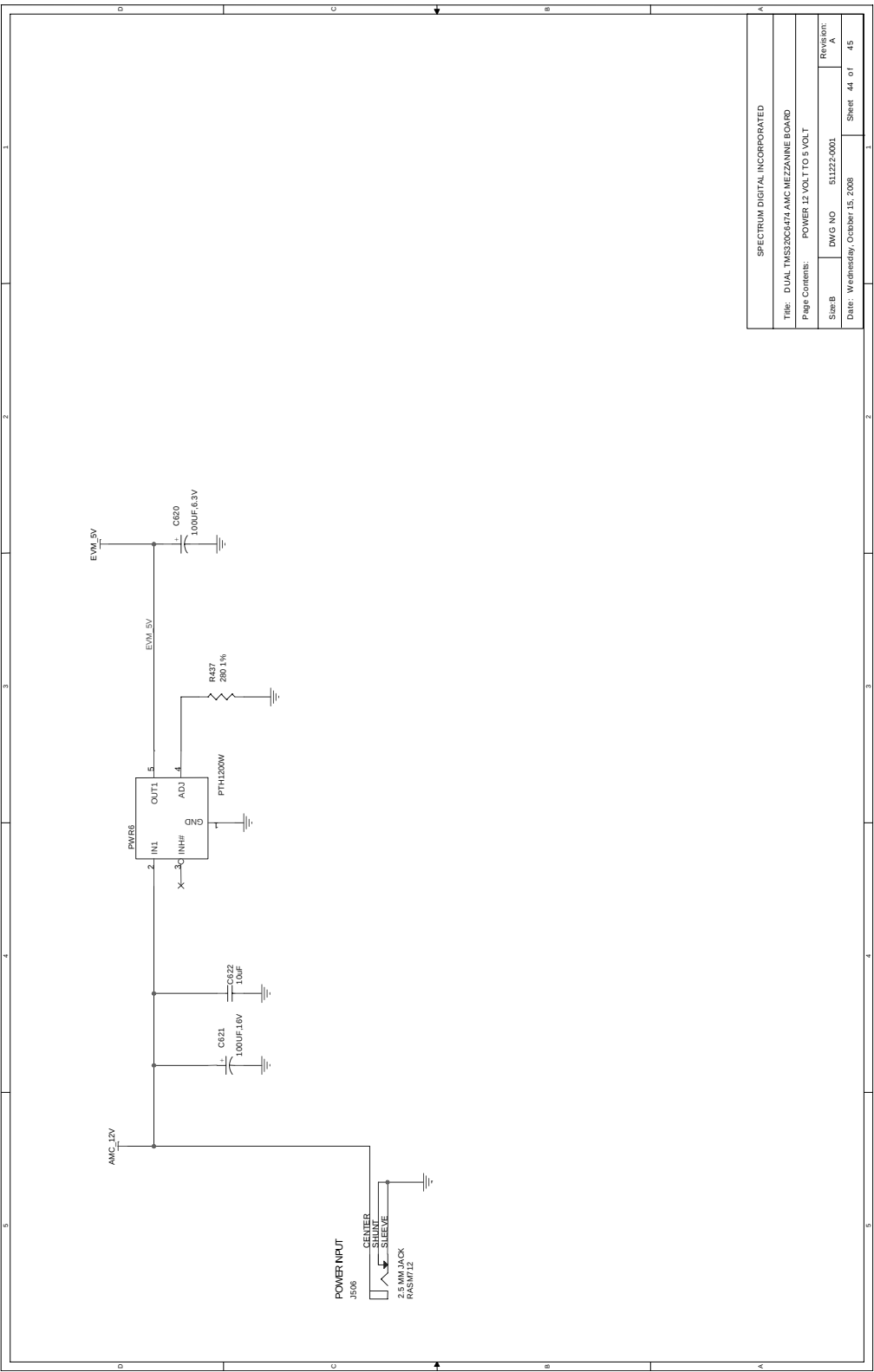




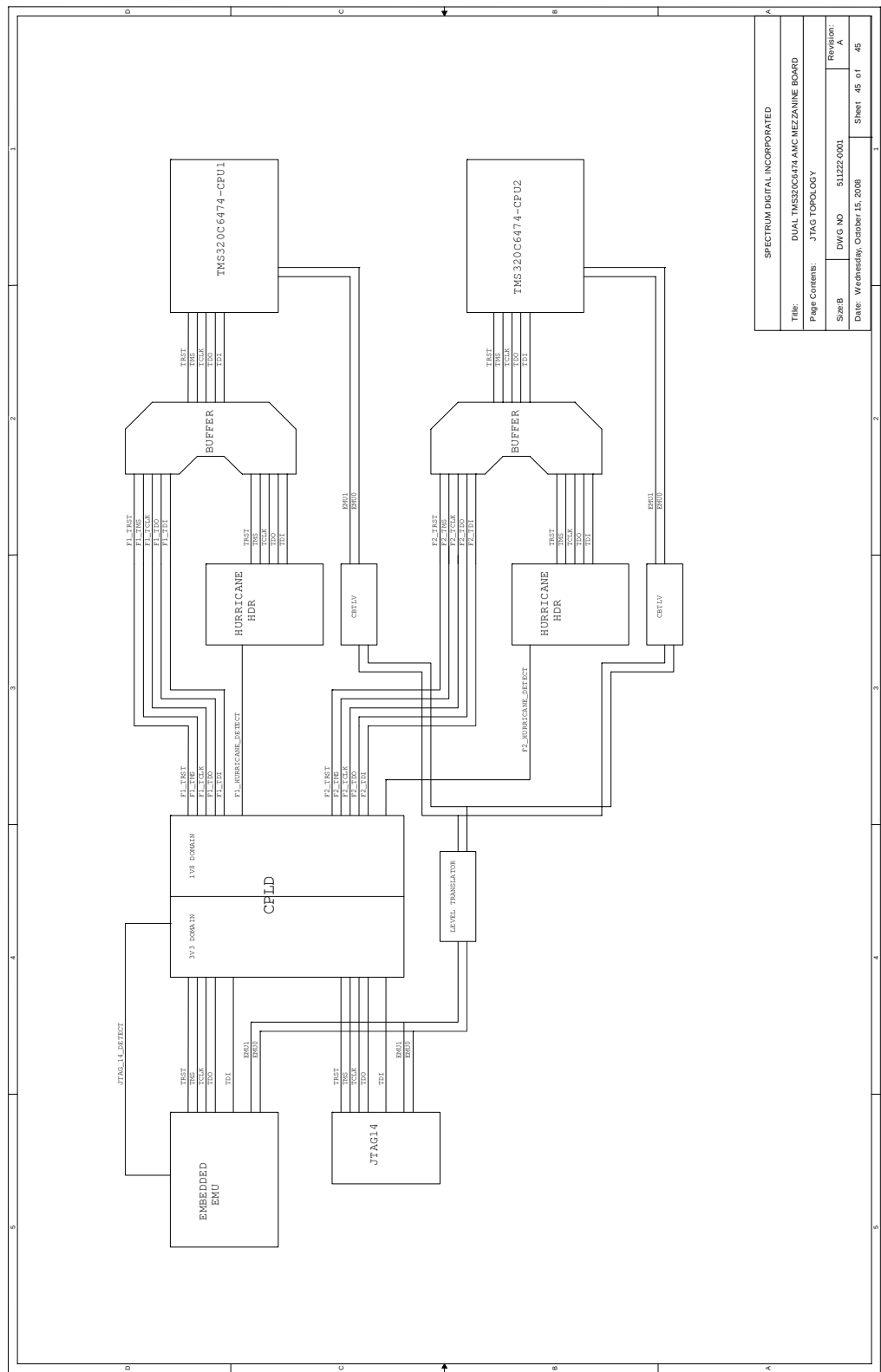
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Date:	Wednesday, October 15, 2008		Sheet 41 of 45







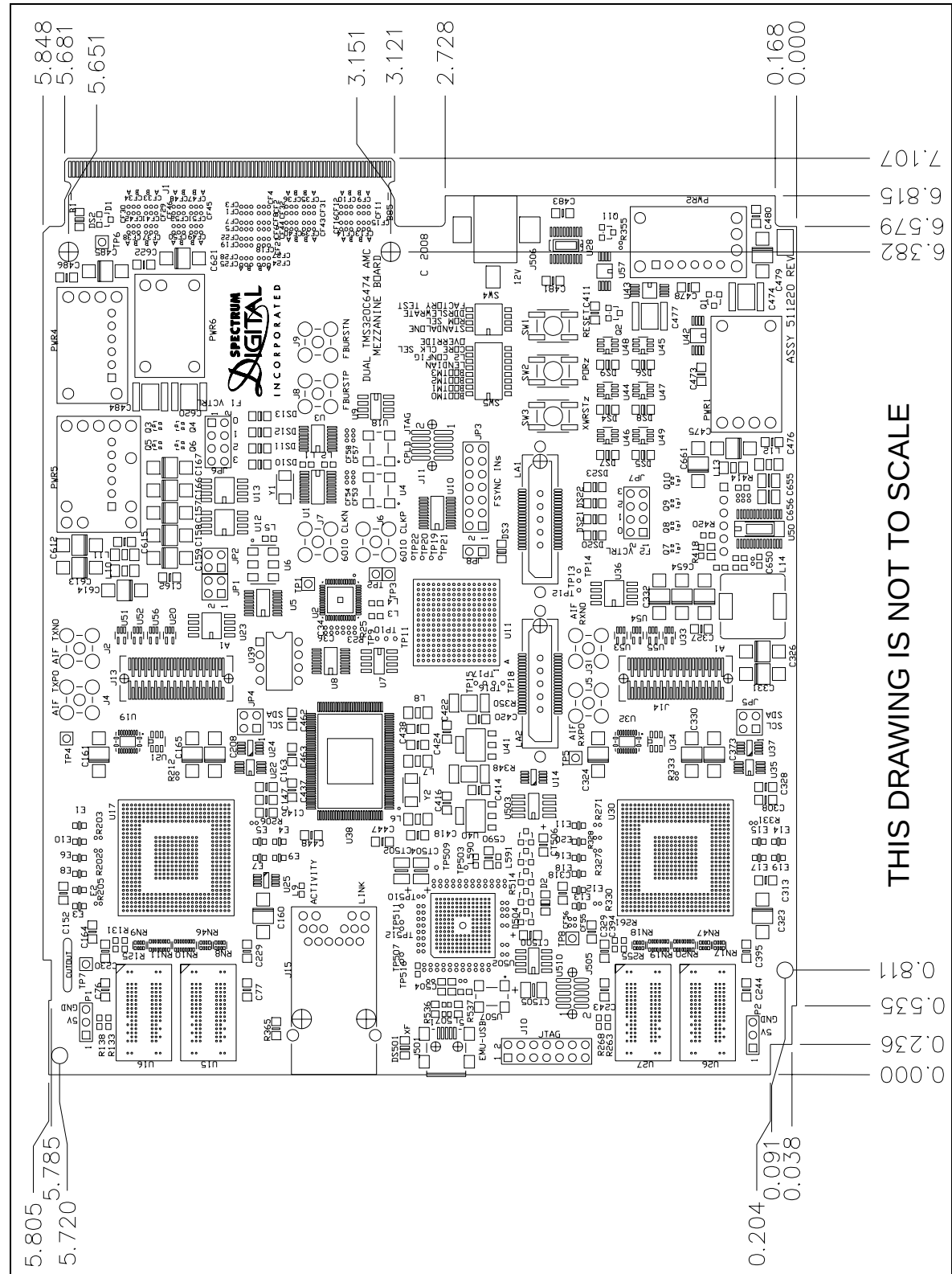
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Sheet B	DWG NO	S11222-0001	Revision: A
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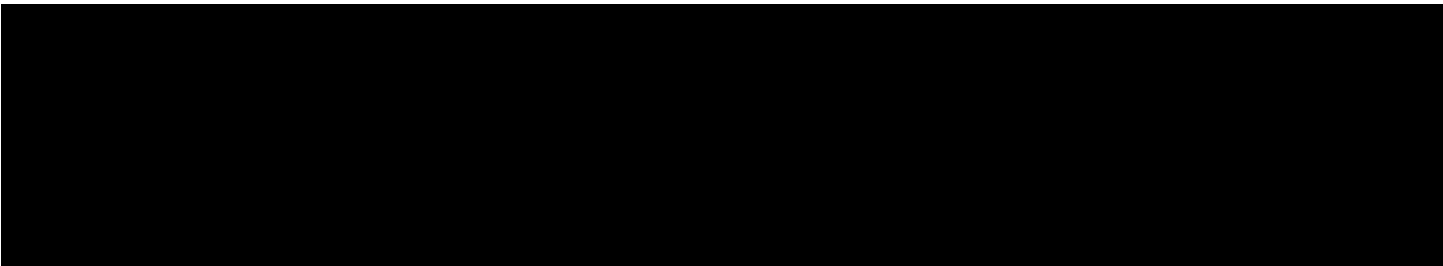


Appendix D

Mechanical Information

This appendix contains the mechanical information about the
TMS320C6474 Mezzanine Board produced by Spectrum Digital.





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