Single-Channel, Adjustable Supervisory Circuit in Ultra-Small Package

Check for Samples: TPS3895, TPS3896, TPS3897, TPS3898

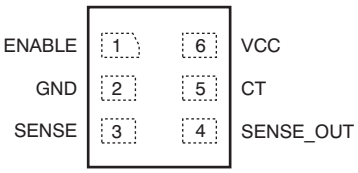
FEATURES

- **Very Small µSON (1.45 mm × 1 mm) Package**
- **Adjustable Threshold down to 500 mV**
- **Threshold Accuracy: 1.0% Over Temperature**
- **Capacitor-Adjustable Delay Time**
- **Low Quiescent Current: 6 µA (typ)**
- **External Enable Input**
- **Open-Drain (rated at 18V)/Push-Pull Output Options**
- **Temperature Range: –40°C to +125°C**
- **Pin-for-Pin Compatible with MAX6895/6/7/8**

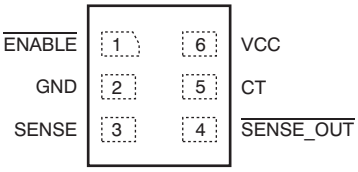
APPLICATIONS

- **DSPs, Microcontrollers, and Microprocessors**
- **Notebook and Desktop Computers**
- **PDAs and Handheld Products**
- **Portable and Battery-Powered Products**
- **FPGA and ASIC**

TPS3895/TPS3897
DRY PACKAGE
(TOP VIEW)



TPS3896/TPS3898
DRY PACKAGE
(TOP VIEW)



DESCRIPTION

The TPS3895, TPS3896, TPS3897, and TPS3898 devices (TPS389x) are a family of very small supervisory circuits that monitors voltage greater than 500 mV with a 0.25% (typical) threshold accuracy and offer a adjustable delay time using external capacitors. The TPS389x family also has a logic enable pin (ENABLE or $\overline{\text{ENABLE}}$) to power on/off the output. With the TPS3895, for example, when the input voltage pin (SENSE) rises above the threshold, and the enable pin (ENABLE) is high, then the output pin (SENSE_OUT) goes high after the capacitor-adjustable delay time. When SENSE falls below the threshold or ENABLE is low, then SENSE_OUT goes low. For truth tables, see Table 2 and Table 3.

For TPS389xA versions, both SENSE and ENABLE have a capacitor-adjustable delay. The output asserts after this capacitor-adjustable delay when both SENSE and ENABLE inputs are good. The TPS389xP devices have a small, 0.2-µs propagation delay from when the enable pin asserts to when the output pin asserts, provided SENSE is above the threshold.

All devices operate from 1.7 V to 6.5 V and have a typical quiescent current of 6 µA with an open-drain output rated at 18 V. The TPS389x is available in an ultra-small µSON package and is fully specified over the temperature range of T_J = –40°C to +125°C.

Table 1. FAMILY COMPARISON

DEVICE	ENABLE	OUTPUT	INPUT (SENSE) DELAY	ENABLE DELAY
TPS3895A	Active high	Active high, push-pull	Capacitor adjustable	Capacitor adjustable
TPS3895P	Active high	Active high, push-pull	Capacitor adjustable	0.2 µs
TPS3896A	Active low	Active low, push-pull	Capacitor adjustable	Capacitor adjustable
TPS3896P	Active low	Active low, push-pull	Capacitor adjustable	0.2 µs
TPS3897A	Active high	Active high, open-drain	Capacitor adjustable	Capacitor adjustable
TPS3897P	Active high	Active high, open-drain	Capacitor adjustable	0.2 µs
TPS3898A	Active low	Active low, open-drain	Capacitor adjustable	Capacitor adjustable
TPS3898P	Active low	Active low, open-drain	Capacitor adjustable	0.2 µs

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	DESCRIPTION
TPS389**wxyyyz**	**w** is output configuration (see Table 1) **x** is different delay from enable pin (see Table 1) **yyy** is package designator **z** is package quantity

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	VCC	–0.3	7	V
	CT	–0.3	V_{CC} + 0.3	V
	ENABLE, SENSE, SENSE_OUT (push-pull)	–0.3	7	V
	SENSE_OUT (open-drain)	–0.3	20	V
Current	SENSE_OUT		±10	mA
Temperature	Operating junction, T_J	–40	+125	°C
	Storage, T_{stg}	–65	+150	°C
Electrostatic discharge rating(3)	Human body model (HBM)		2	kV
	Charge device model (CDM)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS389x DRY (µSON) 6 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	293.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	165.1	
θ_{JB}	Junction-to-board thermal resistance	160.8	
ψ_{JT}	Junction-to-top characterization parameter	27.3	
ψ_{JB}	Junction-to-board characterization parameter	65.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	65.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

Over the operating temperature range of T_J = –40°C to +125°C, and 1.7 V < V_{CC}< 6.5 V, unless otherwise noted. Typical values are at T_J = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	T_J = –40°C to +125°C	1.7		6.5	V
		T_J = 0°C to +85°C	1.65		6.5	V
$V_{(POR)}$	Power-on reset voltage(1)	V_{OL} (max) = 0.2 V , $I_{(SENSE\_OUT)}$ = 15 µA			0.8	V
I_{CC}	Supply current (into VCC pin)	V_{CC} = 3.3 V , no load		6	12	µA
		V_{CC} = 6.5 V , no load		7	12	µA
V_{IT+}	Positive-going input threshold voltage	$V_{(SENSE)}$ rising	0.495	0.5	0.505	V
V_{hys}	Hysteresis voltage	$V_{(SENSE)}$ falling		5		mV
$I_{(SENSE)}$	Input current(2)	$V_{(SENSE)}$ = 0 V or V_{CC}	–15		15	nA
$I_{(CT)}$	CT pin charge current		260	310	360	nA
$V_{(CT)}$	CT pin comparator threshold voltage		1.180	1.238	1.299	V
$R_{(CT)}$	CT pin pull-down resistance			200		Ω
V_{IL}	Low-level input voltage (ENABLE pin)				0.4	V
V_{IH}	High-level input voltage (ENABLE pin)		1.4			V
UVLO	Undervoltage lockout(3)	V_{CC} falling	1.3		1.7	V
I_{lkg}	Leakage current	ENABLE = V_{CC} or GND	–100		100	nA
V_{OL}	Low-level output voltage	V_{CC} ≥ 1.2 V, I_{SINK} = 90 µA (TPS3895/7 only)			0.3	V
		V_{CC} ≥ 2.25 V, I_{SINK} = 0.5 mA			0.3	V
		V_{CC} ≥ 4.5 V, I_{SINK} = 1 mA			0.4	V
V_{OH}	High-level output voltage (push-pull)	V_{CC} ≥ 2.25 V, I_{SOURCE} = 0.5 mA	0.8V_{CC}			V
		V_{CC} ≥ 4.5 V, I_{SOURCE} = 1 mA	0.8V_{CC}			V
$I_{lkg(OD)}$	Open-drain output leakage current	$V_{(SENSE\_OUT)}$ high impedance = 18 V			300	nA
$t_{pd(r)}$	SENSE (rising) to SENSE_OUT propagation delay	$V_{(SENSE)}$ rising, $C_{(CT)}$ = open		40		µs
		$V_{(SENSE)}$ rising, $C_{(CT)}$ = 0.047 µF		190		ms
$t_{pd(f)}$	SENSE (falling) to SENSE_OUT propagation delay	$V_{(SENSE)}$ falling		16		µs
	Startup delay(4)			50		µs
t_w	ENABLE pin minimum pulse duration		1			µs
	ENABLE pin glitch rejection			100		ns
$t_{d(off)}$	ENABLE to SENSE_OUT delay time (output disabled)	ENABLE de-asserted to output de-asserted		200		ns
$t_{d(P)}$	ENABLE to SENSE_OUT delay time (P version)	ENABLE asserted to output asserted delay (P version)		200		ns
$t_{d(A)}$	ENABLE to SENSE_OUT delay time (A version)	ENABLE asserted to output asserted delay (A version), $C_{(CT)}$ = open		20		µs
		ENABLE asserted to output asserted delay (A version), $C_{(CT)}$ = 0.047 µF		190		ms

(1) The lowest supply voltage (V_{CC}) at which output is active (SENSE_OUT is low, $\overline{\text{SENSE\_OUT}}$ is high); $t_r(V_{CC})$ > 15 µs/V. Below $V_{(POR)}$, the output cannot be determined.
(2) Specified by design.
(3) When V_{CC} falls below the UVLO threshold, the output de-asserts (SENSE_OUT goes low, $\overline{\text{SENSE\_OUT}}$ goes high). Below $V_{(POR)}$, the output cannot be determined.
(4) During power on, V_{CC} must exceed 1.7 V for at least 50 µs (plus propagation delay time, $t_{pd(r)}$) before output is in the correct state.

TIMING DIAGRAMS

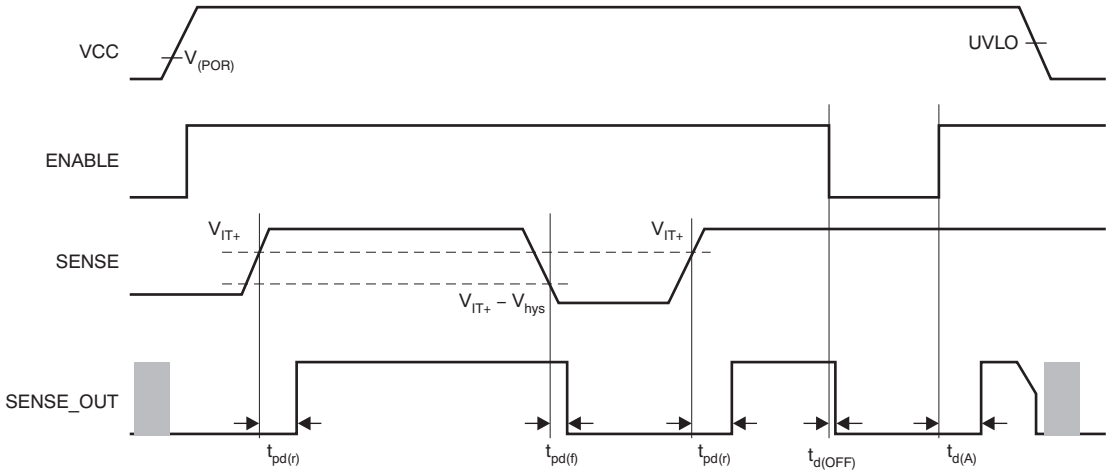


Figure 1. TPS3895A/TPS3897A Timing

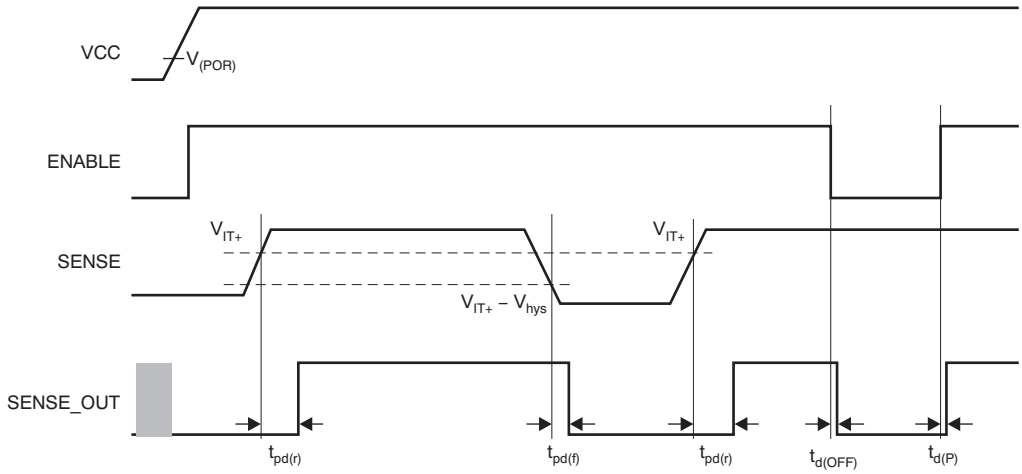


Figure 2. TPS3895P/TPS3897P Timing

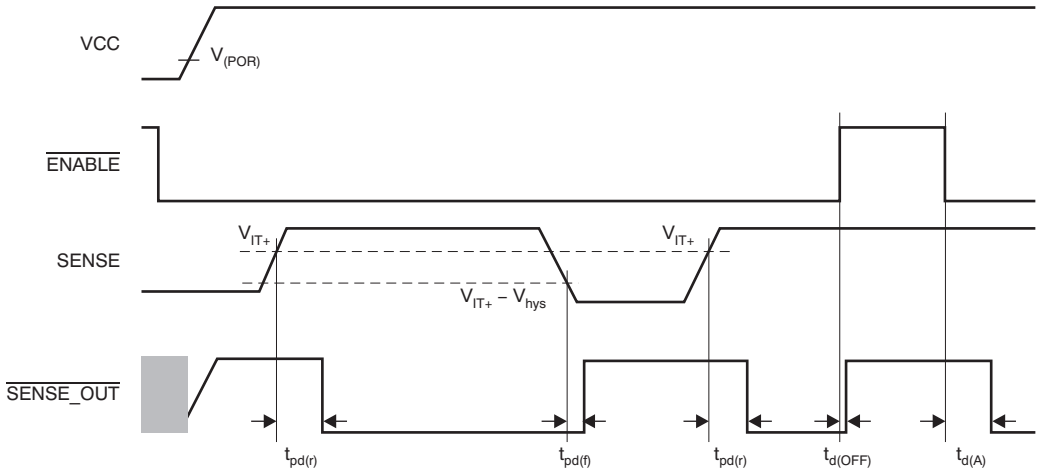


Figure 3. TPS3896A/TPS3898A Timing

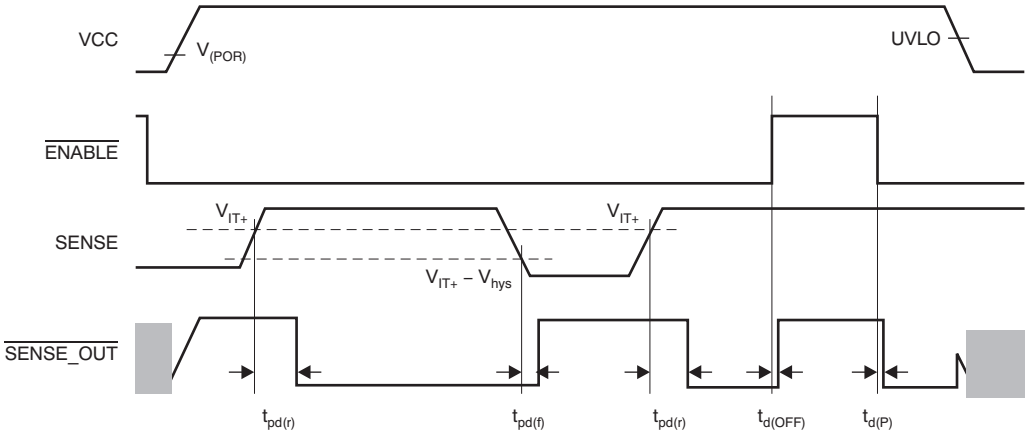
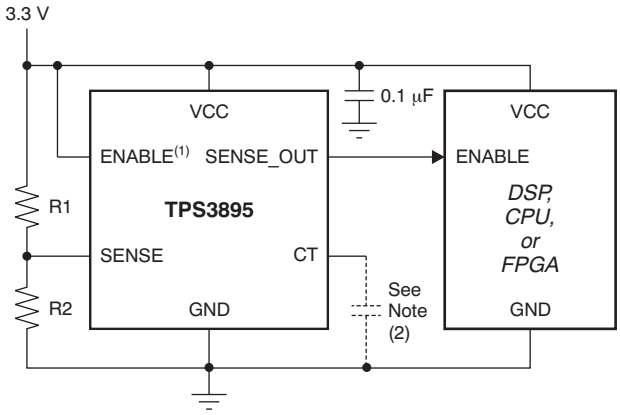


Figure 4. TPS3896P/TPS3898P Timing

TYPICAL APPLICATION



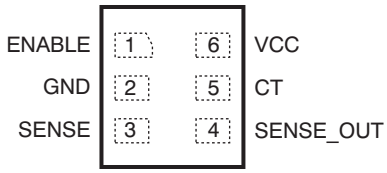
(1) ENABLE can also be driven with a separate 1.5-V or greater power supply.

(2) Capacitor is optional. If capacitor not used, leave CT pin open for 40-µs delay.

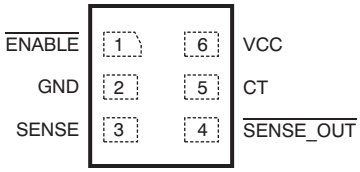
Figure 5. TPS3895 Typical Application

PIN CONFIGURATIONS

DRY PACKAGE: TPS3895, TPS3897
USON-6
(TOP VIEW)



DRY PACKAGE: TPS3896, TPS3898
USON-6
(TOP VIEW)



PIN ASSIGNMENTS

PIN NAME	TPS3895/ TPS3897	TPS3896/ TPS3898	DESCRIPTION
CT	5	5	Capacitor-adjustable delay. The CT pin offers a user-adjustable delay time. Connecting this pin to a ground referenced capacitor sets the delay time for SENSE rising above 0.5 V to SENSE_OUT asserting (or ENABLE asserting to SENSE_OUT asserting for A version devices). $t_{pd(r)}$ (s) = (C_{CT} (µF) × 4) + 40 µs
ENABLE	1	—	Active high input. Driving ENABLE low immediately makes SENSE_OUT go low, independent of $V_{(SENSE)}$. With $V_{(SENSE)}$ already above V_{IT+}, drive ENABLE high to make SENSE_OUT go high after the capacitor-adjustable delay time (A version) or 0.2 µs (P version).
$\overline{\text{ENABLE}}$	—	1	Active low input. Driving $\overline{\text{ENABLE}}$ high immediately makes $\overline{\text{SENSE\_OUT}}$ go high, independent of $V_{(SENSE)}$. With $V_{(SENSE)}$ already above V_{IT+}, drive $\overline{\text{ENABLE}}$ low to make $\overline{\text{SENSE\_OUT}}$ go low after the capacitor-adjustable delay time (A version) or 0.2 µs (P version).
GND	2	2	Ground
SENSE	3	3	This pin is connected to the voltage that is monitored with the use of external resistor. The output asserts after the capacitor-adjustable delay time when $V_{(SENSE)}$ rises above 0.5 V and ENABLE is asserted. The output de-asserts after a minimal propagation delay (16 µs) when $V_{(SENSE)}$ falls below $V_{IT+} – V_{hys}$.
SENSE_OUT	4	—	SENSE_OUT is an open-drain/push-pull output that is immediately driven low after $V_{(SENSE)}$ falls below $V_{IT+} – V_{hys}$ or the ENABLE input is low. SENSE_OUT goes high after the capacitor-adjustable delay time when $V_{(SENSE)}$ is greater than V_{IT+} and the ENABLE pin is high. Open-drain devices(TPS3897/8) can be pulled up to 18 V independent of V_{CC}; pull-up resistors are required for these devices.
$\overline{\text{SENSE\_OUT}}$	—	4	$\overline{\text{SENSE\_OUT}}$ is an open-drain/push-pull output that is immediately driven high after $V_{(SENSE)}$ falls below $V_{IT+} – V_{hys}$ or the $\overline{\text{ENABLE}}$ input is high. $\overline{\text{SENSE\_OUT}}$ goes low after the capacitor-adjustable delay time when $V_{(SENSE)}$ is greater than V_{IT+} and the $\overline{\text{ENABLE}}$ pin is low. Open-drain devices(TPS3897/8) can be pulled up to 18 V independent of V_{CC}; pull-up resistors are required for these devices.
VCC	6	6	Supply voltage input. Connect a 1.7-V to 6.5-V supply to VCC to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

FUNCTIONAL BLOCK DIAGRAMS

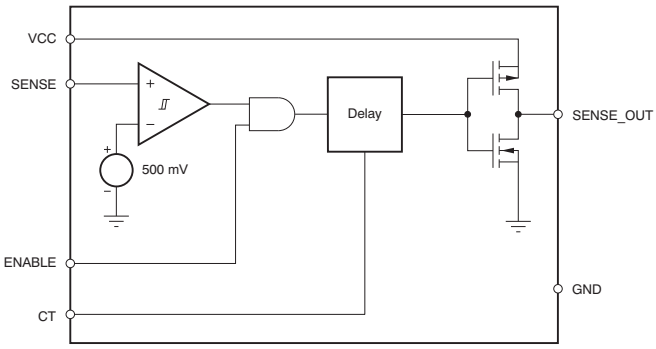


Figure 6. TPS3895A Block Diagram

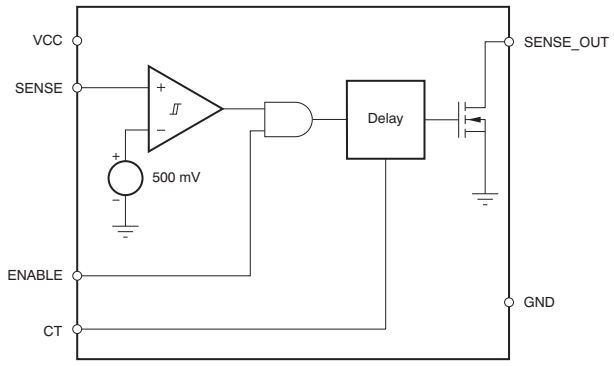


Figure 7. TPS3897A Block Diagram

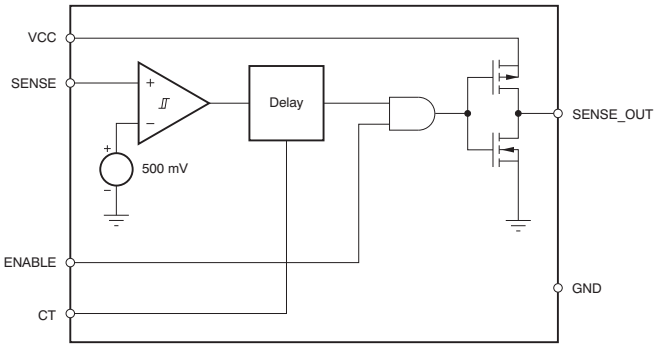


Figure 8. TPS3895P Block Diagram

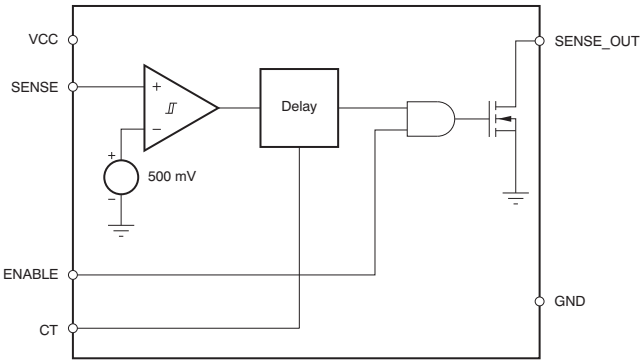


Figure 9. TPS3897P Block Diagram

TYPICAL CHARACTERISTICS

At T_A = +25°C, and V_{CC} = 3.3 V,unless otherwise noted.

SUPPLY CURRENT vs SUPPLY VOLTAGE

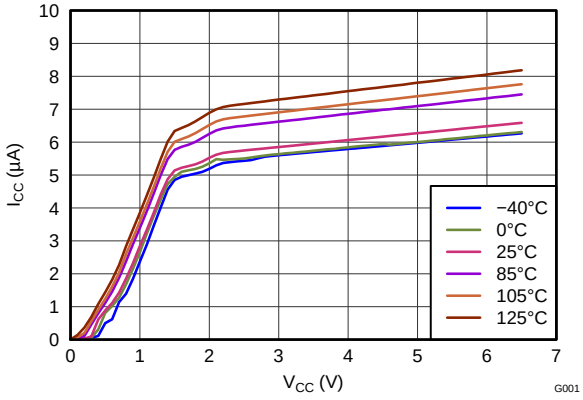


Figure 10.

SENSE_OUT TIMEOUT PERIOD vs C_{CT}

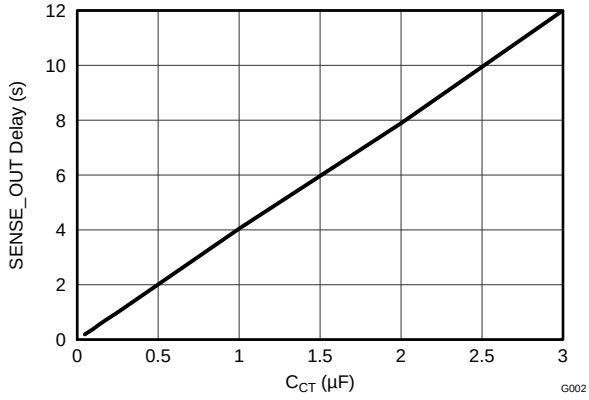


Figure 11.

SENSE_OUT TIMEOUT PERIOD vs TEMPERATURE (C_{CT} = 47 nF)

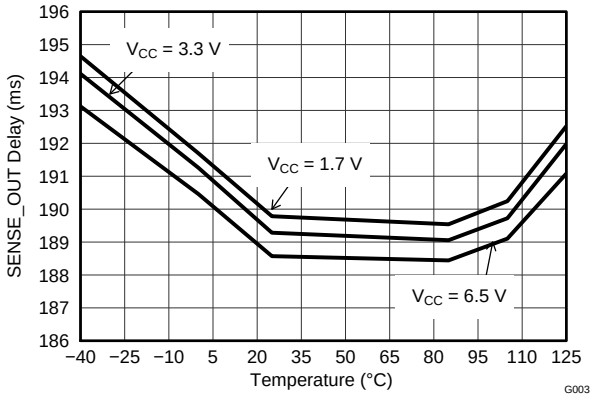


Figure 12.

SENSE THRESHOLD VOLTAGE vs TEMPERATURE

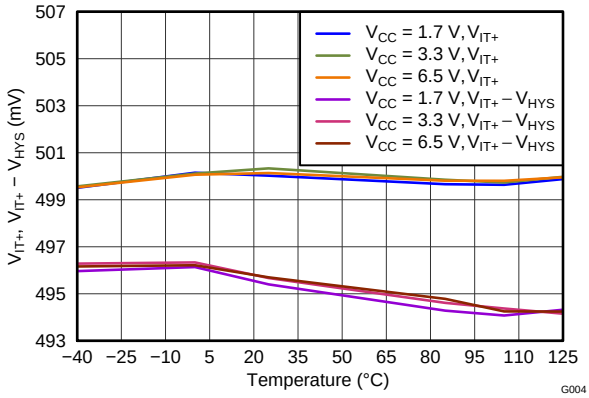


Figure 13.

SENSE MINIMUM PULSE DURATION vs SENSE THRESHOLD OVERDRIVE VOLTAGE

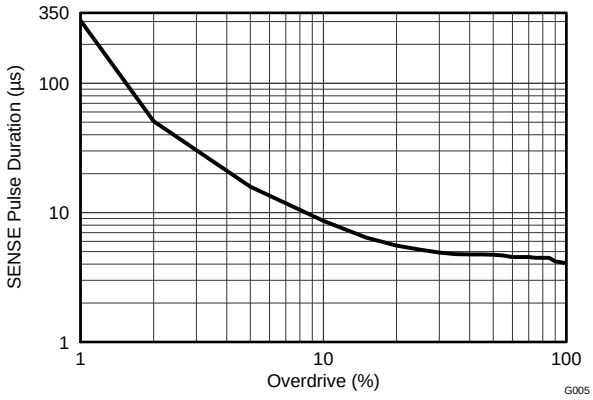


Figure 14.

OUTPUT VOLTAGE LOW vs OUTPUT CURRENT (0 mA to 1 mA)

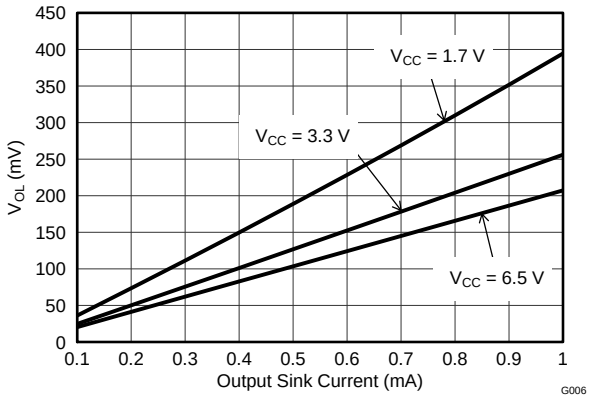


Figure 15.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, and V_{CC} = 3.3 V,unless otherwise noted.

OUTPUT VOLTAGE HIGH vs OUTPUT CURRENT (0 mA to 1 mA)

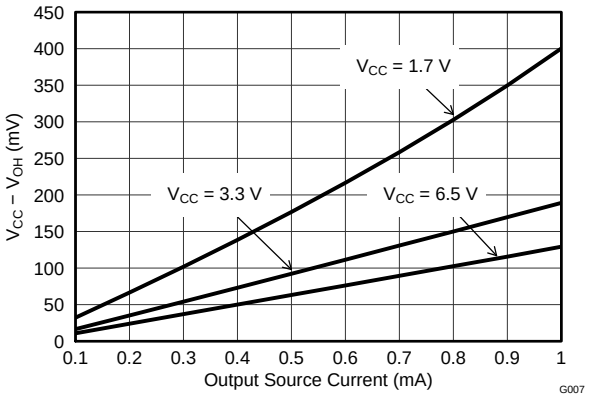


Figure 16.

OUTPUT VOLTAGE LOW AT 1 mA vs TEMPERATURE

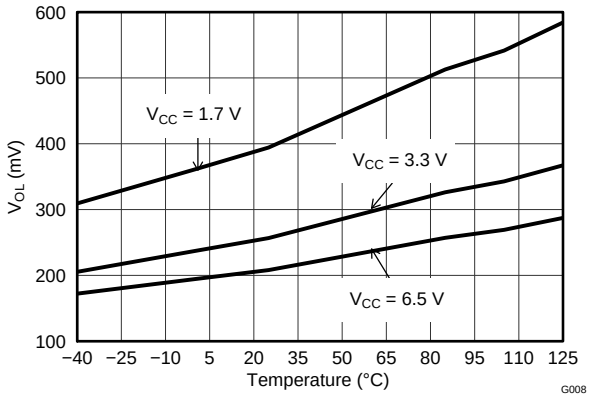


Figure 17.

OUTPUT VOLTAGE HIGH AT 1 mA vs TEMPERATURE

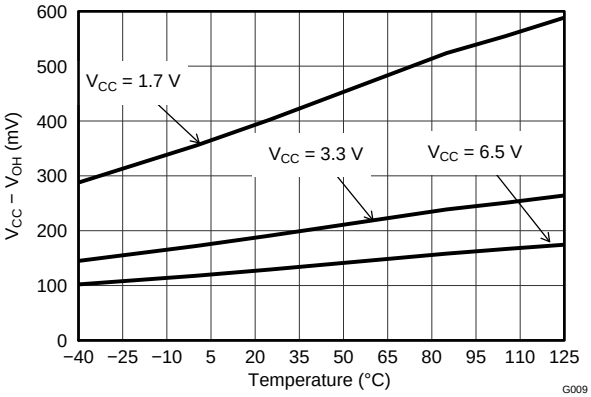


Figure 18.

OUTPUT VOLTAGE LOW vs OUTPUT CURRENT

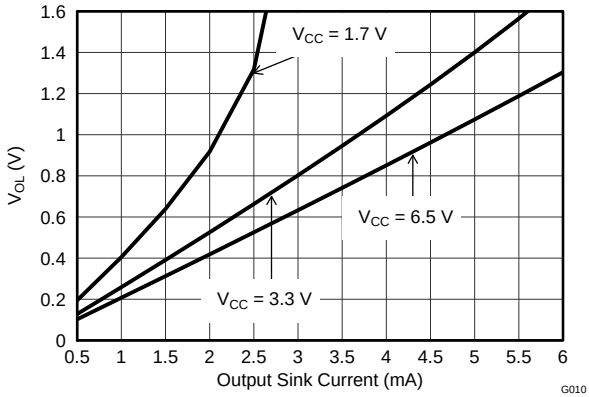


Figure 19.

OUTPUT VOLTAGE HIGH vs OUTPUT CURRENT

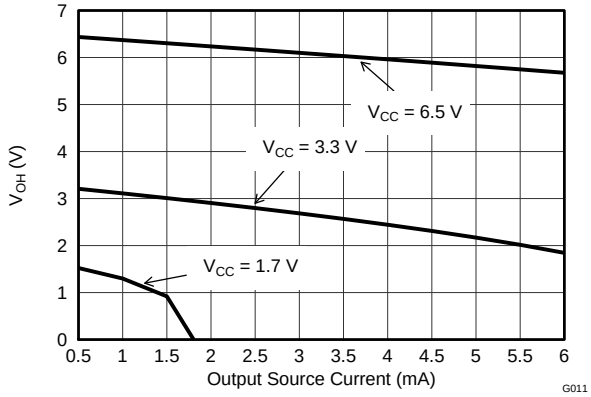


Figure 20.

ENABLE POWER ON/OFF DELAY (TPS3895A)

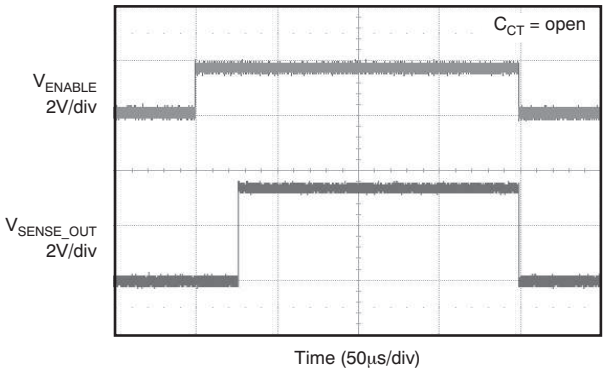


Figure 21.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, and V_{CC} = 3.3 V,unless otherwise noted.

ENABLE POWER ON/OFF DELAY (TPS3895P)

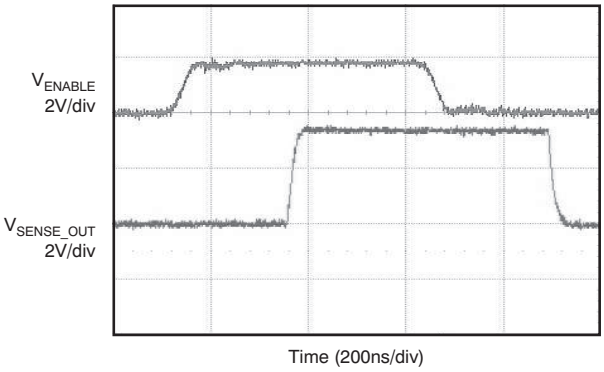


Figure 22.

THEORY OF OPERATION

GENERAL DESCRIPTION

The TPS3895, TPS3896, TPS3897, and TPS3898 devices (TPS389x) are a family of ultra-small supervisory circuits. The TPS389x is designed to assert the SENSE_OUT or $\overline{\text{SENSE\_OUT}}$ signal, as shown in Table 2 and Table 3. When the SENSE pin rises above 0.5 V and the enable input is asserted (ENABLE = high or $\overline{\text{ENABLE}}$ = low) , the output asserts (SENSE_OUT goes high or $\overline{\text{SENSE\_OUT}}$ goes low) after the capacitor-adjustable delay time. The SENSE pin can be set to any voltage threshold above 0.5 V using an external resistor divider. A broad range of output delay times and voltage thresholds can be supported, allowing these devices to be used in wide array of applications.

Table 2. TPS3895/7 Truth Table

CONDITIONS		OUTPUT	STATUS
ENABLE = high	SENSE < V_{IT+}	SENSE_OUT = low	Output not asserted
ENABLE = low	SENSE < V_{IT+}	SENSE_OUT = low	Output not asserted
ENABLE = low	SENSE > V_{IT+}	SENSE_OUT = low	Output not asserted
ENABLE = high	SENSE > V_{IT+}	SENSE_OUT = high	Output asserted after delay

Table 3. TPS3896/8 Truth Table

CONDITIONS		OUTPUT	STATUS
$\overline{\text{ENABLE}}$ = low	SENSE < V_{IT+}	$\overline{\text{SENSE\_OUT}}$ = high	Output not asserted
$\overline{\text{ENABLE}}$ = high	SENSE < V_{IT+}	$\overline{\text{SENSE\_OUT}}$ = high	Output not asserted
$\overline{\text{ENABLE}}$ = high	SENSE > V_{IT+}	$\overline{\text{SENSE\_OUT}}$ = high	Output not asserted
$\overline{\text{ENABLE}}$ = low	SENSE > V_{IT+}	$\overline{\text{SENSE\_OUT}}$ = low	Output asserted after delay

OUTPUT PIN (SENSE_OUT)

In a typical TPS389x application, the SENSE_OUT or $\overline{\text{SENSE\_OUT}}$ outputs are connected to a reset/enable input of the processor (DSP, CPU, FPGA, ASIC, etc.) or connected to the enable input of a voltage regulator.

The TPS3897 and TPS3898 provide open-drain outputs. Pull-up resistors must be used to hold these lines high when SENSE_OUT is asserted or $\overline{\text{SENSE\_OUT}}$ is not asserted. By connecting the pull-up resistors to the proper voltage rails, SENSE_OUT or $\overline{\text{SENSE\_OUT}}$ can be connected to other devices at the correct interface voltage levels. The outputs can be pulled up to 18 V independent of the supply voltage (V_{CC}). To ensure proper voltage levels, some thought should be given to choosing the correct pull-up resistor values. The ability to sink current is determined by the supply voltage; therefore, if V_{CC} = 5 V and the desired output pull-up is 18V, then to obtain a sink current of 1 mA or less (as mentioned in Electrical Characteristics), the pull-up resistor value should be greater than 18 kΩ . By using wired-OR logic, any combination of SENSE_OUT can be merged into one logic signal.

The TPS3895 and TPS3896 provide push-pull outputs. The logic high level of the outputs is determined by the VCC pin voltage. With this configuration, pull-up resistors are not required and some board area can be saved. However, all the interface logic levels should be examined. All the SENSE_OUT and $\overline{\text{SENSE\_OUT}}$ connections must be compatible with the VCC pin logic level.

The SENSE_OUT or $\overline{\text{SENSE\_OUT}}$ outputs are defined for a VCC voltage higher than 0.8 V. Table 2 and Table 3 are truth tables that describe how the outputs are asserted or de-asserted. When the conditions are met, the device changes state from de-asserted to asserted after a preconfigured delay time. However, the transitions from asserted to de-asserted are performed almost immediately with minimal propagation delay of 16 µs (typ). Figure 1 to Figure 4 show the timing diagrams and describe the relationship between the threshold voltages (V_{IT+} and V_{hys}), enable inputs, and respective outputs.

INPUT PIN (SENSE)

The SENSE input pin allows any system voltage above 0.5 V to be monitored. If the voltage at the SENSE pin exceeds V_{IT+}, and provided that the enable pin is asserted (ENABLE = high or $\overline{\text{ENABLE}}$ = low), then the output is asserted after the capacitor-adjustable delay time elapses. When the voltage at the SENSE pin drops below ($V_{IT+} – V_{hys}$), then the output is de-asserted. The comparator has a built-in hysteresis to ensure smooth output assertions and de-assertions. Although not required in most cases, for extremely noisy applications, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the SENSE input in order to reduce sensitivity to transients and layout parasitics.

The TPS389x family monitor the voltage at SENSE with the use of external resistor divider, as shown in Figure 23.

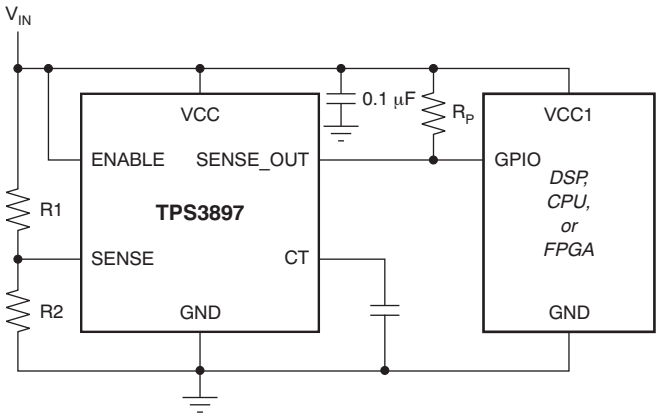


Figure 23. Using TPS3897 to Monitor User-Defined Threshold Voltage

The target threshold voltage can be calculated by using Equation 1:

$$V_{TARGET} = (1+R1/R2) \times 0.5 \text{ (V)} \quad (1)$$

When the input voltage (V_{IN}) shown in Figure 23 is greater than V_{TARGET}, then the output is asserted, provided that the enable pin is asserted (ENABLE = high or $\overline{\text{ENABLE}}$ = low). R1 and R2 can have high values (> 100 kΩ) to minimize current consumption as a result of a low SENSE input current without adding significant error to the resistive divider. Refer to application note SLVA450 to learn more about sizing sense-point resistors.

OUTPUT DELAY TIME PIN (CT)

To program a user-defined, adjustable delay time, an external capacitor must be connected between the CT pin and GND. If the CT pin is left open, there will be a delay of 40 µs. The adjustable delay time can be calculated through Equation 2:

$$t_{pd(r)}\ (s) = (C_{CT}\ (\mu F) \times 4) + 40\ \mu s \quad (2)$$

The reset delay time is determined by the time it takes an on-chip, precision 310 nA current source to charge the external capacitor to 1.24 V. When SENSE > V_{IT+} and with ENABLE high (or $\overline{\text{ENABLE}}$ low), the internal current sources are enabled and begin to charge the external capacitors. When the CT*n* voltage on a capacitor reaches 1.24 V, the corresponding SENSE_OUT or $\overline{\text{SENSE\_OUT}}$ is asserted. Note that a low-leakage type capacitor (such as ceramic) should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

ENABLE PIN (ENABLE)

The enable input allows an external logic signal from other processors, logic circuits, and/or discrete sensors to turn on/off the output. The TPS3895 and TPS3897 offer an active-high enable input (ENABLE) . The TPS3896 and TPS3898 offer an active-low enable input ($\overline{\text{ENABLE}}$). Driving ENABLE low (or $\overline{\text{ENABLE}}$ high) forces SENSE_OUT to go low (or $\overline{\text{SENSE\_OUT}}$ to go high). The 0.4-V (max) low and 1.4-V (min) high allow ENABLE to be driven with a 1.5-V or greater system supply.

The TPS389x family is available in two versions: the TPS389xA and TPS389xP. For TPS389xA devices with V_{SENSE} > V_{IT+}, driving ENABLE high (or $\overline{\text{ENABLE}}$ = low) makes SENSE_OUT go high (or $\overline{\text{SENSE\_OUT}}$ go low) after the capacitor-adjustable delay time. For the TPS389xP versions with V_{SENSE} > V_{IT+}, driving ENABLE high (or $\overline{\text{ENABLE}}$ low) makes SENSE_OUT go high (or $\overline{\text{SENSE\_OUT}}$ go low) after a 0.2-µs delay.

IMMUNITY TO SENSE PIN VOLTAGE TRANSIENTS

The TPS389x is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients depends on threshold overdrive, as shown in the typical characteristic Minimum Pulse Duration vs Threshold Overdrive Voltage (Figure 14).

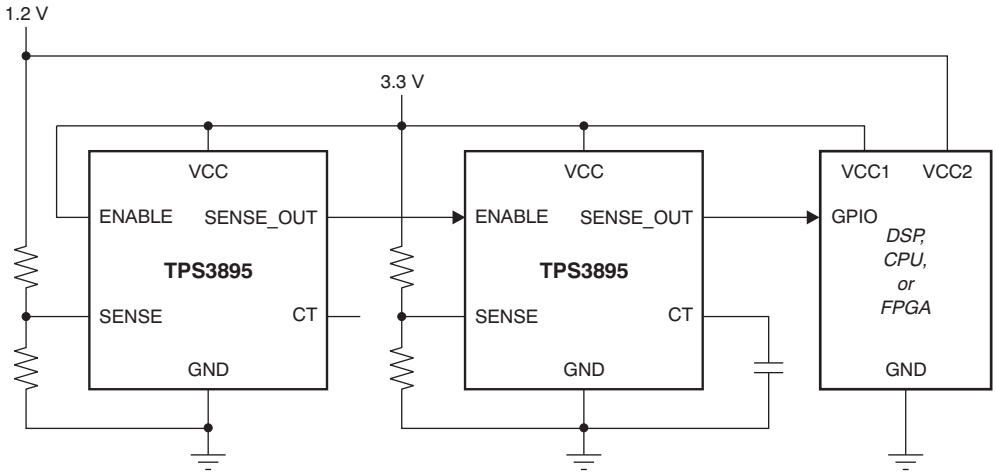


Figure 24. Multiple Voltage Monitoring Using the Enable Pin

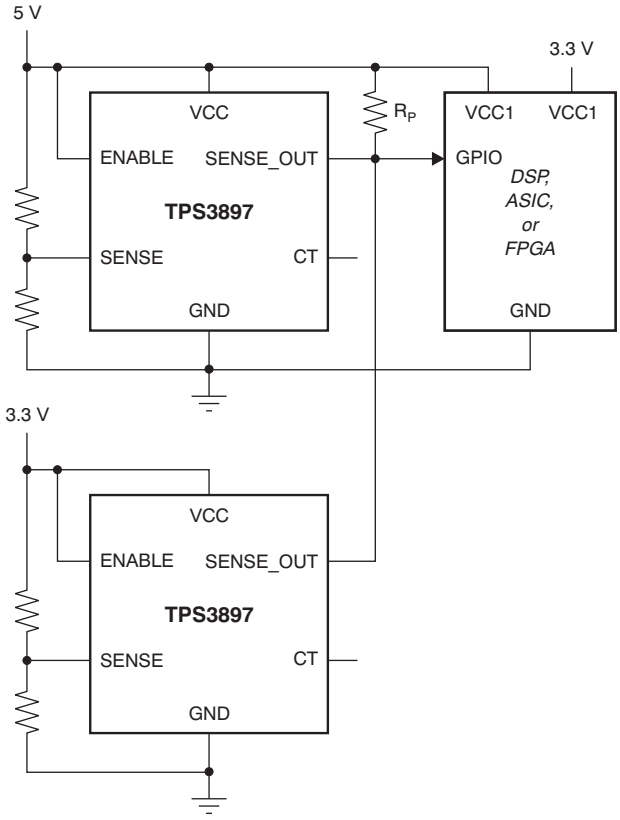


Figure 25. Multiple Voltage Monitoring using Wired-OR Logic at SENSE_OUT

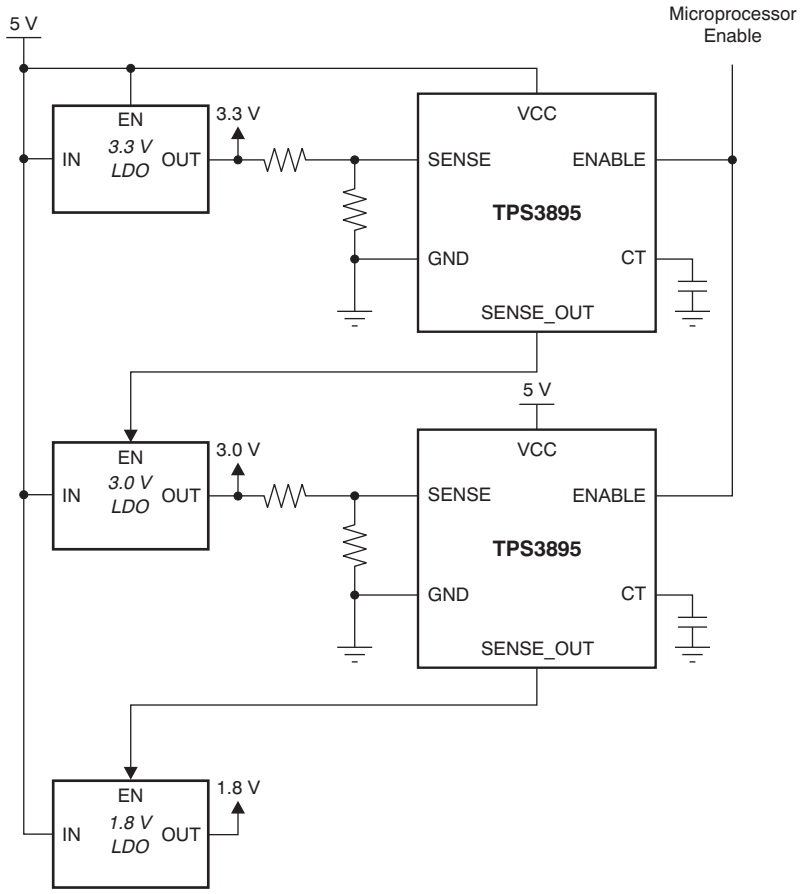


Figure 26. Voltage Sequencing (5 V → 3.3 V → 3.0 V → 1.8 V)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS3895ADRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UN	Samples
TPS3895ADRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UN	Samples
TPS3895PDRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UO	Samples
TPS3895PDRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UO	Samples
TPS3896ADRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UJ	Samples
TPS3896ADRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UJ	Samples
TPS3896PDRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UK	Samples
TPS3896PDRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UK	Samples
TPS3897ADRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UL	Samples
TPS3897ADRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UL	Samples
TPS3897PDRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UM	Samples
TPS3897PDRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UM	Samples
TPS3898ADRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UH	Samples
TPS3898ADRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UH	Samples
TPS3898PDRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UI	Samples
TPS3898PDRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

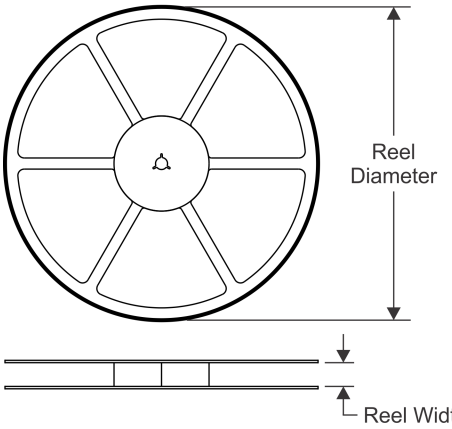
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

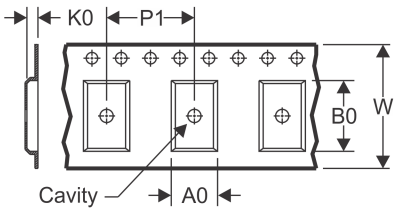
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

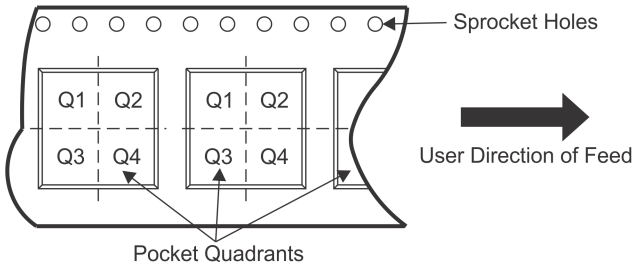


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

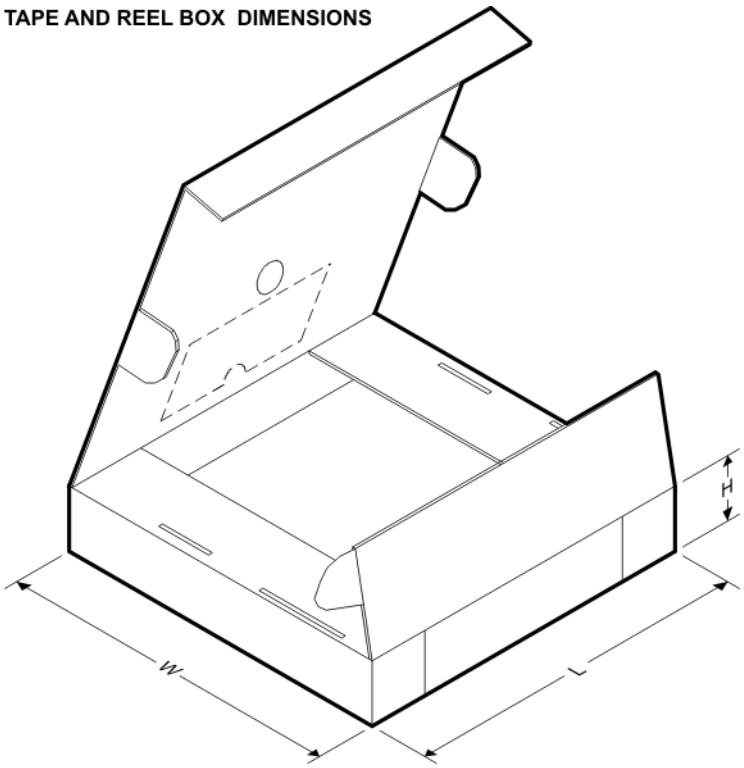
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3895ADRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3895ADRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3895PDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3895PDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3896ADRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3896ADRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3896PDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3896PDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3897ADRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3897ADRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3897PDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3897PDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3898ADRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3898ADRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3898PDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3898PDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1

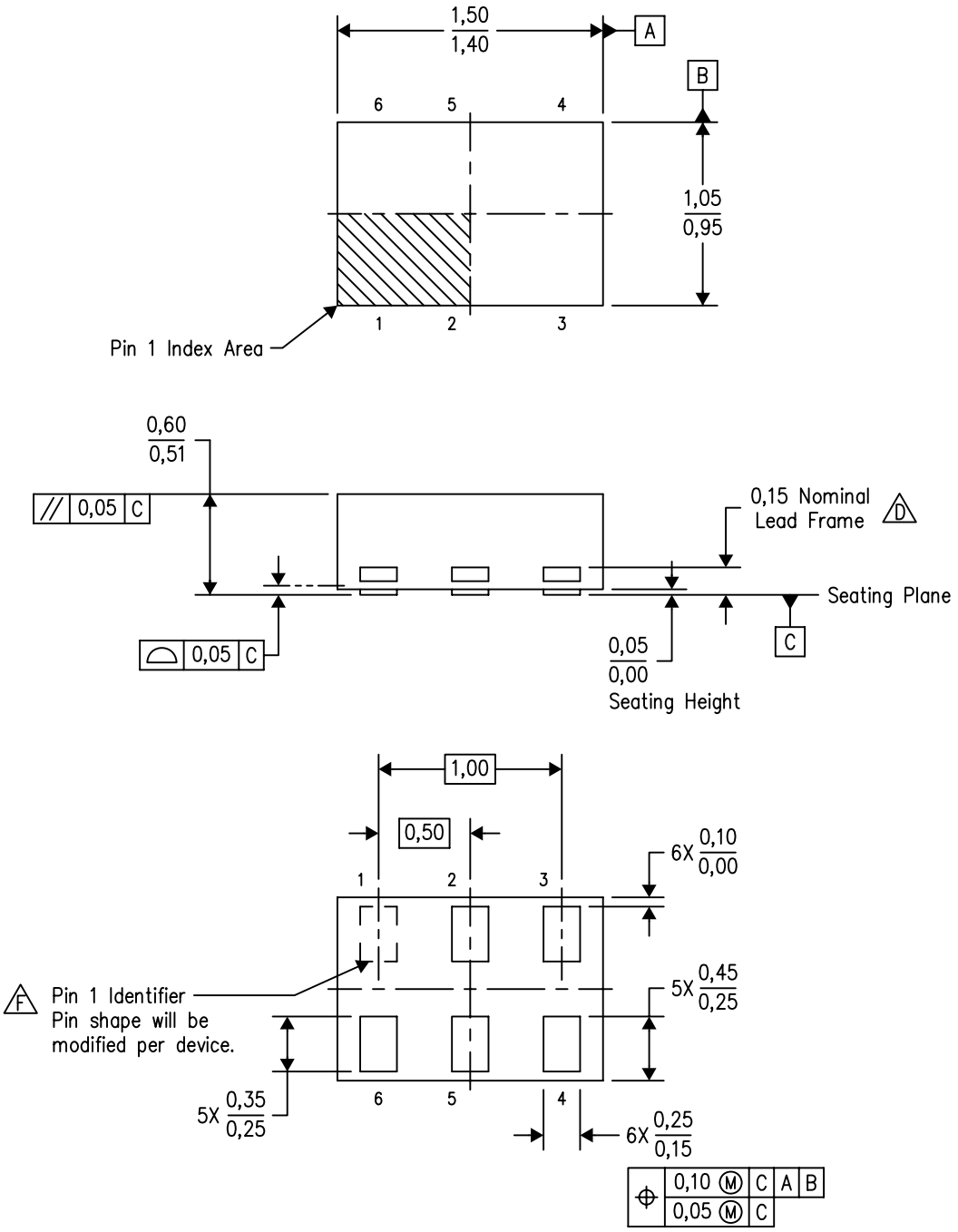
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3895ADRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3895ADRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3895PDRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3895PDRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3896ADRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3896ADRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3896PDRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3896PDRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3897ADRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3897ADRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3897PDRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3897PDRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3898ADRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3898ADRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3898PDRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3898PDRYT	SON	DRY	6	250	203.0	203.0	35.0

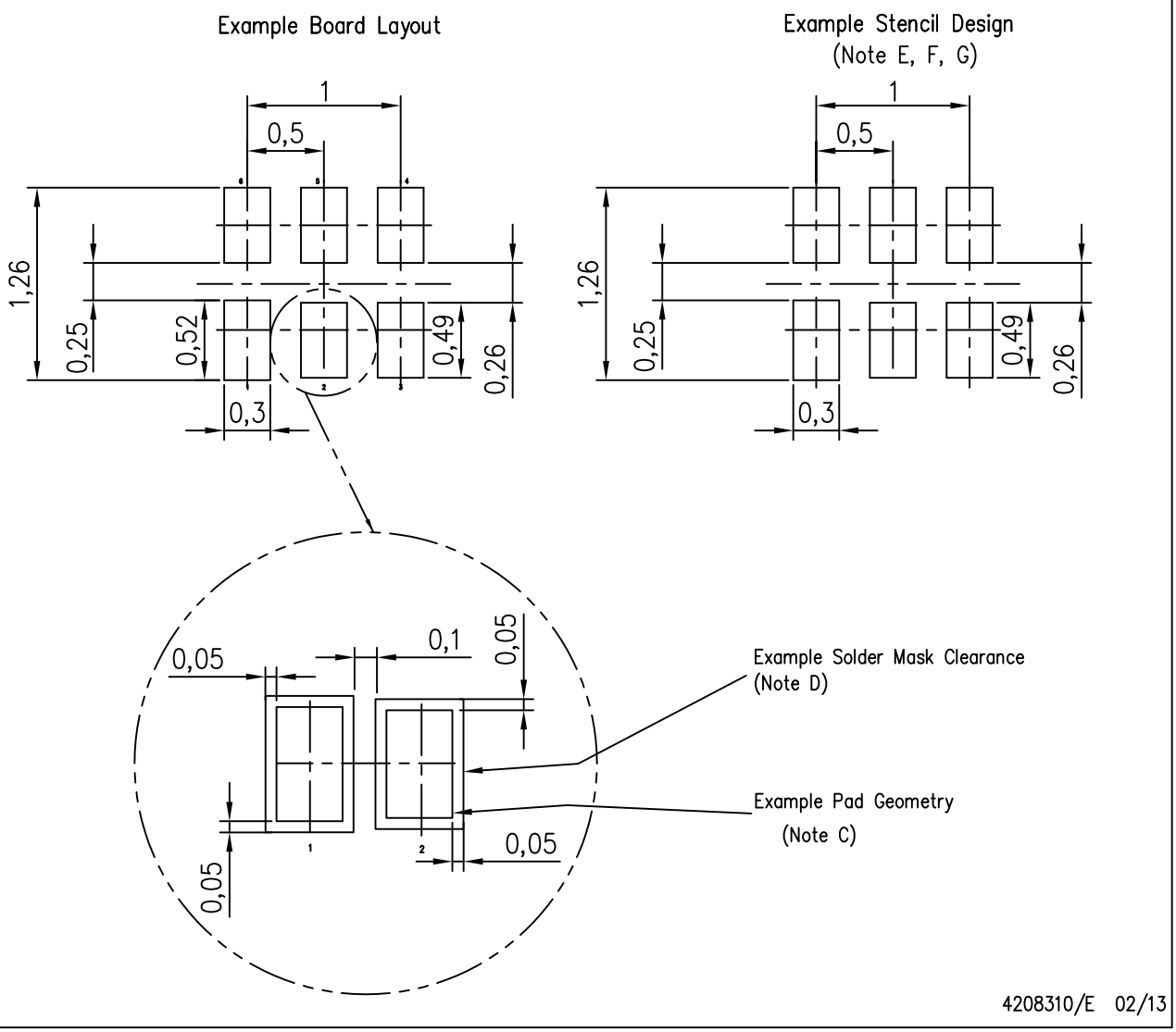
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4207181/F 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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