LOW POWER STEREO AUDIO DAC FOR PORTABLE AUDIO/TELEPHONY

FEATURES

- **Stereo Audio DAC**
  - **95-dBA Signal-to-Noise Ratio**
  - **16/20/24/32-Bit Data**
  - **Supports Rates From 8 kHz to 96 kHz**
  - **3D/Bass/Treble/EQ/De-emphasis Effects**
- **Two Audio Input Pins**
  - **Allows Analog Bypass Path**
- **Four Audio Output Drivers**
  - **Stereo 8-Ω, 500-mW/Channel Speaker Drive Capability**
  - **Stereo Fully Differential or Single-Ended Headphone Drivers**
- **Low Power: 18-mW Stereo 48-kHz Playback With 3.3-V Analog Supply**
- **Programmable Input/Output Analog Gains**
- **Programmable Microphone Bias Level**
- **Headphone Jack Detection**
- **Programmable PLL for Flexible Clock Generation**
- **I^2C Control Bus**
- **Audio Serial Data Bus Supports I^2S, Left/Right-Justified, DSP, and TDM Modes**
- **Extensive Modular Power Control**
- **Internal Selectable LDO Allows Operation From Single 3.3-V Supply**
- **Power Supplies:**
  - **Analog: 2.7 V–3.6 V.**
  - **Digital Core: 1.525 V–1.95 V**
  - **Digital I/O: 1.1 V–3.6 V**
- **Package: 5 ɔ5 mm 32-QFN**

DESCRIPTION

The TLV320DAC32 is a low power stereo audio DAC with and integrated power amplifier designed to drive stereo headphones or speakers. This device also has a pair of analog inputs which allow routing of external signals to the output amplifiers. The playback path includes a mix/mux capability from the stereo DAC and analog inputs, through programmable volume controls, to the headphone outputs. Extensive register-based power control is included, enabling stereo 96-kHz playback as low as 20mW from a 3.3-V analog supply, making it ideal for portable battery-powered audio and telephony applications.

The TLV320DAC32 contains four high-power output drivers. These drivers are capable of driving a variety of load configurations, including up to four channels of single-ended 16-Ω headphones using ac-coupling capacitors, or stereo 16-Ω headphones in a cap-less output configuration. In addition, pairs of drivers can be used to drive 8-Ω speakers in a BTL configuration at 500 mW per channel.

The stereo audio DAC supports sampling rates from 8-kHz to 96-kHz and includes programmable digital filtering in the DAC path for 3D, bass, treble, midrange effects, speaker equalization, and de-emphasis for 32-kHz, 44.1-kHz, and 48-kHz rates.

The serial control bus uses the I2C protocol, while the serial audio data bus is programmable for I2S, left/right-justified, DSP, or TDM modes. A highly programmable PLL is included for flexible clock generation and support for all standard audio rates from a wide range of available MCLKs, varying from 512-kHz to 50-MHz, with special attention paid to the most popular cases of 12-MHz, 13-MHz, 16-MHz, 19.2-MHz, and 19.68-MHz system clocks.

The TLV320DAC32 operates from analog supplies of 2.7 V – 3.6 V, a digital core supply of 1.525 V – 1.95 V, and a digital I/O supply of 1.1 V – 3.6 V. An internal LDO regulator allows the device to internally generate the lower voltage power supply needed for digital core logic, thereby allowing full operation from a single 3.3-V supply voltage.

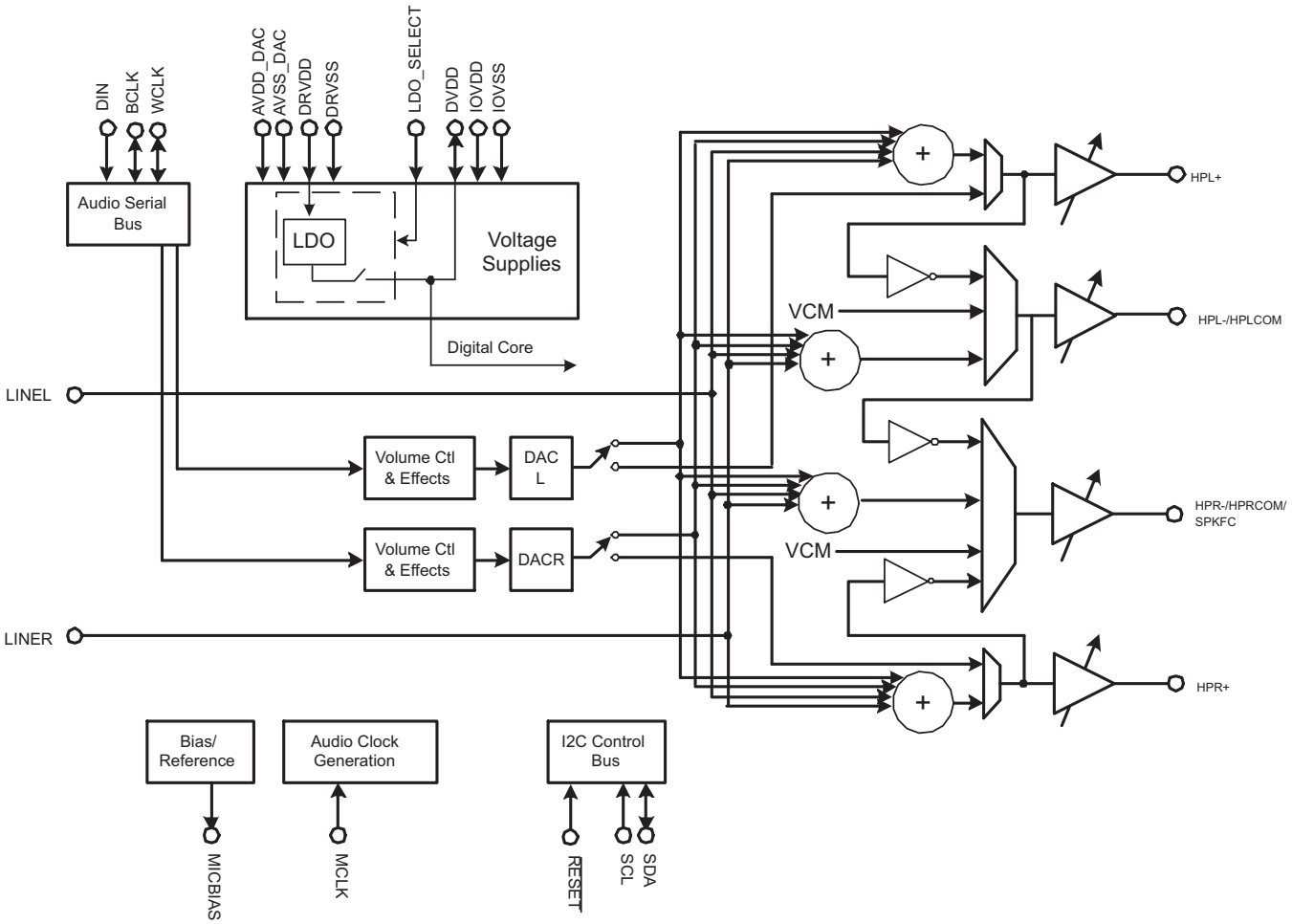
The TLV320DAC32 is a software-compatible subset of the existing TLV320AIC32 and TLV320AIC33 audio codecs, allowing simple transition from a system with record and playback to a system with playback only.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The device is available in a 5 x 5mm 32-lead QFN package.

SIMPLIFIED BLOCK DIAGRAM



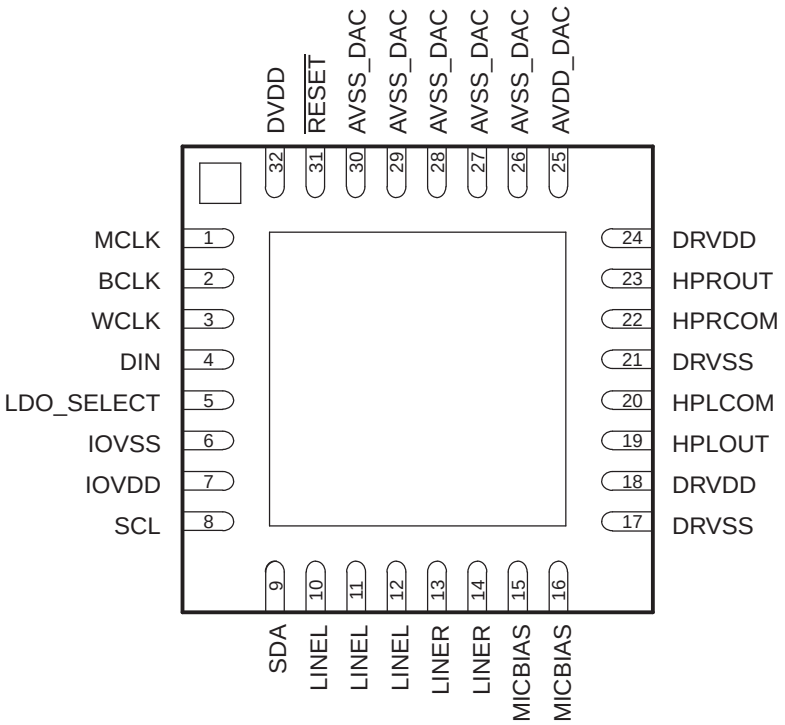
PACKAGING/ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLV320DAC32	QFN-32	RHB	–40C to 85C	TLV320DAC32IRHBT	Tape and Reel, 250
				TLV320DAC32IRHBR	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN ASSIGNMENTS

RHB PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION	
NO	NAME		
1	MCLK	Master Clock Input	
2	BCLK	Audio Serial Data Bus Bit Clock (Input/Output)	
3	WCLK	Audio Serial Data Bus Word Clock (Input/Output)	
4	DIN	Audio Serial Data Bus Data Input (Input)	
5	LDO_SELECT	LDO Regulator Select Pin	0 LDO Bypass — Connect 1.8-V power supply to DVDD pin to provide digital power to the device. Use decoupling capacitors to digital ground.
			1 Internal LDO — Generates 1.8-V internally. Do not connect DVDD pin to the external power supply. Add 0.1- µF decoupling capacitor to digital ground.
6	IOVSS	I/O Ground Supply, connect to digital ground on PCB, 0V	
7	IOVDD	I/O Voltage Supply, 1.1 V – 3.6 V	
8	SCL	I^2C Serial Clock	
9	SDA	I^2C Serial Data Input/Output	
10	LINEL	Line Analog Input (Left)	
11	LINEL	Line Analog Input (Left)	
12	LINEL	Line Analog Input (Left)	
13	LINER	Line Analog Input (Right or Multifunctional)	
14	LINER	Line Analog Input (Right or Multifunctional)	
15	MICBIAS	Microphone Bias Voltage Output	
16	MICBIAS	Microphone Bias Voltage Output	
17	DRVSS	Analog Output Driver Ground Supply, 0 V	
18	DRVDD	Output Driver Voltage Supply, 2.7 V–3.6 V	
19	HPLOUT	High-Power Output Driver (Left Plus)	

TERMINAL FUNCTIONS (continued)

TERMINAL		DESCRIPTION
NO	NAME	
20	HPLCOM	High-Power Output Driver (Left Minus or Multifunctional)
21	DRVSS	Analog Output Driver Ground Supply, 0 V
22	HPRCOM	High-Power Output Driver (Right Minus or Multifunctional)
23	HPROUT	High-Power Output Driver (Right Plus)
24	DRVDD	Output Driver Voltage Supply, 2.7 V–3.6 V
25	AVDD_DAC	Analog and DAC Voltage Supply, 2.7 V–3.6 V
26,27, 28,29, 30	AVSS_DAC	Analog and DAC Ground Supply, 0 V
31	$\overline{\text{RESET}}$	Reset
32	DVDD	Digital Core Voltage Supply, add 0.1-µF capacitor to digital ground. Connect to 1.8-V power supply if LDO_SELECT = 0 V.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

		VALUE	UNIT
	AVDD_DAC to AVSS_DAC, DRVDD to DRVSS	–0.3 to 3.9	V
	AVDD_DAC to DRVSS	–0.3 to 3.9	V
	IOVDD to IOVSS	–0.3 to 3.9	V
	DVDD to IOVSS	–0.3 to 2.5	V
	AVDD_DAC to DRVDD	–0.1 to 0.1	V
	Digital input voltage to IOVSS	–0.3 V to IOVDD+0.3	V
	Analog input voltage to AVSS_DAC	–0.3 V to AVDD_DAC+0.3	V
	Operating temperature range	-40 to +85	C
	Storage temperature range	-65 to +105	C
T_J Max	Junction temperature	105	C
	Power dissipation	(T_J Max – T_A) / θ_{JA}	
θ_{JA}	Thermal impedance	44	C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) ESD compliance tested to EIA / JESD22-A114-B and passed.

DISSIPATION RATINGS(1)

T_A = 25C POWER RATING	DERATING FACTOR	T_A = 75C POWER RATING	T_A = 85C POWER RATING
1.82 W	22.7 mW/C	681 mW	454 mW

(1) This data was taken using 2 oz. trace and copper pad that is soldered directly to a JEDEC standard 4-layer 3 in ɔ3 in PCB.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD_DAC, DRVDD(1)	Analog supply voltage	2.7	3.3	3.6	V
DVDD(1)	Digital core supply voltage	1.525	1.8	1.95	V
IOVDD(1)	Digital I/O supply voltage	1.1	1.8	3.6	V
V_I	Analog full-scale 0-dB input voltage (DRVDD = 3.3 V)		0.707		V_{RMS}
	Stereo headphone-output load resistance	16			Ω
	Digital output load capacitance		10		pF
T_A	Operating free-air temperature	–40		85	C

(1) Analog voltage values are with respect to AVSS_DAC, DRVSS; digital voltage values are with respect to IOVSS.

ELECTRICAL CHARACTERISTICS

At 25C, AVDD_DAC, DRVDD, IOVDD = 3.3 V, DVDD = 1.8 V, Fs = 48 kHz, 16-bit audio data (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG MIXER					
Input resistance	LINE inputs		100		kΩ
Input capacitance	LINE inputs		10		pF
Input volume control minimum attenuation setting			0		dB
Input volume control maximum attenuation setting			78		dB
Input volume control attenuation step size			0.5		dB
MICROPHONE BIAS					
Bias voltage	Programmable settings, load = 750 Ω		2.0		V
		2.25	2.5	2.75	
			DRVDD-0.2		
Current sourcing	2.5-V Setting			4	mA
DAC DIGITAL INTERPOLATION FILTER	**Fs = 48 kHz**				
Passband	High-pass filter disabled			0.45Ös	Hz
Passband ripple	High-pass filter disabled		0.06		dB
Transition band		0.45Ös		0.55Ös	Hz
Stopband		0.55Ös		7.5Ös	Hz
Stopband attenuation			65		dB
Group delay			21/Fs		Sec
SINGLE-ENDED STEREO HEADPHONE DRIVER	**AC-coupled output configuration(1)**				
0-dB full-scale output voltage	0-dB Gain to high power outputs. Output common-mode voltage setting = 1.65 V		0.65		V_{RMS}
Programmable output common mode voltage (applicable to Line Outputs also)	First option		1.35		V
	Second option		1.50		
	Third option		1.65		
	Fourth option		1.8		

(1) Unless otherwise noted, all measurements use output common-mode voltage setting of 1.35 V, 0-dB output level control gain, 16-Ω single-ended load.

ELECTRICAL CHARACTERISTICS (continued)

At 25C, AVDD_DAC, DRVDD, IOVDD = 3.3 V, DVDD = 1.8 V, Fs = 48 kHz, 16-bit audio data (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Maximum programmable output level control gain				9		dB
	Programmable output level control gain step size				1		dB
P_O	Maximum output power	R_L = 32 Ω, 0.1% THD			25		mW
		R_L = 16 Ω, 0.1% THD			50		
SNR	Signal-to-noise ratio(2)			85	94		dB
	Total harmonic distortion	1-kHz Output, P_O = 26 mW, R_L = 16 Ω			–79	–60	dB%
					0.011		
	Channel separation	1 kHz, 0-dB Input			85		dB
	Power supply rejection ratio	1 KHz, 100 mVpp on AVDD_DAC, DRVDD1/2			52		dB
	Mute attenuation	1-kHz Output			107		dB
DIFFERENTIAL STEREO HEADPHONE DRIVER							
	0-dB full-scale output voltage	0-dB Gain to high power outputs. Output common-mode voltage setting = 1.65 V, Differential output configuration(3)			1.27		V
SNR	Signal-to-noise ratio(4)				95		dB
DIFFERENTIAL SPEAKER DRIVER							
P_O	Maximum output power	DRVDD = 3.6 V, HPLCOM = 1.8 V, HPLCOM/HPRCOM Gain = 5, R_L = 8 Ω			0.5		W
	0-dB Full-scale output voltage	0-dB Gain for HPLCOM/HPRCOM, Output common-mode voltage setting = 1.65 V, R_L = 8 Ω			1.15		Vrms
	Total harmonic distortion	Fs = 48 kHz, 0-dB Full-scale signal, 0-dB Gain at HPLCOM/HPRCOM, R_L = 8 Ω			–71		dB
DIGITAL I/O							
V_{IL}	Input low level	I_{IL} = +5 µA		–0.3		0.3 ıIOVDD	V
V_{IH}	Input high level(5)	I_{IH} = +5 µA, IOVDD > 1.6 V		0.7 ıIOVDD			V
		I_{IH} = +5 µA, IOVDD < 1.6 V		IOVDD			
V_{OL}	Output low level	I_{IH} = 2 TTL loads				0.1 ıIOVDD	V
V_{OH}	Output high level	I_{OH} = 2 TTL loads		0.8 ıIOVDD			V
SUPPLY CURRENT							
Headphone amplifier	Current	AVDD_DAC+DRVDD	LINEL/R only routed to single-ended stereo headphones, DAC = off, Analog Mixer = on, PLL = off, LDO = off, analog mixer enabled, no signal applied		3.99		mA
		DVDD			0.025		
		IOVDD			0.001		
	Power	AVDD_DAC+DRVDD			13.17		mW
		DVDD			0.045		
		IOVDD			0.003		

(2) Ratio of output level with a 1-kHz full-scale input, to the output level playing an all-zero signal, measured , A-weighted over a 20-Hz to 20-kHz bandwidth.
(3) Unless otherwise noted, all measurements use output common-mode voltage setting of 1.35 V, 0-dB output level control gain, 16-Ω differential load.
(4) Ratio of output level with a 1-kHz full-scale input, to the output level playing an all-zero signal, measured , A-weighted over a 20-Hz to 20-kHz bandwidth.
(5) When IOVDD < 1.6 V, minimum V_{IH} is 1.1 V.

ELECTRICAL CHARACTERISTICS (continued)

At 25C, AVDD_DAC, DRVDD, IOVDD = 3.3 V, DVDD = 1.8 V, Fs = 48 kHz, 16-bit audio data (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DAC + Headphone amplifier	Current	AVDD_DAC+DRVDD	Fs = 48 kHz, DAC = on, Analog Mixer = off, Single-Ended Headphone Driver = on, PLL = off, LDO = off, DAC direct (analog mixer bypassed)		4.3		mA
		DVDD			2		
		IOVDD			0.015		
	Power	AVDD_DAC+DRVDD			14.2		mW
		DVDD			3.6		
		IOVDD			0.05		
DAC + Analog Mixer + Headphone amplifier	Current	AVDD_DAC+DRVDD	Fs = 48 kHz, DAC = on, Analog Mixer = on, Single-Ended Headphone Driver = on, PLL = off, LDO = off		4.99		mA
		DVDD			2.07		
		IOVDD			0.015		
	Power	AVDD_DAC+DRVDD			16.5		mW
		DVDD			3.73		
		IOVDD			0.05		
DAC + PLL + Analog Mixer + Headphone amplifier	Current	AVDD_DAC+DRVDD	Fs = 48 kHz, DAC = on, Analog Mixer = on, Single-Ended Headphone Driver = on, PLL = on, LDO = off		6.08		mA
		DVDD			2.81		
		IOVDD			0.016		
	Power	AVDD_DAC+DRVDD			20.06		mW
		DVDD			5.06		
		IOVDD			0.05		
LDO	Current	AVDD_DAC+DRVDD	All circuit blocks = off		2		mA
		DVDD			0		
		IOVDD			0		
	Power	AVDD_DAC+DRVDD			6.6		mW
		DVDD			0		
		IOVDD			0		
Power down	Current	AVDD_DAC+DRVDD	All supply voltages applied, all blocks programmed in lowest power state		0.1		µA
		DVDD			0.5		
		IOVDD			0.1		
	Power	AVDD_DAC+DRVDD			0.33		µW
		DVDD			0.9		
		IOVDD			0.33		

AUDIO DATA SERIAL INTERFACE TIMING DIAGRAM

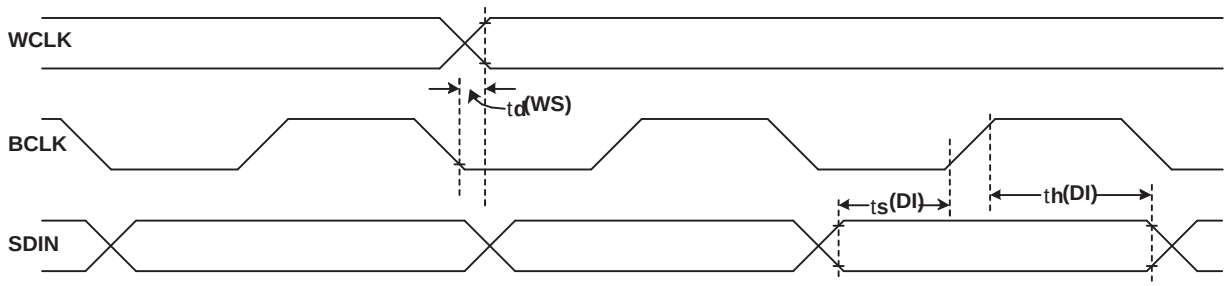


Figure 1. I²S/LJF/RJF Timing in Master Mode

TIMING CHARACTERISTICS(1)

All specifications typical at 25C, DVDD = 1.8 V

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d (WS)	WCLK delay time		50		15	ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		30		10	ns
t_f	Fall time		30		10	ns

(1) All timing specifications are measured at characterization but not tested at final test.

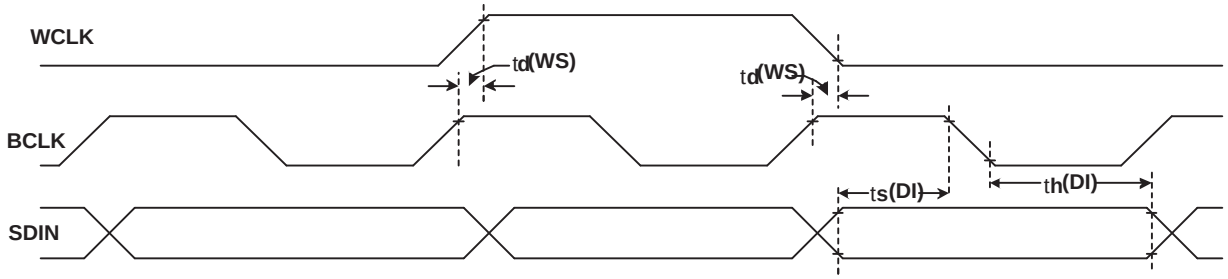


Figure 2. DSP Timing in Master Mode

TIMING CHARACTERISTICS(1)

All specifications typical at 25C, DVDD = 1.8 V

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d (WS)	WCLK delay time		50		15	ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		30		10	ns
t_f	Fall time		30		10	ns

(1) All timing specifications are measured at characterization but not tested at final test.

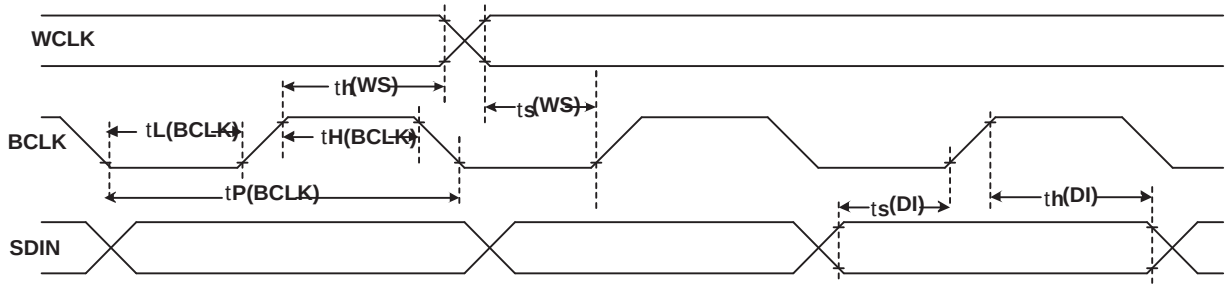


Figure 3. I²S/LJF/RJF Timing in Slave Mode

TIMING CHARACTERISTICS(1)

All specifications typical at 25C, DVDD = 1.8 V

(1) All timing specifications are measured at characterization but not tested at final test.

TIMING CHARACTERISTICS (continued)

All specifications typical at 25C, DVDD = 1.8 V

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H (BCLK)	BCLK high period	70		35		ns
t_L (BCLK)	BCLK low period	70		35		ns
t_s(WS)	WCLK setup time	10		6		ns
t_h(WS)	WCLK hold time	10		6		ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		8		4	ns
t_f	Fall time		8		4	ns

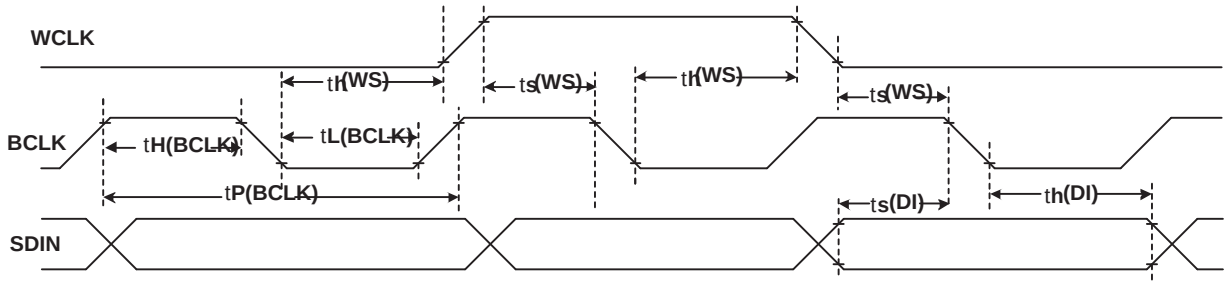


Figure 4. DSP Timing in Slave Mode

TIMING CHARACTERISTICS(1)

All specifications typical at 25C, DVDD = 1.8 V

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H (BCLK)	BCLK high period	70		35		ns
t_L (BCLK)	BCLK low period	70		35		ns
t_s(WS)	WCLK setup time	10		8		ns
t_h(WS)	WCLK hold time	10		8		ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		8		4	ns
t_f	Fall time		8		4	ns

(1) All timing specifications are measured at characterization but not tested at final test.

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
POWER
(HPLOUT Differential 16.2 Ω)

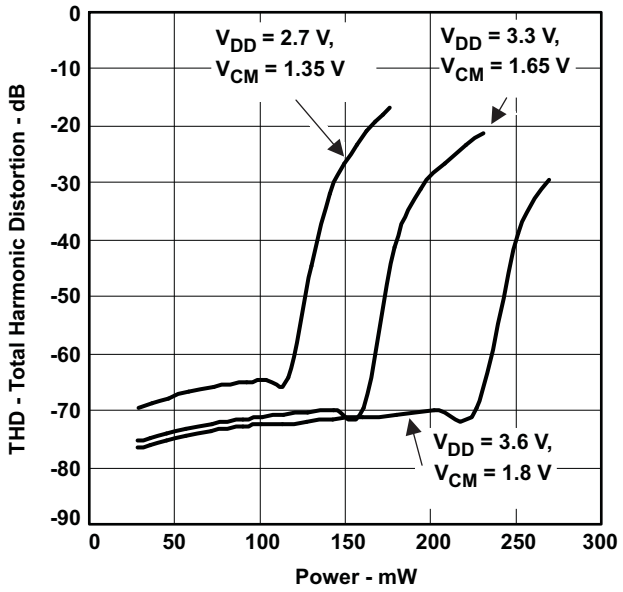


Figure 5.

TOTAL HARMONIC DISTORTION
vs
POWER
(HPROUT Differential 16.2 Ω)

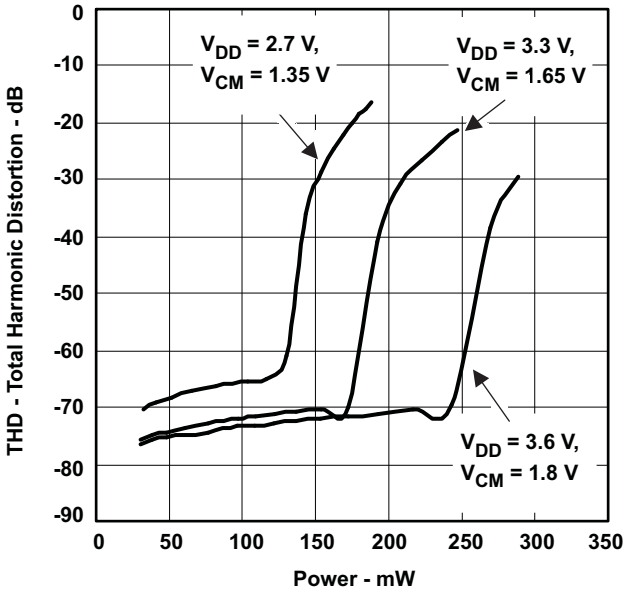


Figure 6.

TOTAL HARMONIC DISTORTION
vs
POWER
(HPLOUT Single Ended 16.2 Ω)

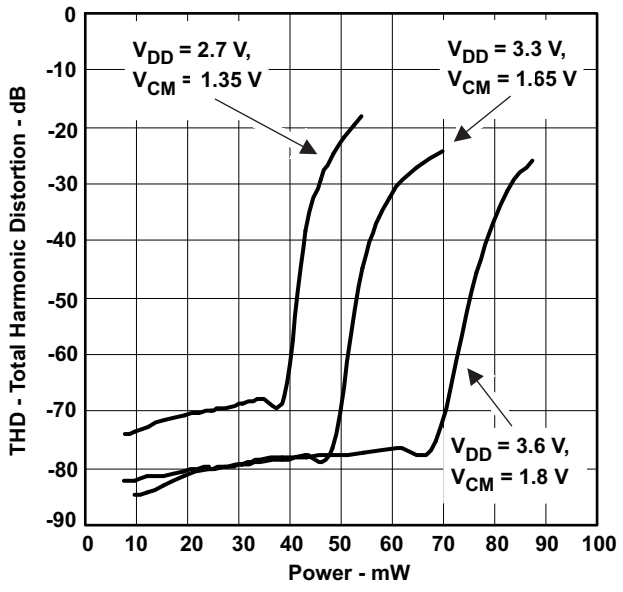


Figure 7.

TOTAL HARMONIC DISTORTION
vs
POWER
(HPROUT Single Ended 16.2 Ω)

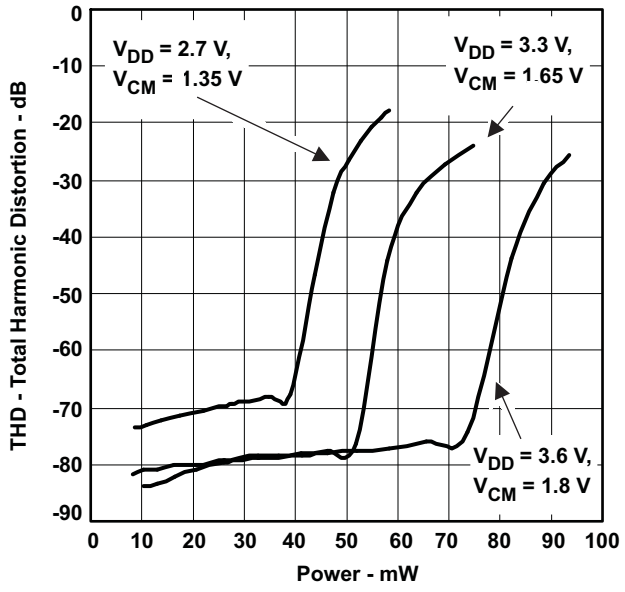


Figure 8.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION
vs
POWER
(HPLCOM - HPRCOM Differential 8.2 Ω)

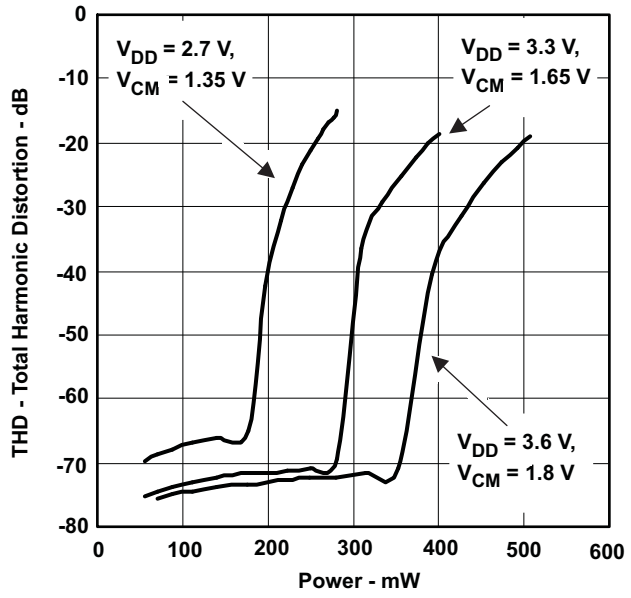


Figure 9.

MIC BIAS VOLTAGE
vs
SUPPLY VOLTAGE

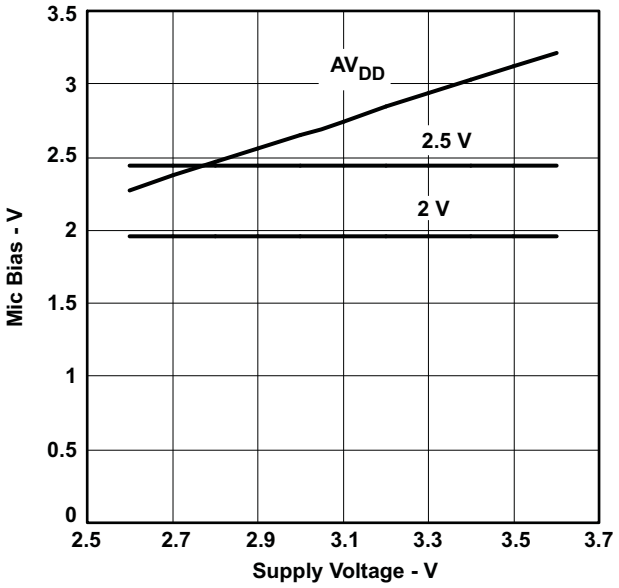


Figure 10.

LEFT/RIGHT CHANNEL DAC FREQUENCY RESPONSE
vs
FREQUENCY

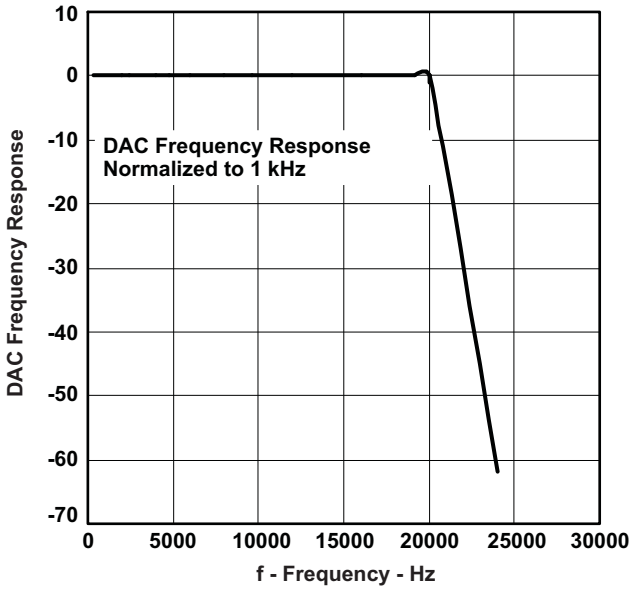


Figure 11.

HEADPHONE OUTPUT
vs
ANALOG MIXER ATTENUATION

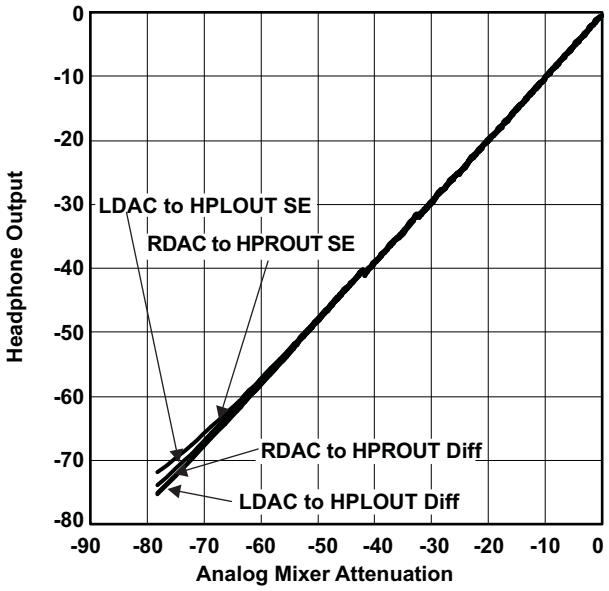


Figure 12.

TYPICAL CHARACTERISTICS (continued)

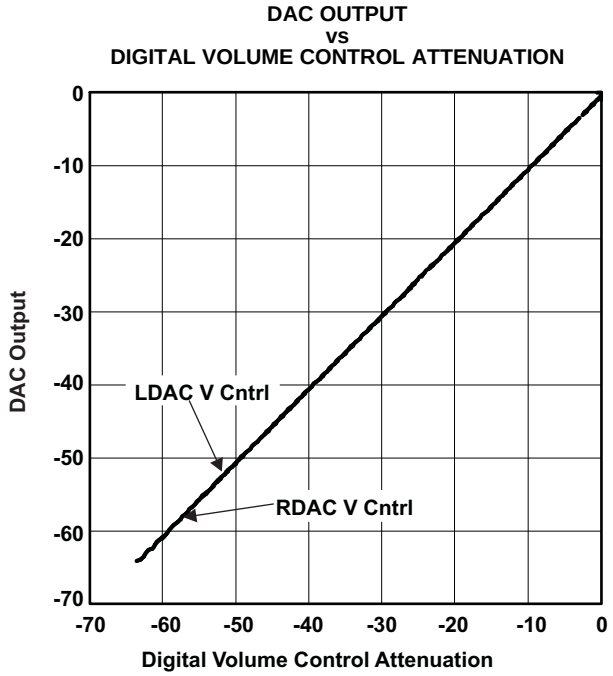


Figure 13.

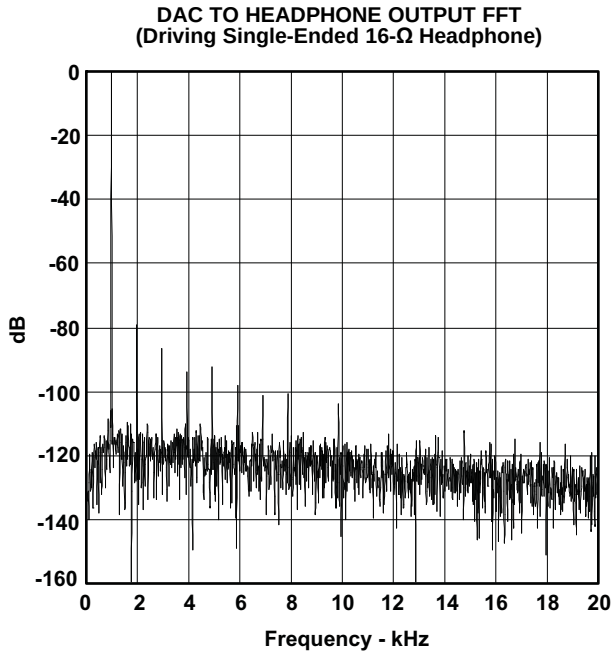


Figure 14.

TYPICAL CHARACTERISTICS (continued)

TYPICAL CIRCUIT CONFIGURATION

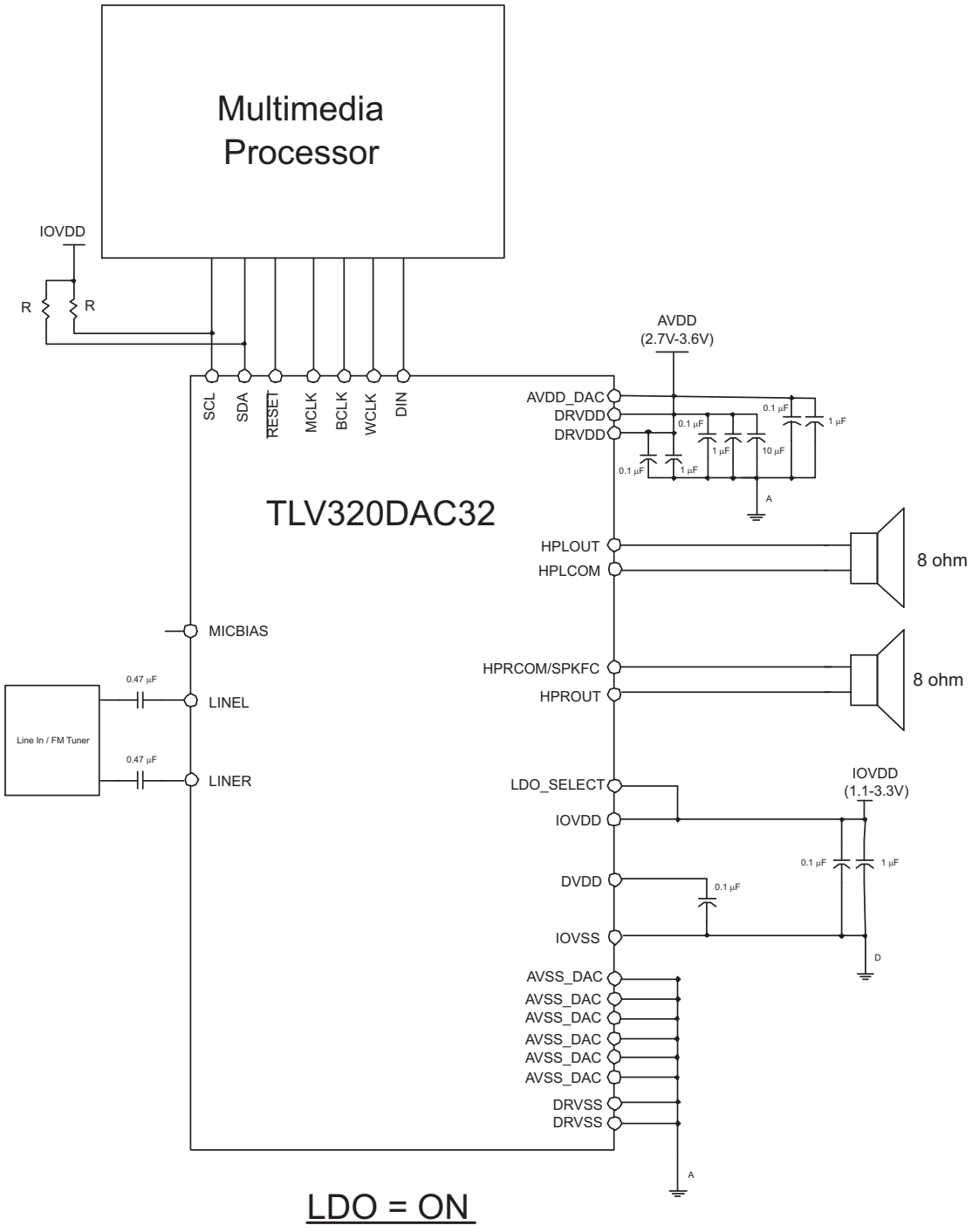


Figure 15. Internal 8-Ω Speaker Driver with LDO

TYPICAL CHARACTERISTICS (continued)

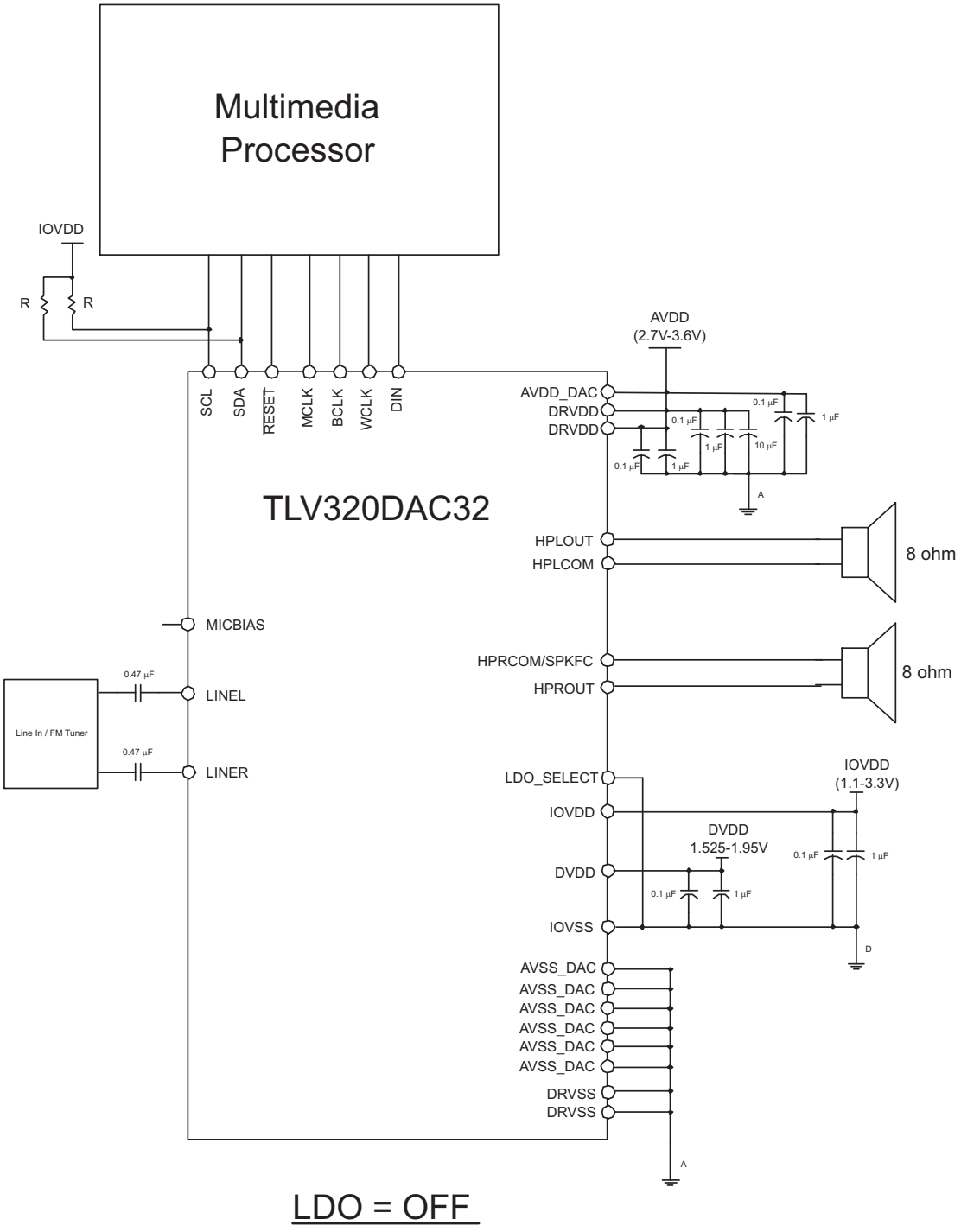


Figure 16. Internal 8-Ω Speaker Driver with External DVDD Supply (LDO Off)

TYPICAL CHARACTERISTICS (continued)

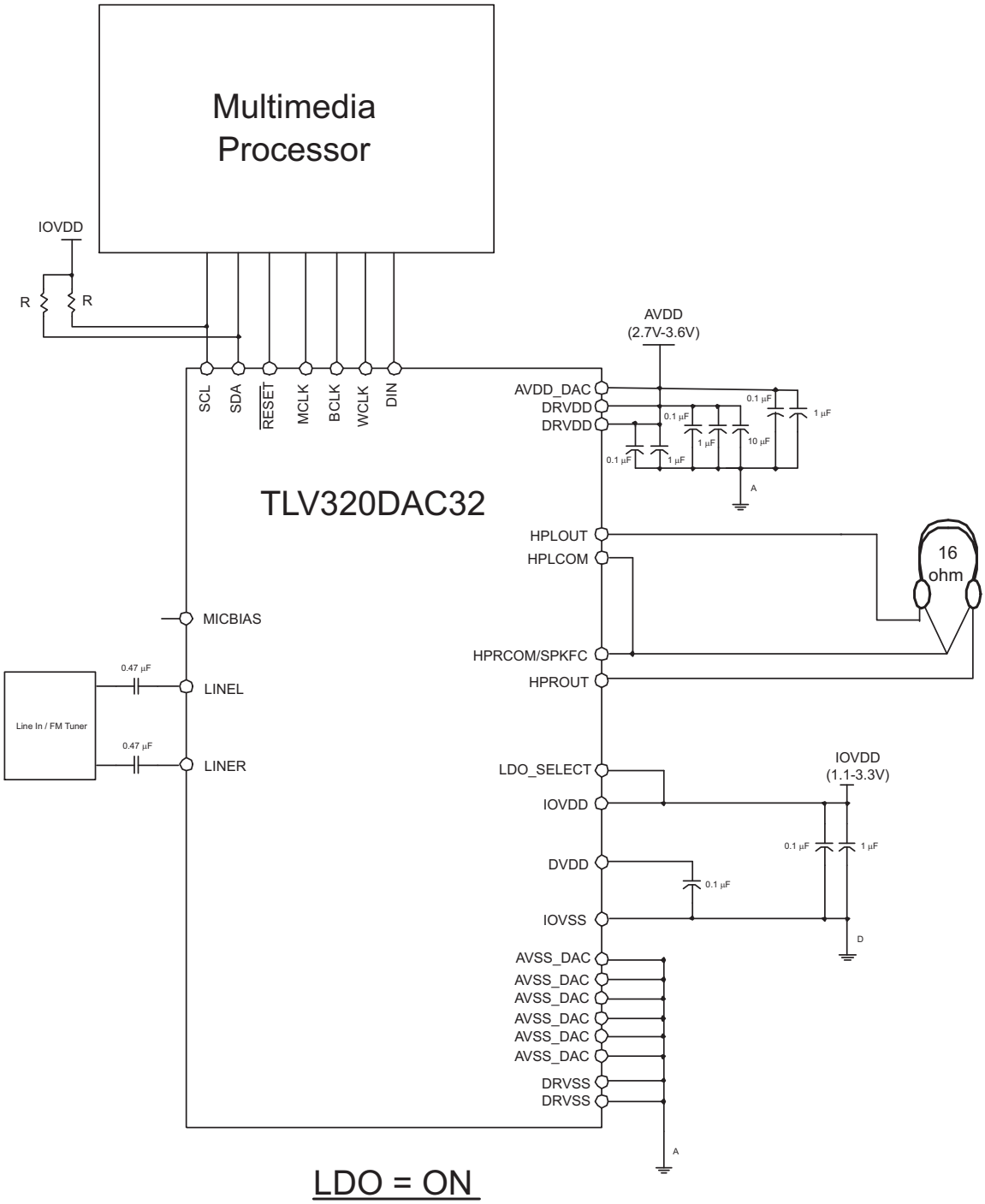


Figure 17. Capless Connection of Headphone Driver with LDO

TYPICAL CHARACTERISTICS (continued)

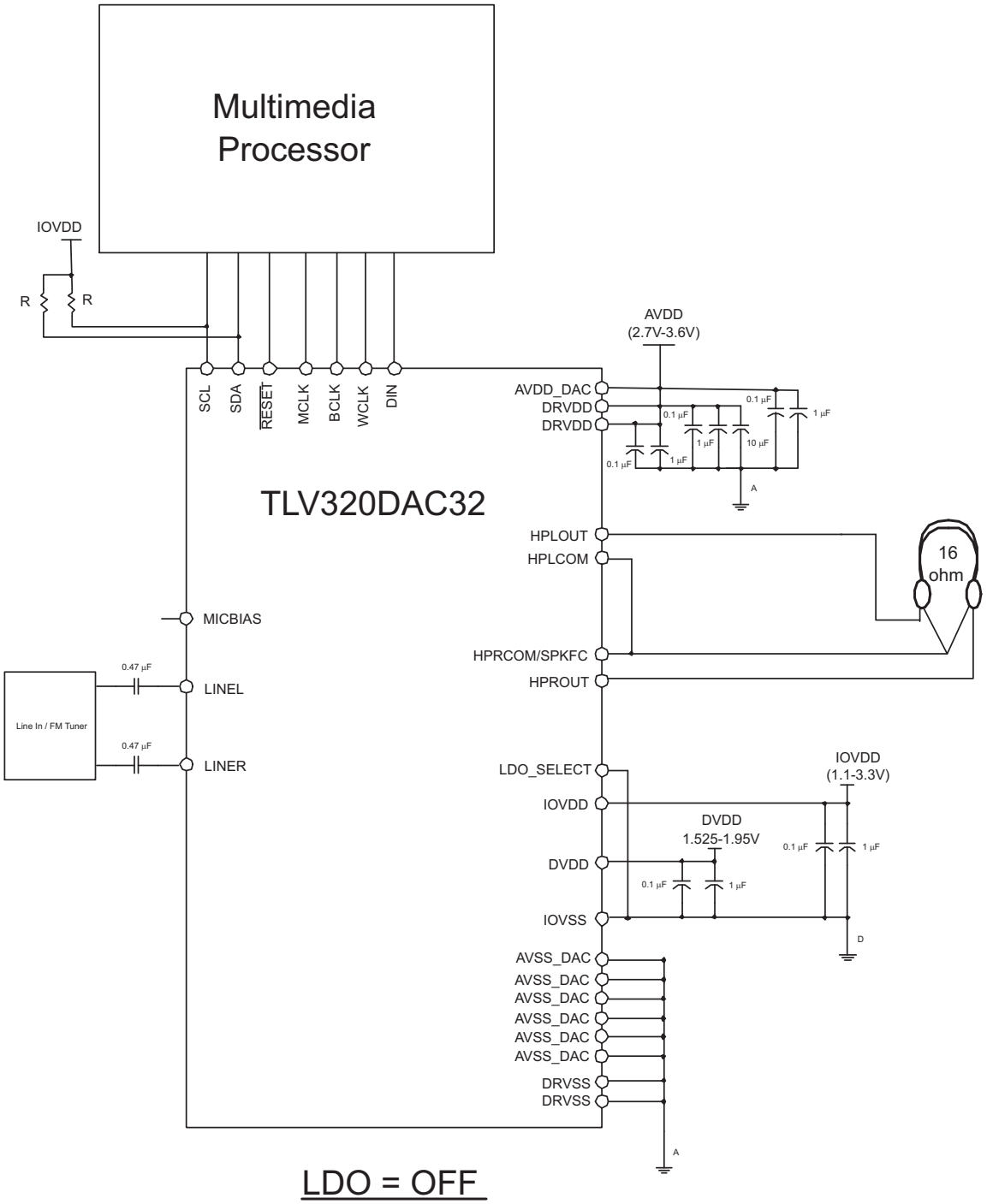


Figure 18. Capless Connection of Headphone Driver with External DVDD Supply (LDO Off)

TYPICAL CHARACTERISTICS (continued)

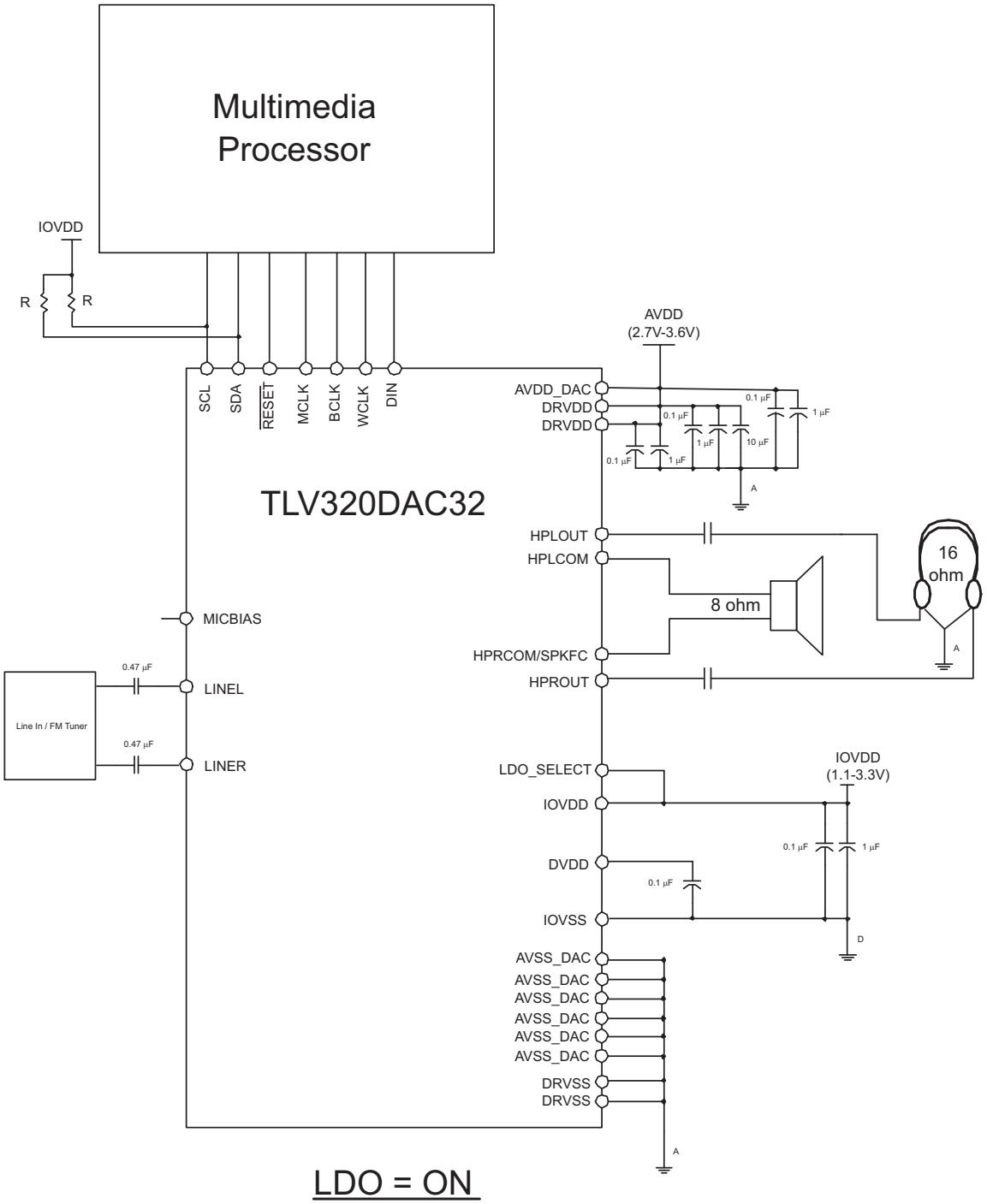


Figure 19. Internal 8-Ω Speaker Driver (Differential Mono Configuration) with Stereo Headphones Using Internal LDO

TYPICAL CHARACTERISTICS (continued)

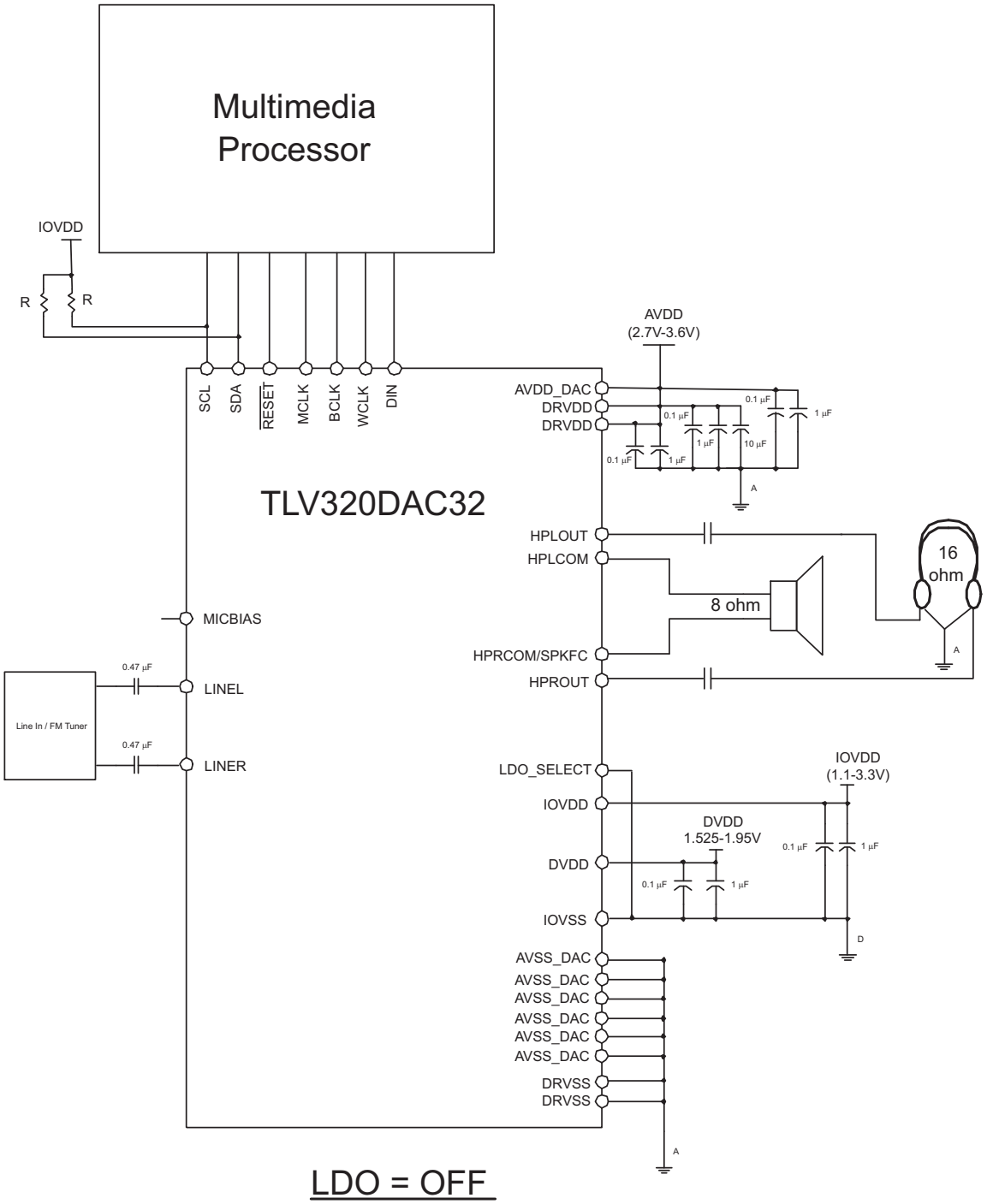


Figure 20. Internal 8-Ω Speaker Driver (Differential Mono Configuration) with Stereo Headphones with External DVDD Supply (LDO Off)

OVERVIEW

The TLV320DAC32 is a highly flexible, low power stereo audio DAC with extensive feature integration, intended for application in smartphones, PDAs, and portable computing, communication, and entertainment applications. Available in a 5x5mm 32-lead QFN, the product integrates a host of features to reduce cost, board space, and power consumption in space-constrained, battery powered portable applications.

The TLV320DAC32 consists of the following blocks:

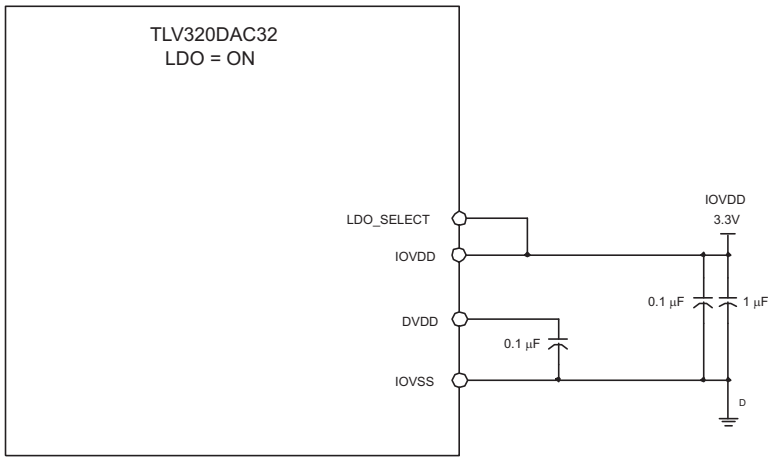
- Stereo audio multi-bit delta-sigma DAC (8 kHz – 96 kHz)
- Programmable digital audio effects processing (3-D, bass, treble, mid-range, EQ, de-emphasis)
- Two analog audio input pins
- Four high-power audio output drivers (headphone/speaker drive capability)
- Fully programmable PLL
- Programmable voltage level for microphone biasing
- Headphone/headset jack detection with interrupt
- Selectable internal LDO regulator for systems that only have +3.3V power available.

The I^2C interface supports both standard and fast communication modes.

LDO OPERATION

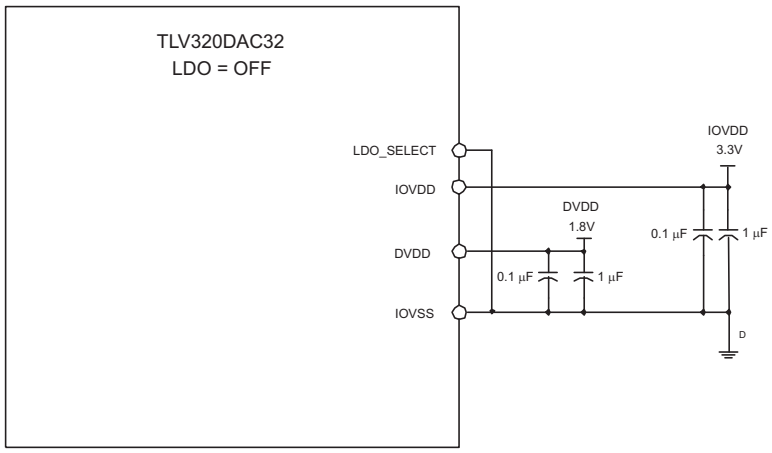
The TLV320DAC32 includes a LDO voltage regulator that can be used in systems where a 1.8V power supply is not available. In systems where the LDO is used, 3.3V power is applied to the device, and the internal LDO regulator generates the 1.8V needed to operate the internal digital core. The LDO functionality is controlled by the state of the LDO_SELECT pin (pin 5 in QFN package). To enable the LDO function, apply IOVDD to the LDO_SELECT pin. To disable the LDO function, connect the LDO_SELECT pin to ground. The correct operation of the device requires that the LDO_SELECT pin must be connected to either IOVDD or ground. When the LDO is bypassed, the DVDD pin must be connected to a 1.8V power supply.

A small value ceramic capacitor should be connected between the DVDD pin and digital ground, even when the internal LDO is used. This capacitor provides power supply decoupling for either power supply condition. See Figure 21 and Figure 22 for proper connection and use of the internal LDO.



A. See tables for voltage range of IOVDD

Figure 21. LDO Function Operating



A. See tables for voltage range of DVDD and IOVDD

Figure 22. LDO Function Bypassed, DVDD Supplied Externally

HARDWARE RESET

The TLV320DAC32 requires a hardware reset after power-up for proper operation. After all power supplies are at their specified values, the $\overline{\text{RESET}}$ pin must be driven low for at least 10 ns. If this reset sequence is not performed, the 'DAC32 may not respond properly to register reads/writes.

FLEXIBLE POWER DOWN

The TLV320DAC32 allows power down for many individual circuit blocks. This flexibility allows the user to be able to optimize functionality while minimizing power consumption for each application. The power consumption for the device by function can be seen in Table 1.

Table 1. Total Power Dissipation

FUNCTION	POWER DISSIPATION	UNITS
Headphone amplifier only	13.2	mW
DAC + headphone amplifier, (Analog Mixer bypassed) PLL = off, LDO = off	18.1	mW
DAC + headphone amplifier, PLL = off, LDO = off	20.2	mW
DAC + headphone amplifier, PLL = on, LDO = off	25.2	mW
Power down	1.23	µW

DIGITAL CONTROL SERIAL INTERFACE

The register map of the TLV320DAC32 actually consists of two pages of registers, with each page containing 128 registers. The register at address zero on each page is used as a page control register, and writing to this register determines the active page for the device. All subsequent read/write operations will access the page that is active at the time, unless a register write is performed to change the active page. Only two pages of registers are implemented in this product, with the active page defaulting to page 0 upon device reset. The Page 0 is dedicated to DAC and device functionality setup, while Page 1 is used to setup the Digital Audio Effects Processor, and for use in applying digital de-emphasis to the digital audio playback stream.

For example, at device reset, the active page defaults to page 0, and thus all register read/write operations for addresses 1 to 127 will access registers in page 0. If registers on page 1 must be accessed, the user must write the 8-bit sequence “0x01” to register 0, the page control register, to change the active page from page 0 to page 1. After this write, it is recommended the user also read back the page control register, to safely ensure the

change in page control has occurred properly. Future read/write operations to addresses 1 to 127 will now access registers in page 1. When page 0 registers must be accessed again, the user writes the 8-bit sequence “0x00” to register 0, the page control register, to change the active page back to page 0. After a recommended read of the page control register, all further read/write operations to addresses 1 to 127 will now access page 0 registers again.

It is considered to be a best practice, that when writing to PAGE 1, all five of the digital filter’s coefficients of the Bi-Quad structure be updated to the new values before resuming digital audio playback.

I²C CONTROL MODE

The TLV320DAC32 supports the I²C control protocol using 7-bit addressing and is capable of both standard and fast modes. For I²C fast mode, note that the minimum timing for each of t_{HD-STA}, t_{SU-STA}, and t_{SU-STO} is 0.9 µs, as seen in Figure 23. The TLV320DAC32 will respond to the I²C address of 0011000. I²C is a two-wire open-drain interface supporting multiple devices and masters on a single bus. Devices on the I2C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pull-up resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

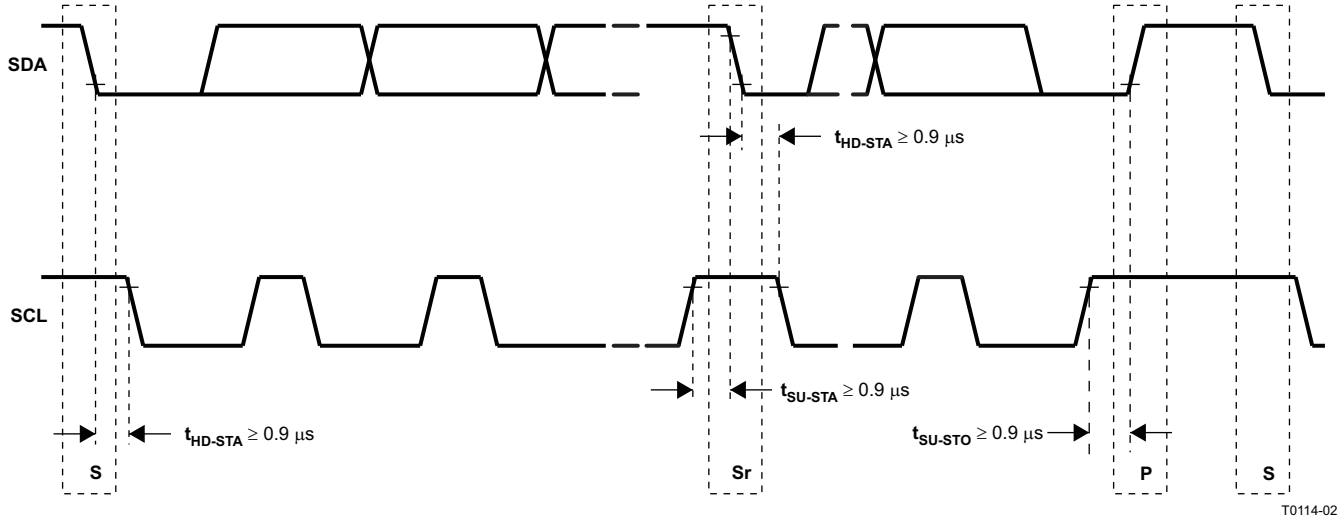


Figure 23. I²C Interface Timing

Communication on the I²C bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I2C devices can act as masters or slaves, but the TLV320DAC32 can only act as a slave device.

An I²C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data is transmitted across the I²C bus in groups of eight bits. To send a bit on the I2C bus, the SDA line is driven to the appropriate level while SCL is LOW (a LOW on SDA indicates the bit is zero; a HIGH indicates the bit is one). Once the SDA line has settled, the SCL line is brought HIGH, then LOW. This pulse on SCL clocks the SDA bit into the receiver’s shift register.

The I²C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends info to a slave, the master drives the data line. The master always drives the clock line. The TLV320DAC32 never drives SCL, because it cannot act as a master. On the TLV320DAC32, SCL is an input only.

Most of the time the bus is idle, no communication is taking place, and both lines are HIGH. When communication is taking place, the bus is active. Only master devices can start a communication. They do this by causing a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is LOW. If the data line changes state while the clock line is HIGH, it is either a START condition or its counterpart, a STOP condition. A START condition is when the clock line is HIGH and the data line goes from HIGH to LOW. A STOP condition is when the clock line is HIGH and the data line goes from LOW to HIGH.

After the master issues a START condition, it sends a byte that indicates which slave device it wants to communicate with. This byte is called the address byte. Each device on an I^2C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I2C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I^2C bus, whether it is address or data, is acknowledged with an acknowledge bit. When a master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA LOW. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA LOW to acknowledge this to the slave. It then sends a clock pulse to clock the bit. (Remember that the master always drives the clock line.)

A not-acknowledge is performed by simply leaving SDA HIGH during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not−acknowledge because no device is present at that address to pull the line LOW.

When a master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

The TLV320DAC32 also responds to and acknowledges a General Call, which consists of the master issuing a command with a slave address byte of 00H.

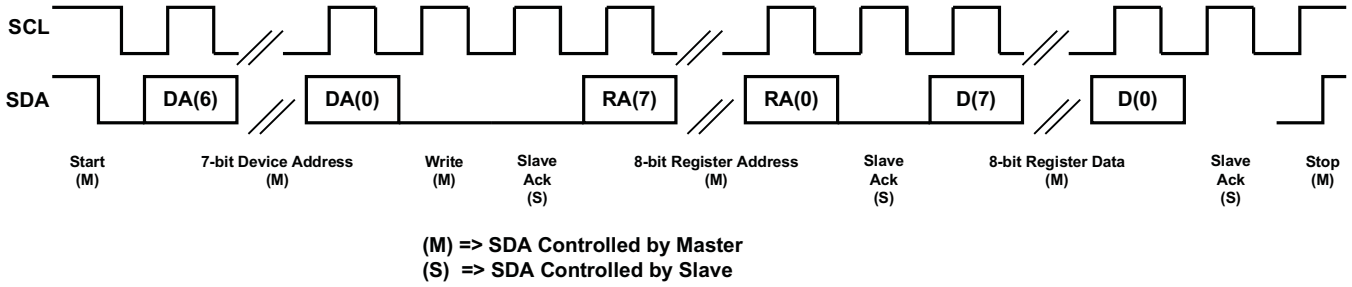


Figure 24. I^2C Write

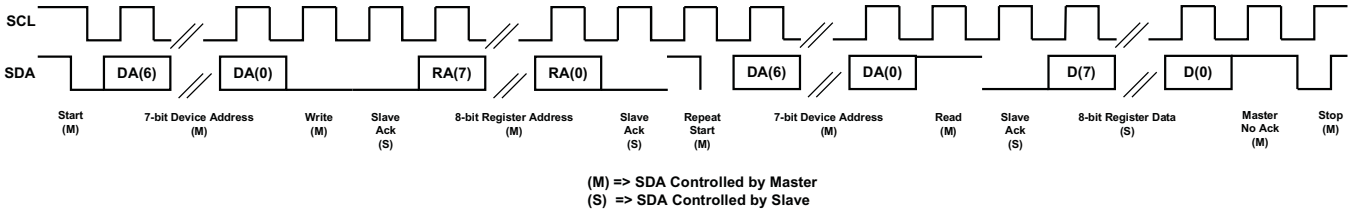


Figure 25. I^2C Read

In the case of an I2C register write, if the master does not issue a STOP condition, then the device enters auto-increment mode. So in the next eight clocks, the data on SDA will be treated as data for the next incremental register.

Similarly, in the case of an I2C register read, after the device has sent out the 8-bit data from the addressed register, if the master issues a ACKNOWLEDGE, the slave will take over control of SDA bus and transmit for the next 8 clocks the data of the next incremental register.

DIGITAL AUDIO DATA SERIAL INTERFACE

Audio data is transferred between the host processor and the TLV320DAC32 via the digital audio data serial interface, or “audio bus”. The audio bus of the TLV320DAC32 can be configured for left or right justified, I2S, DSP, or TDM modes of operation, where communication with standard telephony PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits. In addition, the word clock (WCLK) and bit clock (BCLK) can be independently configured in either master or slave mode, for flexible connectivity to a wide variety of processors.

The word clock (WCLK) is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum DAC sampling frequency selected.

The bit clock (BCLK) is used to clock in the digital audio data across the serial bus. When in master mode, this signal can be programmed in two further modes: continuous transfer mode, and 256-clock mode. In continuous transfer mode, only the minimal number of bit clocks needed to transfer the audio data are generated, so in general the number of bit clocks per frame will be two times the data width. For example, if data width is chosen as 16-bits, then 32 bit clocks will be generated per frame. If the bit clock signal in master mode will be used by a PLL in another device, it is recommended that the 16-bit or 32-bit data width selections be used. These cases result in a low jitter bit clock signal being generated, having frequencies of 32*Fs or 64*Fs. In the cases of 20-bit and 24-bit data width in master mode, the bit clocks generated in each frame will not all be of equal period, due to the device not having a clean 40*Fs or 48*Fs clock signal readily available. The average frequency of the bit clock signal is still accurate in these cases (being 40*Fs or 48*Fs), but the resulting clock signal has higher jitter than in the 16-bit and 32-bit cases and may reduce the overall DAC performance.

In 256-clock mode, a constant 256 bit clocks per frame are generated, independent of the data width chosen. By using this capability with the ability to program at what bit clock in a frame the audio data will begin, time-division multiplexing (TDM) can be accomplished, resulting in multiple DACS able to use a single audio serial data bus.

When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface will be put into a tri-state output condition.

RIGHT JUSTIFIED MODE

In right-justified mode, the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of word clock. Similarly, the LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

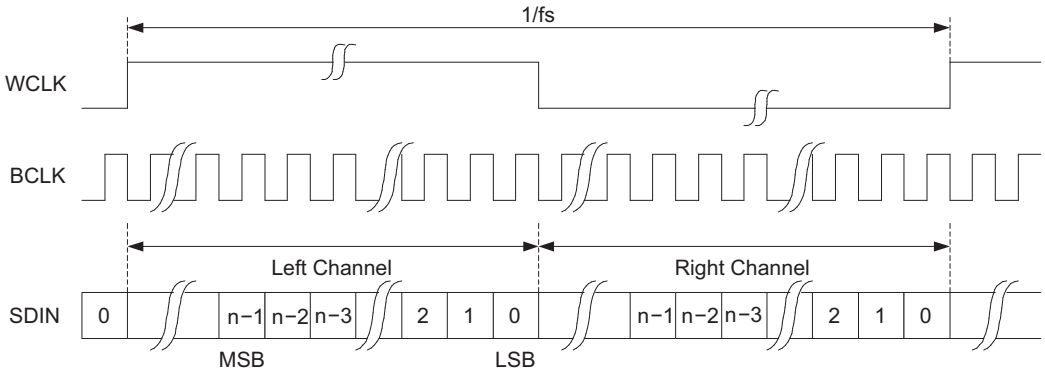


Figure 26. Right Justified Serial Bus Mode Operation

LEFT JUSTIFIED MODE

In left-justified mode, the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. Similarly the MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

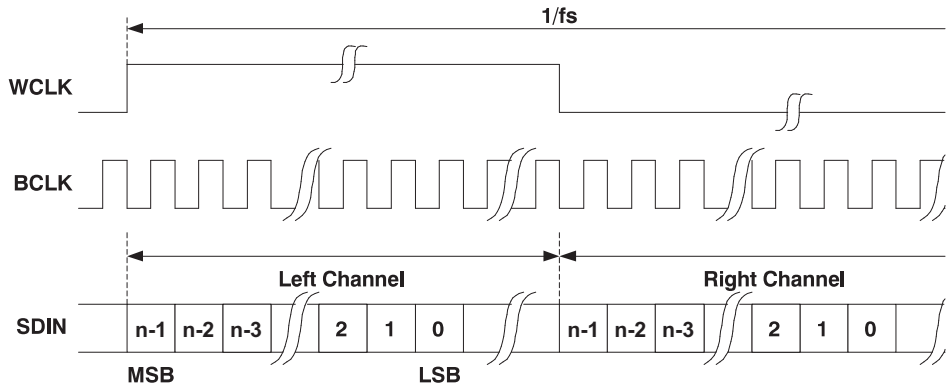


Figure 27. Left Justified Serial Data Bus Mode Operation

I²S MODE

In I2S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

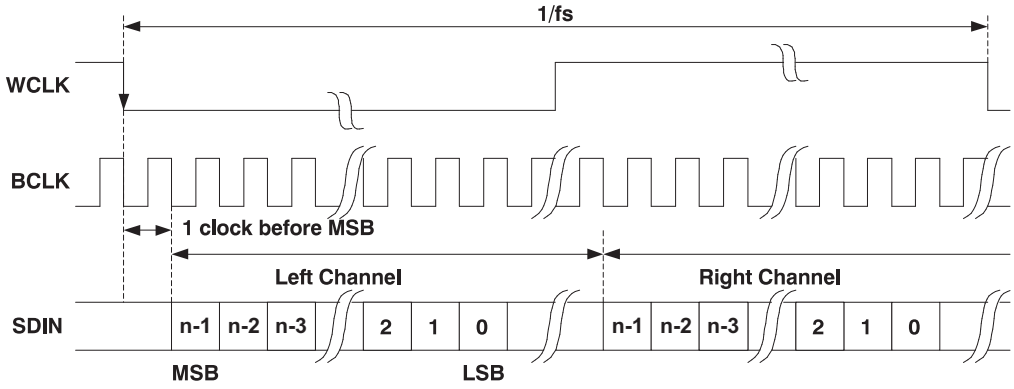


Figure 28. I²S Serial Data Bus Mode Operation

DSP MODE

In DSP mode, the rising edge of the word clock starts the data transfer with the left channel data first and immediately followed by the right channel data. Each data bit is valid on the falling edge of the bit clock.

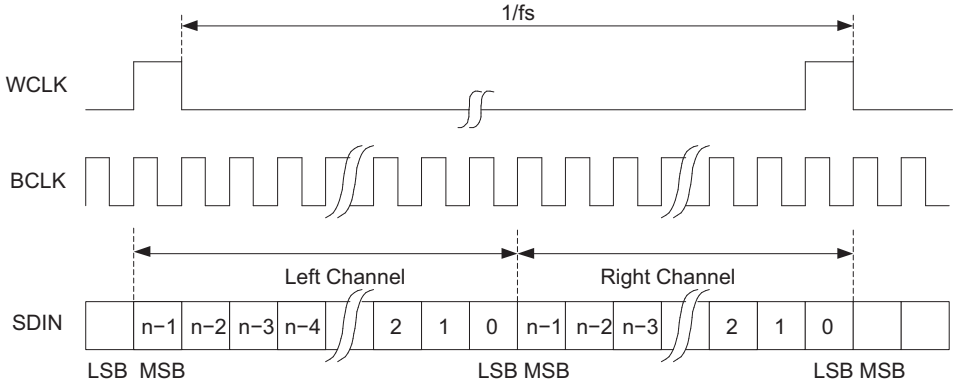


Figure 29. DSP Serial Bus Mode Operation

TDM DATA TRANSFER

Time-division multiplexed data transfer can be realized in any of the above transfer modes if the 256-clock bit clock mode is selected, although it is recommended to be used in either left-justified mode or DSP mode. By changing the programmable offset, the bit clock in each frame where the data begins can be changed. For incoming data, the dac simply ignores data on the bus except where it is expected based on the programmed offset.

Note that the location of the data when an offset is programmed is different, depending on what transfer mode is selected. In DSP mode, both left and right channels of data are transferred immediately adjacent to each other in the frame. This differs from left-justified mode, where the left and right channel data will always be a half-frame apart in each frame. In this case, as the offset is programmed from zero to some higher value, both the left and right channel data move across the frame, but still stay a full half-frame apart from each other. This is depicted in Figure 30 below for the two cases.

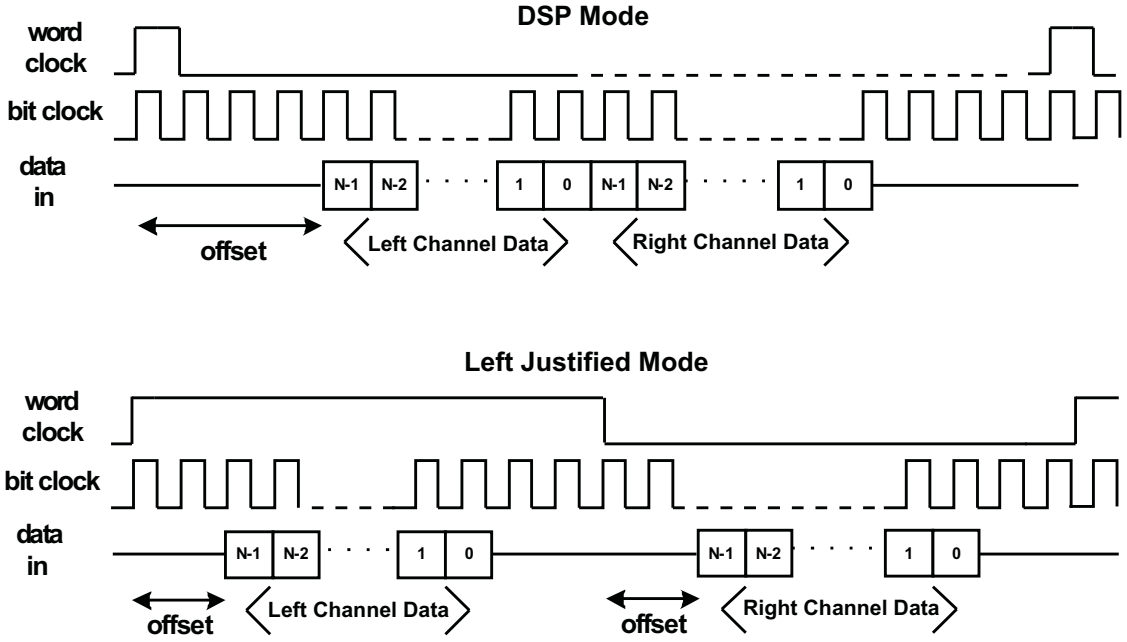


Figure 30. DSP Mode and Left Justified Modes, Showing the Effect of a Programmed Data Word Offset

AUDIO DATA CONVERTERS

The TLV320DAC32 supports the following standard audio sampling rates: 8-kHz, 11.025-kHz, 12-kHz, 16-kHz, 22.05-kHz, 24-kHz, 32-kHz, 44.1-kHz, 48-kHz, 88.2-kHz, and 96-kHz.

The data converter is based on the concept of an Fsref rate that is used internal to the part, and it is related to the actual sampling rates of the dac through a series of ratios. For typical sampling rates, Fsref will be either 44.1-kHz or 48-kHz, although it can realistically be set over a wider range of rates up to 96-kHz, with additional restrictions applying if the PLL is used. This concept is used to set the sampling rates of the DAC, and also to enable high quality playback of low sampling rate data, without high frequency audible noise being generated.

The sampling rate of the DAC can be set to Fsref/NDAC or 2*Fsref/NDAC, with NDAC being 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, or 6.

AUDIO CLOCK GENERATION

The audio dac in the TLV320DAC32 needs an internal audio master clock at a frequency of 256*Fsref, which can be obtained in a variety of manners from an external clock signal applied to the device.

A more detailed diagram of the audio clock section of the TLV320DAC32 is shown in Figure 31.

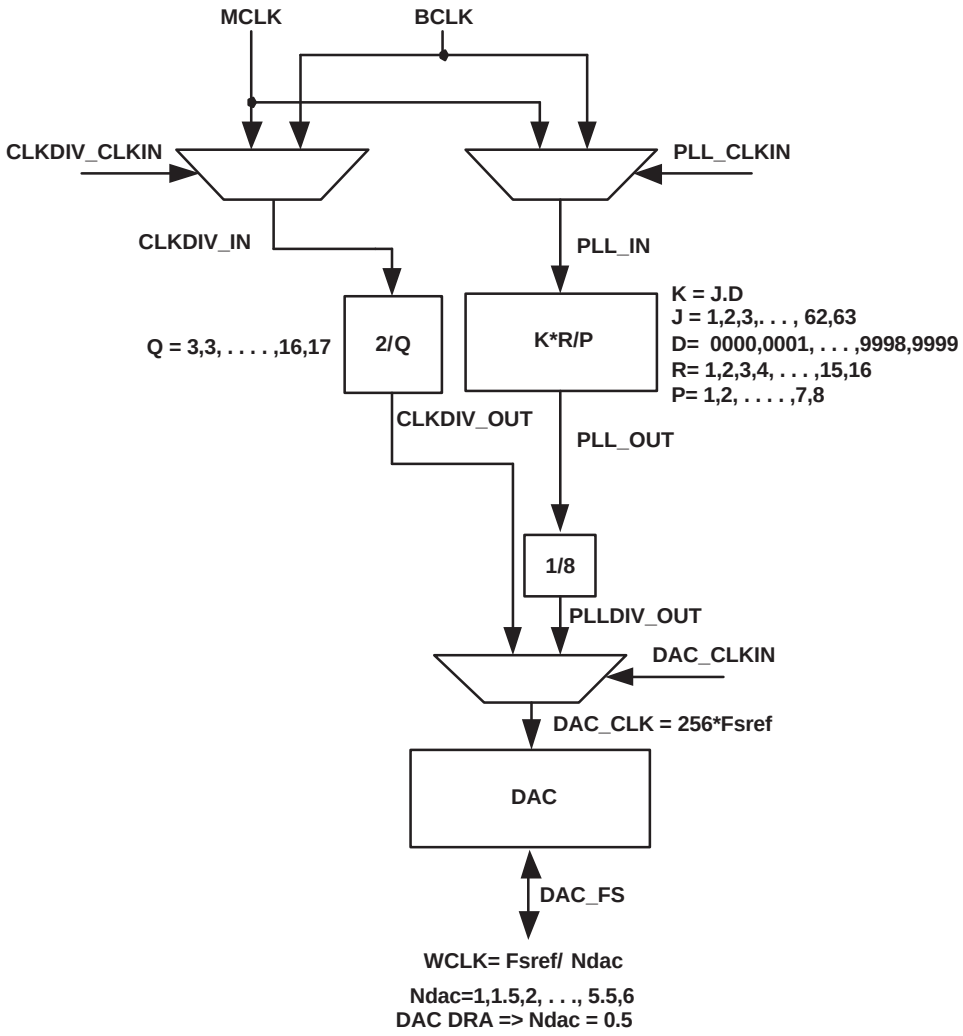


Figure 31. Audio Clock Generation Processing

The TLV320DAC32 can accept an MCLK input from 2-MHz to 50-MHz, which can then be passed through either a programmable divider or a PLL, to get the proper internal audio master clock needed by the part. Alternatively, the BCLK input can also be used to generate the internal audio master clock.

A primary concern is proper operation of the dac at various sample rates with the limited MCLK frequencies available in the application system. This device includes a highly programmable PLL to accommodate such situations easily. The integrated PLL can generate audio clocks from a wide variety of possible MCLK inputs, with particular focus paid to the standard MCLK rates already widely used.

When the PLL is disabled,

Where Q = 2, 3, …, 17

CLKDIV_IN can be MCLK or BCLK, selected by register 102, bits D7-D6.

NOTE – when NDAC = 1.5, 2.5, 3.5, 4.5, or 5.5, odd values of Q are not allowed. In this mode, MCLK can be as high as 50 MHz, and Fsref should fall within 39 kHz to 53 kHz.

When the PLL is enabled,

Fsref = (PLLCLK_IN ɹK ɹR) / (2048 ɹP), where

P = 1, 2, 3,…, 8

R = 1, 2, …, 16

K = J.D

J = 1, 2, 3, …, 63
D = 0000, 0001, 0002, 0003, …, 9998, 9999
PLLCLK_IN can be MCLK or BCLK, selected by Page 0, register 102, bits D5-D4

P, R, J, and D are register programmable. J is the integer portion of K (the numbers to the left of the decimal point), while D is the fractional portion of K (the numbers to the right of the decimal point, assuming four digits of precision).

Examples:

If K = 8.5, then J = 8, D = 5000
If K = 7.12, then J = 7, D = 1200
If K = 14.03, then J = 14, D = 0300
If K = 6.0004, then J = 6, D = 0004

When the PLL is enabled and D = 0000, the following conditions must be satisfied to meet specified performance:

2 MHz ≤ (PLLCLK_IN / P) ≤ 20 MHz
80 MHz ≤ (PLLCLK _IN ɹK ɹR / P) ≤ 110 MHz
4 ≤ J ≤ 55

When the PLL is enabled and D≠0000, the following conditions must be satisfied to meet specified performance:

10 MHz ≤ PLLCLK _IN / P ≤ 20 MHz
80 MHz ≤ PLLCLK _IN ɹK ɹR / P ≤ 110 MHz
4 ≤ J ≤ 11
R = 1

Example:

MCLK = 12 MHz and Fsref = 44.1 kHz
Select P = 1, R = 1, K = 7.5264, which results in J = 7, D = 5264

Example:

MCLK = 12 MHz and Fsref = 48.0 kHz
Select P = 1, R = 1, K = 8.192, which results in J = 8, D = 1920

The table below lists several example cases of typical MCLK rates and how to program the PLL to achieve Fsref = 44.1 kHz or 48 kHz.

Fsref = 44.1 kHz						
MCLK (MHz)	**P**	**R**	**J**	**D**	**ACHIEVED FSREF**	**% ERROR**
2.8224	1	1	32	0	44100.00	0.0000
5.6448	1	1	16	0	44100.00	0.0000
12.0	1	1	7	5264	44100.00	0.0000
13.0	1	1	6	9474	44099.71	0.0007
16.0	1	1	5	6448	44100.00	0.0000
19.2	1	1	4	7040	44100.00	0.0000
19.68	1	1	4	5893	44100.30	–0.0007
48.0	4	1	7	5264	44100.00	0.0000
Fsref = 48 kHz						
MCLK (MHz)	**P**	**R**	**J**	**D**	**ACHIEVED FSREF**	**% ERROR**
2.048	1	1	48	0	48000.00	0.0000
3.072	1	1	32	0	48000.00	0.0000
4.096	1	1	24	0	48000.00	0.0000
6.144	1	1	16	0	48000.00	0.0000
8.192	1	1	12	0	48000.00	0.0000
12.0	1	1	8	1920	48000.00	0.0000
13.0	1	1	7	5618	47999.71	0.0006

16.0	1	1	6	1440	48000.00	0.0000
19.2	1	1	5	1200	48000.00	0.0000
19.68	1	1	4	9951	47999.79	0.0004
48.0	4	1	8	1920	48000.00	0.0000

STEREO AUDIO DAC

The TLV320DAC32 includes a stereo audio DAC supporting sampling rates from 8-kHz to 96-kHz. Each channel of the stereo audio DAC consists of a digital audio processing block, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20-kHz. This is realized by keeping the upsampled rate constant at 128 x Fsref and changing the oversampling ratio as the input sample rate is changed. For an Fsref of 48-kHz, the digital delta-sigma modulator always operates at a rate of 6.144-MHz. This ensures that quantization noise generated within the delta-sigma modulator stays low within the frequency band below 20-kHz at all sample rates. Similarly, for an Fsref rate of 44.1-kHz, the digital delta-sigma modulator always operates at a rate of 5.6448-MHz.

The following restrictions apply in the case when the PLL is powered down and double-rate audio mode is enabled in the DAC.

Allowed Q values = 4, 8, 9, 12, 16

Q values where equivalent Fsref can be achieved by turning on PLL

Q = 5, 6, 7 (set P = 5 / 6 / 7 and K = 16.0 and PLL enabled)

Q = 10, 14 (set P = 5, 7 and K = 8.0 and PLL enabled)

DIGITAL AUDIO PROCESSING

The DAC channel consists of optional filters for de-emphasis and bass, treble, midrange level adjustment, speaker equalization, and 3-D effects processing. The de-emphasis function is implemented by a programmable digital filter block with fully programmable coefficients (see Page-1/Reg-21-26 for left channel, Page-1/Reg-47-52 for right channel). If de-emphasis is not required in a particular application, this programmable filter block can be used for some other purpose. The de-emphasis filter transfer function is given by:

$$H(z) = \frac{N0 + N1 \times z^{-1}}{32768 - D1 \times z^{-1}} \quad (1)$$

where the N0, N1, and D1 coefficients are fully programmable individually for each channel. The coefficients that should be loaded to implement standard de-emphasis filters are given in Table 1.

Table 2. De-Emphasis Coefficients for Common Audio Sampling Rates

SAMPLING FREQUENCY	N0	N1	D1
32-kHz	16950	–1220	17037
44.1-kHz	15091	–2877	20555
48-kHz(1)	14677	–3283	21374

(1) The 48-kHz coefficients listed above are used as the default values.

In addition to the de-emphasis filter block, the DAC digital effects processing includes a fourth order digital IIR filter with programmable coefficients (one set per channel). This filter is implemented as cascade of two biquad sections with frequency response given by:

$$\left(\frac{N0 + 2 \times N1 \times z^{-1} + N2 \times z^{-2}}{32768 - 2 \times D1 \times z^{-1} - D2 \times z^{-2}}\right)\left(\frac{N3 + 2 \times N4 \times z^{-1} + N5 \times z^{-2}}{32768 - 2 \times D4 \times z^{-1} - D5 \times z^{-2}}\right) \quad (2)$$

The N and D coefficients are fully programmable, and the entire filter can be enabled or bypassed. The structure of the filtering when configured for independent channel processing is shown below in Figure 32, with LB1 corresponding to the first left-channel biquad filter using coefficients N0, N1, N2, D1, and D2. LB2 similarly corresponds to the second left-channel biquad filter using coefficients N3, N4, N5, D4, and D5. The RB1 and RB2 filters refer to the first and second right-channel biquad filters, respectively.

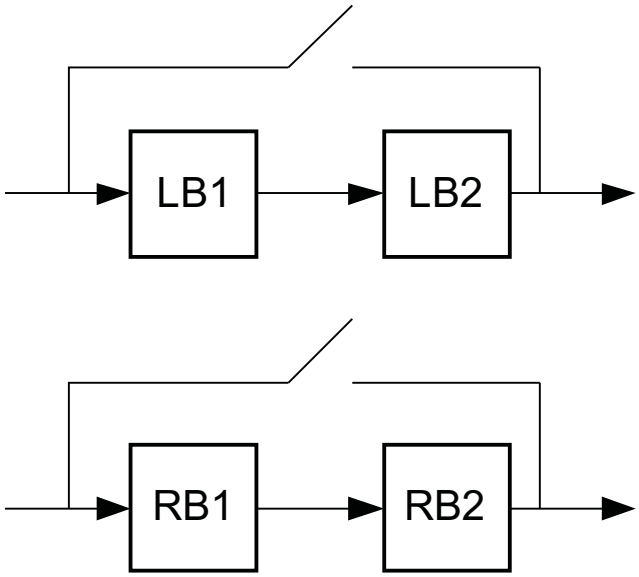


Figure 32. Structure of the Digital Effects Processing for Independent Channel Processing

The coefficients for this filter implement a variety of sound effects, with bass-boost or treble boost being the most commonly used in portable audio applications. The default N and D coefficients in the part are given in Table 2 and implement a shelving filter with 0-dB gain from DC to approximately 150-Hz, at which point it rolls off to a 3-dB attenuation for higher frequency signals, thus giving a 3-dB boost to signals below 150-Hz. The N and D coefficients are represented by 16-bit two's complement numbers with values ranging from -32768 to +32767.

Table 3. Default Digital Effects Processing Filter Coefficients, When in Independent Channel Processing Configuration

Coefficients				
N0 = N3	**D1 = D4**	**N1 = N4**	**D2 = D5**	**N2 = N5**
27619	32131	–27034	–31506	26461

The digital processing also includes capability to implement 3-D processing algorithms by providing means to process the mono mix of the stereo input, and then combine this with the individual channel signals for stereo output playback. The architecture of this processing mode, and the programmable filters available for use in the system, is shown in Figure 33. Note that the programmable attenuation block provides a method of adjusting the level of 3-D effect introduced into the final stereo output. This combined with the fully programmable biquad filters in the system enables the user to fully optimize the audio effects for a particular system and provide extensive differentiation from other systems using the same device.

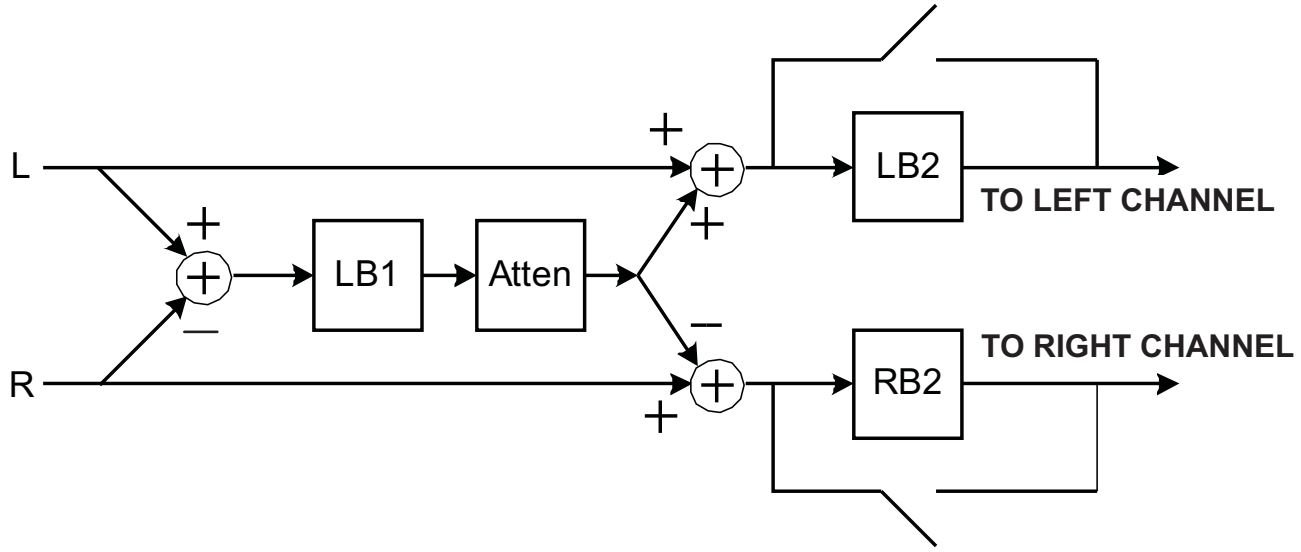


Figure 33. Architecture of the Digital Audio Processing When 3-D Effects are Enabled

It is recommended that the digital effects filters should be disabled while the filter coefficients are being modified. Since updating all 5 digital coefficients using the I2C control port can take more than 1 LRCLK cycle, it is therefore possible that a filter using partially updated coefficients may actually implement an unstable filter and lead to an oscillation or objectionable audio output. By first disabling the filters, then changing the all of the coefficients as needed, and then re-enabling the filters, these types of effects can be entirely avoided.

DIGITAL INTERPOLATION FILTER

The digital interpolation filter upsamples the output of the digital audio processing block by the required oversampling ratio before data is provided to the digital delta-sigma modulator and analog reconstruction filter stages. The filter provides a linear phase output with a group delay of 21/Fs. In addition, programmable digital interpolation filtering is included to provide enhanced image filtering and reduce signal images caused by the upsampling process that are below 20-kHz. For example, upsampling an 8-kHz signal produces signal images at multiples of 8-kHz (i.e., 8-kHz, 16-kHz, 24-kHz, etc). The images at 8-kHz and 16-kHz are below 20-kHz and still audible to the listener; therefore, they must be filtered heavily to maintain a good quality output. The interpolation filter in this device is designed to maintain at least 65-dB rejection of images that land below 7.455 Fs. In order to utilize the programmable interpolation capability, the Fsref should be programmed to a higher rate (restricted to be in the range of 39-kHz to 53-kHz when the PLL is in use), and the actual Fs is set using the NDAC divider. For example, if Fs = 8-kHz is required, then Fsref can be set to 48-kHz, and the DAC Fs set to Fsref/6. This ensures that all images of the 8-kHz data are sufficiently attenuated well beyond a 20-kHz audible frequency range.

DELTA-SIGMA AUDIO DAC

The stereo audio DAC incorporates a third order multi-bit delta-sigma modulator followed by an analog reconstruction filter. The DAC provides high-resolution, low-noise performance, using oversampling and noise shaping techniques. The analog reconstruction filter design consists of a 6 tap analog FIR filter followed by a continuous time RC filter. The analog FIR operates at a rate of 128 x Fsref (6.144 MHz when Fsref = 48-kHz, 5.6448-MHz when Fsref = 44.1-kHz). Note that the DAC analog performance may be degraded by excessive clock jitter on the MCLK input. Therefore, care must be taken in the system design to keep jitter on this clock to a minimum.

AUDIO DAC DIGITAL VOLUME CONTROL

The audio DAC includes a digital volume control block which implements a programmable digital gain. The volume level can be varied from 0-dB to –63.5-dB in 0.5-dB steps, in addition to a mute bit, independently for each channel. The volume level of both channels can also be changed simultaneously by the master volume control. Gain changes are implemented with a soft-stepping algorithm, which only changes the actual volume by a maximum of one step per input sample, either up or down, until the desired volume level is reached. The rate of soft-stepping can be further slowed to one step per two input samples through a register bit.

Because of soft-stepping, the host does not know the exact time that the DAC has been actually muted. This may be important if the host wishes to mute the DAC before making a significant change, such as changing sample rates. In order to help with this situation, the device provides a flag back to the host via a read-only register bit that alerts the host when the part has completed the soft-stepping and the actual volume has reached the desired volume level. These flags can be found at register locations: Page0/Reg-51/D1, Page0/Reg-58/D1, Page0/Reg-65/D1, Page0/Reg-72/D1. The soft-stepping feature can be disabled through register programming. If soft-stepping is enabled, the MCLK signal should be kept applied to the device until the DAC power-down flag is set. When this flag is set, the internal soft-stepping process and power down sequence is complete, and the MCLK can then be stopped if desired.

The TLV320DAC32 also includes functionality to detect when the user switches on or off the de-emphasis or digital audio processing functions. It is recommended to first (1) soft-mute the DAC volume control, (2) change the operation of the digital effects processing by downloading the new filter coefficients to the appropriate registers, and then (3) soft-unmute the device. This avoids any possible pop/clicks in the audio output due to instantaneous changes in the filtering. A similar algorithm should be used when first powering up or down the DAC. The system should begin operation at power up with the volume control muted, then soft-steps the volume up to the desired volume level. At power down, the logic first soft-steps the volume down to the mute level, and then powers down the circuitry.

AUDIO DAC COMMON-MODE ADJUSTMENT

The output common-mode voltage and output range of the audio DAC are determined by an internal bandgap reference, in contrast to other DACS that may use a resistor-divider version of the supply. This voltage reference scheme is used to reduce the coupling of power supply noise (such as 217-Hz noise in a GSM cellphone) into the audio signal path.

However, due to the possible wide variation in analog supply range (2.7V – 3.6V), an output common-mode voltage setting of 1.35V, which would be used for a 2.7V supply case, will be overly conservative if the supply is actually much larger, such as 3.3V or 3.6V. In order to optimize device operation, the TLV320DAC32 includes a programmable output common-mode level, which can be set by register programming to a level most appropriate to the actual supply range used by a particular application. The output common-mode level can be varied among four different values, ranging from 1.35V (most appropriate for low supply ranges, near 2.7V) to 1.8V (most appropriate for high supply ranges, near 3.6V). Note that there is also some limitation on the range of DVDD voltage as well in determining which setting is most appropriate .

Table 4. Appropriate Settings

CM SETTING	RECOMMENDED AVDD_DAC, DRVDD	RECOMMENDED DVDD
1.35	2.7 V – 3.6 V	1.525 V – 1.95 V
1.50	3.0 V – 3.6 V	1.65 V – 1.95 V
1.65 V	3.3 V – 3.6 V	1.8 V – 1.95 V
1.8 V	3.6 V	1.95 V

AUDIO DAC POWER CONTROL

The stereo DAC can be fully powered up or down, and in addition, the analog circuitry in each individual DAC channel can be powered up or down independently. This provides power savings when only a mono playback stream is needed.

AUDIO ANALOG INPUTS

The TLV320DAC32 includes two single-ended audio inputs that are sent to an output mixer with volume control capability. By configuring the mixer to accept multiple inputs, an analog mixing function occurs. Mixing of multiple mixer inputs can easily lead to outputs that exceed the range of the internal opamps, thereby resulting in saturation and clipping of the mixed output signal. Note that whenever mixing is being implemented, the user should take adequate precautions to avoid such a saturation case from occurring. In general, the analog mixed signal should not exceed 2Vp-p (single-ended).

In most mixing applications, there is also a general need to adjust the levels of the individual signals being mixed. For example, if a soft signal and a large signal are to be mixed and played together, the soft signal generally should be amplified to a level comparable to the large signal before mixing. In order to accommodate this need, the TLV320DAC32 includes input volume control on each of the individual inputs before they are mixed, with gain programmable from 0dB to -78dB in 0.5dB steps. Soft-stepping of the input level control settings is implemented in this device, with the speed and functionality following the settings used by the DAC.

ANALOG INPUT BYPASS PATH FUNCTIONALITY

The TLV320DAC32 includes the additional ability to route two analog input signals around the DAC and then connect to the output drivers. This capability is useful in a cellphone, for example, when a separate FM radio device provides a stereo analog output signal that needs to be routed to headphones. The TLV320DAC32 supports this in a low power mode by providing a direct analog path through the device to the output drivers, while the DACS can be completely powered down to save power. When programmed correctly, the device can connect the analog input signals LINEL and LINER through the volume control which is connected to the output stage.

MICBIAS GENERATION

The TLV320DAC32 includes a programmable microphone bias output voltage (MICBIAS), capable of providing output voltages of 2.0V or 2.5V (both derived from the on-chip bandgap voltage) with 4mA output current drive. In addition, the MICBIAS may be programmed to be switched to AVDD_DAC directly through an on-chip switch, or it can be powered down completely when not needed, for power savings. This function is controlled by register programming in Page-0/Reg-25.

ANALOG HIGH POWER OUTPUT DRIVERS

The TLV320DAC32 includes four high power output drivers with extensive flexibility in their usage. These output drivers are individually capable of driving 40mW each into a 16-Ω load in single-ended configuration, and they can be used in pairs to drive up to 325mW into an 8-Ω load connected in bridge-terminated load (BTL) configuration between two driver outputs.

The high power output drivers can be configured in a variety of ways, including:

- driving up to two fully differential output signals
- driving up to four single-ended output signals
- driving two single-ended output signals, with one or two of the remaining drivers driving a fixed VCM level, for a pseudo-differential stereo output
- driving one or two 8-Ω speakers connected BTL between pairs of driver output pins
- driving stereo headphones in single-ended configuration with two drivers, while the remaining two drivers are connected in BTL configuration to an 8-Ω speaker

The output stage architecture with the volume control and mixing blocks leading to the high power output drivers is shown in Figure 34. Note that each of these drivers have a output level control which allows gain adjustments up to +9dB on the output signal. Note that this output level adjustment is not intended to be used as a standard volume control, but instead is included for additional full-scale output signal level control.

The output drivers, HPROUT and HPLOUT, include a direct connection path (L/R DAC_Direct) between the stereo DAC outputs and the output drivers. This pathway allows bypassing of the analog volume controls and the mixing networks. This functionality provides the highest quality DAC playback performance while reducing power dissipation, but this mode can only be utilized if the DAC output does not need to be mixed with the external analog input signals.

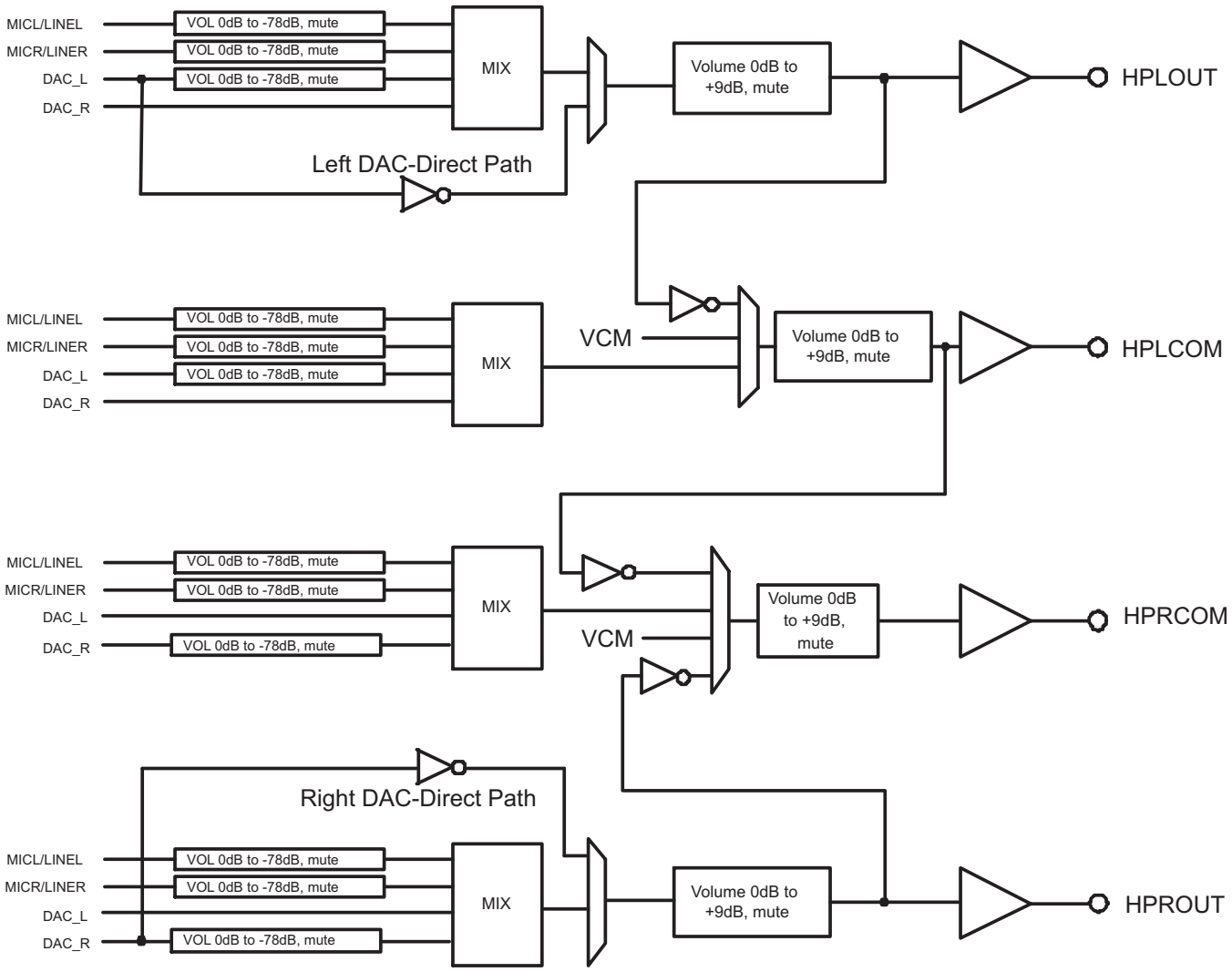


Figure 34. Architecture of the output stage leading to the high power output drivers

The high power output drivers include additional circuitry to avoid artifacts on the audio output during power-on and power-off transient conditions. The user should first program the type of output configuration being used in Page-0/Reg-14, to allow the device to select the optimal power-up scheme to avoid output artifacts. The power-up delay time for the high power output drivers is also programmable over a wide range of time delays, from instantaneous up to 4-sec, using Page-0/Reg-42.

When these output drivers are powered down, they can be placed into a variety of output conditions based on register programming. If lowest power operation is desired, then the outputs can be placed into a tri-state condition, and all power to the output stage is removed. However, this generally results in the output nodes drifting to rest near the upper or lower analog supply voltage, due to small leakage currents at the pins. This then results in a longer delay requirement to avoid output artifacts (pops and clicks) during driver power-on. In order to reduce this required power-on delay, the TLV320DAC32 includes an option for the output pins of the drivers to be weakly driven to the VCM level they would normally rest at when powered with no signal applied. This output VCM level is determined by an internal bandgap voltage reference, and thus results in extra power dissipation when the drivers are in power down. However, this option provides the fastest method for transitioning the drivers from power down to full power operation without any output artifact introduced.

The device includes a further option that falls between the other two – while it requires less power drawn while the output drivers are in power down, it also takes a slightly longer delay to power-up without artifact than if the bandgap reference is kept powered up. In this alternate mode, the powered-down output driver pin is weakly driven to a voltage of approximately half the DRVDD1/2 supply level using an internal voltage divider. This voltage will not match the actual VCM of a fully powered driver, but due to the output voltage being close to its final value, a much shorter power-up delay time setting can be used and still avoid any audible output artifacts. These output voltage options are controlled in Page-0/Reg-42.

The high power output drivers can also be programmed at power up with the output level control in a highly attenuated state, and when UN-Muted, the output driver will automatically slowly increase the gain to reach the desired output level setting that was programmed prior to the Un-Mute setting. This capability is disabled by default setting but can be enabled in Page-0/Reg-40.

SHORT CIRCUIT OUTPUT PROTECTION

The TLV320DAC32 includes programmable short-circuit protection for the high power output drivers, for maximum flexibility in a given application. By default, if these output drivers are shorted, they will automatically limit the maximum amount of current that can be sourced to or sunk from a load, thereby protecting the device from an over-current condition. In this mode, the user can read Page-0/Reg-95 to determine whether the part is in short-circuit protection or not, and then decide whether to program the device to power down the output drivers. However, the device includes further capability to automatically power down an output driver whenever it does enter into short-circuit protection, without requiring intervention from the user. In this case, the output driver will stay in a power down condition until the user specifically programs it to power down and then power back up again, to clear the short-circuit flag.

JACK / HEADSET DETECTION

The TLV320DAC32 includes extensive capability to monitor a headphone, microphone, or headset jack, determine if a plug has been inserted into the jack, and then determine what type of headset/headphone is wired to the plug. Figure 35 shows one configuration of the device that enables detection and determination of headset type when a pseudo-differential (capless) stereo headphone output configuration is used. The registers used for this function are Page-0/Reg 14, 37, 38, and 13. The type of headset detected can be read back from Page-0/Reg-13. Note that for best results, it is recommended to select a MICBIAS value as high as possible, and to program the output driver common-mode level at a 1.35V or 1.5V level.

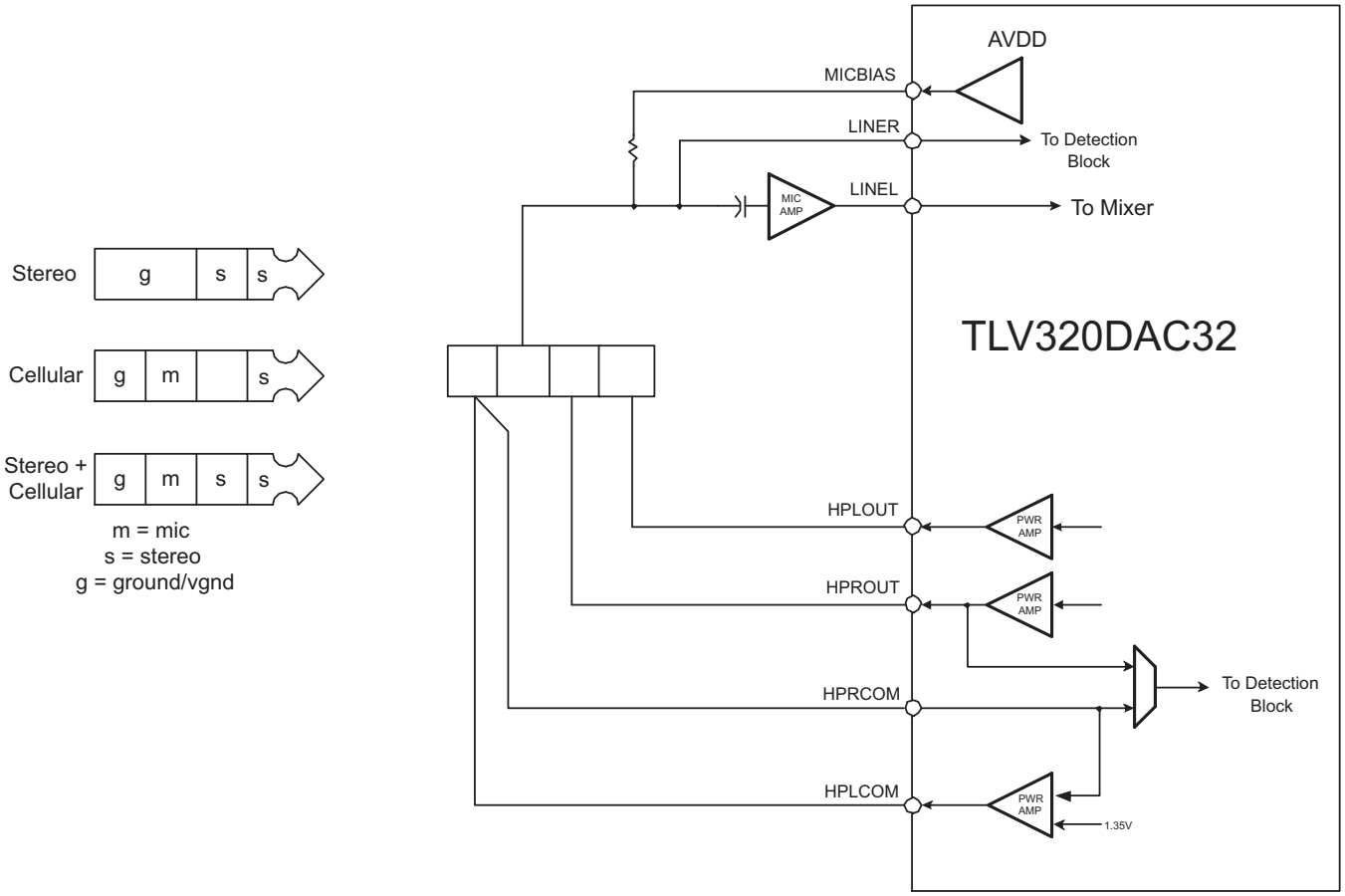


Figure 35. Configuration of device for jack detection using a pseudo-differential (capless) headphone output connection.

A modified output configuration used when the output drivers are ac-coupled is shown in Figure 36. Note that in this mode, the device cannot accurately determine the type of headset inserted if a mono or stereo headphone.

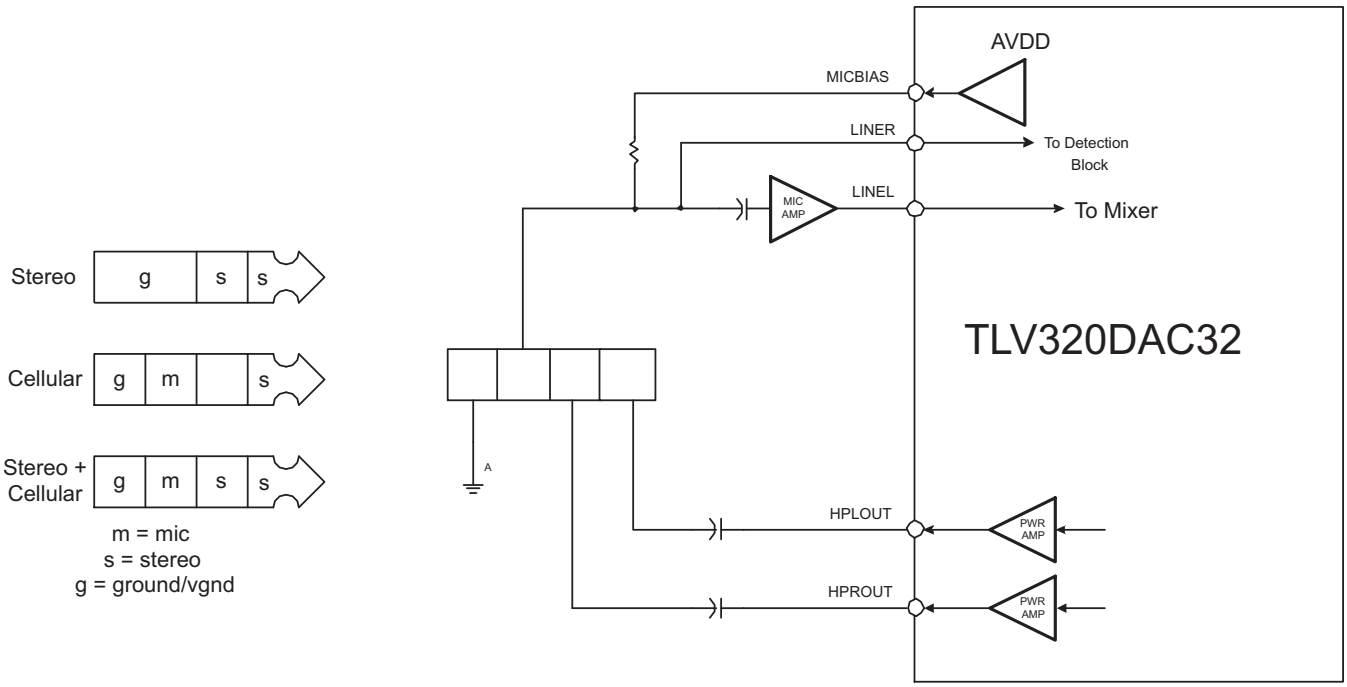


Figure 36. Configuration of device for jack detection using an ac-coupled stereo headphone output connection.

An output configuration for the case of the outputs driving fully differential stereo headphones is shown in Figure 37. In this mode there is a requirement on the jack side that either HPLCOM or HPLOUT get shorted to ground if the plug is removed, which can be implemented using a spring terminal in a jack. For this mode to function properly, short-circuit detection should be enabled and configured to power-down the drivers if a short-circuit is detected. The registers that control this functionality are in Page-0/Reg-38/Bit-D2-D1.

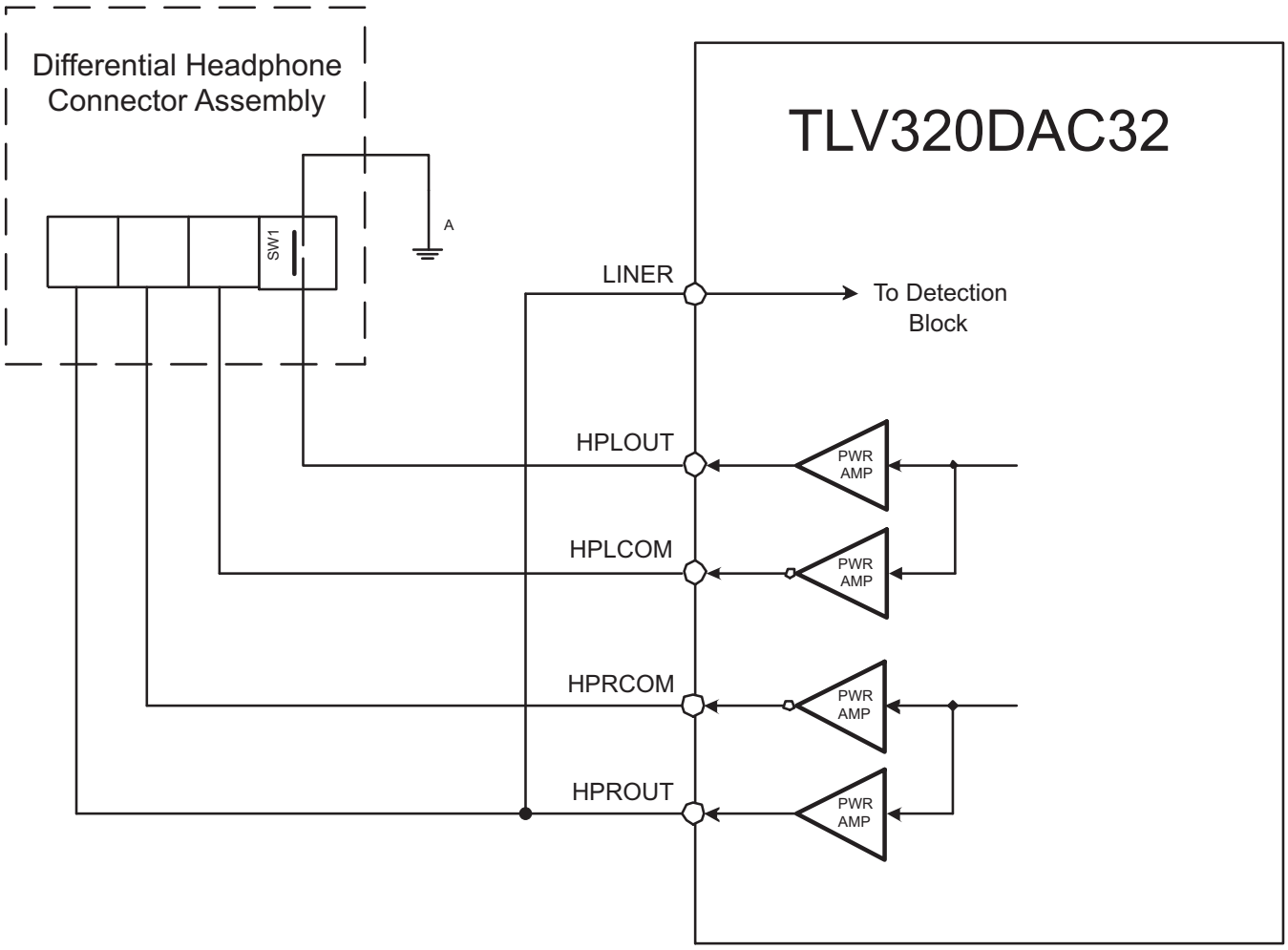


Figure 37. Configuration of device for jack detection using a fully differential stereo headphone output connection.

CONTROL REGISTERS

The control registers for the TLV320DAC32 are described in detail below. All registers are 8-bit in width, with D7 referring to the most significant bit of each register, and D0 referring to the least significant bit.

Page 0 / Register 0: Page Select Register

BIT(1)	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	X	0000000	Reserved, write only zeros to these register bits
D0	R/W	0	Page Select Bit Writing zero to this bit sets Page-0 as the active page for following register accesses. Writing a one to this bit sets Page-1 as the active page for following register accesses. It is recommended that the user read this register bit back after each write, to ensure that the proper page is being accessed for future register read/writes.

(1) When resetting registers related to routing and volume controls of output drivers, it is recommended to reset them by writing directly to the registers instead of using software reset.

Page 0 / Register 1: Software Reset Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	W	0	Software Reset Bit 0 : Don't Care 1 : Self clearing software reset
D6–D0	W	0000000	Reserved. Do not write to these bits.

Page 0 / Register 2: DAC Sample Rate Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	Reserved. Do not write to these bits.
D3-D0	R/W	0000	DAC Sample Rate Select 0000 : DAC Fs = Fsref/1 0001 : DAC Fs = Fsref/1.5 0010 : DAC Fs = Fsref/2 0011 : DAC Fs = Fsref/2.5 0100 : DAC Fs = Fsref/3 0101 : DAC Fs = Fsref/3.5 0110 : DAC Fs = Fsref/4 0111 : DAC Fs = Fsref/4.5 1000 : DAC Fs = Fsref/5 1001: DAC Fs = Fsref/5.5 1010: DAC Fs = Fsref / 6 1011–1111 : Reserved, do not write these sequences.

Page 0 / Register 3: PLL Programming Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PLL Control Bit 0: PLL is disabled 1: PLL is enabled
D6–D3	R/W	0010	PLL Q Value 0000: Q = 16 0001 : Q = 17 0010 : Q = 2 0011 : Q = 3 0100 : Q = 4 … 1110: Q = 14 1111: Q = 15
D2–D0	R/W	000	PLL P Value 000: P = 8 001: P = 1 010: P = 2 011: P = 3 100: P = 4 101: P = 5 110: P = 6 111: P = 7

Page 0 / Register 4: PLL Programming Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R/W	000001	PLL J Value 000000: Reserved, do not write this sequence 000001: J = 1 000010: J = 2 000011: J = 3 … 111110: J = 62 111111: J = 63
D1–D0	R/W	00	Reserved, write only zeros to these bits

Table 1. Page 0 / Register 5: PLL Programming Register C(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00000000	PLL D(13:6) – Eight most significant bits of a 14-bit unsigned integer valid values for D are from zero to 9999, represented by a 14-bit integer located in Page-0/Reg-5-6. Values should not be written into these registers that would result in a D value outside the valid range.

(1) When programming PLL D value, register 5 should always be written first, immediately followed by register 6. Even if only the MSB or LSB of the value changes, both registers should be written.

Page 0 / Register 6: PLL Programming Register D

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R/W	00000000	PLL D(5:0) – Six least significant bits of a 14-bit unsigned integer valid values for D are from zero to 9999, represented by a 14-bit integer located in Page-0/Reg-5-6. Values should not be written into these registers that would result in a D value outside the valid range.
D1-D0	R	00	Reserved. Do not write to these bits.

Page 0 / Register 7: DAC Datapath Setup Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Fsref setting 0: Fsref = 48-kHz 1: Fsref = 44.1-kHz
D6	R/W	0	Reserved. Only write zero to this bit.
D5	R/W	0	DAC Dual Rate Control 0: DAC dual rate mode is disabled 1: DAC dual rate mode is enabled
D4–D3	R/W	00	Left DAC Datapath Control 00: Left DAC datapath is off (muted) 01: Left DAC datapath plays left channel input data 10: Left DAC datapath plays right channel input data 11: Left DAC datapath plays mono mix of left and right channel input data
D2–D1	R/W	00	Right DAC Datapath Control 00: Right DAC datapath is off (muted) 01: Right DAC datapath plays right channel input data 10: Right DAC datapath plays left channel input data 11: Right DAC datapath plays mono mix of left and right channel input data
D0	R/W	0	Reserved. Only write zero to this register.

Page 0 / Register 8: Audio Serial Data Interface Control Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Bit Clock Directional Control 0: Bit clock is an input (slave mode) 1: Bit clock is an output (master mode)
D6	R/W	0	Word Clock Directional Control 0: Word clock is an input (slave mode) 1: Word clock is an output (master mode)
D5	R/W	0	Reserved. Only write zero this bit.
D4	R/W	0	Bit/ Word Clock Drive Control 0: Bit clock and word clock will not be transmitted when in master mode if DAC is powered down 1: Bit clock and word clock will continue to be transmitted when in master mode, even if DAC is powered down
D3	R/W	0	Reserved. Only write zero to this bit.
D2	R/W	0	3-D Effect Control 0: Disable 3-D digital effect processing 1: Enable 3-D digital effect processing
D1-D0	R/W	00	Reserved. Only write zeroes to these bits.

Page 0 / Register 9: Audio Serial Data Interface Control Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Audio Serial Data Interface Transfer Mode 00: Serial data bus uses I^2S mode 01: Serial data bus uses DSP mode 10: Serial data bus uses right-justified mode 11: Serial data bus uses left-justified mode
D5–D4	R/W	00	Audio Serial Data Word Length Control 00: Audio data word length = 16-bits 01: Audio data word length = 20-bits 10: Audio data word length = 24-bits 11: Audio data word length = 32-bits
D3	R/W	0	Bit Clock Rate Control in master mode only This register only has effect when bit clock is programmed as an output 0: Continuous-transfer mode used to determine master mode bit clock rate 1: 256-clock transfer mode used, resulting in 256 bit clocks per frame
D2	R/W	0	DAC Re-Sync 0: Don't Care 1: Re-Sync Stereo DAC with Digital Interface if the group delay changes by more than DACFS/4.
D1	R/W	0	Reserved. Only write zero to this bit.
D0	R/W		Re-Sync Mute Behavior 0: Re-Sync is done without soft-muting the channel. (DAC) 1: Re-Sync is done by internally soft-muting the channel. (DAC)

Page 0 / Register 10: Audio Serial Data Interface Control Register C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	00000000	Audio Serial Data Word Offset Control This register determines where valid data is placed or expected in each frame, by controlling the offset from beginning of the frame where valid data begins. The offset is measured from the rising edge of word clock when in DSP mode. 00000000: Data offset = 0 bit clocks 00000001: Data offset = 1 bit clock 00000010: Data offset = 2 bit clocks … Note: In continuous transfer mode the maximum offset is 17 for I^2S/LJF/RJF modes and 16 for DSP mode. In 256-clock mode, the maximum offset is 242 for I^2S/LJF/RJF and 241 for DSP modes. 11111110: Data offset = 254 bit clocks 11111111: Data offset = 255 bit clocks

Page 0 / Register 11: Audio DAC Overflow Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	0	Reserved. Only write zeroes to these bits.
D5	R	0	Left DAC Overflow Flag This is a sticky bit, so will stay set if an overflow occurs, even if the overflow condition is removed. The register bit reset to 0 after it is read. 0: No overflow has occurred 1: An overflow has occurred
D4	R	0	Right DAC Overflow Flag This is a sticky bit, so will stay set if an overflow occurs, even if the overflow condition is removed. The register bit reset to 0 after it is read. 0: No overflow has occurred 1: An overflow has occurred
D3–D0	R/W	0001	PLL R Value 0000: R = 16 0001 : R = 1 0010 : R = 2 0011 : R = 3 0100 : R = 4 … 1110: R = 14 1111: R = 15

Page 0 / Register 12: Audio DAC Digital Filter Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	00	Reserved. Only write zeroes to these bits.
D3	R/W	0	Left DAC Digital Effects Filter Control 0: Left DAC digital effects filter disabled (bypassed) 1: Left DAC digital effects filter enabled
D2	R/W	0	Left DAC De-emphasis Filter Control 0: Left DAC de-emphasis filter disabled (bypassed) 1: Left DAC de-emphasis filter enabled
D1	R/W	0	Right DAC Digital Effects Filter Control 0: Right DAC digital effects filter disabled (bypassed) 1: Right DAC digital effects filter enabled
D0	R/W	0	Right DAC De-emphasis Filter Control 0: Right DAC de-emphasis filter disabled (bypassed) 1: Right DAC de-emphasis filter enabled

Page 0 / Register 13: Headset / Button Press Detection Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Headset Detection Control 0: Headset detection disabled 1: Headset detection enabled
D6-D5	R	00	Headset Type Detection Results 00: No headset detected 01: Stereo headset detected 10: Cellular headset detected 11: Stereo + cellular headset detected
D4-D2	R/W	000	Headset Glitch Suppression Debounce Control for Jack Detection 000: Debounce = 16msec(sampled with 2ms clock) 001: Debounce = 32msec(sampled with 4ms clock) 010: Debounce = 64msec(sampled with 8ms clock) 011: Debounce = 128msec(sampled with 16ms clock) 100: Debounce = 256msec(sampled with 32ms clock) 101: Debounce = 512msec(sampled with 64ms clock) 110: Reserved, do not write this bit sequence to these register bits. 111: Reserved, do not write this bit sequence to these register bits.

Page 0 / Register 13: Headset / Button Press Detection Register A (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1-D0	R/W	00	Headset Glitch Suppression Debounce Control for Button Press 00: Debounce = 0msec 01: Debounce = 8msec(sampled with 1ms clock) 10: Debounce = 16msec(sampled with 2ms clock) 11: Debounce = 32msec(sampled with 4ms clock)

Page 0 / Register 14: Headset / Button Press Detection Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Driver Capacitive Coupling 0: Programs high-power outputs for capless driver configuration 1: Programs high-power outputs for ac-coupled driver configuration
D6(1)	R/W	0	High Power Stereo Output Driver Configuration A Note: do not set bits D6 and D3 both high at the same time. 0: A stereo fully-differential output configuration is not being used 1: A stereo fully-differential output configuration is being used
D5	R	0	Button Press Detection Flag This register is a sticky bit, and will stay set to 1 after a button press has been detected, until the register is read. Upon reading this register, the bit is reset to zero. 0: A button press has not been detected 1: A button press has been detected
D4	R	0	Headset Detection Flag 0: A headset has not been detected 1: A headset has been detected
D3(1)	R/W	0	Stereo Output Driver Configuration B Note: do not set bits D6 and D3 both high at the same time. 0: A stereo pseudo-differential output configuration is not being used 1: A stereo pseudo-differential output configuration is being used
D2–D0	R	000	Reserved. Write only zeros to these bits.

(1) Do not set D6 and D3 to 1 simultaneously

Page 0 / Register 15–24: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00000000	Reserved. Only write zeroes to these bits.

Page 0 / Register 25: MICBIAS Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	MICBIAS Level Control 00: MICBIAS output is powered down 01: MICBIAS output is powered to 2.0 V 10: MICBIAS output is powered to 2.5 V 11: MICBIAS output is connected to AVDD_DAC
D5–D3	R	000	Reserved. Write only zeros to these register bits.
D2–D0	R	XXX	Read only bits. Do not write to these register bits.

Page 0 / Register 26–36: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	00000000	Reserved. Only write zeroes to these bits.

Page 0 / Register 37: DAC Power and Output Driver Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left DAC Power Control 0: Left DAC not powered up 1: Left DAC is powered up
D6	R/W	0	Right DAC Power Control 0: Right DAC not powered up 1: Right DAC is powered up
D5–D4	R/W	00	HPLCOM Output Driver Configuration Control 00: HPLCOM configured as differential of HPLOUT 01: HPLCOM configured as constant VCM output 10: HPLCOM configured as independent single-ended output 11: Reserved. Do not write this sequence to these register bits.
D3–D0	R	000	Reserved. Write only zeros to these register bits.

Page 0 / Register 38: High Power Output Driver Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only zeros to these register bits.
D5-D3	R/W	000	HPRCOM Output Driver Configuration Control 000: HPRCOM configured as differential of HPROUT 001: HPRCOM configured as constant VCM output 010: HPRCOM configured as independent single-ended output 011: HPRCOM configured as differential of HPLCOM 100: HPRCOM configured as external feedback with HPLCOM as constant VCM output 101–111: Reserved. Do not write these sequences to these register bits.
D2	R/W	0	Short Circuit Protection Control 0: Short circuit protection on all high power output drivers is disabled 1: Short circuit protection on all high power output drivers is enabled
D1	R/W	0	Short Circuit Protection Mode Control 0: If short circuit protection enabled, it will limit the maximum current to the load 1: If short circuit protection enabled, it will power down the output driver automatically when a short is detected
D0	R	0	Reserved. Write only zero to this register bit.

Page 0 / Register 39: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	00000000	Reserved. Do not write to this register.

Page 0 / Register 40: High Power Output Stage Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Output Common-Mode Voltage Control 00: Output common-mode voltage = 1.35V 01: Output common-mode voltage = 1.5V 10: Output common-mode voltage = 1.65V 11: Output common-mode voltage = 1.8V
D5–D4	R/W	00	LINEL Bypass Path Control 00: LINEL bypass is disabled 01: LINEL bypass uses LINEL 10: Reserved. Do not write this sequence to these register bits. 11: Reserved. Do not write this sequence to these register bits.

Page 0 / Register 40: High Power Output Stage Control Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3–D2	R/W	00	LINER Bypass Path Control 00: LINER bypass is disabled 01: LINER bypass uses LINER 10: Reserved. Do not write this sequence to these register bits. 11: Reserved. Do not write this sequence to these register bits.
D1–D0	R/W	00	Output Volume Control Soft-Stepping 00: Output soft-stepping = one step per Fs 01: Output soft-stepping = one step per 2Fs 10: Output soft-stepping disabled 11: Reserved. Do not write this sequence to these register bits.

Page 0 / Register 41: DAC Output Switching Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Left DAC Output Switching Control 00: Left DAC bypass disabled. 01: Reserved. Do not write to this bit. 10: Left DAC bypass enabled (Left DAC direct path enabled) 11: Reserved. Write only zero to this register bit.
D5–D4	R/W	00	Right DAC Output Switching Control 00: Right DAC bypass disabled. 01: Reserved. Do not write to this bit. 10: Right DAC bypass enabled (Right DAC direct path enabled) 11: Reserved. Write only zero to this register bit.
D3–D2	R/W	00	Reserved. Write only zeros to these bits.
D1–D0	R/W	00	DAC Digital Volume Control Functionality 00: Left and right DAC channels have independent volume controls 01: Left DAC volume follows the right channel control register 10: Right DAC volume follows the left channel control register 11: Left and right DAC channels have independent volume controls (same as 00)

Page 0 / Register 42: Output Driver Pop Reduction Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	Output Driver Power-On Delay Control 0000: Driver power-on time = 0-µsec 0001: Driver power-on time = 10-µsec 0010: Driver power-on time = 100-µsec 0011: Driver power-on time = 1-msec 0100: Driver power-on time = 10-msec 0101: Driver power-on time = 50-msec 0110: Driver power-on time = 100-msec 0111: Driver power-on time = 200-msec 1000: Driver power-on time = 400-msec 1001: Driver power-on time = 800-msec 1010: Driver power-on time = 2-sec 1011: Driver power-on time = 4-sec 1100–1111: Reserved. Do not write these sequences to these register bits.
D3-D2	R/W	00	Driver Ramp-up Step Timing Control 00: Driver ramp-up step time = 0-msec 01: Driver ramp-up step time = 1-msec 10: Driver ramp-up step time = 2-msec 11: Driver ramp-up step time = 4-msec
D1	R/W	0	Weak Output Common-mode Voltage Control 0: Weakly driven output common-mode voltage is generated from bandgap reference 1: Weakly driven output common-mode voltage is generated from resistor divider off the AVDD_DAC supply
D0	R/W	0	Reserved. Write only zero to this register bit.

Page 0 / Register 43: Left DAC Digital Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Left DAC Digital Mute 0: The left DAC channel is not muted 1: The left DAC channel is muted
D6–D0	R/W	0000000	Left DAC Digital Volume Control Setting 0000000: Gain = 0.0-dB 0000001: Gain = –0.5-dB 0000010: Gain = –1.0-dB … 1111101: Gain = –62.5-dB 1111110: Gain = –63.0-dB 1111111: Gain = –63.5-dB

Page 0 / Register 44: Right DAC Digital Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Right DAC Digital Mute 0: The right DAC channel is not muted 1: The right DAC channel is muted
D6–D0	R/W	0000000	Right DAC Digital Volume Control Setting 0000000: Gain = 0.0-dB 0000001: Gain = –0.5-dB 0000010: Gain = –1.0-dB … 1111101: Gain = –62.5-dB 1111110: Gain = –63.0-dB 1111111: Gain = –63.5-dB

Output Stage Volume Controls

A basic analog volume control with range from 0 dB to -78 dB and mute is replicated multiple times in the output stage network, connected to each of the analog signals that route to the output stage. In addition, to enable completely independent mixing operations to be performed for each output driver, each analog signal coming into the output stage may have up to four separate volume controls. These volume controls all have approximately 0.5-dB step programmability over most of the gain range, with steps increasing slightly at the lowest attenuations. Table 5 lists the detailed gain versus programmed setting for this basic volume control.

Table 5. Output Stage Volume Control Settings and Gains

Gain Setting	Analog Gain (dB)	Gain Setting	Analog Gain (dB)	Gain Setting	Analog Gain (dB)	Gain Setting	Analog Gain (dB)
0 0.0		30	-15.0	60	-30.1	90	-45.2
1	-0.5	31	-15.5	61	-30.6	91	-45.8
2	-1.0	32	-16.0	62	-31.1	92	-46.2
3	-1.5	33	-16.5	63	-31.6	93	-46.7
4	-2.0	34	-17.0	64	-32.1	94	-47.4
5	-2.5	35	-17.5	65	-32.6	95	-47.9
6	-3.0	36	-18.0	66	-33.1	96	-48.2
7	-3.5	37	-18.6	67	-33.6	97	-48.7
8	-4.0	38	-19.1	68	-34.1	98	-49.3
9	-4.5	39	-19.6	69	-34.6	99	-50.0
10	-5.0	40	-20.1	70	-35.1	100	-50.3
11	-5.5	41	-20.6	71	-35.7	101	-51.0
12	-6.0	42	-21.1	72	-36.1	102	-51.4
13	-6.5	43	-21.6	73	-36.7	103	-51.8
14	-7.0	44	-22.1	74	-37.1	104	-52.2

Table 5. Output Stage Volume Control Settings and Gains (continued)

Gain Setting	Analog Gain (dB)	Gain Setting	Analog Gain (dB)	Gain Setting	Analog Gain (dB)	Gain Setting	Analog Gain (dB)
15	-7.5	45	-22.6	75	-37.7	105	-52.7
16	-8.0	46	-23.1	76	-38.2	106	-53.7
17	-8.5	47	-23.6	77	-38.7	107	-54.2
18	-9.0	48	-24.1	78	-39.2	108	-55.3
19	-9.5	49	-24.6	79	-39.7	109	-56.7
20	-10.0	50	-25.1	80	-40.2	110	-58.3
21	-10.5	51	-25.6	81	-40.7	111	-60.2
22	-11.0	52	-26.1	82	-41.2	112	-62.7
23	-11.5	53	-26.6	83	-41.7	113	-64.3
24	-12.0	54	-27.1	84	-42.2	114	-66.2
25	-12.5	55	-27.6	85	-42.7	115	-68.7
26	-13.0	56	-28.1	86	-43.2	116	-72.2
27	-13.5	57	-28.6	87	-43.8	117	-78.3
28	-14.0	58	-29.1	88	-44.3	118–127	Mute
29	-14.5	59	-29.6	89	-44.8		

Page 0 / Register 45: LINEL to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEL Output Routing Control 0: LINEL is not routed to HPLOUT 1: LINEL is routed to HPLOUT
D6-D0	R/W	0000000	LINEL to HPLOUT Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5

Page 0 / Register 46: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00000000	Reserved. Do not write to this register.

Page 0 / Register 47: DAC_L to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L Output Routing Control 0: DAC_L is not routed to HPLOUT 1: DAC_L is routed to HPLOUT
D6-D0	R/W	0000000	DAC_L to HPLOUT Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5

Page 0 / Register 48: LINER to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINER Output Routing Control 0: LINER is not routed to HPLOUT 1: LINER is routed to HPLOUT
D6-D0	R/W	0000000	LINER to HPLOUT Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5

Page 0 / Register 49: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00000000	Reserved. Do not write to this register.

Page 0 / Register 50: DAC_R to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R Output Routing Control 0: DAC_R is not routed to HPLOUT 1: DAC_R is routed to HPLOUT
D6-D0	R/W	0000000	Reserved. Do not write to these register bits.

Page 0 / Register 51: HPLOUT Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	HPLOUT Output Level Control 0000: Output level control = 0-dB 0001: Output level control = 1-dB 0010: Output level control = 2-dB ... 1000: Output level control = 8-dB 1001: Output level control = 9-dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPLOUT Mute 0: HPLOUT is muted 1: HPLOUT is not muted
D2	R/W	1	HPLOUT Power Down Drive Control 0: HPLOUT is weakly driven to a common-mode when powered down 1: HPLOUT is tri-stated with powered down
D1	R	0	HPLOUT Volume Control Status 0: All programmed gains to HPLOUT have been applied 1: Not all programmed gains to HPLOUT have been applied yet
D0	R/W	0	HPLOUT Power Control 0: HPLOUT is not fully powered up 1: HPLOUT is fully powered up

Page 0 / Register 52: LINEL to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEL Output Routing Control 0: LINEL is not routed to HPLCOM 1: LINEL is routed to HPLCOM
D6-D0	R/W	0000000	LINEL to HPLCOM Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5

Page 0 / Register 53: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00000000	Reserved. Do not write to this register.

Page 0 / Register 54: DAC_L to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L Output Routing Control 0: DAC_L is not routed to HPLCOM 1: DAC_L is routed to HPLCOM

Page 0 / Register 54: DAC_L to HPLCOM Volume Control Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	0000000	DAC_L to HPLCOM Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5

Page 0 / Register 55: LINER to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINER Output Routing Control 0: LINER is not routed to HPLCOM 1: LINER is routed to HPLCOM
D6-D0	R/W	0000000	LINER to HPLCOM Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5

Page 0 / Register 56: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00000000	Reserved. Do not write to this register.

Page 0 / Register 57: DAC_R to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R Output Routing Control 0: DAC_R is not routed to HPLCOM 1: DAC_R is routed to HPLCOM
D6-D0	R/W	0000000	Reserved. Do not write to these register bits.

Page 0 / Register 58: HPLCOM Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	HPLCOM Output Level Control 0000: Output level control = 0-dB 0001: Output level control = 1-dB 0010: Output level control = 2-dB ... 1000: Output level control = 8-dB 1001: Output level control = 9-dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPLCOM Mute 0: HPLCOM is muted 1: HPLCOM is not muted
D2	R/W	1	HPLCOM Power Down Drive Control 0: HPLCOM is weakly driven to a common-mode when powered down 1: HPLCOM is tri-stated with powered down
D1	R	0	HPLCOM Volume Control Status 0: All programmed gains to HPLCOM have been applied 1: Not all programmed gains to HPLCOM have been applied yet
D0	R/W	0	HPLCOM Power Control 0: HPLCOM is not fully powered up 1: HPLCOM is fully powered up

Page 0 / Register 59: LINEL to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEL Output Routing Control 0: LINEL is not routed to HPROUT 1: LINEL is routed to HPROUT

Page 0 / Register 59: LINEL to HPROUT Volume Control Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	0000000	LINEL to HPROUT Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5

Page 0 / Register 60: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00000000	Reserved. Do not write to this register.

Page 0 / Register 61: DAC_L to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L Output Routing Control 0: DAC_L is not routed to HPROUT 1: DAC_L is routed to HPROUT
D6-D0	R/W	0000000	Reserved. Do not write to these register bits.

Page 0 / Register 62: LINER to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINER Output Routing Control 0: LINER is not routed to HPROUT 1: LINER is routed to HPROUT
D6-D0	R/W	0000000	LINER to HPROUT Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5

Page 0 / Register 63: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00000000	Reserved. Do not write to this register.

Page 0 / Register 64: DAC_R to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R Output Routing Control 0: DAC_R is not routed to HPROUT 1: DAC_R is routed to HPROUT
D6-D0	R/W	0000000	DAC_R to HPROUT Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5

Page 0 / Register 65: HPROUT Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	HPROUT Output Level Control 0000: Output level control = 0-dB 0001: Output level control = 1-dB 0010: Output level control = 2-dB ... 1000: Output level control = 8-dB 1001: Output level control = 9-dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPROUT Mute 0: HPROUT is muted 1: HPROUT is not muted

Page 0 / Register 65: HPROUT Output Level Control Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2	R/W	1	HPROUT Power Down Drive Control 0: HPROUT is weakly driven to a common-mode when powered down 1: HPROUT is tri-stated with powered down
D1	R	0	HPROUT Volume Control Status 0: All programmed gains to HPROUT have been applied 1: Not all programmed gains to HPROUT have been applied yet
D0	R/W	0	HPROUT Power Control 0: HPROUT is not fully powered up 1: HPROUT is fully powered up

Page 0 / Register 66: LINEL to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEL Output Routing Control 0: LINEL is not routed to HPRCOM 1: LINEL is routed to HPRCOM
D6-D0	R/W	0000000	LINEL to HPRCOM Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5

Page 0 / Register 67: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00000000	Reserved. Do not write to this register.

Page 0 / Register 68: DAC_L to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L Output Routing Control 0: DAC_L is not routed to HPRCOM 1: DAC_L is routed to HPRCOM
D6-D0	R/W	0000000	Reserved. Only write zeros to these bits.

Page 0 / Register 69: LINER to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINER Output Routing Control 0: LINER is not routed to HPRCOM 1: LINER is routed to HPRCOM
D6-D0	R/W	0000000	LINER to HPRCOM Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5

Page 0 / Register 70: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00000000	Reserved. Do not write to this register.

Page 0 / Register 71: DAC_R to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R Output Routing Control 0: DAC_R is not routed to HPRCOM 1: DAC_R is routed to HPRCOM

Page 0 / Register 71: DAC_R to HPRCOM Volume Control Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	0000000	DAC_R to HPRCOM Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5

Page 0 / Register 72: HPRCOM Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	HPRCOM Output Level Control 0000: Output level control = 0-dB 0001: Output level control = 1-dB 0010: Output level control = 2-dB ... 1000: Output level control = 8-dB 1001: Output level control = 9-dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPRCOM Mute 0: HPRCOM is muted 1: HPRCOM is not muted
D2	R/W	1	HPRCOM Power Down Drive Control 0: HPRCOM is weakly driven to a common-mode when powered down 1: HPRCOM is tri-stated with powered down
D1	R	0	HPRCOM Volume Control Status 0: All programmed gains to HPRCOM have been applied 1: Not all programmed gains to HPRCOM have been applied yet
D0	R/W	0	HPRCOM Power Control 0: HPRCOM is not fully powered up 1: HPRCOM is fully powered up

Page 0 / Register 73-93: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00000000	Reserved. Do not write to these registers.

Page 0 / Register 94: Module Power Status Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left DAC Power Status 0: Left DAC not fully powered up 1: Left DAC fully powered up
D6	R	0	Right DAC Power Status 0: Right DAC not fully powered up 1: Right DAC fully powered up
D5–D3	R	0	Reserved. Do not write to these bits.
D2	R	0	HPLOUT Driver Power Status 0: HPLOUT Driver is not fully powered up 1: HPLOUT Driver is fully powered up
D1	R	0	HPROUT Driver Power Status 0: HPROUT Driver is not fully powered up 1: HPROUT Driver is fully powered up
D0	R	0	Reserved. Do not write to this register bit.

Page 0 / Register 95: Output Driver Short Circuit Detection Status Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPLOUT Short Circuit Detection Status 0: No short circuit detected at HPLOUT 1: Short circuit detected at HPLOUT
D6	R	0	HPROUT Short Circuit Detection Status 0: No short circuit detected at HPROUT 1: Short circuit detected at HPROUT
D5	R	0	HPLCOM Short Circuit Detection Status 0: No short circuit detected at HPLCOM 1: Short circuit detected at HPLCOM
D4	R	0	HPRCOM Short Circuit Detection Status 0: No short circuit detected at HPRCOM 1: Short circuit detected at HPRCOM
D3	R	0	HPLCOM Power Status 0: HPLCOM is not fully powered up 1: HPLCOM is fully powered up
D2	R	0	HPRCOM Power Status 0: HPRCOM is not fully powered up 1: HPRCOM is fully powered up
D1-D0	R	00	Reserved. Do not write to these register bits.

Page 0 / Register 96: Sticky Interrupt Flags Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPLOUT Short Circuit Detection Status 0: No short circuit detected at HPLOUT driver 1: Short circuit detected at HPLOUT driver
D6	R	0	HPROUT Short Circuit Detection Status 0: No short circuit detected at HPROUT driver 1: Short circuit detected at HPROUT driver
D5	R	0	HPLCOM Short Circuit Detection Status 0: No short circuit detected at HPLCOM driver 1: Short circuit detected at HPLCOM driver
D4	R	0	HPRCOM Short Circuit Detection Status 0: No short circuit detected at HPRCOM driver 1: Short circuit detected at HPRCOM driver
D3	R	0	Button Press Detection Status 0: No Headset Button Press detected 1: Headset Button Pressed
D2	R	0	Headset Detection Status 0: No Headset insertion/removal is detected 1: Headset insertion/removal is detected
D1-D0	R	00	Reserved. Do not write to these bits.

Page 0 / Register 97: Real-time Interrupt Flags Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPLOUT Short Circuit Detection Status 0: No short circuit detected at HPLOUT driver 1: Short circuit detected at HPLOUT driver
D6	R	0	HPROUT Short Circuit Detection Status 0: No short circuit detected at HPROUT driver 1: Short circuit detected at HPROUT driver
D5	R	0	HPLCOM Short Circuit Detection Status 0: No short circuit detected at HPLCOM driver 1: Short circuit detected at HPLCOM driver

Page 0 / Register 97: Real-time Interrupt Flags Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4	R	0	HPRCOM Short Circuit Detection Status 0: No short circuit detected at HPRCOM driver 1: Short circuit detected at HPRCOM driver
D3	R	0	Button Press Detection Status(1) 0: No Headset Button Press detected 1: Headset Button Pressed
D2	R	0	Headset Detection Status 0: No Headset is detected 1: Headset is detected
D1-D0	R	00	Reserved. Do not write to these bits.

(1) This bit is a sticky bit, cleared only when Page 0, Register 14 is read.

Page 0 / Register 98–100: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000	Reserved. Do not write to these registers.

Page 0 / Register 101: Additional Control Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D1	R	0	Reserved. Do not write to these bits.
D0	R/W	0	DAC_CLKIN Source Selection 0: DAC_CLKIN uses PLLDIV_OUT 1: DAC_CLKIN uses CLKDIV_OUT

Page 0 / Register 102: Clock Generation Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	CLKDIV_IN Source Selection 00: CLKDIV_IN uses MCLK 01: Reserved. Do not write to this bit. 10: CLKDIV_IN uses BCLK 11: Reserved. Do not use.
D5-D4	R/W	00	PLLCLK_IN Source Selection 00: PLLCLK_IN uses MCLK 01: Reserved. Do not write to this bit. 10: PLLCLK _IN uses BCLK 11: Reserved. Do not use.
D3-D0	R/W	0010	PLL Clock Divider N Value 0000: N=16 0001: N=17 0010: N=2 0011: N=3 … 1111: N=15

Page 0 / Register 103–127: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	00000000	Reserved. Do not write to these registers.

Page 1 / Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D1	X	0000000	Reserved, write only zeros to these register bits
D0	R/W	0	Page Select Bit Writing zero to this bit sets Page-0 as the active page for following register accesses. Writing a one to this bit sets Page-1 as the active page for following register accesses. It is recommended that the user read this register bit back after each write, to ensure that the proper page is being accessed for future register read/writes. This register has the same functionality on page-0 and page-1.

Table 2. Page 1 / Register 1: Left Channel Audio Effects Filter N0 Coefficient MSB Register(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01101011	Left Channel Audio Effects Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

(1) When programming any coefficient value in Page 1, the MSB register should always be written first, immediately followed by the LSB register. Even if only the MSB or LSB of the coefficient changes, both registers should be written in this sequence.

Page 1 / Register 2: Left Channel Audio Effects Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	11100011	Left Channel Audio Effects Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 3: Left Channel Audio Effects Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	10010110	Left Channel Audio Effects Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 4: Left Channel Audio Effects Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01100110	Left Channel Audio Effects Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 5: Left Channel Audio Effects Filter N2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01100111	Left Channel Audio Effects Filter N2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 6: Left Channel Audio Effects Filter N2 Coefficient LSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01011101	Left Channel Audio Effects Filter N2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 7: Left Channel Audio Effects Filter N3 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01101011	Left Channel Audio Effects Filter N3 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 8: Left Channel Audio Effects Filter N3 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	11100011	Left Channel Audio Effects Filter N3 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 9: Left Channel Audio Effects Filter N4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	10010110	Left Channel Audio Effects Filter N4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 10: Left Channel Audio Effects Filter N4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01100110	Left Channel Audio Effects Filter N4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 11: Left Channel Audio Effects Filter N5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01100111	Left Channel Audio Effects Filter N5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 12: Left Channel Audio Effects Filter N5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01011101	D7-D0 R/W 00000000 Left Channel Audio Effects Filter N5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from -32768 to +32767.

Page 1 / Register 13: Left Channel Audio Effects Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01111101	Left Channel Audio Effects Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 14: Left Channel Audio Effects Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	10000011	Left Channel Audio Effects Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 15: Left Channel Audio Effects Filter D2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	10000100	Left Channel Audio Effects Filter D2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 16: Left Channel Audio Effects Filter D2 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	11101110	Left Channel Audio Effects Filter D2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 17: Left Channel Audio Effects Filter D4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01111101	Left Channel Audio Effects Filter D4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 18: Left Channel Audio Effects Filter D4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	10000011	Left Channel Audio Effects Filter D4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 19: Left Channel Audio Effects Filter D5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	10000100	Left Channel Audio Effects Filter D5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 20: Left Channel Audio Effects Filter D5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	11101110	Left Channel Audio Effects Filter D5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 21: Left Channel De-emphasis Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00111001	Left Channel De-emphasis Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 22: Left Channel De-emphasis Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01010101	Left Channel De-emphasis Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 23: Left Channel De-emphasis Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	11110011	Left Channel De-emphasis Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 24: Left Channel De-emphasis Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00101101	Left Channel De-emphasis Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 25: Left Channel De-emphasis Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01010011	Left Channel De-emphasis Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 26: Left Channel De-emphasis Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01111110	Left Channel De-emphasis Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 27: Right Channel Audio Effects Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01101011	Right Channel Audio Effects Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 28: Right Channel Audio Effects Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	11100011	Right Channel Audio Effects Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 29: Right Channel Audio Effects Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	10010110	Right Channel Audio Effects Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 30: Right Channel Audio Effects Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01100110	Right Channel Audio Effects Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 31: Right Channel Audio Effects Filter N2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01100111	Right Channel Audio Effects Filter N2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 32: Right Channel Audio Effects Filter N2 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01011101	Right Channel Audio Effects Filter N2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 33: Right Channel Audio Effects Filter N3 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01101011	Right Channel Audio Effects Filter N3 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 34: Right Channel Audio Effects Filter N3 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	11100011	Right Channel Audio Effects Filter N3 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 35: Right Channel Audio Effects Filter N4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	10010110	Right Channel Audio Effects Filter N4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 36: Right Channel Audio Effects Filter N4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01100110	Right Channel Audio Effects Filter N4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 37: Right Channel Audio Effects Filter N5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01100111	Right Channel Audio Effects Filter N5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 38: Right Channel Audio Effects Filter N5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01011101	Right Channel Audio Effects Filter N5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 39: Right Channel Audio Effects Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01111101	Right Channel Audio Effects Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 40: Right Channel Audio Effects Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	10000011	Right Channel Audio Effects Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 41: Right Channel Audio Effects Filter D2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	10000100	Right Channel Audio Effects Filter D2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 42: Right Channel Audio Effects Filter D2 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	11101110	Right Channel Audio Effects Filter D2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 43: Right Channel Audio Effects Filter D4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01111101	Right Channel Audio Effects Filter D4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 44: Right Channel Audio Effects Filter D4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	10000011	Right Channel Audio Effects Filter D4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 45: Right Channel Audio Effects Filter D5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	10000100	Right Channel Audio Effects Filter D5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 46: Right Channel Audio Effects Filter D5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	11101110	Right Channel Audio Effects Filter D5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 47: Right Channel De-emphasis Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00111001	Right Channel De-emphasis Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 48: Right Channel De-emphasis Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01010101	Right Channel De-emphasis Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 49: Right Channel De-emphasis Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	11110011	Right Channel De-emphasis Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 50: Right Channel De-emphasis Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00101101	Right Channel De-emphasis Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 51: Right Channel De-emphasis Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01010011	Right Channel De-emphasis Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 52: Right Channel De-emphasis Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01111110	Right Channel De-emphasis Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 53: 3-D Attenuation Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01111111	3-D Attenuation Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 54: 3-D Attenuation Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	11111111	3-D Attenuation Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 55–127: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	00000000	Reserved. Do not write to these registers.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLV320DAC32IRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC32I	Samples
TLV320DAC32IRHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC32I	Samples
TLV320DAC32IRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC32I	Samples
TLV320DAC32IRHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC32I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

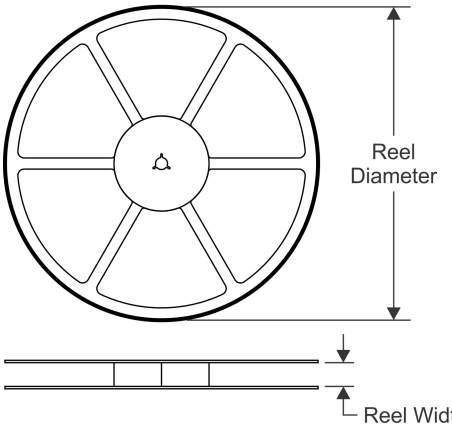
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

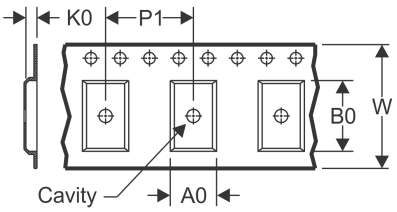
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

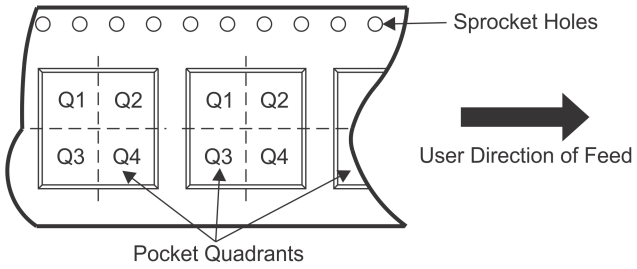


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

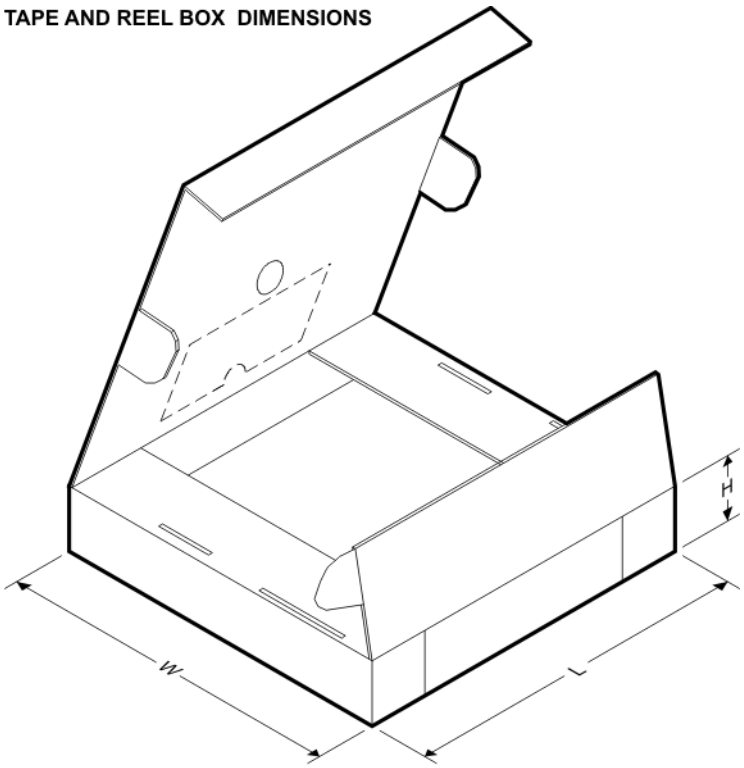
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320DAC32IRHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLV320DAC32IRHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

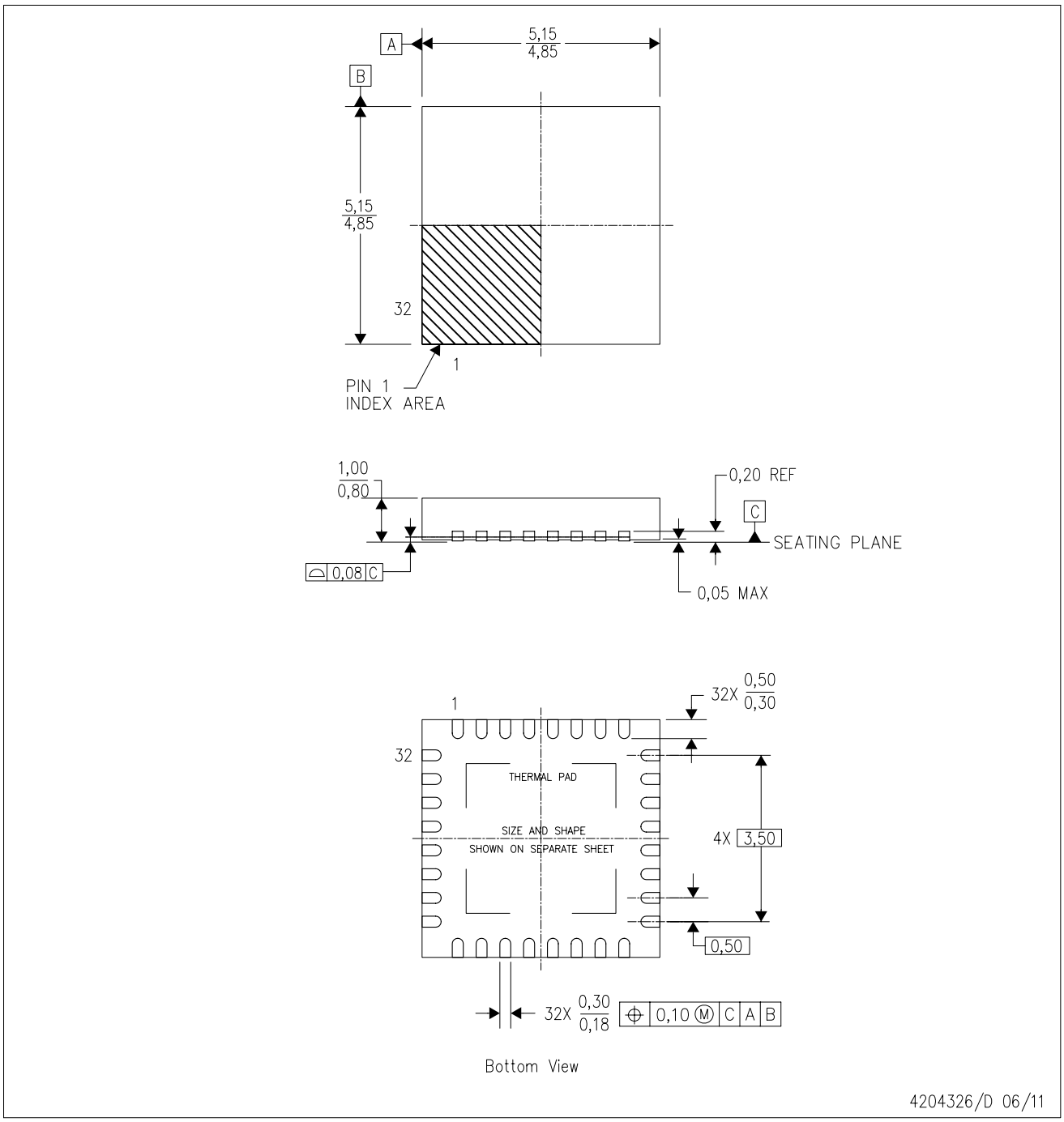
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320DAC32IRHBR	QFN	RHB	32	3000	338.1	338.1	20.6
TLV320DAC32IRHBT	QFN	RHB	32	250	210.0	185.0	35.0

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

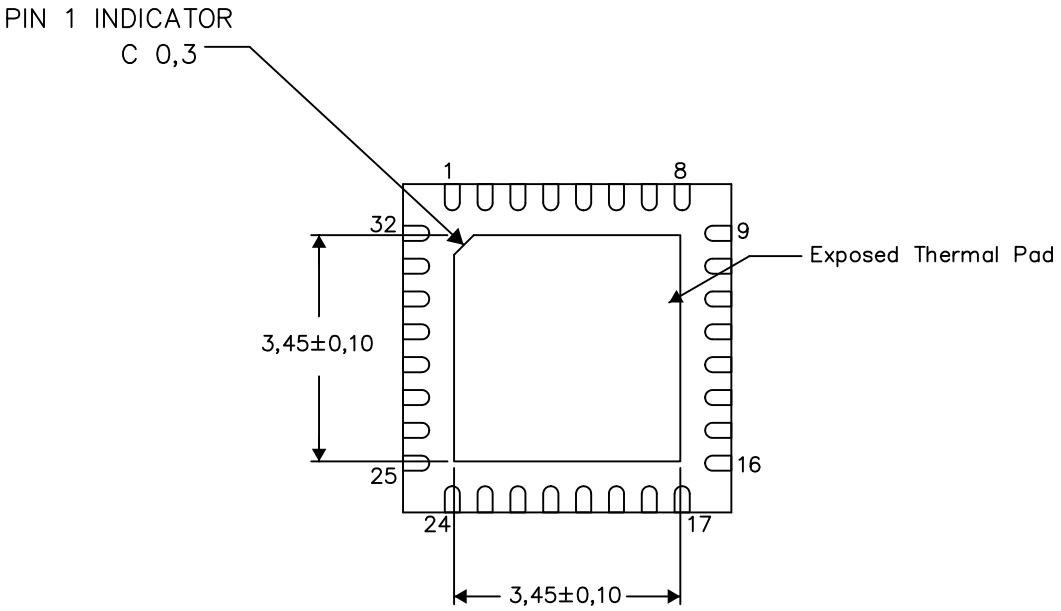
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



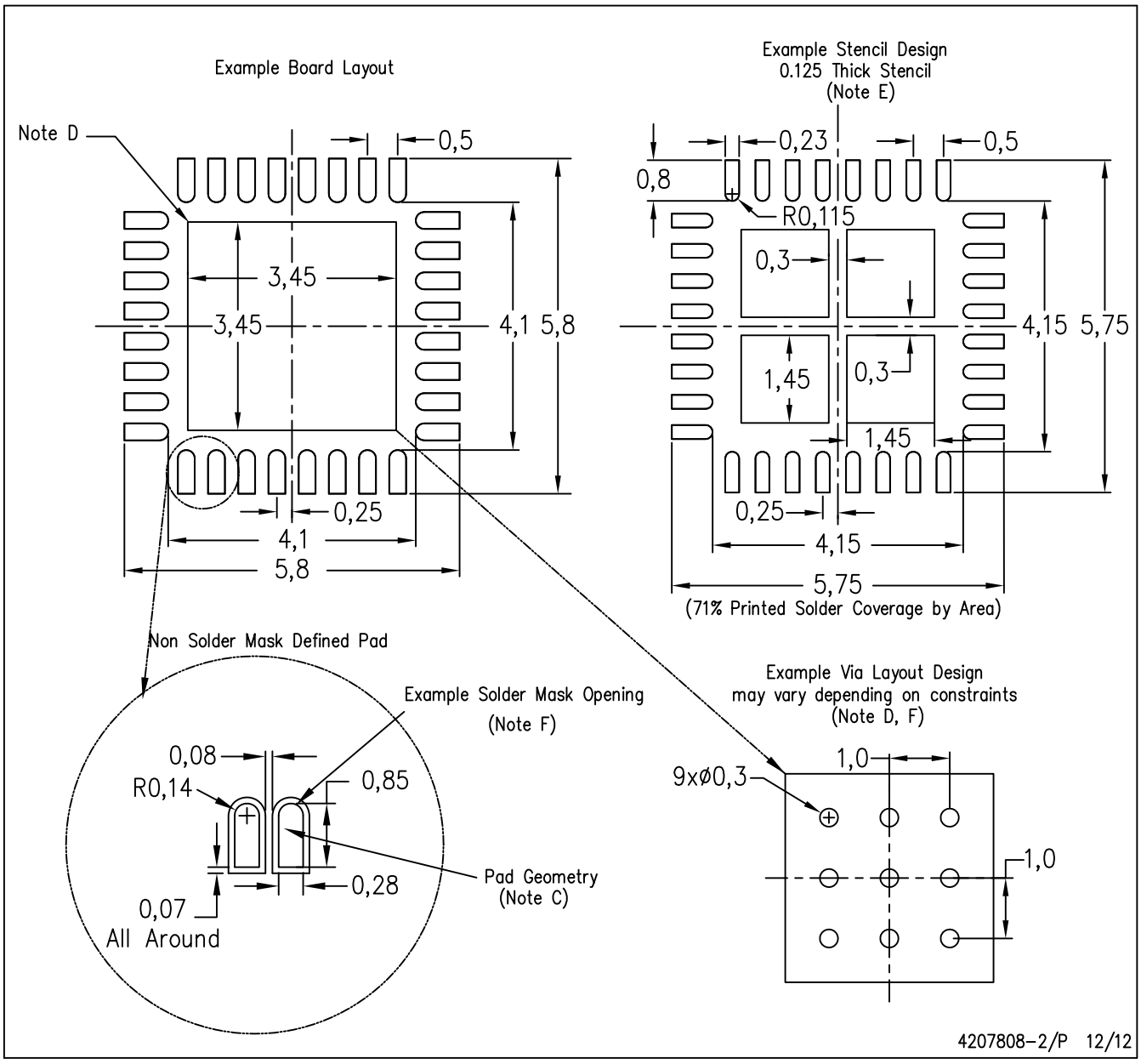
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/X 12/12

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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