

## FEATURES

- **12-Bit 150ksps ADCs in MSOP Package**
- Single 3V Supply
- Low Supply Current: 450μA (Typ)
- Auto Shutdown Reduces Supply Current to 10μA at 1ksps
- True Differential Inputs
- 1-Channel (LTC1860L) or 2-Channel (LTC1861L) Versions
- SPI/MICROWIRE™ Compatible Serial I/O
- High Speed Upgrade to LTC1285/LTC1288
- Pin Compatible with 16-Bit LTC1864L/LTC1865L
- No Minimum Data Transfer Rate

## APPLICATIONS

- High Speed Data Acquisition
- Portable or Compact Instrumentation
- Low Power Battery-Operated Instrumentation
- Isolated and/or Remote Data Acquisition

## DESCRIPTION

The LTC®1860L/LTC1861L are 12-bit A/D converters that are offered in MSOP and SO-8 packages and operate on a single 3V supply. At 150ksps, the supply current is only 450μA. The supply current drops at lower speeds because the LTC1860L/LTC1861L automatically power down between conversions. These 12-bit switched capacitor successive approximation ADCs include sample-and-holds. The LTC1860L has a differential analog input with an external reference pin. The LTC1861L offers a software-selectable 2-channel MUX and an external reference pin on the MSOP version.

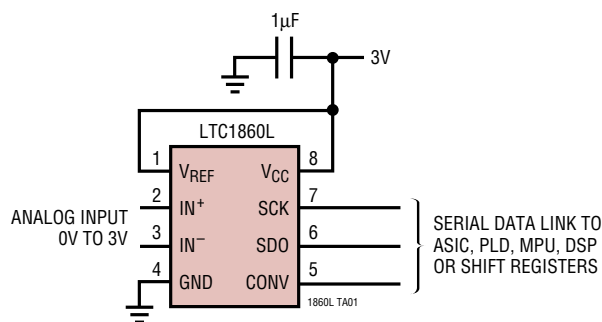
The 3-wire, serial I/O, MSOP or SO-8 package and extremely high sample rate-to-power ratio make these ADCs ideal choices for compact, low power, high speed systems.

These ADCs can be used in ratiometric applications or with external references. The high impedance analog inputs and the ability to operate with reduced spans down to 1V full scale allow direct connection to signal sources in many applications, eliminating the need for external gain stages.

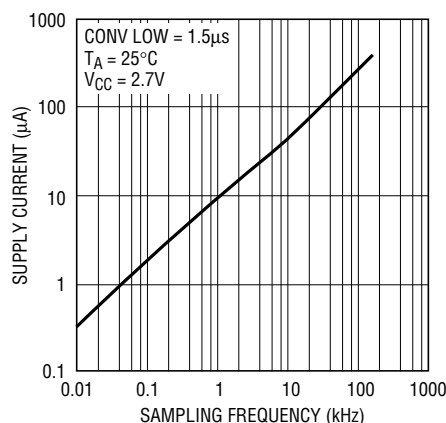
LT, LTC and LT are registered trademarks of Linear Technology Corporation.  
MICROWIRE is a trademark of National Semiconductor Corporation.

## TYPICAL APPLICATION

**Single 3V Supply, 150ksps, 12-Bit Sampling ADC**



**Supply Current vs Sampling Frequency**

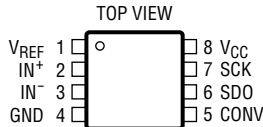
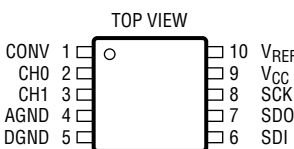
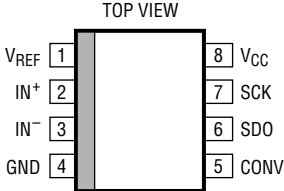
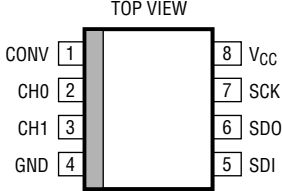


# LTC1860L/LTC1861L

## ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage ( $V_{CC}$ )	7V	Power Dissipation	400mW
Ground Voltage Difference		Operating Temperature Range	
AGND, DGND LTC1861L MSOP Package	$\pm 0.3V$	LTC1860LC/LTC1861LC	0°C to 70°C
Analog Input	(GND – 0.3V) to ( $V_{CC} + 0.3V$ )	LTC1860LI/LTC1861LI	–40°C to 85°C
Digital Input	(GND – 0.3V) to 7V	Storage Temperature Range	–65°C to 150°C
Digital Output	(GND – 0.3V) to ( $V_{CC} + 0.3V$ )	Lead Temperature (Soldering, 10 sec)	300°C

## PACKAGE/ORDER INFORMATION

 <p>MS8 PACKAGE 8-LEAD PLASTIC MSOP <math>T_{JMAX} = 150^{\circ}C, \theta_{JA} = 210^{\circ}C/W</math></p>	ORDER PART NUMBER	 <p>MS PACKAGE 10-LEAD PLASTIC MSOP <math>T_{JMAX} = 150^{\circ}C, \theta_{JA} = 210^{\circ}C/W</math></p>	ORDER PART NUMBER
	LTC1860LCMS8 LTC1860LIMS8		LTC1861LCMS LTC1861LIMS
	MS8 PART MARKING		MS PART MARKING
	LTD2 LTD3		LTD4 LTD5
 <p>S8 PACKAGE 8-LEAD PLASTIC SO <math>T_{JMAX} = 150^{\circ}C, \theta_{JA} = 175^{\circ}C/W</math></p>	ORDER PART NUMBER	 <p>S8 PACKAGE 8-LEAD PLASTIC SO <math>T_{JMAX} = 150^{\circ}C, \theta_{JA} = 175^{\circ}C/W</math></p>	ORDER PART NUMBER
	LTC1860LCS8 LTC1860LIS8		LTC1861LCS8 LTC1861LIS8
	S8 PART MARKING		S8 PART MARKING
	1860L 1860LI		1861L 1861LI

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are  $T_A = 25^{\circ}C$ .  $V_{CC} = 2.7V$ ,  $V_{REF} = 2.5V$ ,  $f_{SCK} = f_{SCK(MAX)}$  as defined in Recommended Operating Conditions, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	●	12			Bits
No Missing Codes Resolution	●	12			Bits
INL	(Note 3)	●		$\pm 1$	LSB
Transition Noise			0.13		LSB <sub>RMS</sub>
Gain Error	●			$\pm 20$	mV
Offset Error	●		$\pm 2$	$\pm 5$	mV
Input Differential Voltage Range	$V_{IN} = IN^+ - IN^-$	●	0	$V_{REF}$	V
Absolute Input Range	$IN^+$ Input	–0.05		$V_{CC} + 0.05$	V
	$IN^-$ Input	–0.05		$V_{CC}/2$	V
$V_{REF}$ Input Range	LTC1860L S0-8 and MSOP, LTC1861L MSOP	1		$V_{CC}$	V
Analog Input Leakage Current	(Note 4)	●		$\pm 1$	$\mu A$
$C_{IN}$ Input Capacitance	In Sample Mode		12		pF
	During Conversion		5		pF

18601LI

## DYNAMIC ACCURACY

$T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3\text{V}$ ,  $V_{REF} = 3\text{V}$ ,  $f_{\text{SAMPLE}} = 150\text{kHz}$ , unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio			72		dB
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	1kHz Input Signal		72		dB
THD	Total Harmonic Distortion Up to 5th Harmonic	1kHz Input Signal		86		dB
	Full Power Bandwidth			10		MHz
	Full Linear Bandwidth	$S/(N + D) \geq 68\text{dB}$		30		kHz

**DIGITAL AND DC ELECTRICAL CHARACTERISTICS** The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 2.7\text{V}$ ,  $V_{REF} = 2.5\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IH}$	High Level Input Voltage	$V_{CC} = 3.3\text{V}$ ●	1.9			V
$V_{IL}$	Low Level Input Voltage	$V_{CC} = 2.7\text{V}$ ●			0.45	V
$I_{IH}$	High Level Input Current	$V_{IN} = V_{CC}$ ●			2.5	$\mu\text{A}$
$I_{IL}$	Low Level Input Current	$V_{IN} = 0\text{V}$ ●			-2.5	$\mu\text{A}$
$V_{OH}$	High Level Output Voltage	$V_{CC} = 2.7\text{V}$ , $I_O = 10\mu\text{A}$ ● $V_{CC} = 2.7\text{V}$ , $I_O = 360\mu\text{A}$ ●	2.3 2.1	2.6 2.45		V V
$V_{OL}$	Low Level Output Voltage	$V_{CC} = 2.7\text{V}$ , $I_O = 400\mu\text{A}$ ●			0.3	V
$I_{OZ}$	Hi-Z Output Leakage	$CONV = V_{CC}$ ●			$\pm 3$	$\mu\text{A}$
$I_{SOURCE}$	Output Source Current	$V_{OUT} = 0\text{V}$		-6.5		mA
$I_{SINK}$	Output Sink Current	$V_{OUT} = V_{CC}$		6.5		mA
$I_{REF}$	Reference Current (LTC1860L SO-8, MSOP and LTC1861L MSOP)	$CONV = V_{CC}$ ● $f_{\text{SMPL}} = f_{\text{SMPL}}(\text{MAX})$ ●		0.001 0.01	3 0.1	$\mu\text{A}$ mA
$I_{CC}$	Supply Current	$CONV = V_{CC}$ After Conversion ● $f_{\text{SMPL}} = f_{\text{SMPL}}(\text{MAX})$ ●		0.5 0.45	10 1.0	$\mu\text{A}$ mA
$P_D$	Power Dissipation	$f_{\text{SMPL}} = f_{\text{SMPL}}(\text{MAX})$		1.22		mW

**RECOMMENDED OPERATING CONDITIONS** The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are  $T_A = 25^\circ\text{C}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{CC}$	Supply Voltage		2.7		3.6	V
$f_{\text{SCK}}$	Clock Frequency	●	DC		8	MHz
$t_{\text{CYC}}$	Total Cycle Time		$12 \cdot \text{SCK} + t_{\text{CONV}}$			$\mu\text{s}$
$t_{\text{SMPL}}$	Analog Input Sampling Time (Note 5)	LTC1860L LTC1861L	12 10			SCK SCK
$t_{\text{SUCONV}}$	Setup Time $CONV \downarrow$ Before First $\text{SCK} \uparrow$ , (See Figure 1)		60			ns
$t_{\text{HDI}}$	Holdtime $\text{SDI}$ After $\text{SCK} \uparrow$	LTC1861L	30			ns
$t_{\text{SUDI}}$	Setup Time $\text{SDI}$ Stable Before $\text{SCK} \uparrow$	LTC1861L	30			ns
$t_{\text{WHCLK}}$	SCK High Time	$f_{\text{SCK}} = f_{\text{SCK}}(\text{MAX})$	45%			$1/f_{\text{SCK}}$
$t_{\text{WLCLK}}$	SCK Low Time	$f_{\text{SCK}} = f_{\text{SCK}}(\text{MAX})$	45%			$1/f_{\text{SCK}}$
$t_{\text{WHCONV}}$	$CONV$ High Time Between Data Transfer Cycles		$t_{\text{CONV}}$			$\mu\text{s}$
$t_{\text{WLCONV}}$	$CONV$ Low Time During Data Transfer		12			SCK
$t_{\text{HCONV}}$	Hold Time $CONV$ Low After Last $\text{SCK} \uparrow$		26			ns

**TIMING CHARACTERISTICS** The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 2.7\text{V}$ ,  $V_{REF} = 2.5\text{V}$ ,  $f_{SCK} = f_{SCK(MAX)}$  as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{CONV}$	Conversion Time (See Figure 1)	●		3.7	4.66	$\mu\text{s}$
$f_{SAMPL(MAX)}$	Maximum Sampling Frequency	●	150			kHz
$t_{dDO}$	Delay Time, $SCK\downarrow$ to SDO Data Valid	$C_{LOAD} = 20\text{pF}$ ●		45	55 60	ns ns
$t_{dis}$	Delay Time, $CONV\uparrow$ to SDO Hi-Z	●		55	120	ns
$t_{en}$	Delay Time, $CONV\downarrow$ to SDO Enabled	$C_{LOAD} = 20\text{pF}$ ●		35	120	ns
$t_{hDO}$	Time Output Data Remains Valid After $SCK\downarrow$	$C_{LOAD} = 20\text{pF}$ ●	5	15		ns
$t_r$	SDO Rise Time	$C_{LOAD} = 20\text{pF}$		25		ns
$t_f$	SDO Fall Time	$C_{LOAD} = 20\text{pF}$		12		ns

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All voltage values are with respect to GND.

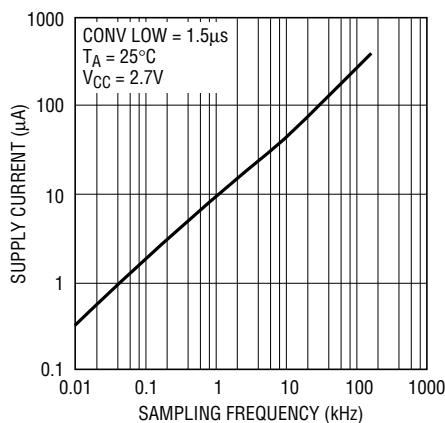
**Note 3:** Integral nonlinearity is defined as deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 4:** Channel leakage current is measured while the part is in sample mode.

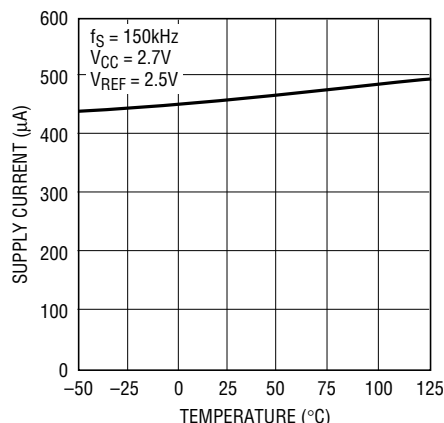
**Note 5:** Assumes  $f_{SCK} = f_{SCK(MAX)}$ . In the case of the LTC1860L SCK does not have to be clocked during this time if the SDO data word is not desired. In the case of the LTC1861L a minimum of 2 clocks are required on the SCK input after CONV falls to configure the MUX during this time.

## TYPICAL PERFORMANCE CHARACTERISTICS

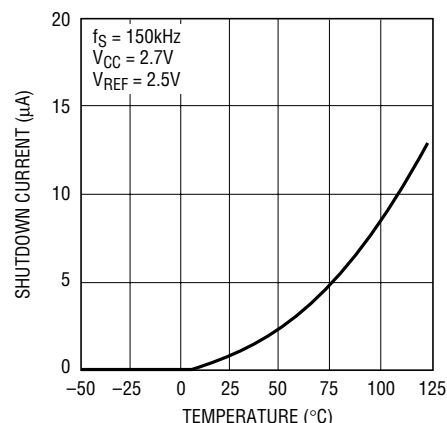
**Supply Current vs Sampling Frequency**



**Supply Current vs Temperature**

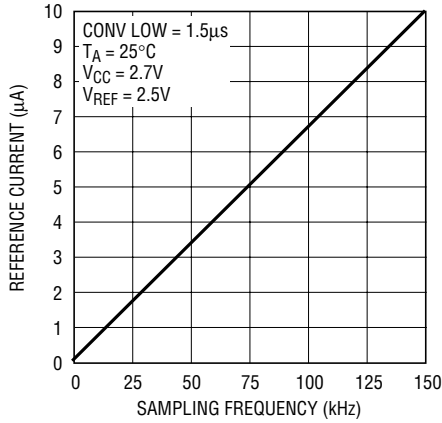


**Sleep Current vs Temperature**



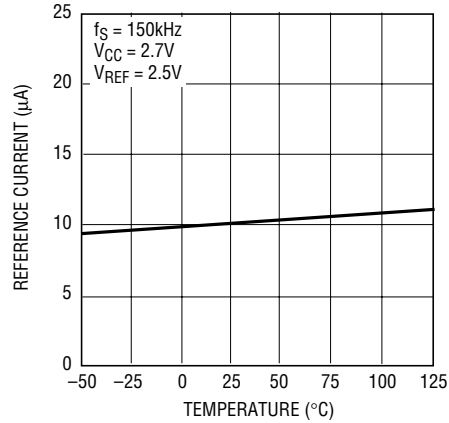
# TYPICAL PERFORMANCE CHARACTERISTICS

## Reference Current vs Sampling Rate



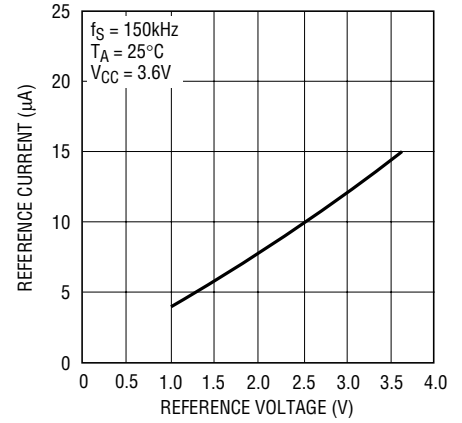
1860L/61L G04

## Reference Current vs Temperature



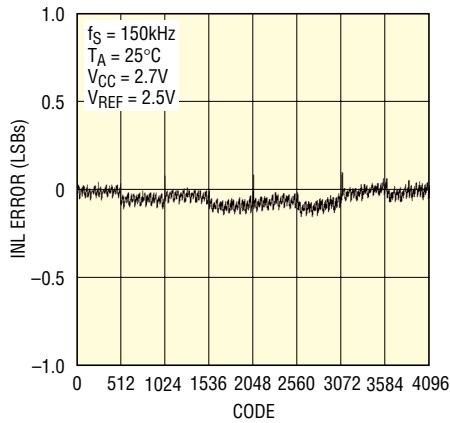
1860L/61L G05

## Reference Current vs Reference Voltage



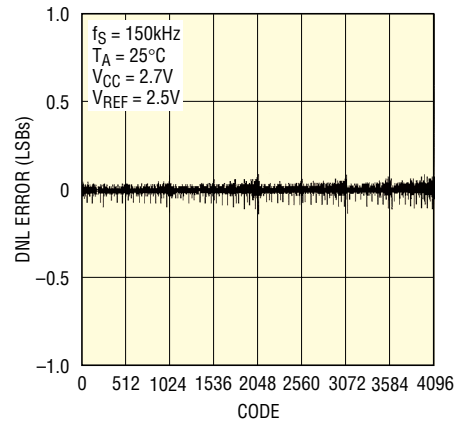
1860L/61L G06

## Typical INL Curve



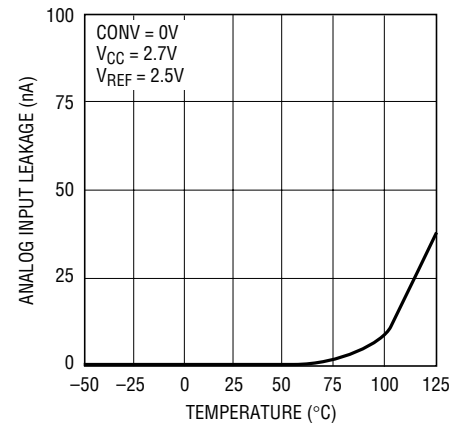
1860L/61L G07

## Typical DNL Curve



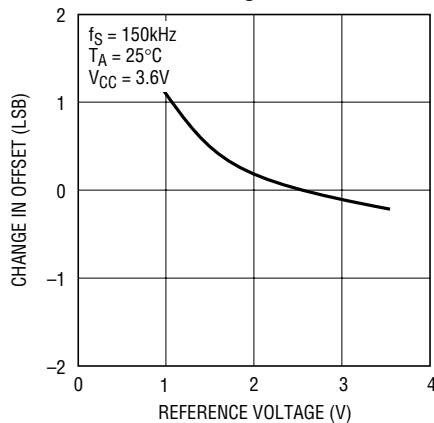
1860L/61L G08

## Analog Input Leakage vs Temperature



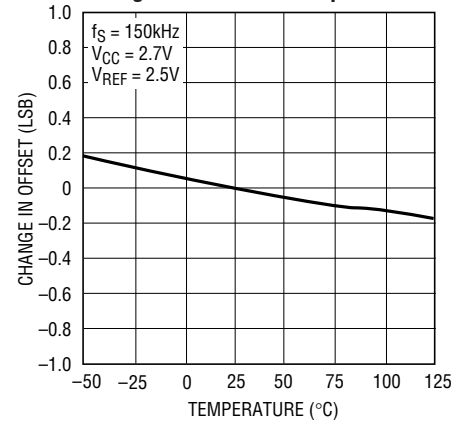
1860L/61L G09

## Change in Offset vs Reference Voltage



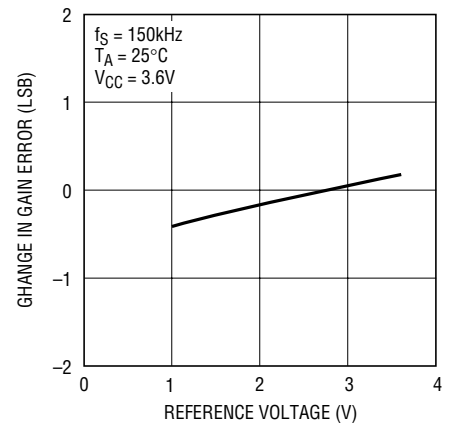
1860L/61L G10

## Change in Offset vs Temperature



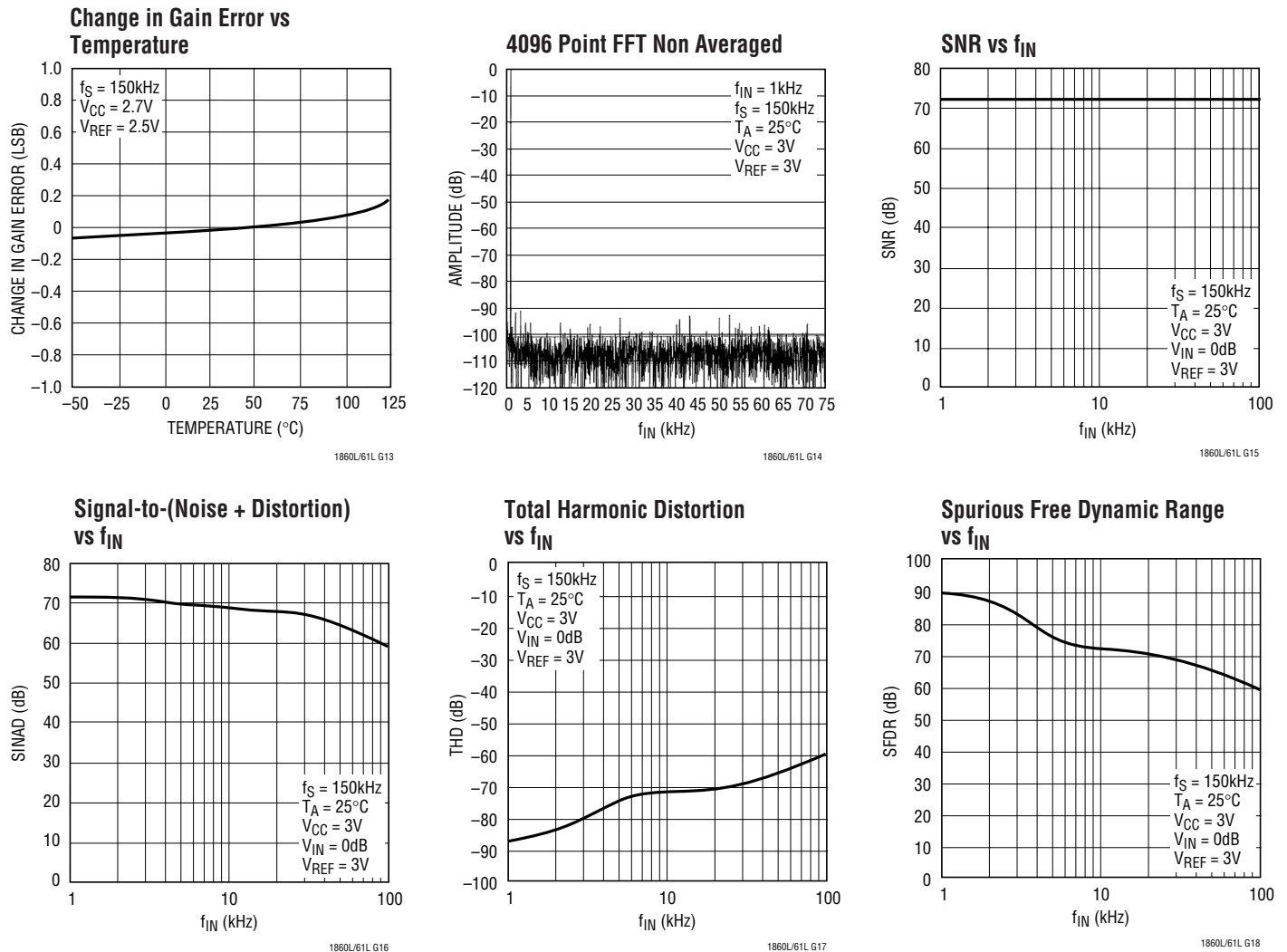
1860L/61L G11

## Change in Gain Error vs Reference Voltage



1860L/61L G12

## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS LTC1860L

**$V_{REF}$  (Pin 1):** Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

**$IN^+$ ,  $IN^-$  (Pins 2, 3):** Analog Inputs. These inputs must be free of noise with respect to GND.

**GND (Pin 4):** Analog Ground. GND should be tied directly to an analog ground plane.

**CONV (Pin 5):** Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left

high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

**SDO (Pin 6):** Digital Data Output. The A/D conversion result is shifted out of this pin.

**SCK (Pin 7):** Shift Clock Input. This clock synchronizes the serial data transfer.

**$V_{CC}$  (Pin 8):** Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

## PIN FUNCTIONS

### LTC1861L (MSOP Package)

**CONV (Pin 1):** Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

**CH0, CH1 (Pins 2, 3):** Analog Inputs. These inputs must be free of noise with respect to AGND.

**AGND (Pin 4):** Analog Ground. AGND should be tied directly to an analog ground plane.

**DGND (Pin 5):** Digital Ground. DGND should be tied directly to an analog ground plane.

**SDI (Pin 6):** Digital Data Input. The A/D configuration word is shifted into this input.

**SDO (Pin 7):** Digital Data Output. The A/D conversion result is shifted out of this output.

**SCK (Pin 8):** Shift Clock Input. This clock synchronizes the serial data transfer.

**V<sub>CC</sub> (Pin 9):** Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

**V<sub>REF</sub> (Pin 10):** Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to AGND.

### LTC1861L (SO-8 Package)

**CONV (Pin 1):** Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

**CH0, CH1 (Pins 2, 3):** Analog Inputs. These inputs must be free of noise with respect to GND.

**GND (Pin 4):** Analog Ground. GND should be tied directly to an analog ground plane.

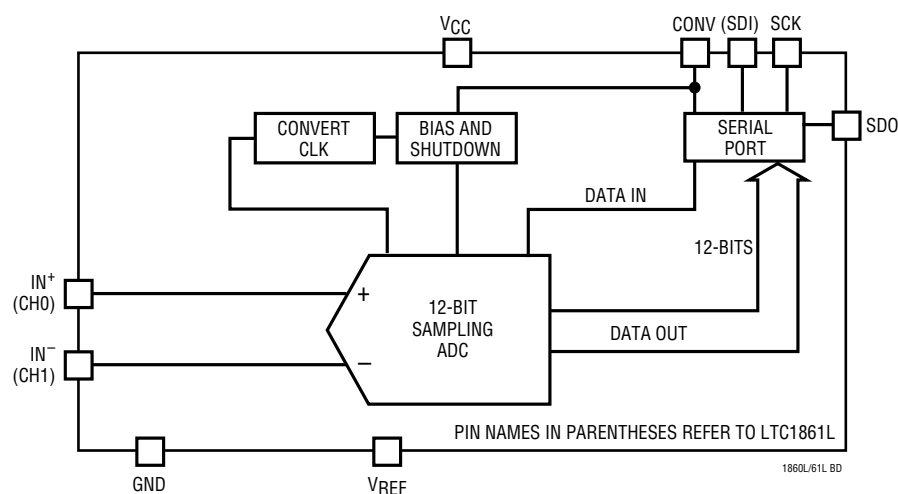
**SDI (Pin 5):** Digital Data Input. The A/D configuration word is shifted into this input.

**SDO (Pin 6):** Digital Data Output. The A/D conversion result is shifted out of this output.

**SCK (Pin 7):** Shift Clock Input. This clock synchronizes the serial data transfer.

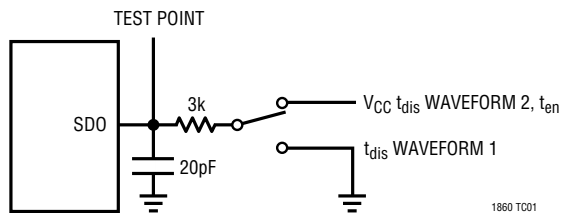
**V<sub>CC</sub> (Pin 8):** Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane. V<sub>REF</sub> is tied internally to this pin.

## FUNCTIONAL BLOCK DIAGRAM



## TEST CIRCUITS

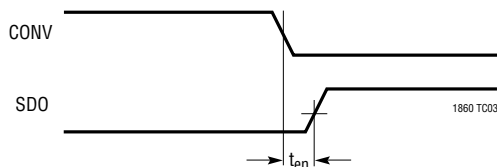
Load Circuit for  $t_{dDO}$ ,  $t_r$ ,  $t_f$ ,  $t_{dis}$  and  $t_{en}$



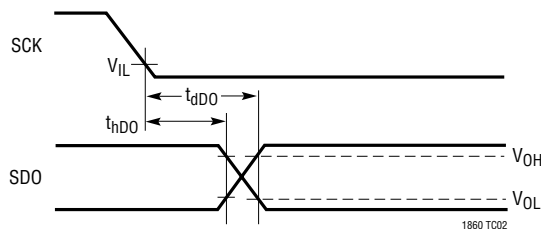
Voltage Waveforms for SDO Rise and Fall Times,  $t_r$ ,  $t_f$



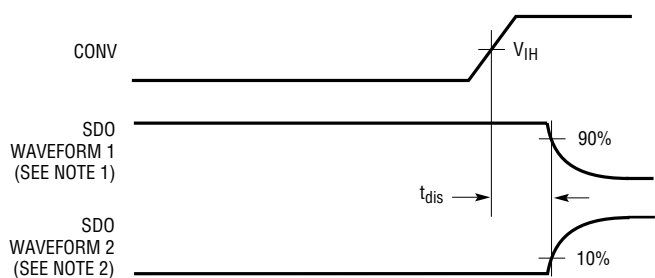
Voltage Waveforms for  $t_{en}$



Voltage Waveforms for SDO Delay Times,  $t_{dDO}$  and  $t_{hDO}$



Voltage Waveforms for  $t_{dis}$



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL

## APPLICATIONS INFORMATION

### LTC1860L OPERATION

#### Operating Sequence

The LTC1860L conversion cycle begins with the rising edge of CONV. After a period equal to  $t_{CONV}$ , the conversion is finished. If CONV is left high after this time, the LTC1860L goes into sleep mode drawing only leakage current. On the falling edge of CONV, the LTC1860L goes into sample mode and SDO is enabled. SCK synchronizes the data transfer with each bit being transmitted from SDO on the falling SCK edge. The receiving system should capture the data from SDO on the rising edge of SCK. After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 1.

#### Analog Inputs

The LTC1860L has a unipolar differential analog input. The converter will measure the voltage between the “IN+” and “IN-” inputs. A zero code will occur when IN+ minus IN- equals zero. Full scale occurs when IN+ minus IN- equals  $V_{REF}$  minus 1LSB. See Figure 2. Both the “IN+” and “IN-” inputs are sampled at the same time, so common mode noise on the inputs is rejected by the ADC. If “IN-” is grounded and  $V_{REF}$  is tied to  $V_{CC}$ , a rail-to-rail input span will result on “IN+” as shown in Figure 3.

#### Reference Input

The voltage on the reference input of the LTC1860L (and the LTC1861L MSOP package) defines the full-scale range of the A/D converter. These ADCs can operate with reference voltages from  $V_{CC}$  to 1V.



## APPLICATIONS INFORMATION

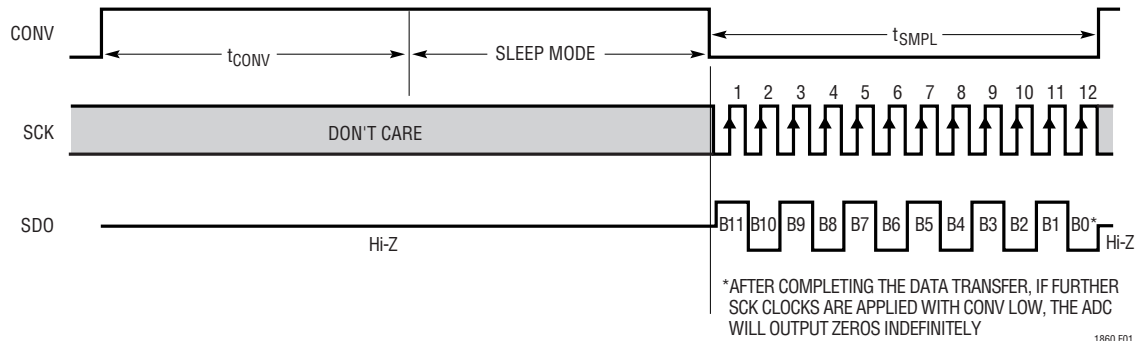


Figure 1. LTC1860L Operating Sequence

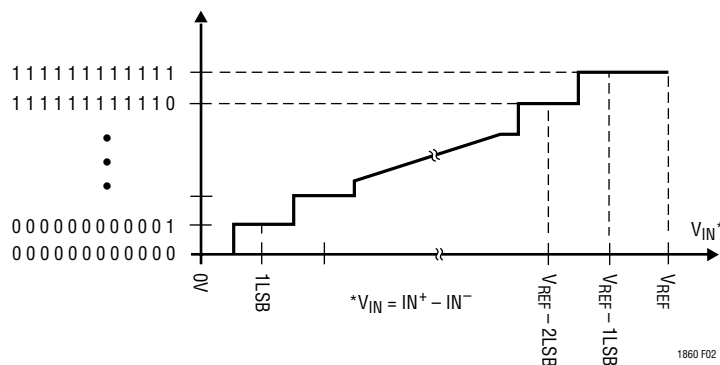


Figure 2. LTC1860L Transfer Curve

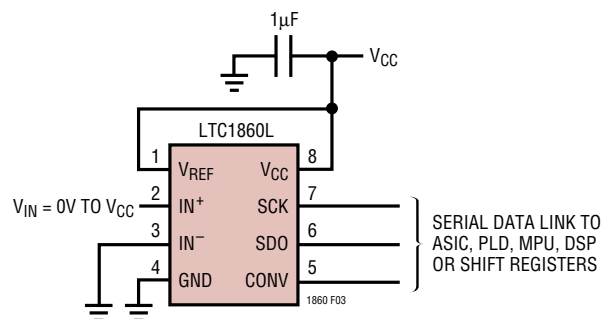


Figure 3. LTC1860L with Rail-to-Rail Input Span

## LTC1861L OPERATION

### Operating Sequence

The LTC1861L conversion cycle begins with the rising edge of CONV. After a period equal to  $t_{\text{CONV}}$ , the conversion is finished. If CONV is left high after this time, the LTC1861L goes into sleep mode. The LTC1861L's 2-bit data word is clocked into the SDO input on the rising edge of SCK after CONV goes low. Additional inputs on the SDO pin are then ignored until the next CONV cycle. The shift clock (SCK) synchronizes the data transfer with each bit being transmitted on the falling SCK edge and captured on the rising SCK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex). After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 4.

### Analog Inputs

The two bits of the input word (SDI) assign the MUX configuration for the next requested conversion. For a

given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "-" signs in the selected row of Table 1. In single-ended mode, all input channels are measured with respect to GND (or AGND). A zero code will occur when the "+" input minus the "-" input equals zero. Full scale occurs when the "+" input minus the "-" input equals  $V_{\text{REF}}$  minus 1LSB. See Figure 5. Both the "+" and "-" inputs are sampled at the same time so common mode noise is rejected. The input span in the SO-8 package is fixed at  $V_{\text{REF}} = V_{\text{CC}}$ . If the "-" input in differential mode is grounded, a rail-to-rail input span will result on the "+" input.

### Reference Input

The reference input of the LTC1861L SO-8 package is internally tied to  $V_{\text{CC}}$ . The span of the A/D converter is therefore equal to  $V_{\text{CC}}$ . The voltage on the reference input of the LTC1861L MSOP package defines the span of the A/D converter. The LTC1861L MSOP package can operate with reference voltages from 1V to  $V_{\text{CC}}$ .

APPLICATIONS INFORMATION

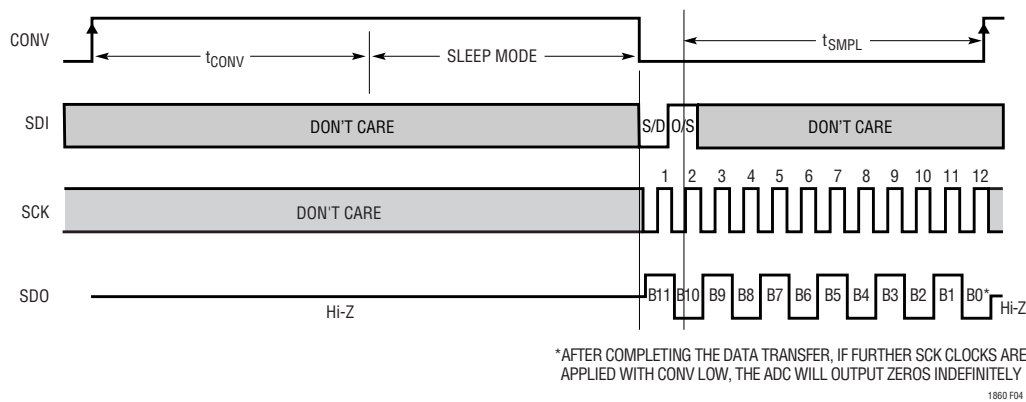


Figure 4. LTC1861L Operating Sequence

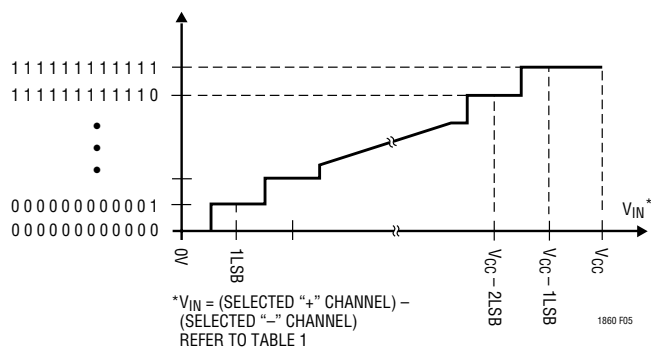


Figure 5. LTC1861L Transfer Curve

Table 1. Multiplexer Channel Selection

	MUX ADDRESS		CHANNEL #		GND
	SGL/DIFF	ODD/SIGN	0	1	
SINGLE-ENDED MUX MODE	1	0	+	–	–
	1	1		+	–
DIFFERENTIAL MUX MODE	0	0	+	–	
	0	1	–	+	

GENERAL ANALOG CONSIDERATIONS

Grounding

The LTC1860L/LTC1861L should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance, use a printed circuit board. The ground pins (AGND and DGND for the LTC1861L MSOP package and GND for the LTC1860L and LTC1861L SO-8 package) should be tied directly to the analog ground plane with minimum lead length.

Bypassing

For good performance, the  $V_{CC}$  and  $V_{REF}$  pins must be free of noise and ripple. Any changes in the  $V_{CC}/V_{REF}$  voltage with respect to ground during the conversion cycle can

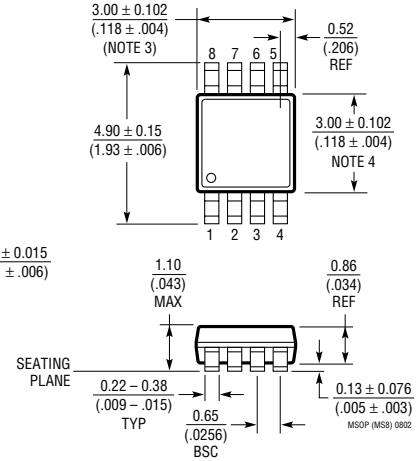
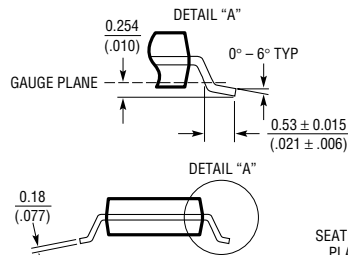
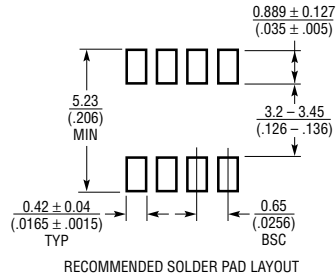
induce errors or noise in the output code. Bypass the  $V_{CC}$  and  $V_{REF}$  pins directly to the analog ground plane with a minimum of 1 $\mu$ F tantalum. Keep the bypass capacitor leads as short as possible.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1860L/LTC1861L have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem if source resistances are less than 200 $\Omega$  or high speed op amps are used (e.g., the LT<sup>®</sup>1211, LT1469, LT1807, LT1810, LT1630, LT1226 or LT1215). But if large source resistances are used, or if slow settling op amps drive the inputs, take care to ensure the transients caused by the current spikes settle completely before the conversion begins.

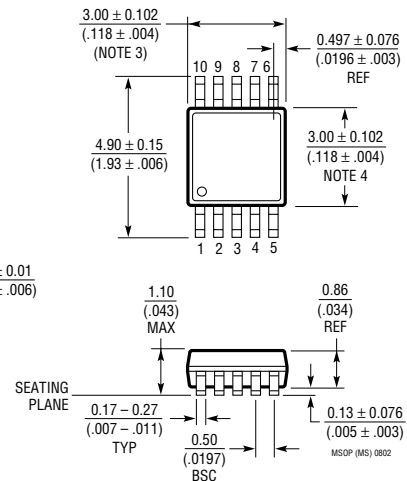
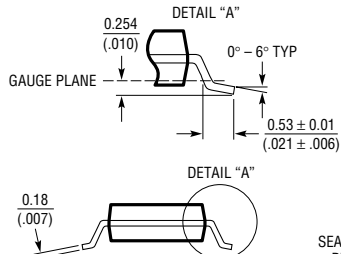
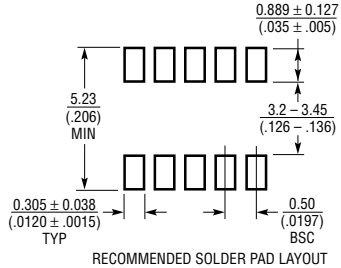
# PACKAGE DESCRIPTION

## MS8 Package 8-Lead Plastic MSOP (Reference LTC DWG # 05-08-1660)



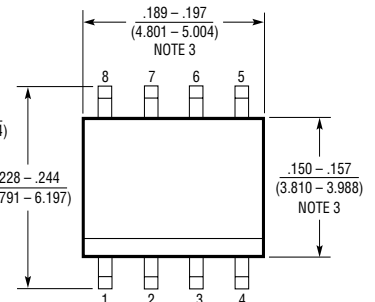
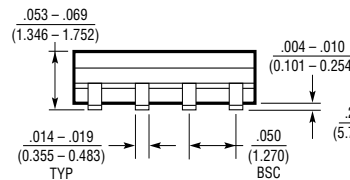
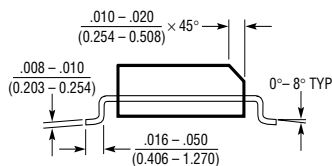
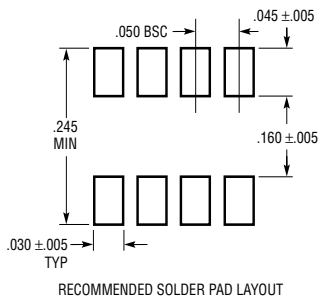
- NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
  2. DRAWING NOT TO SCALE
  3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
  4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
  5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

## MS Package 10-Lead Plastic MSOP (Reference LTC DWG # 05-08-1661)



- NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
  2. DRAWING NOT TO SCALE
  3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
  4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
  5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

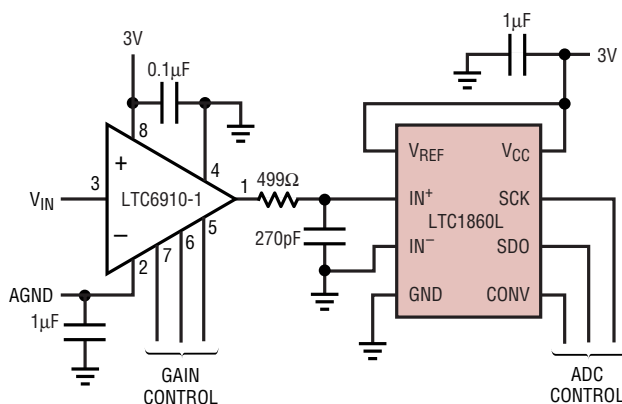
## S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



- NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
  2. DRAWING NOT TO SCALE
  3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

## TYPICAL APPLICATION

Tiny 2-Chip Data-Acquisition System



LTC6910-1 (IN TSOT-23 PACKAGE) COMPACTLY ADDS 40dB OF INPUT GAIN RANGE TO THE LTC1860L (IN MSOP 8-PIN PACKAGE). SINGLE 3V SUPPLY

1860L/61L TA03

## RELATED PARTS

PART NUMBER	SAMPLE RATE	POWER DISSIPATION	DESCRIPTION
<b>12-Bit Serial I/O ADCs</b>			
LTC1286/LTC1298	12.5ksps/11.1ksps	1.3mW/1.7mW	1-Channel with Ref. Input (LTC1286), 2-Channel (LTC1298), 5V
LTC1400	400ksps	75mW	1-Channel, Bipolar or Unipolar Operation, Internal Reference, 5V
LTC1401	200ksps	15mW	SO-8 with Internal Reference, 3V
LTC1402	2.2Msps	90mW	Serial I/O, Bipolar or Unipolar, Internal Reference
LTC1404	600ksps	25mW	SO-8 with Internal Reference, Bipolar or Unipolar, 5V
LTC1860/LTC1861	250ksps	4.25mW	SO-8, MS8, 1-Channel, 5V/SO-8, MS, 2-Channel, 5V
<b>14-Bit Serial I/O ADCs</b>			
LTC1417	400ksps	20mW	16-Pin SSOP, Unipolar or Bipolar, Reference, 5V
LTC1418	200ksps	15mW	Serial/Parallel I/O, Internal Reference, 5V
<b>16-Bit Serial I/O ADCs</b>			
LTC1609	200ksps	65mW	Configurable Bipolar or Unipolar Input Ranges, 5V
LTC1864/LTC1865	250ksps	4.25mW	SO-8, MS8, 1-Channel, 5V/SO-8, MS, 2-Channel, 5V
LTC1864L/LTC1865L	150ksps	1.22mW	SO-8, MS8, 1-Channel, 3V/SO-8, MS, 2-Channel, 3V
<b>References</b>			
LT1460	Micropower Precision Series Reference		Bandgap, 130µA Supply Current, 10ppm/°C, Available in SOT-23
LT1790	Micropower Low Dropout Reference		60µA Supply Current, 10ppm/°C, SOT-23

# AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit [www.ameya360.com](http://www.ameya360.com)

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd  
Minhang District, Shanghai , China

➤ Sales :

Direct     +86 (21) 6401-6692  
Email       amall@ameya360.com  
QQ          800077892  
Skype       ameyasales1 ameyasales2

➤ Customer Service :

Email       service@ameya360.com

➤ Partnership :

Tel          +86 (21) 64016692-8333  
Email       mkt@ameya360.com