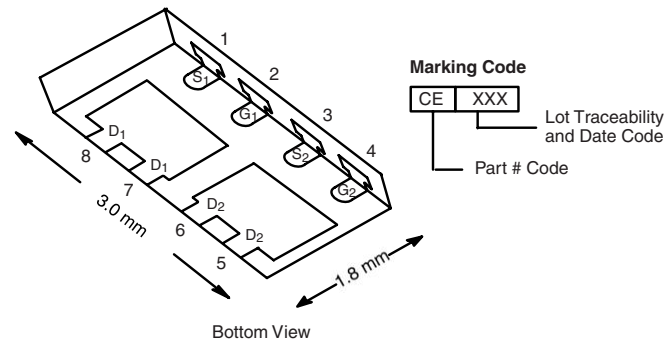


Dual N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
100	0.567 at $V_{GS} = 10$ V	2.5	2.2 nC

PowerPAK® ChipFET Dual



Ordering Information: Si5980DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

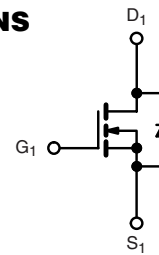
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® ChipFET® Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.8 mm Profile
- Compliant to RoHS Directive 2002/95/EC



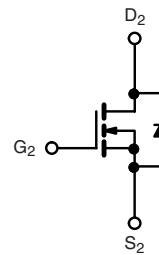
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load Supply
- Power Supply



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	2.5	A
	$T_C = 70^\circ\text{C}$	2.0	
	$T_A = 25^\circ\text{C}$	1.3 ^{b, c}	
	$T_A = 70^\circ\text{C}$	1.0 ^{b, c}	
Pulsed Drain Current	I_{DM}	3	A
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	6 ^a	A
	$T_A = 25^\circ\text{C}$	1.7 ^{b, c}	
Single Pulse Avalanche Current	I_{AS}	2	A
Avalanche Energy	E_{AS}	0.2	mJ
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	7.8	W
	$T_C = 70^\circ\text{C}$	5.0	
	$T_A = 25^\circ\text{C}$	2.0 ^{b, c}	
	$T_A = 70^\circ\text{C}$	1.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{d, e}		260	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	49	61	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	13	16	$^\circ\text{C/W}$

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 5$ s.

d. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 110°C/W .

SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		112		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 7.3		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 3 V, V _{GS} = 10 V	3			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 0.4 A		0.472	0.567	Ω
Forward Transconductance ^a	g _{fs}	V _{DS} = 20 V, I _D = 1.3 A		2		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		78		pF
Output Capacitance	C _{oss}			11		
Reverse Transfer Capacitance	C _{rss}			4		
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 1.3 A		2.2	3.3	nC
Gate-Source Charge	Q _{gs}			1.0		
Gate-Drain Charge	Q _{gd}			0.4		
Gate Resistance	R _g	f = 1 MHz	0.5	2.4	4.8	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 50 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 1 Ω		7	14	ns
Rise Time	t _r			10	20	
Turn-Off Delay Time	t _{d(off)}			7	14	
Fall Time	t _f			8	16	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 50 Ω I _D ≅ 1 A, V _{GEN} = 7.5 V, R _g = 1 Ω		8	16	
Rise Time	t _r			11	20	
Turn-Off Delay Time	t _{d(off)}			8	16	
Fall Time	t _f			9	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			6	A
Pulse Diode Forward Current	I _{SM}				3	
Body Diode Voltage	V _{SD}	I _S = 1 A, V _{GS} = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 1 A, dI/dt = 100 A/μs, T _J = 25 °C		22	33	ns
Body Diode Reverse Recovery Charge	Q _{rr}			20	30	nC
Reverse Recovery Fall Time	t _a			15		ns
Reverse Recovery Rise Time	t _b			7		

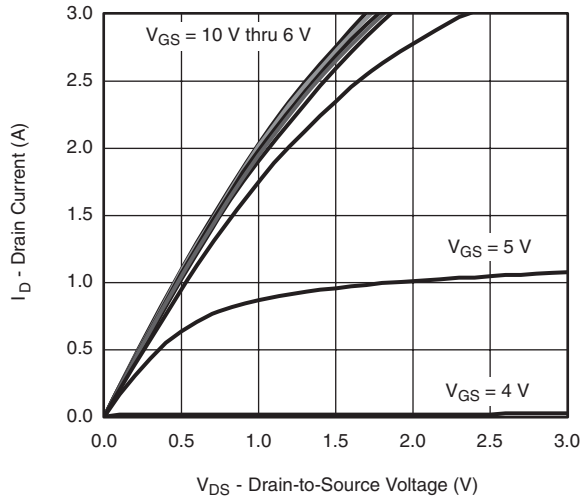
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

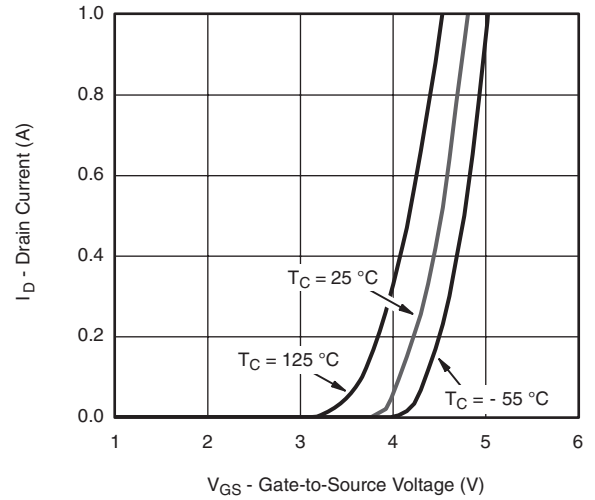
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

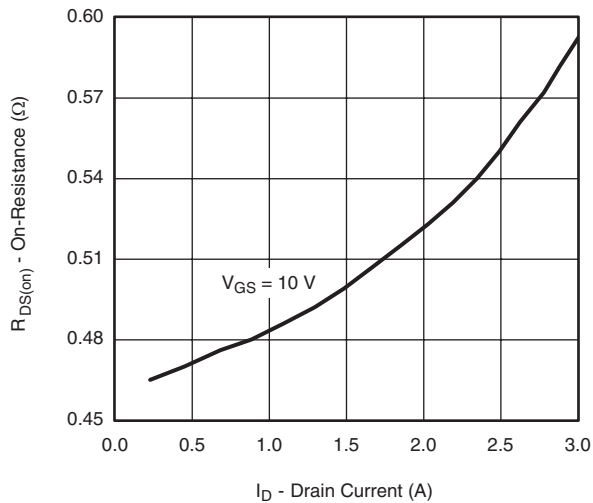
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



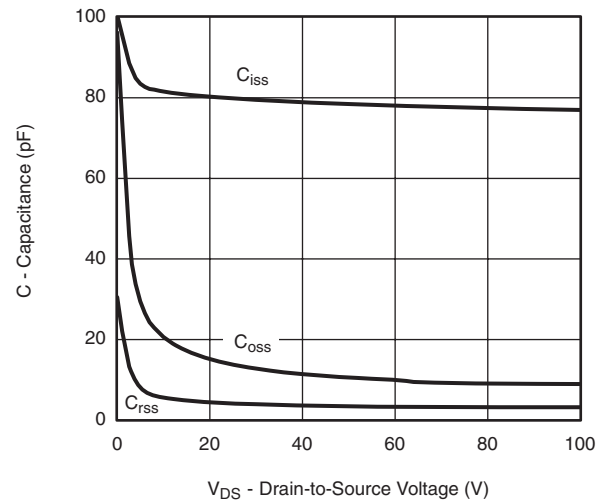
Output Characteristics



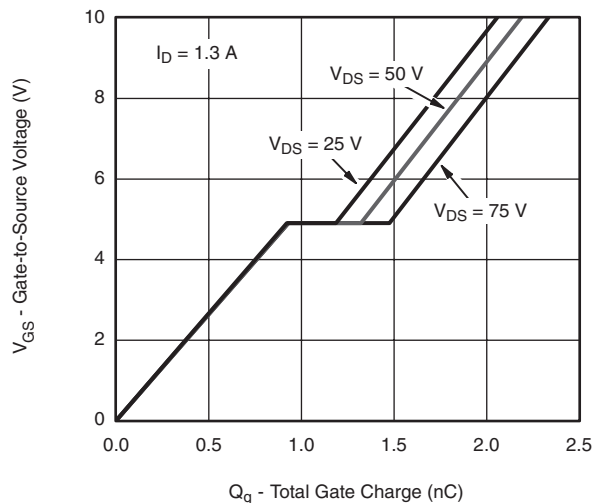
Transfer Characteristics



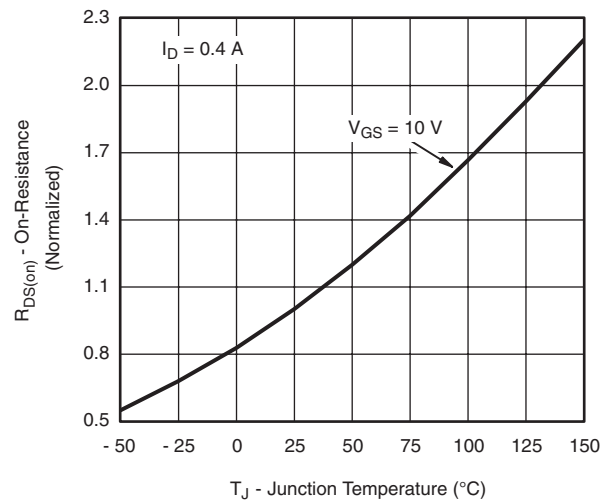
On-Resistance vs. Drain Current and Gate Voltage



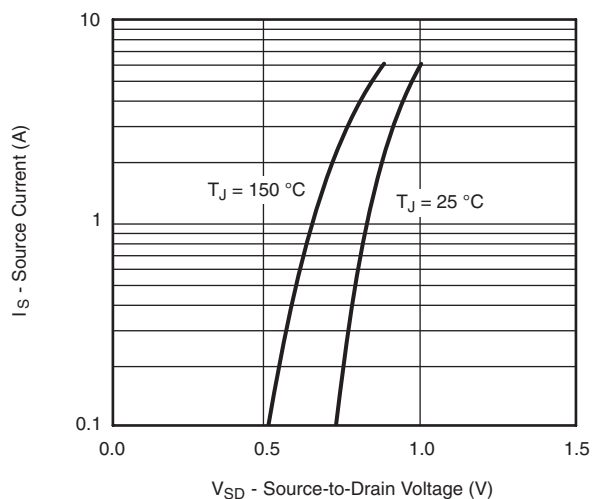
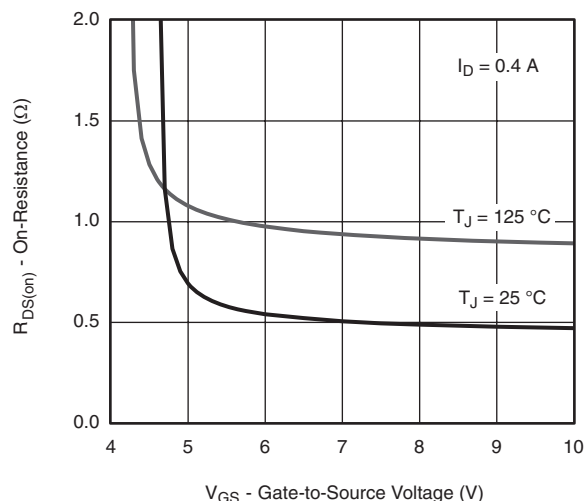
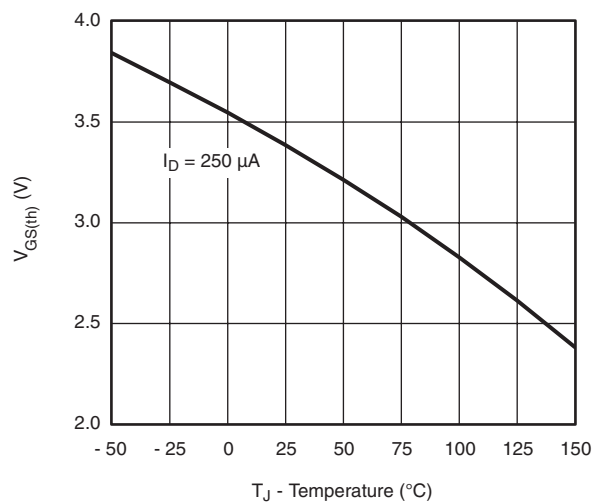
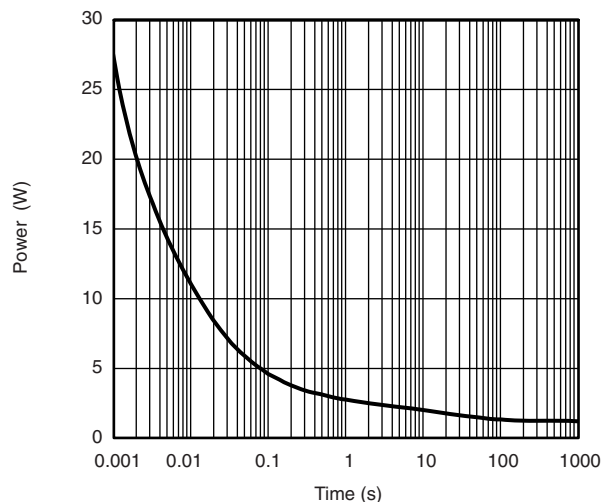
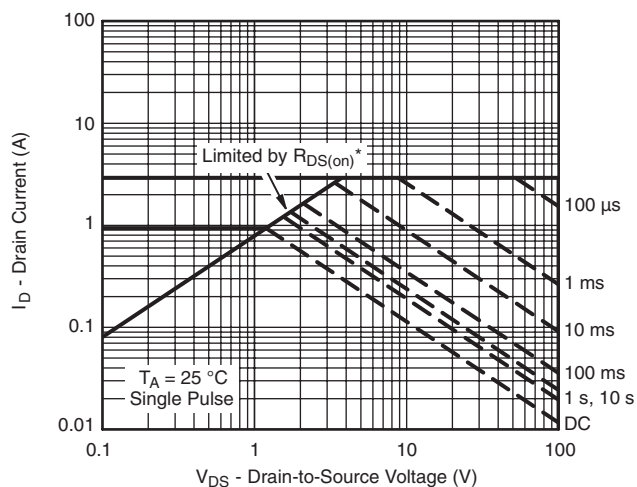
Capacitance



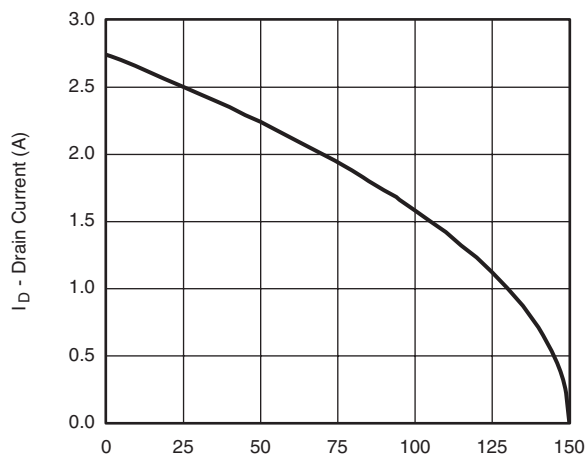
Gate Charge



On-Resistance vs. Junction Temperature

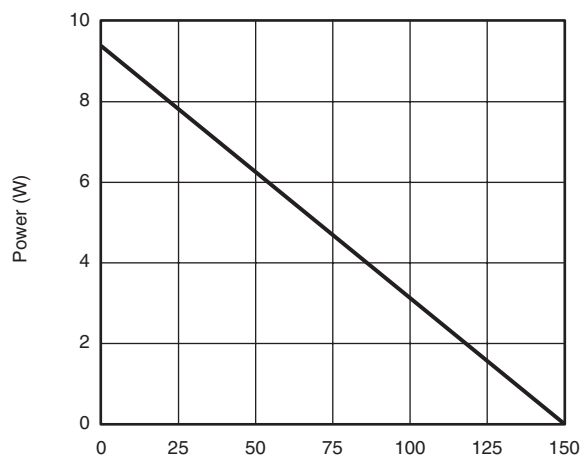
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area**

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



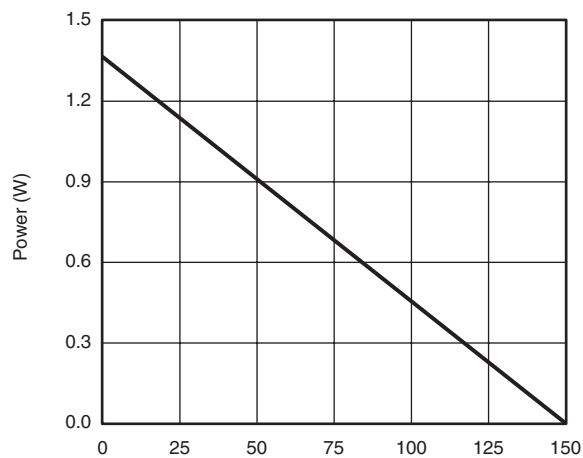
T_C - Case Temperature (°C)

Current Derating*



T_C - Case Temperature (°C)

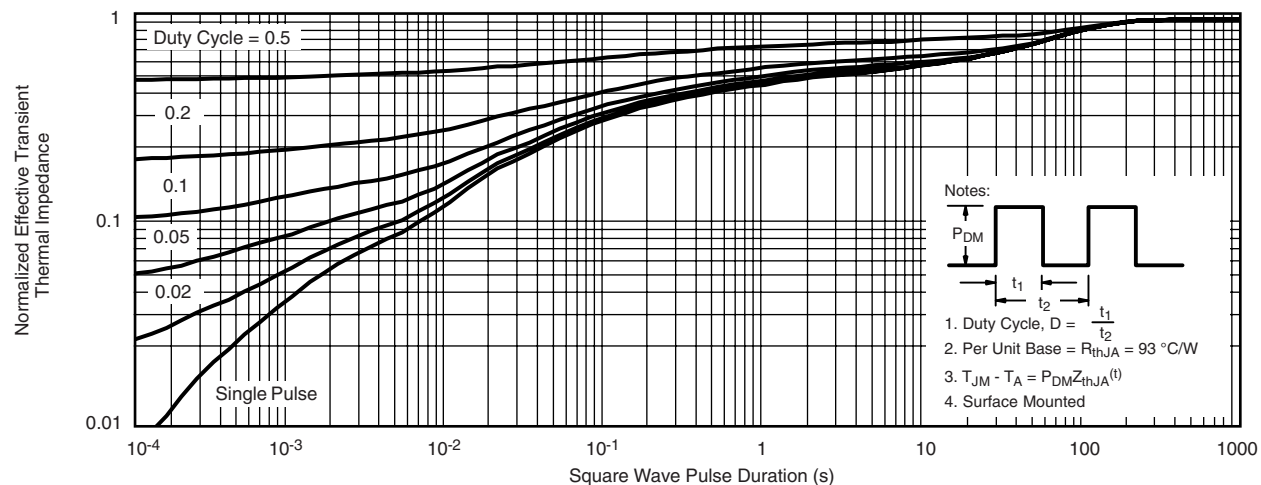
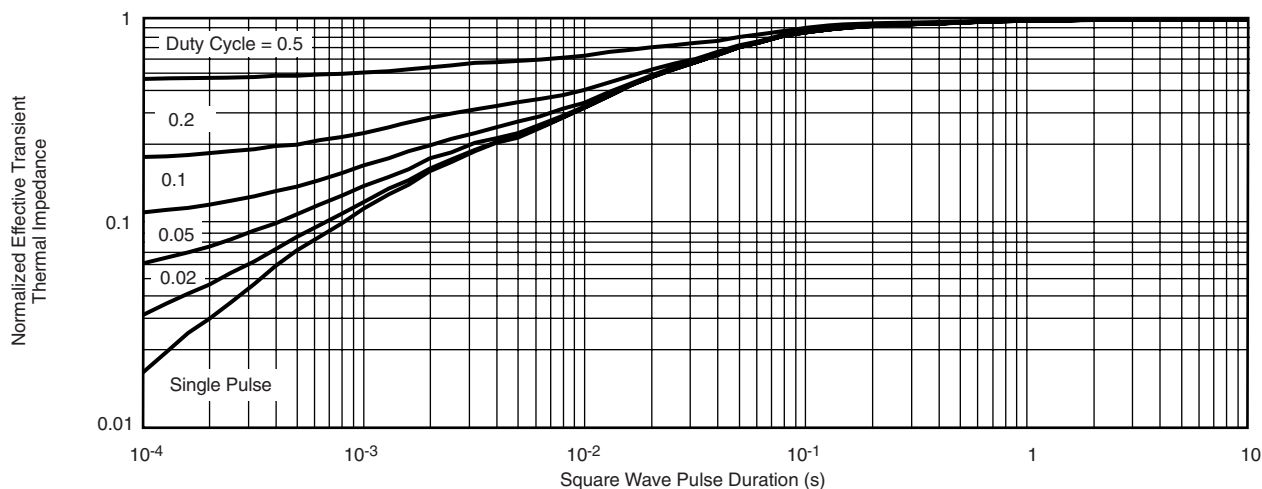
Power, Junction-to-Case



T_A - Ambient Temperature (°C)

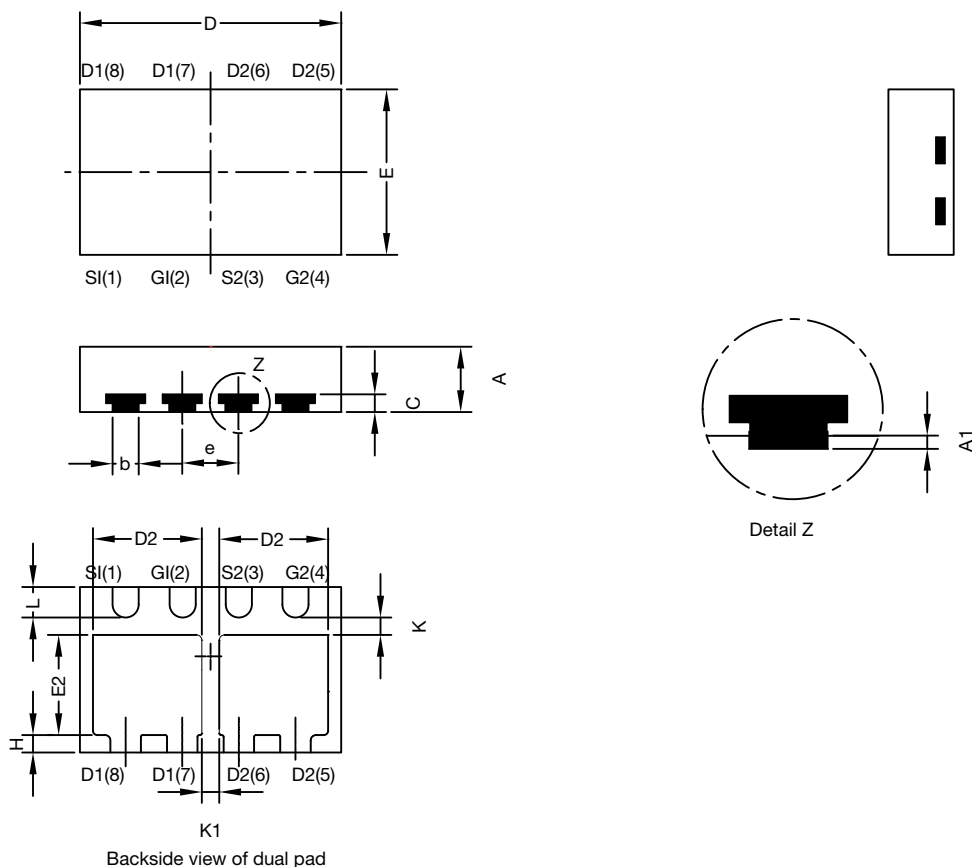
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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PowerPAK® ChipFET® Dual PAD

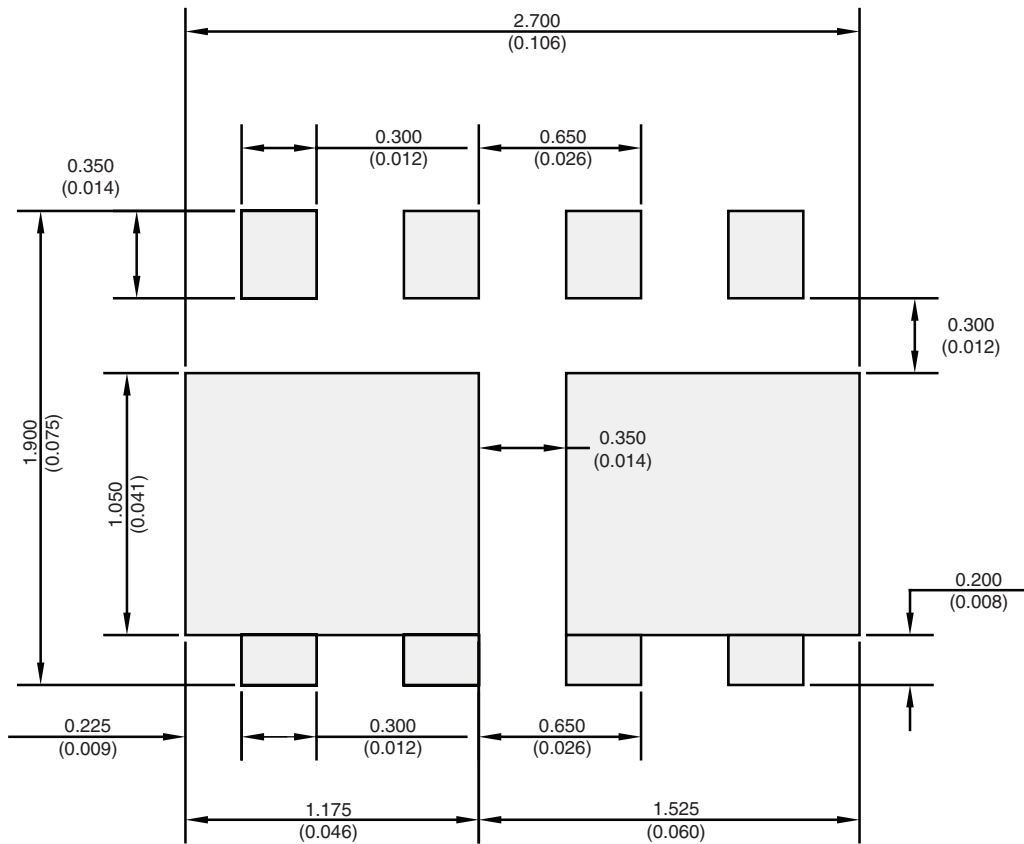


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D2	1.07	1.20	1.32	0.042	0.047	0.062
E	1.82	1.90	1.98	0.072	0.075	0.078
E2	0.92	1.05	1.17	0.036	0.041	0.046
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.20	-	-	0.008	-	-
K1	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016
C14-0307-Rev. D, 05-May-14 DWG: 5940						

Note

- Millimeters will govern

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Dual



Recommended Minimum Pads
Dimensions in mm/(Inches)

Note: This is Flipped Mirror Image
Pin #1 Location is Top Left Corner



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Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692
Email amall@ameya360.com
QQ 800077892
Skype ameyasales1 ameyasales2

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333
Email mkt@ameya360.com