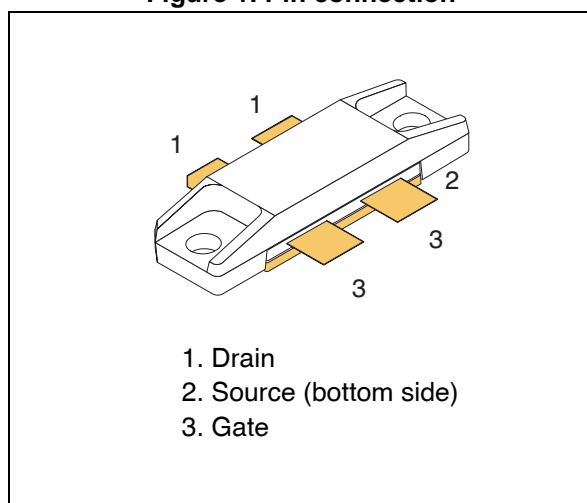


Figure 1. Pin connection



Features

- Gold metallization
- Excellent thermal stability
- Common source push-pull configuration
- $P_{OUT} = 300\text{ W min. with } 20\text{ dB gain @ } 175\text{ MHz}$
- In compliance with the 2002/95/EC European directive
- ST air cavity packaging technology - STAC™ package

Description

The STAC2932B is a gold metallized N-channel MOS field-effect RF power transistor, intended for use in 50 V DC large signal applications up to 250 MHz.

The STAC2932B benefits from the latest generation of efficient, patent-pending package technology, otherwise known as STAC™.

Table 1. Device summary

Order code	Marking	Base qty.	Package	Packaging
STAC2932BW	STAC2932 ⁽¹⁾	20	STAC244B	Tray

1. For more details please refer to [Chapter 7: Marking, packing and shipping specifications](#).

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1 Electrical data

1.1 Maximum ratings

($T_{CASE} = 25\text{ °C}$)

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}^{(1)}$	Drain source voltage	125	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 1\text{ M}\Omega$)	125	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current	40	A
P_{DISS}	Power dissipation	625	W
T_J	Max. operating junction temperature	200	°C
T_{STG}	Storage temperature	-65 to +150	°C

1. $T_J = 150\text{ °C}$

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	0.28	°C/W

2 Electrical characteristics

$T_{CASE} = +25\text{ }^{\circ}\text{C}$

2.1 Static

Table 4. Static (per side)

Symbol	Test conditions		Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$	$I_{DS} = 100\text{ mA}$	125			V
I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 50\text{ V}$			50	μA
I_{GSS}	$V_{GS} = 20\text{ V}$	$V_{DS} = 0\text{ V}$			250	nA
$V_{GS(Q)}$	$V_{DS} = 10\text{ V}$	$I_D = 250\text{ mA}$	1.5	2.5	4.0	V
$V_{DS(ON)}$	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}$			3.0	V
G_{FS}	$V_{DS} = 10\text{ V}$	$I_D = 5\text{ A}$	5			S
C_{ISS}	$V_{GS} = 0\text{ V}$ $V_{DS} = 50\text{ V}$ $f = 1\text{ MHz}$			468		pF
C_{OSS}				206		pF
$CRSS$				16		pF

2.2 Dynamic

Table 5. Dynamic

Symbol	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	$V_{DD} = 50\text{ V}$, $I_{DQ} = 2 \times 250\text{ mA}$, $P_{IN} = 4\text{ W}$, $f = 175\text{ MHz}$	300	390		W
h_D	$V_{DD} = 50\text{ V}$, $I_{DQ} = 2 \times 250\text{ mA}$, $P_{IN} = 4\text{ W}$, $f = 175\text{ MHz}$	55	68		%

3 Impedance

Figure 2. Current conventions

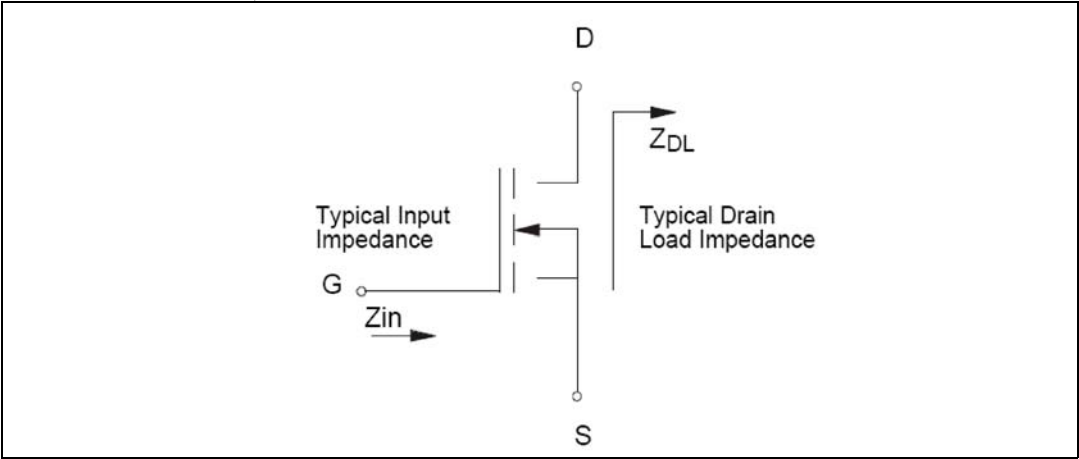


Table 6. Impedance data

Freq. (MHz)	$Z_{IN} (\Omega)$	$Z_{DL} (\Omega)$
175 MHz	$2.0 - j2.0$	$3.5 + j5.2$

Note: Measured gate to gate and drain to drain, respectively.

4 Typical performance

Figure 3. Capacitances vs drain supply voltage Figure 4. Output power vs drain supply voltage

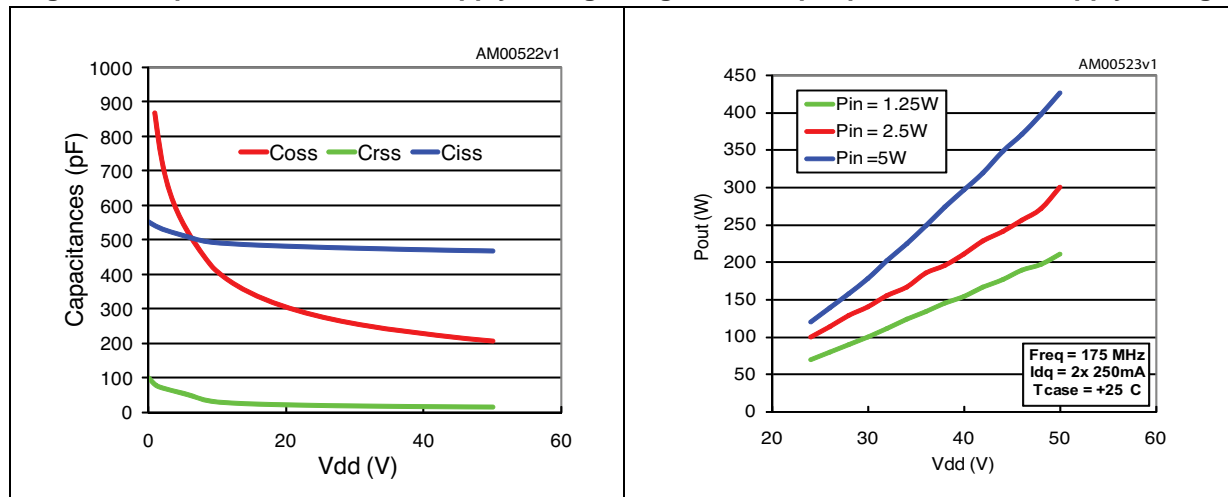


Figure 5. Output power vs gate voltage

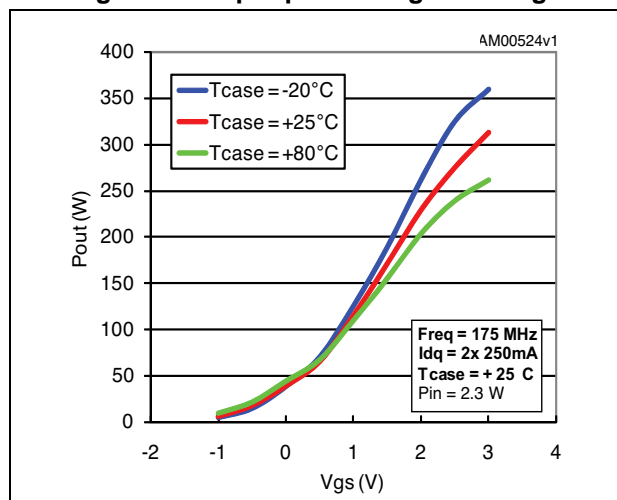


Figure 6. Output power vs input power

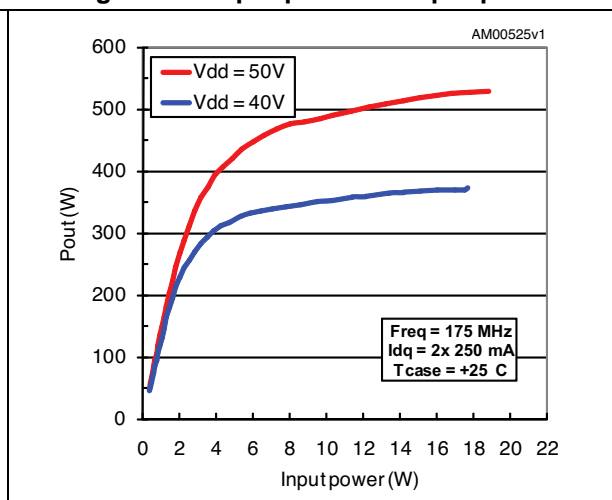


Figure 7. Output power vs input power and case temperature

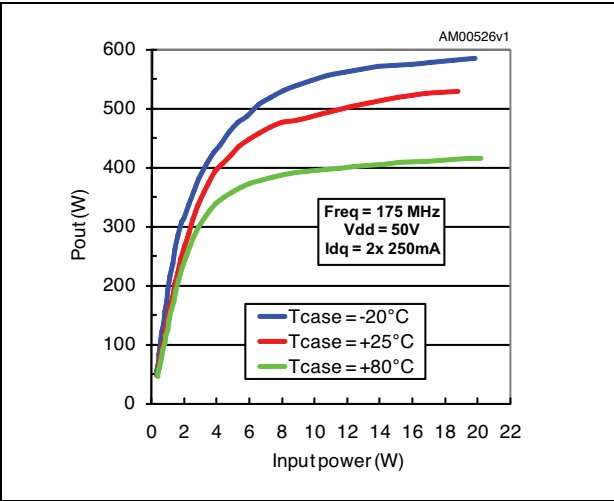
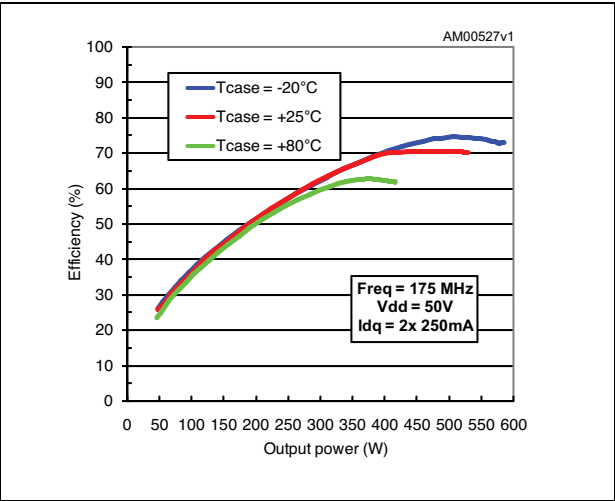


Figure 8. Efficiency vs output power and case temperature



5 Test circuit

Figure 9. 175 MHz test circuit schematic (production test circuit)

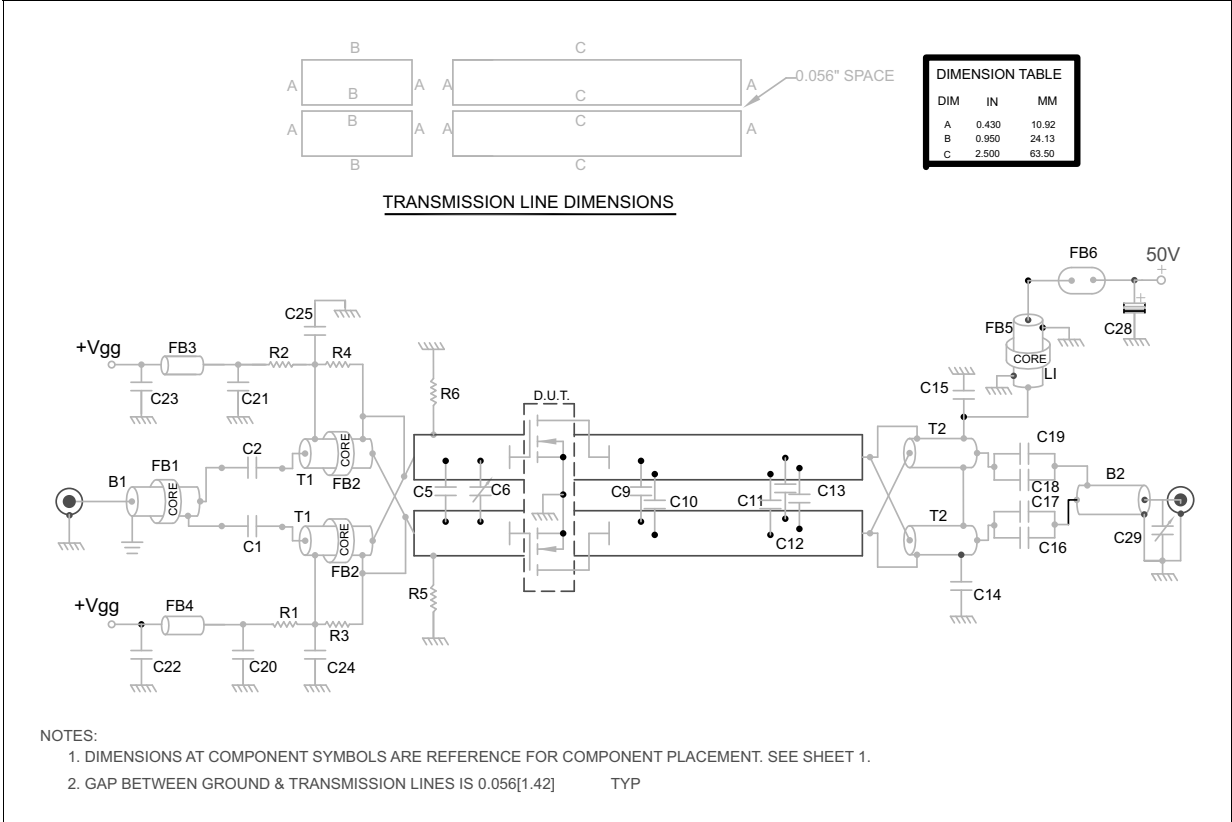


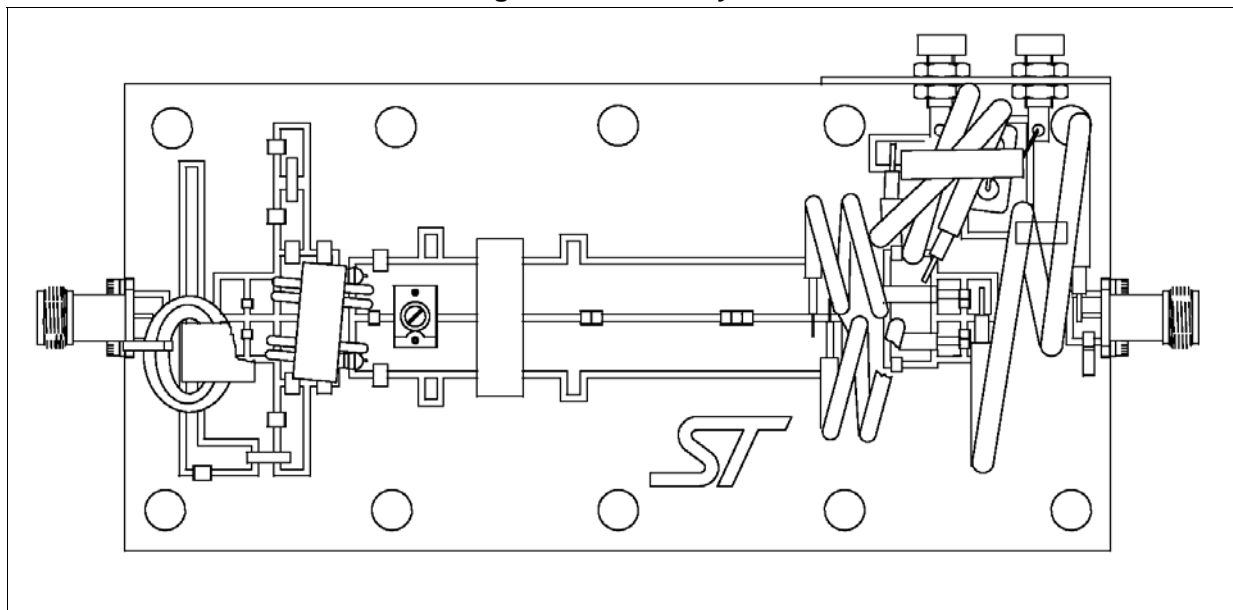
Table 7. 175 MHz test circuit part list

Component	Description
C1, C2, C14, C15, C24, C25	1200 pF ATC 700B chip capacitor
C5	75 pF ATC 100B chip capacitor
C6	ST406 variable capacitor
C9, C10	47 pF ATC 100B chip capacitor
C11, C12, C13	43 pF ATC 100B chip capacitor
C16, C18	470 pF ATC 100B chip capacitor
C17, C19, C20, C21	10,000 pF ATC 200B chip capacitor
C22, C23	0.1 μ F 200 V chip capacitor
C28	10 μ F 100 V electrolytic capacitor
C29	0.8 - 8 pF variable capacitor
R1, R2, R5, R6	430 Ω , 1/2 W chip resistor

Table 7. 175 MHz test circuit part list (continued)

Component	Description
R3, R4	270 Ω 1/2 W axial lead resistor
B1	RG-316 50 Ω 11.8" thru ferrite toroidal
B2	RG-142 50 Ω 11.8"
T1	4:1, RG-316 25 Ω , 5.9", 2 turns thru ferrite core
T2	1:4, 25 Ω semi-rigid cable, OD.141", 5.9"
L1	$\lambda/4$ inductor, RG-142 50 Ω , 11.8", 3 turns thru ferrite toroid
FB1,FB5	Ferrite toroidal
FB2, FB6	Multi-aperture core
FB3, FB4	Surface mount ferrite bead
PCB	Rogers ultralam 2000, Er 2.55, 0.060"

Figure 10. Circuit layout



6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 11. STAC244B mechanical data drawing

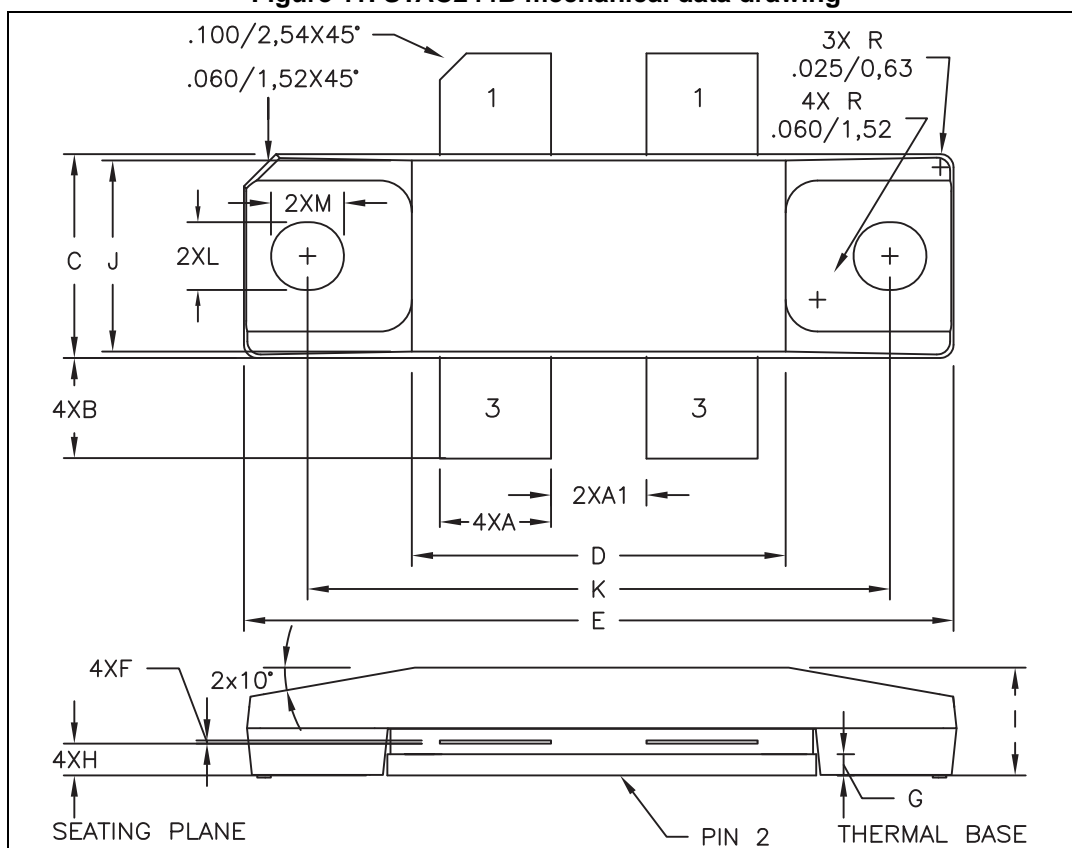


Table 8. STAC244B mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.08		5.59
A1	4.32		4.83
B	4.32		5.33
C	9.65		9.91
D	17.78		18.08
E	33.88		34.19
F	0.10		0.15
G		1.02	
H	1.45		1.70
I	4.83		5.33
J	9.27		9.52
K	27.69		28.19
L	3.12	3.23	3.33
M	3.35	3.45	3.56

7 Marking, packing and shipping specifications

Table 9. Packing and shipping specifications

Order code	Packaging	Pcs per tray	Dry pack humidity	Lot code
STAC2932BW	Tray	20	< 10 %	Not mixed

Figure 12. Marking layout

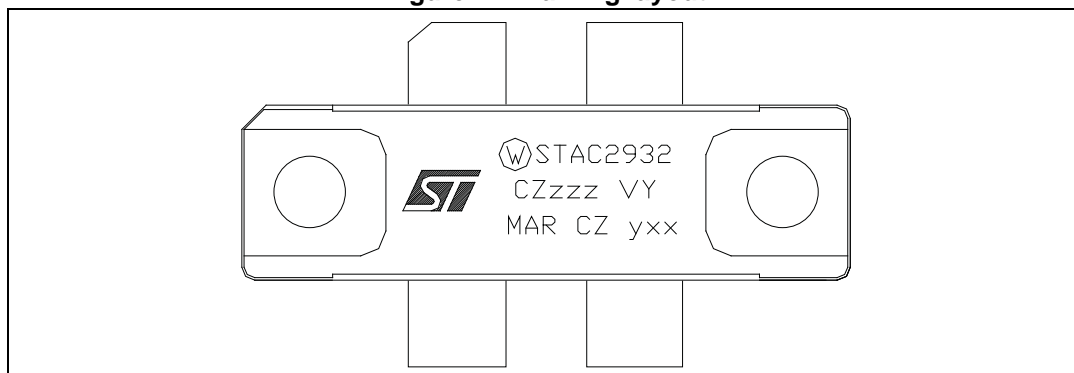


Table 10. Marking specifications

Symbol	Description
W	Wafer process code
CZ	Assembly plant
xxx	Last 3 digit of diffusion lot
VY	Diffusion plant
MAR	Country of origin
CZ	Test and finishing plant
y	Assembly year
yy	Assembly week

8 Revision history

Table 11. Document revision history

Date	Revision	Changes
20-Mar-2009	1	First release.
29-Jun-2010	2	Updated features and description on cover page.
12-Aug-2011	3	Update figures on coverpage and Section 6: Package mechanical data . Inserted Section 7: Marking, packing and shipping specifications . Minor text changes.
05-Sep-2011	4	Update L and M dimensions Table 8 on page 11 .
12-Jan-2012	5	Minor text changes to improve readability.
27-Jan-2014	6	Modified pin labeling in Figure 1: Pin connection .

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