

**PRELIMINARY**



# **WMS7201**

**256-TAP NON-VOLATILE DIGITAL POTENTIOMETER**



## **1. GENERAL DESCRIPTION**

The WMS7201 is a 256-tap, single-channel non-volatile digital potentiometer available in 10K $\Omega$ , 50K $\Omega$  and 100K $\Omega$  end-to-end resistances. These devices can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications.

The output of the potentiometer is determined by the wiper position, which varies linearly between VA and VB terminal according to the content stored in the volatile Tap Register (TR). The settings of the TR can be provided either directly by the user through the industry standard SPI interface, or by the non-volatile memory (NVMEM0~3) where the previous settings are stored. When changes are made to the TR to establish a new wiper position, the value of the setting can be saved into any non-volatile memory location (NVMEM0~3) by executing a NVMEM save operation. Upon powerup the content of the NVMEM0 is automatically loaded to the Tap Register.

The WMS7201 contains a single potentiometer in 8-pin PDIP, SOIC, MSOP or 10 pin TSSOP packages and can operate over a wide operating voltage range from 2.7V to 5.5V. A selectable output buffer is built-in for those applications where an output buffer is required.

## **2. FEATURES**

- 256 taps for the potentiometer
- End-to-end resistance available in 10K $\Omega$ , 50K $\Omega$  and 100K $\Omega$
- Selectable output buffer for each channel
- SPI Serial Interface for data transfer and potentiometer control
- Daisy-chain operation for multiple devices (10-pin TSSOP package only)
- Nonvolatile storage of four wiper positions per channel with power-on recall from NVMEM0
- Low standby current (1 $\mu$ A Max. with output buffer inactive)
- Endurance 100K typical stores per bit
- Register Data Retention 100 years
- Industrial temperature range: -40 ~ 85°C
- Wide operating voltage range: 2.7V ~ 5.5V
- Package option:
  - 8-pin MSOP, 8-pin SOIC, 8-pin PDIP, 10-pin TSSOP

The diagram illustrates the Tap Control Logic (TCL) architecture. It features a **Serial Interface** block that receives external signals: **CLK** (clock), **CS** (chip select), **SDI** (serial data input), **SDO**<sup>1</sup> (serial data output), **WP**<sup>1</sup> (write protect), and **V<sub>DD</sub>**. The **Serial Interface** is connected to an **NV Memory Control** block, which in turn manages the **NV Memory**. The **NV Memory** contains a **Power on/Preset Mem Tap** (9<sup>th</sup> bit) and **3 Addressable Preset Tap values** (each 9<sup>th</sup> bit). The **NV Memory Control** also feeds into a **Tap Register**, which is connected to a **Decoder**. The **Decoder** outputs to a 3-to-1 multiplexer (represented by a triangle with three inputs). The outputs of this multiplexer are connected to an adder/subtractor block (represented by a triangle with a '+' and '-' sign). The output of the adder/subtractor is connected to a **MUX** (multiplexer) block. The **MUX** also receives inputs from the **NV Memory** and the **Tap Register**. The final output of the **MUX** is connected to the **VA1**, **VW1**, and **VB1** pins. The **V<sub>SS</sub>** pin is also shown at the bottom right.

Note 1: Available in 10-pin TSSOP packages only.



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## 5. PIN CONFIGURATION

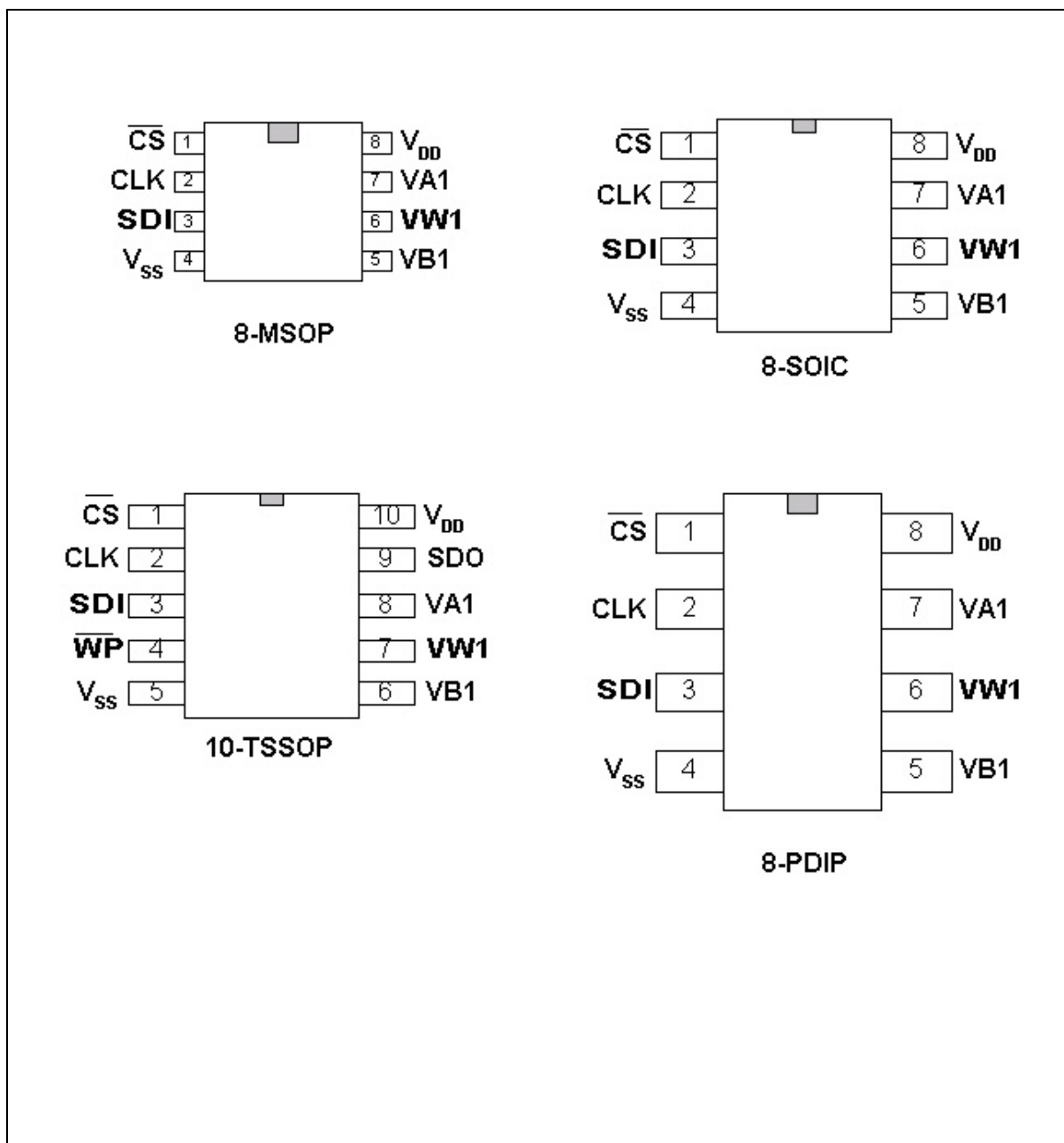


FIGURE 2 – PACKAGE TYPES



## 6. PIN DESCRIPTION

TABLE 1 – PIN DESCRIPTION

PIN NAME	PIN NO	I/O	DESCRIPTION
CLK	2	I	Serial Clock pin. Data Shifts in one bit at a time on positive clock (CLK) edges
$\overline{\text{CS}}$	1	I	Chip Select pin. When $\overline{\text{CS}}$ is HIGH, WMS7201 is deselected and the SDO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state. CS LOW enables WMS7201, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on CS is required prior to the start of any operation.
SDI	3	I	Serial Data Input pin. All opcodes, byte addresses and data to be written to the registers are input on this pin. Data is latched by the rising edge of the serial clock.
SDO <sup>1</sup>	NC	O	Serial Data Output pin with open-drain output. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock except for the 1 <sup>st</sup> bit, which is clocked out by the falling edge of CS. Also can be used to daisy-chain several parts. (Only 10-pin TSSOP package)
$\overline{\text{WP}}$ <sup>1</sup>	NC	I	Hardware Write Protect pin. When active LOW $\overline{\text{WP}}$ prevents any changes to the present contents except retrieving NVMEM contents. (Only 10-pin TSSOP package)
V <sub>DD</sub>	8	-	Power Supply
V <sub>SS</sub>	4	-	Ground pin, logic ground reference
VA1	7	-	A terminal of potentiometer '1', equivalent to the HI terminal connection on a mechanical potentiometer
VB1	5	-	B terminal of potentiometer '1', equivalent to the LO terminal connection on a mechanical potentiometer
VW1	6	O	Wiper terminal of potentiometer '1', equivalent to the wiper terminal of a mechanical potentiometer



## 7. FUNCTIONAL DESCRIPTION

The WMS7201 series, a family of 256-tap, nonvolatile digitally programmable potentiometers is designed to operate as both a potentiometer or a variable resistor depending upon the output configuration selected.

The chip can store four 9-bit words in nonvolatile memory (NVMEM0 ~ NVMEM3) and the word stored in the NVMEM0 will be used to set the tap register values when the device is powered up.

The WMS7201 is controlled by a serial SPI interface that allows setting tap register value as well as storing data in the nonvolatile memory.

### 7.1. POTENTIOMETER AND RHEOSTAT MODES

The WMS7201 can operate as either a rheostat or as a potentiometer (voltage divider). When in the potentiometer configuration there are two possible modes. One is without the output buffer and the other mode is with the output buffer. Selecting the mode is done by controlling bit D8 of the data register. D8 = 0 sets the output buffer off and D8 = 1 sets it on.

**Note that this bit can only be set by loading the value to the NVMEM with instructions #5 and then loading the TAP register with instruction #6 from NVMEM. This bit cannot be controlled by directly writing the value to the chip when the tap register is set.**

#### 7.1.1. Rheostat Configuration

The WMS7201 acts as a two terminal resistive element in the rheostat configuration where one terminal is either one of the end point pins of the resistor (VA and VB) and the other terminal is the wiper (VW) pin. This configuration controls the resistance between the two terminals and the resistance can be adjusted by sending the corresponding tap register setting commands to the WMS7201 or loading a pre-set tap register value from nonvolatile memory NVMEM0 ~ NVMEM3.

#### 7.1.2. Potentiometer Configuration

In potentiometer configuration an input voltage is connected to one of the end point pins (VA or VB). The voltage on the wiper pin will be proportional to the voltage difference between VA and VB and the wiper setting. The resistance cannot be directly measured in this configuration.

### 7.2. PROGRAMMING MODES

Two program modes are available for the WMS7201:

- **Direct program mode.** The tap register setting can be changed either by loading a predetermined value from an external microcontroller or by using the UP/DOWN command. The UP and DOWN commands change the tap register setting incrementally i.e., 1 LSB at a time. The UP and DOWN commands will not wrap around at the ends of the scale.
- **NVMEM restore mode.** One of the previously stored settings can be loaded into the TR register from the non-volatile memory. Four 9-bit non-volatile memories, are available for to store the tap register settings. The first register, NVMEM0, stores the favorite or default tap register setting that will be loaded into the tap register at system power up or software power on reset operation.



### **7.3. NON-VOLATILE MEMORY (NVMEM)**

The WMS7201 has four NVMEM positions available for storing the output buffer operating mode and the potentiometer setting. These NVMEM positions can be directly written through the SPI using a write command (#5) with address and data bytes. Another command (#7) is available that stores the current output buffer operating mode and potentiometer settings into the selected NVMEM position. Bit A3 and A2 in the instruction byte decide which NVMEM position is used. (See Table 5)

The potentiometer is loaded with the value stored in the NVMEM position 0 on power up.

#### **7.3.1 Write Protect of NVMEM**

Write-Protect ( $\overline{WP}$ ) disables any changes of current content in the NVMEM regardless of the commands, except that NVMEM setting can be retrieved using commands 4, 6 of Table 5. Therefore, Write-Protect ( $\overline{WP}$ ) pin provides hardware NVMEM protection feature with  $\overline{WP}$  tied to Vss.  $\overline{WP}$ , which is active at logic LOW, should be tied directly to  $V_{DD}$  if it is not being used. This function is only available on the 10-pin package.

### **7.4 FLOW CONTROL**

Reading and writing to NVMEM requires an internal access cycle to complete before the next command can be sent.

**Read Tap Register (#2)**

**Read NVMEM (#4)**

**Program NVMEM (#5)**

**Load Tap Register(#6)**

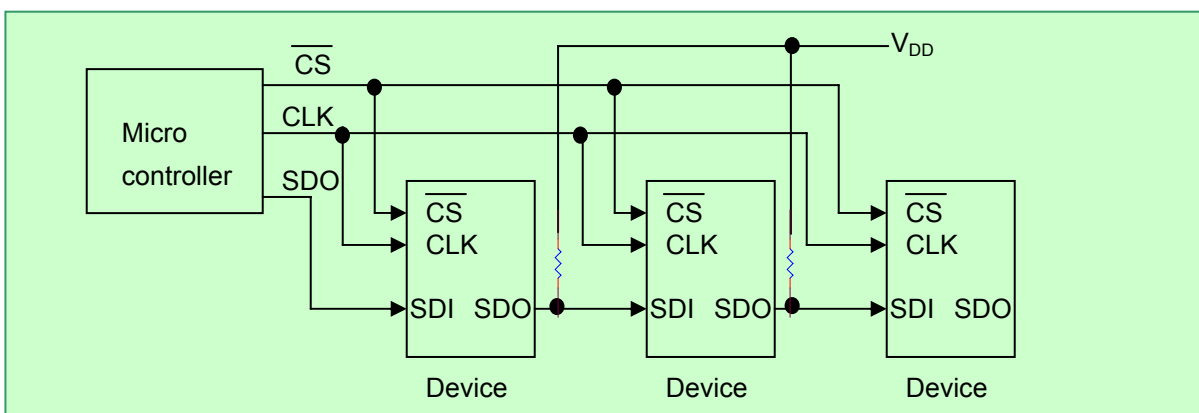
**Program NVMEM with Tap Register (#7)**





### 7.5. DAISY CHAIN

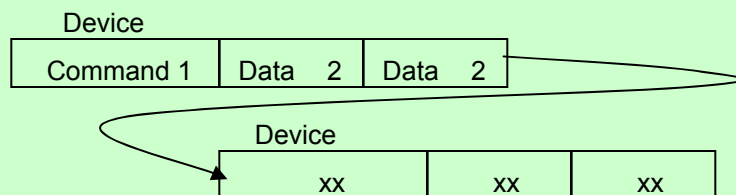
Multiple devices can be controlled by the same bus without the need for extra  $\overline{\text{CS}}$  lines from the microcontroller by daisy chaining the devices with the SDO of the first device connected to SDI of the next device as shown in figure 3 when using the 10-pin package.



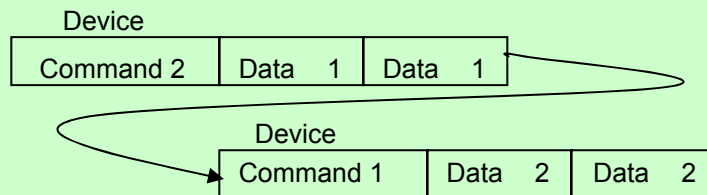
**FIGURE 3 – DAISY CHAIN CONFIGURATION [10-PIN TSSOP PACKAGE ONLY]**

A complete command is 24 bits including the instruction and the two data bytes. When shifting 24 bits in to the first device in the chain, the 24 bits of the previous command will be shifted out. So to set up two devices in a daisy chain, a total of 48 bits must be sent where the first 24 bits will be shifted out to the second device and the 24 bits shifted in last will remain in the first device.

1. Command and data for device 2 is shifted into device 1, this will propagate to Device 2 when the next 24 bits are shifted in.



2. Command and data for device 1 is shifted into device 1. Now Device 1 and 2 are correctly set up. 10-pin TSSOP package only.



**FIGURE 4 – DAISY CHAIN COMMAND EXAMPLE**



## 7.6. SERIAL DATA INTERFACE

The WMS7201 contains a four-wire SPI interface:

- **SDO** (Serial Data Output) Used for reading out the internal register contents and for daisy chaining multiple devices on the 10-pin package.
- **SDI** (Serial Data Input) Used for clocking in commands and potentiometer settings.
- **$\overline{CS}$**  (Chip Select) This pin must be pulled LOW before starting to send a command and pulled HIGH to signal the end of the command; this pin can be used to control multiple devices on the bus.
- **CLK** (Clock) The SDI bits are shifted in on the rising edge of the clock and SDO data is shifted out on the falling edge of the clock.

The key features of this interface include:

- Independently programmable Read & Write to all registers
- Direct parallel refresh of Tap register from corresponding internal NVMEM registers
- Increment and decrement instruction for Tap register
- Nonvolatile storage of the present Tap register values into one of the four NVMEM registers available.
- Configurable output buffer amplifier to allow both the functions of a potentiometer and a variable resistor
- Four 9-bit non-volatile registers store four preset wiper positions and the first one will be recalled to set the wiper position during power up.

The serial interface uses an SPI compatible uniform 24-bit word format as shown below. This format is used for all members of the WMS720x family. The data is sent MSB first.

**TABLE 2 – 24-BIT DATA WORD FORMAT**

MSB																							LSB
C3	C2	C1	C0	A3	A2	A1	A0	X	X	X	X	X	X	X	D8	D7	D6	D5	D4	D3	D2	D1	D0

C3-C0 are the command bits that control the operation of the digital potentiometer according to the command instructions shown in the Instruction Set in Table 5 in Section 7.7.

A1 and A0 are the address bits that determine which channel is activated in the WMS720x family as shown in the table below. For the WMS7201 A0 and A1 are always set to 0.



TABLE 3 – A1 AND A0 ADDRESS BIT DECODE TABLE

[A1 A0]	[0 0]	[0 1]	[1 0]	[1 1]
Channel	0	1	2	3

A3 and A2 are the address bits that decide which NVMEM memory to be accessed, as shown in the table below.

TABLE 4 – A3 AND A2 ADDRESS BIT DECODE TABLE

[A3 A2]	[0 0]	[0 1]	[1 0]	[1 1]
NVMEM	0	1	2	3

D7-D0 are the data values to be loaded into the Tap Register to set the wiper position, while D8 is used to set the output mode. D8 has to be loaded into the NVMEM0~3 first and then the “**Load Tap Register**” command (#6) has to be executed to load D8 into the output-selection MUX to set the output mode. D8=0 sets the output to Buffer Off mode while D8=1 sets to Buffer On mode.

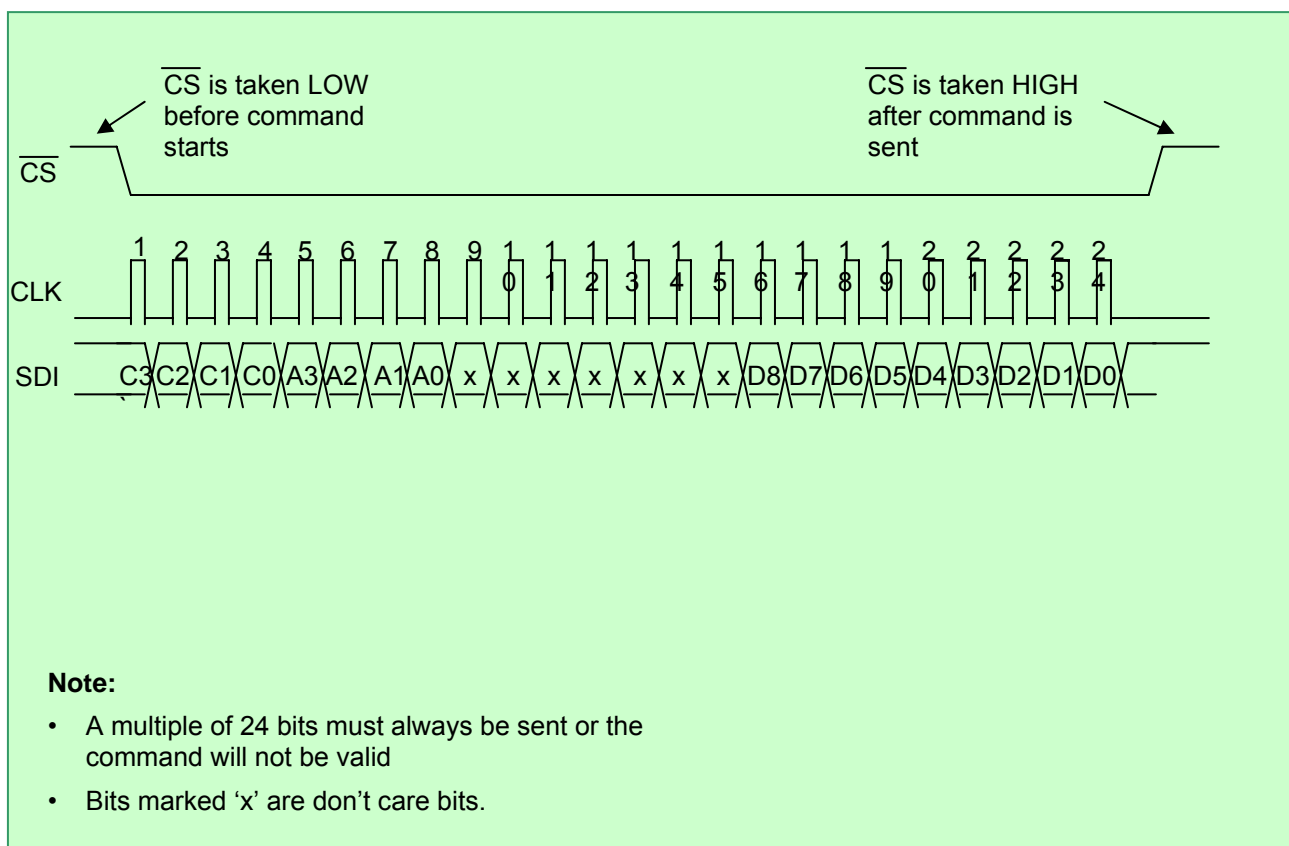


FIGURE 5 – SPI COMMAND WAVEFORMS



## 7.7. INSTRUCTION SET

TABLE 5 – INSTRUCTION SET

Inst No.	Instruction Byte C3 C2 C1 C0 A3 A2 A1 A0	Data Byte 1 D15 D14 D13 D12 D11 D10 D9 D8	Data Byte 2 D7 D6 D5 D4 D3 D2 D1 D0	Operation
1	0 0 0 0 x x x x	x x x x x x x x	x x x x x x x x	<b>No Operation (NOP).</b> Do nothing
2	1 1 0 0 x x A1 A0	x x x x x x x x	x x x x x x x x	<b>Read Tap Register</b> and output selection MUX register
3	0 1 0 0 x x A1 A0	x x x x x x x x	D7 D6 D5 D4 D3 D2 D1 D0	<b>Write to Tap Register</b> with D7-D0
4	1 0 1 0 A3 A2 A1 A0	x x x x x x x x	x x x x x x x x	<b>Read NVMEM</b> pointed to by A3-A0
5	0 0 1 0 A3 A2 A1 A0	x x x x x x x x	D7 D6 D5 D4 D3 D2 D1 D0	<b>Program NVMEM</b> pointed to by A3-A0 with D8-D0
6	1 0 1 1 A3 A2 A1 A0	x x x x x x x x	x x x x x x x x	<b>Load Tap Register</b> and output selection MUX register with the contents of NVMEM pointed to by A3-A0
7	0 0 1 1 A3 A2 A1 A0	x x x x x x x x	x x x x x x x x	<b>Program NVMEM</b> pointed to by A3-A0 with the contents of Tap Register and output selection MUX register
8	0 1 1 1 x x A1 A0	x x x x x x x x	x x x x x x x x	<b>Up:</b> Increment setting of TR by one tap
9	1 1 1 1 x x A1 A0	x x x x x x x x	x x x x x x x x	<b>Down:</b> Decrement setting of TR by one tap
10	1 0 0 0 x x x x	x x x x x x x x	x x x x x x x x	<b>Sleep:</b> Discontinue clock supply to the logic and memories
11	0 0 0 1 x x x x	x x x x x x x x	x x x x x x x x	<b>Wake Up:</b> Clock supply to the logic and memories
12	1 1 0 1 A3 A2 A1 A0	x x x x x x x x	x x x x x x x x	<b>Byte-erase NVMEM</b> pointed to by A3-A0
13	1 0 0 1 x x x x	x x x x x x x x	x x x x x x x x	<b>Power On Reset:</b> Software reset the part to the power up state

Note: C3-C0 are the command op-code; A3, A2 are the NVMEM address; A1, A0 are the channel address.

## 7.8. BASIC OPERATION

This chapter describes the sequences of commands to send to the WMS7201 and how to use the different features.

### 7.8.1 Sending a Command

1. Take the chip out of SLEEP mode.
2. Check that the write protect is set correctly if writing to NVMEM (10-pin TSSOP package only).
3. Pull the  $\overline{\text{CS}}$  pin LOW before sending data to the device.



4. 24 clock pulses are sent for each command. SDI must be valid on the rising edge of the clock, SDO is valid on the falling edge of the clock or  $\overline{CS}$ .
5. Take  $\overline{CS}$  HIGH after the command has completed
6. If command 2, 4, 5, 6 or 7 is sent, wait  $T_{SV}$  time before sending the next command.

### 7.8.2 Wake Up/Sleep/Power Commands

The chip is in SLEEP mode after:

- $V_{DD}$  is applied
- A Power on Reset command is sent
- A SLEEP command is sent

Before any operations can be performed the WAKE UP command must be sent.

When a SLEEP command is sent, the chip retains its resistor settings as long as the chip is powered up but cannot accept any other commands than a WAKE UP command.

**TABLE 6 – POWER RELATED COMMANDS**

Inst. No.	Command Name:	Command Byte	Data Byte 1	Data Byte 2	Comment
11	Wake Up	0 0 0 1 x x x x	x x x x x x x x	x x x x x x x x	Wake Up entire chip
10	Sleep	1 0 0 0 x x x x	x x x x x x x x	x x x x x x x x	Send chip into power save mode
13	Power on Reset	1 0 0 1 x x x x	x x x x x x x x	x x x x x x x x	Reset Chip
1	NOP	0 0 0 0 x x x x	x x x x x x x x	x x x x x x x x	Dummy instruction

The commands above control the entire chip.

### 7.8.3 Write to Tap Register (TR)

The microcontroller can write a value directly into the tap register or send an increment or decrement command to control the tap register. Alternatively, the contents of an NVMEM location can be written to the tap register. The only way to change the output buffer mode is to write the desired value of bit D8 into an NVMEM location and then load the corresponding NVMEM location into the tap register.



TABLE 7 – WRITING TO THE TAP REGISTERS

Inst. No.	Command Name:	Command Byte	Data Byte 1	Data Byte 2	Comment
3	Write to Tap Register	0 1 0 0 x x 0 0	x x x x x x x x	D7 D6 D5 D4 D3 D2 D1 D0	Writes a value to the tap register.
8	Up	0 1 1 1 x x 0 0	x x x x x x x x	x x x x x x x x	Increment tap register value by one
9	Down	1 1 1 1 x x 0 0	x x x x x x x x	x x x x x x x x	Decrement tap register value by one
6	Load Tap Register	1 0 1 1 A3 A2 0 0	x x x x x x x x	x x x x x x x x	Load the selected NVMEM location into the tap register

#### 7.8.4 Programming Non-Volatile Memory (NVMEM)

The value stored in the NVMEM location is 9 bits, the 8 bits (D7-D0) of the tap register plus 1 bit (D8) of the output buffer mode. The NVMEM position must be erased before writing to it. There are two ways to program a value into NVMEM.

Write a value directly from the microcontroller.

Load the current potentiometer setting into NVMEM.

TABLE 8 – PROGRAMMING NVMEM

Inst. No	Command Name	Command Byte	Data Byte 1	Data Byte 2	Comment
12	Erase NVMEM	1 1 0 1 A3 A2 0 0	x x x x x x x x	x x x x x x x x	Erases the 9 bit word pointed to by A3, A2, A1 and A0.
5	Program NVMEM	0 0 1 0 A3 A2 0 0	x x x x x x x D8	D7 D6 D5 D4 D3 D2 D1 D0	Writes a value to the NVMEM register.
7	Program NVMEM with Tap Register	0 0 1 1 A3 A2 0 0	x x x x x x x x	x x x x x x x x	Takes the current potentiometer settings and saves in the selected NVMEM location.

For programming NVMEM, the following sequence must be followed:

1. Erase word at NVMEM location
2. Program word at NVMEM location



### 7.8.5 Reading Tap Register and NVMEM Location (10-pin TSSOP package only)

The contents of the tap register or any NVMEM location can be read back through the SDO pin. When a command is sent, the data is clocked out on the falling edge of the clock. Since daisy-chain operation requires data from one command to be clocked out when the next command arrives, any read command must be followed by another command to get the correct data on the SDO pin.

**TABLE 9 – READING THE TAP REGISTER**

Inst. No.	Command Name:	Command Byte	Data Byte 1	Data Byte 2	Comment
4	Read NVMEM	1 0 1 0 A3 A2 0 0	x x x x x x x x	x x x x x x x x	Read the value of the selected NVMEM location
2	Read Tap Register	1 1 0 0 x x 0 0	x x x x x x x x	x x x x x x x x	Read the value of the selected tap register
1	NOP to Read Register	0 0 0 0 x x x x	x x x x x x x D8	D7 D6 D5 D4 D3 D2 D1 D0	Output data to SDO pin

To read the contents of either the tap register or a NVMEM location, the following sequence must be followed.

1. Send the desired read command (#2 or #4)
2. Send another command such as NOP and read the SDO pin on the falling edge of the clock. The other command could be any command, but to make sure that the chip does not change anything, send either another Read command or a NOP command (#1).



## 8. TIMING DIAGRAMS

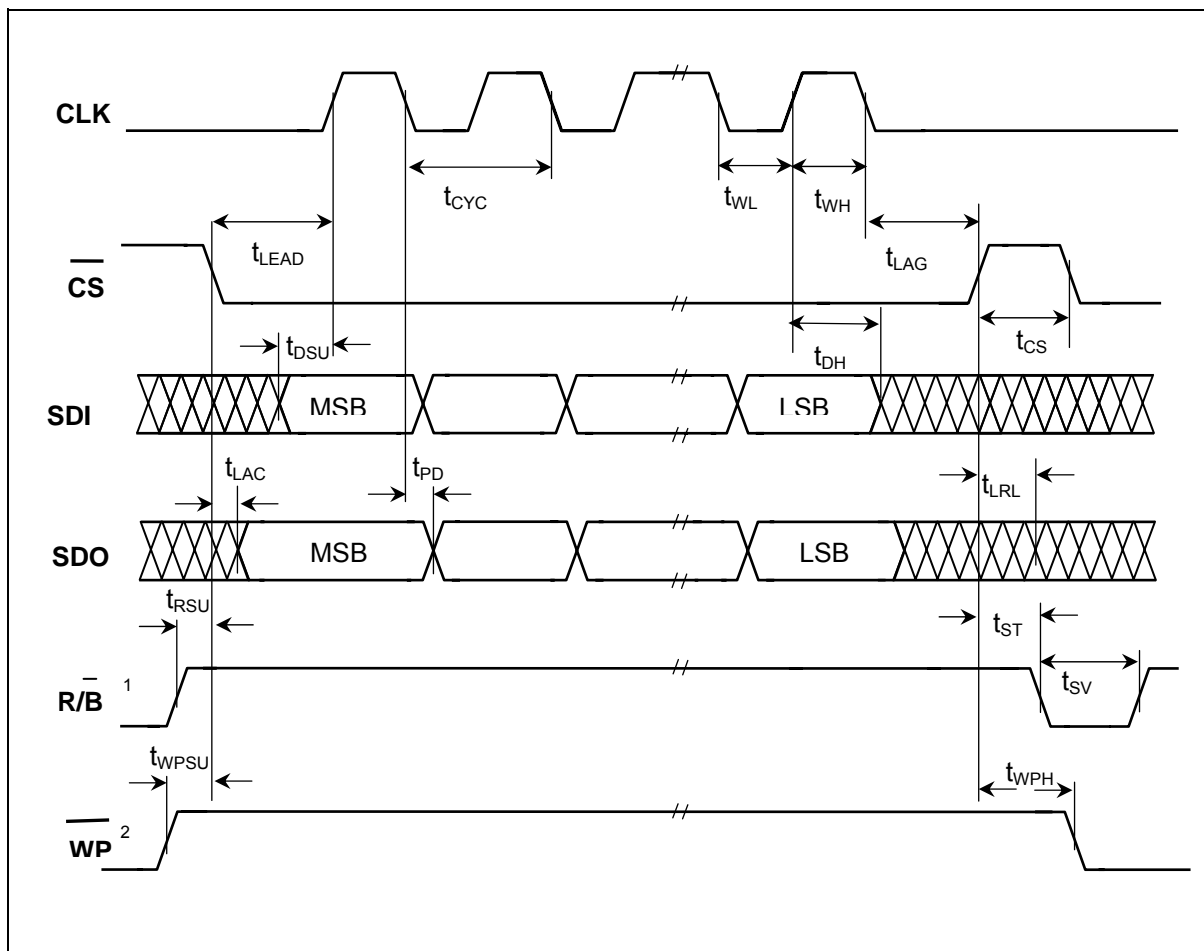


FIGURE 6 – WMS7201 TIMING DIAGRAM

Notes: (1) Internal signal only. (2) Only on 10-pin TSSOP package.





TABLE 10 – TIMING PARAMETERS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SPI Clock Cycle Time	$t_{CYC}$	100		ns
SPI Clock HIGH Time	$t_{WH}$	50		ns
SPI Clock LOW Time	$t_{WL}$	50		ns
Lead Time	$t_{LEAD}$	100		ns
Lag Time	$t_{LAG}$	100		ns
SDI Setup Time	$t_{DSU}$	20		ns
SDI Hold Time	$t_{DH}$	20		ns
$\overline{CS}$ to SDO – SPI Line Acquire <sup>1</sup>	$t_{LAC}$	5		ns
$\overline{CS}$ to SDO – SPI Line Release <sup>1</sup>	$t_{LRL}$	5		ns
CLK to SDO Propagation Delay <sup>1</sup>	$t_{PD}$	1		ns
Store to NVMEM Save Time	$t_{SV}$		2	ms
$\overline{CS}$ Deselect Time	$t_{CS}$	600		ns
Startup Time	$t_{ST}$	0.1		ms
$\overline{WP}$ Setup Time <sup>1</sup>	$t_{WPSU}$	10		ns
$\overline{WP}$ Hold Time <sup>1</sup>	$t_{WPH}$	10		ns

Note: The interface timing characteristics apply to all parts but are guaranteed by design and not subject to production test.

Note 1: 10-pin package only.



## 9. ABSOLUTE MAXIMUM RATINGS

TABLE 11 – ABSOLUTE MAXIMUM RATINGS

Condition	Value
Junction temperature	150°C
Storage temperature	-65° to +150°C
Voltage applied to any pad	(V <sub>ss</sub> – 0.3V) to (V <sub>DD</sub> + 0.3V)
V <sub>DD</sub> – V <sub>SS</sub>	-0.3 to 7.0V

Note: Exposure to conditions beyond those listed under: Absolute Maximum Ratings, may adversely affect the life and reliability of the device.



## 10. ELECTRICAL CHARACTERISTICS

TABLE 12 – ELECTRICAL CHARACTERISTICS

All Parameters apply across specified operating ranges unless noted ( $V_{DD}$ : 2.7V~5.5V; Temp:  $-40^{\circ}\text{C}$ ~ $85^{\circ}\text{C}$ )  
Typical values:  $V_{DD}$ =5V and  $T$ = $25^{\circ}\text{C}$

PARAMETER	SYMBOL	MIN.	TYP	MAX.	UNITS	CONDITIONS
<b>Rheostat Mode</b>						
Nominal Resistance	R	-20		+20	%	$T=25^{\circ}\text{C}$ , $V_W$ open
Different Non Linearity	DNL	-1	0.3	+1	LSB	
Integral Non Linearity	INL	-1	0.5	+1	LSB	
Rheostat Tempco <sup>1</sup>	$\Delta R_{AB}/\Delta T$		500		ppm/ $^{\circ}\text{C}$	
Wiper Resistance <sup>2</sup>	$R_W$		50	100	$\Omega$	$V_{DD}=5V$ , $I=V_{DD}/R_{Total}$
			80	120	$\Omega$	$V_{DD}=2.7V$ , $I=V_{DD}/R_{Total}$
<b>Potentiometer Mode</b>						
Resolution <sup>1</sup>	N	8			Bits	
Different Non Linearity <sup>2</sup>	DNL	-1		+1	LSB	
Integral Non Linearity <sup>2</sup>	INL	-1		+1	LSB	
Potentiometer Tempco <sup>1</sup>	$\Delta V_W/\Delta T$		+20		ppm/ $^{\circ}\text{C}$	Code = 80h
Full Scale Error	$V_{FSE}$	-1		0	LSB	Code = Full Scale
Zero Scale Error	$V_{ZSE}$	0		1	LSB	Code = Zero Scale
<b>Resistor Terminal</b>						
Voltage Range <sup>1</sup>	$V_A, V_B, V_W$	$V_{SS}$		$V_{DD}$	V	
Terminal Capacitance <sup>1</sup>	$C_A, C_B$		30		pF	
Wiper Capacitance <sup>1</sup>			30		pF	
<b>Dynamic Characteristics<sup>1</sup></b>						
	$BW_{10K}$		1.5		MHz	$V_{DD}=5V$ , $V_B=V_{SS}$ Code = Full Scale
Bandwidth –3dB	$BW_{50K}$		300		KHz	Code = 80h
	$BW_{100K}$		200		KHz	CL=30pf
Settling Time to 1 LSB	$T_S$		80	100	$\mu\text{s}$	$V_{DD}=5.5V=V_A$ , $V_B=V_{SS}$
<b>Analog Output (Buffer enabled)</b>						
Amp Output Current <sup>2</sup>	$I_{OUT}$	3			mA	$V_O=1/2$ scale
Amp Output Resistance <sup>2</sup>	$R_{out}$		1	10	$\Omega$	
Total Harmonic Distortion <sup>1</sup>	THD			0.08	%	$V_A=2.5V$ , $V_{DD}=5V$ , $f=1\text{kHz}$ , $V_{IN}=1V_{RMS}$
<b>Digital Inputs/Outputs</b>						
Input High Voltage	$V_{IH}$	$0.7V_{DD}$			V	
Input Low Voltage	$V_{IL}$			$0.3V_{DD}$	V	
Output Low Voltage	$V_{OL}$			0.4	V	$I_{OL}=2\text{mA}$
Input Leakage Current	$I_{LI}$	-1		+1	$\mu\text{A}$	$CS = V_{DD}$ , $V_{in}=V_{SS}$

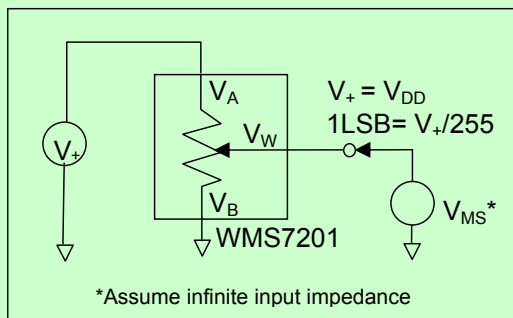


Output Leakage Current	$I_{LO}$	-1		+1	uA	$\sim V_{DD}$ $\overline{CS}=V_{DD}, Vin=V_{SS}$ $\sim V_{DD}$
Input Capacitance <sup>1</sup>	$C_{IN}$		25		pF	$V_{DD}=5V, fc = 1Mhz$ Code = 80h
Output Capacitance <sup>1</sup>	$C_{OUT}$		25		pF	$V_{DD}=5V, fc = 1Mhz$ Code = 80h
<b>Power Requirements</b>						
Operating Voltage <sup>1</sup>	$V_{DD}$	2.7		5.5	V	
Operating Current	$I_{DDR}$		1	1.8	mA	All ops except NVMEM program
Operating Current	$I_{DDW}$		1	2	mA	During Non- volatile memory program
Standby Current	$I_{SA}$	0.5		1	mA	Buffer is active, , no load
	$I_{SB}^2$		0.1	1	uA	Buffer is inactive, Power Down, No load
Power Supply Rejection Ratio	PSRR			1	LSB/V	$V_{DD}=5V\pm 10\%$ , Code=80h

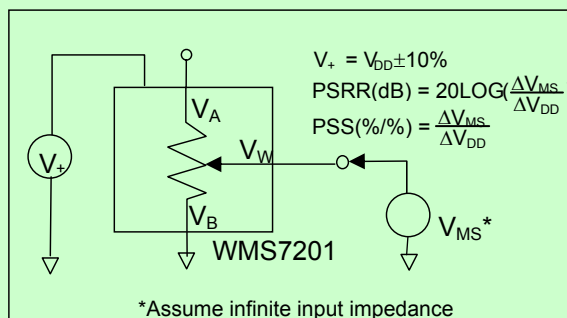
Note: 1. Not subject to production test; 2. Only on Final Test; 3.  $V_{DD} = +2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T = 25^{\circ}C$ , unless otherwise noted.



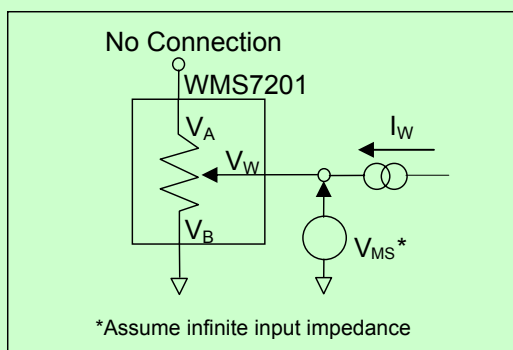
## 10.1 TEST CIRCUITS



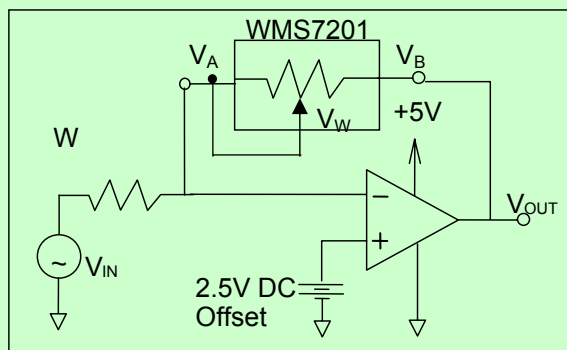
Potentiometer divider nonlinearity error test circuit (INL, DNL)



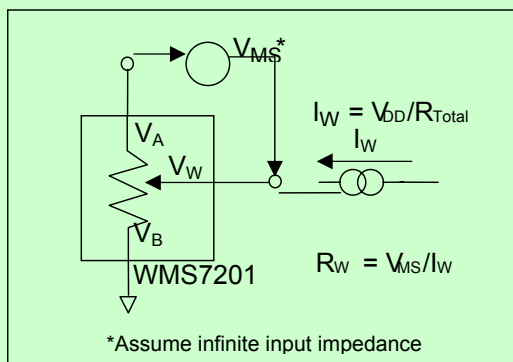
Power supply sensitivity test circuit (PSS, PSRR)



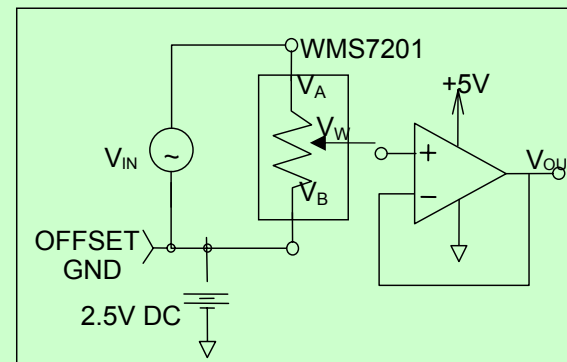
Resistor position nonlinearity error test circuit (Rheostat Operation: R-INL, R-DNL)



Capacitance test circuit



Wiper resistance test circuit



Gain vs. frequency test circuit

FIGURE 7 – TEST CIRCUITS



## 11. TYPICAL APPLICATION CIRCUIT

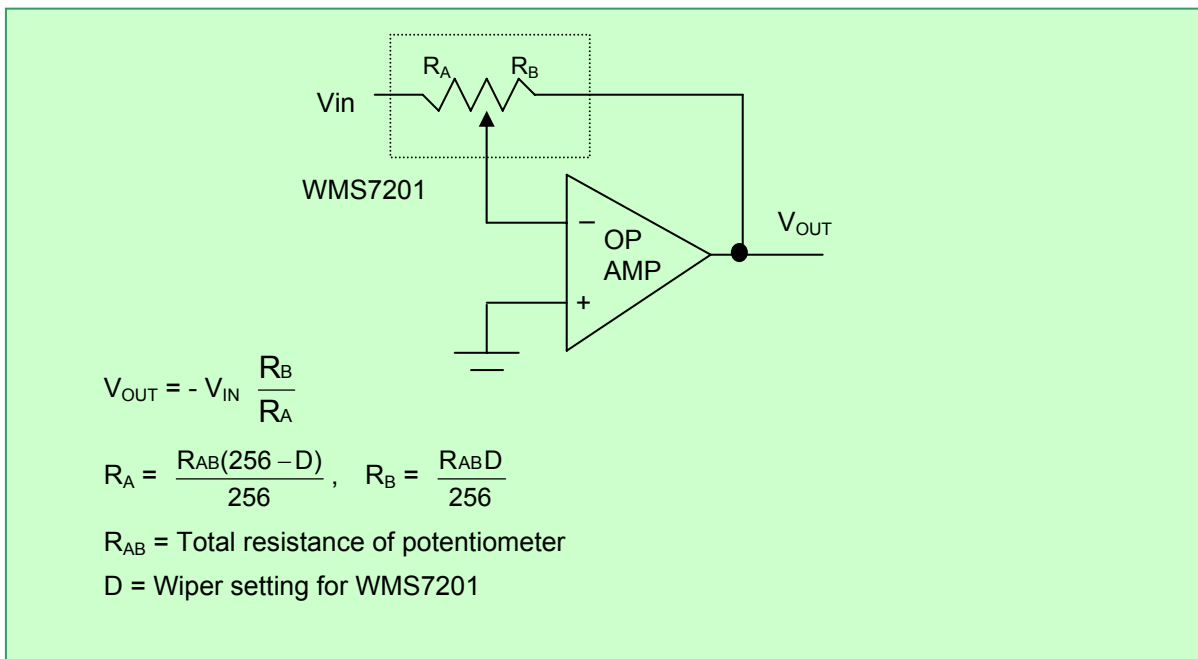


FIGURE 8 – PROGRAMMABLE INVERTING GAIN AMPLIFIER USING THE WMS7201

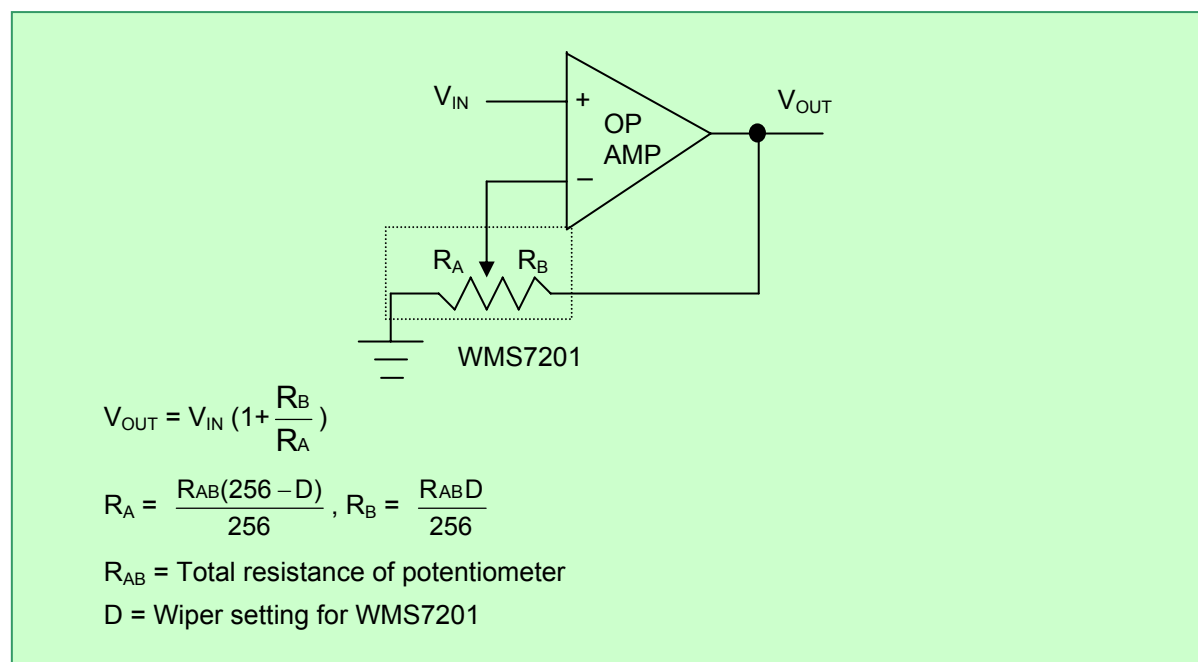
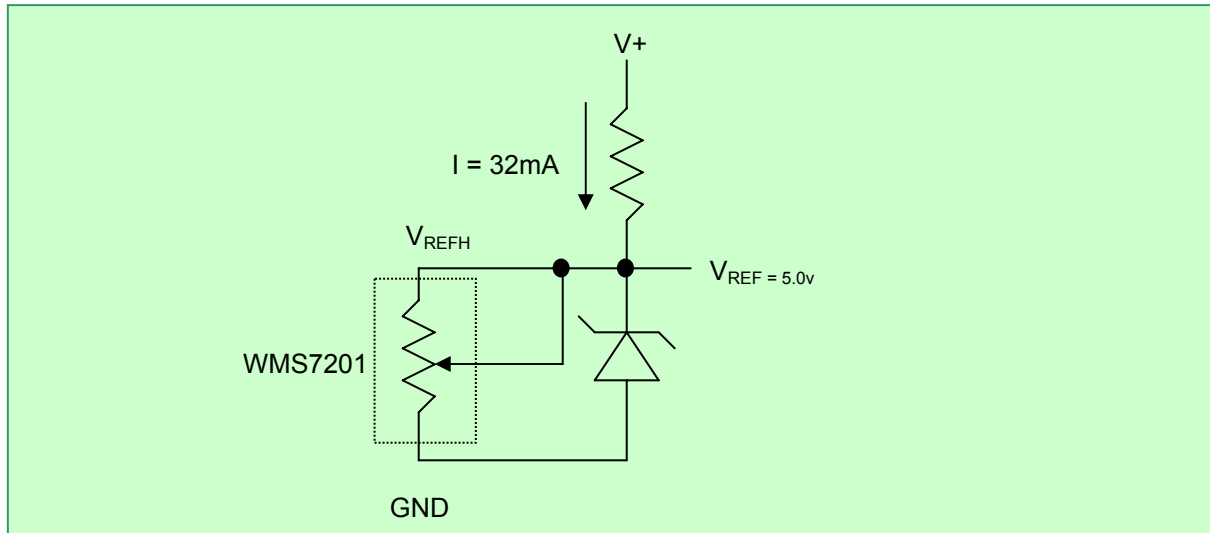
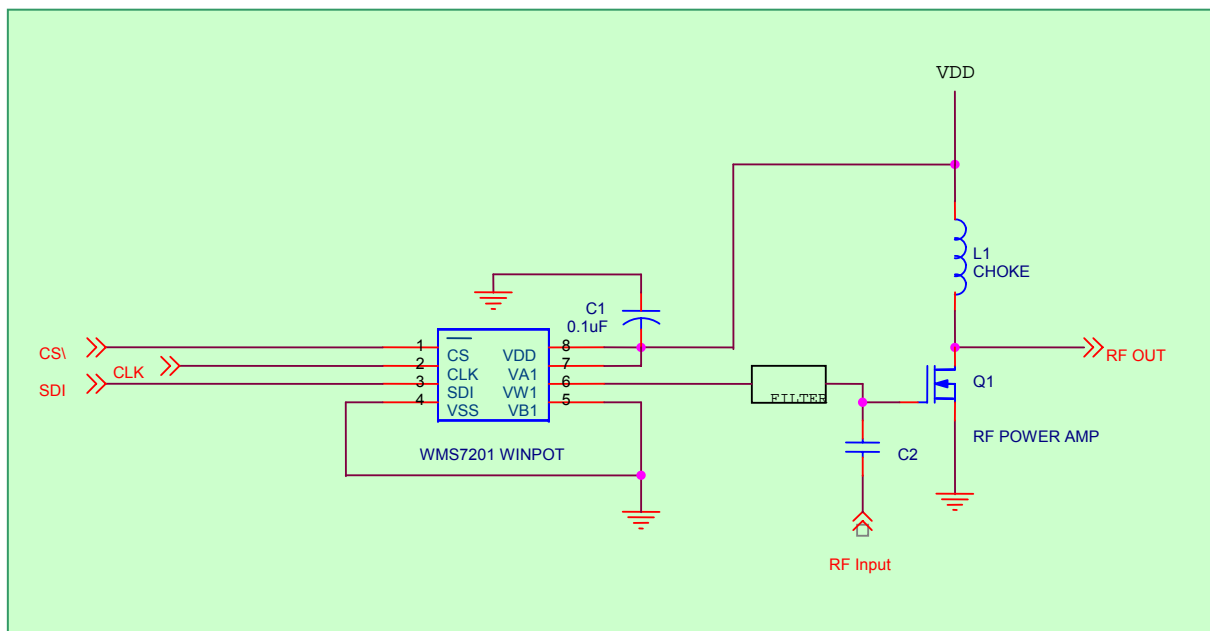


FIGURE 9 – PROGRAMMABLE NON-INVERTING GAIN AMPLIFIER USING THE WMS7201



**FIGURE 10 – WMS7201 TRIMMING VOLTAGE REFERENCE**



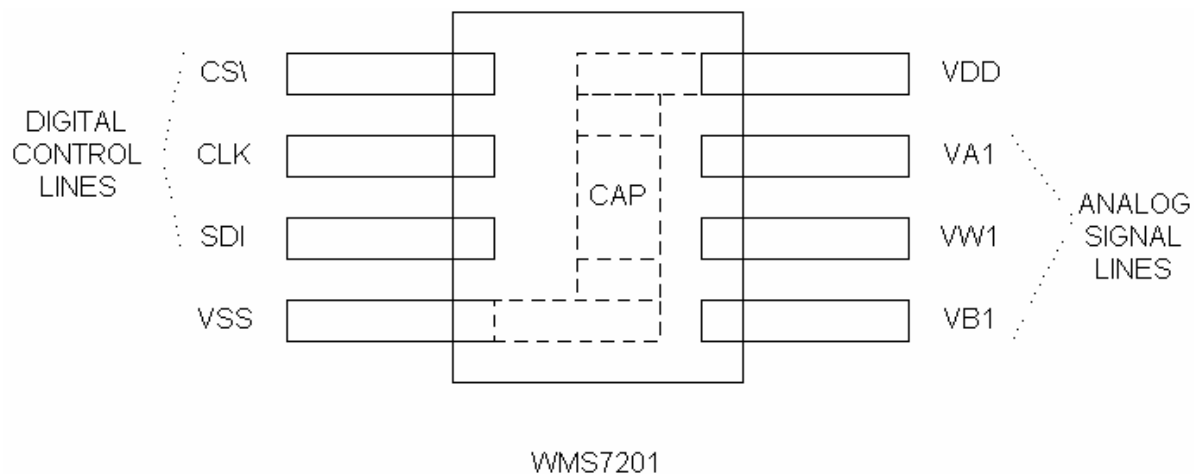
**FIGURE 11 – WMS7201 RF AMP CONTROL**



### 11.1. LAYOUT CONSIDERATIONS

A 0.1 $\mu$ F bypass capacitor as close as possible to the V<sub>DD</sub> pin is recommended for best performance. Often this can be done by placing the surface mount capacitor on the bottom side of the PC board, directly between the V<sub>DD</sub> and V<sub>SS</sub> pins. Care should be taken to separate the analog and digital traces. Sensitive traces should not run under the device or close to the bypass capacitors.

A dedicated plane for analog ground helps in reducing ground noise for sensitive analog signals.

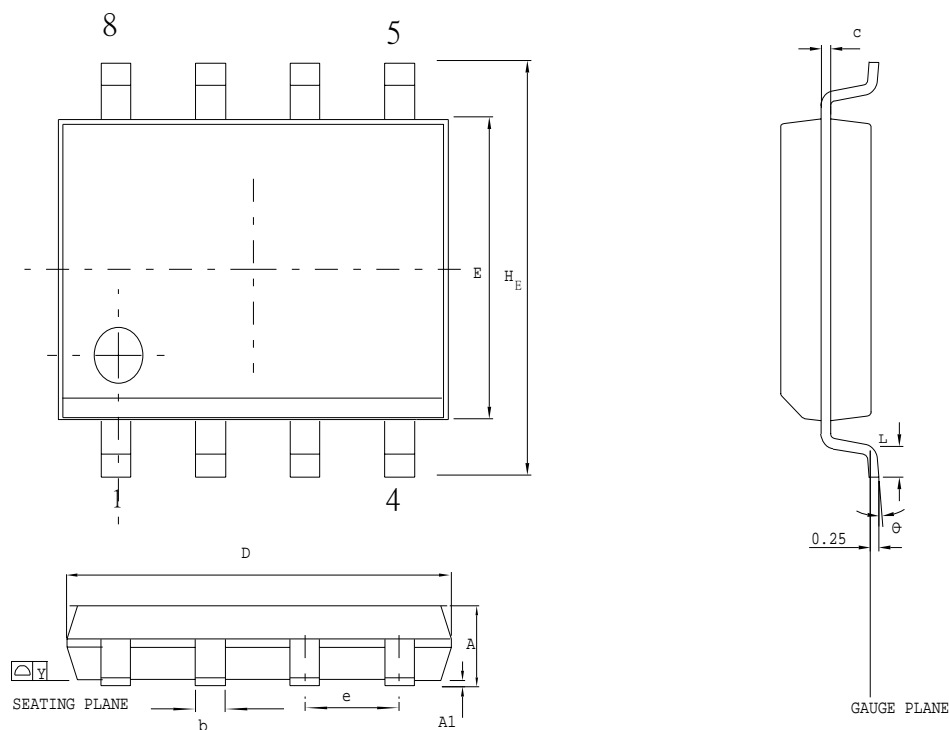


**FIGURE 12 – WMS7201 LAYOUT**





## 12. PACKAGE DRAWINGS AND DEMINSIONS



Control demensions are in milimeters .



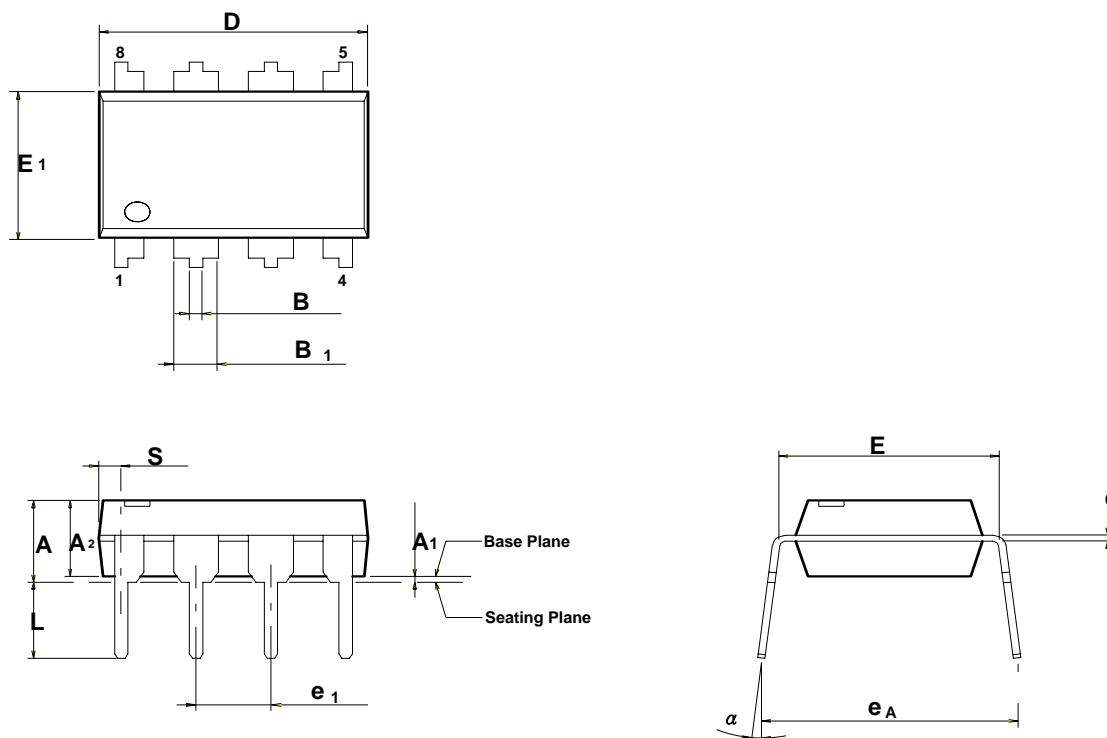
SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
E	3.80	4.00	0.150	0.157
D	4.80	5.00	0.188	0.196
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	5.80	6.20	0.228	0.244
Y		0.10		0.004
L	0.40	1.27	0.016	0.050
$\theta$	0	10	0	10

FIGURE 13 – 8L SOIC – 150MIL



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
<b>A</b>	—	—	0.175	—	—	4.45
<b>A<sub>1</sub></b>	0.010	—	—	0.25	—	—
<b>A<sub>2</sub></b>	0.125	0.130	0.135	3.18	3.30	3.43
<b>B</b>	0.016	0.018	0.022	0.41	0.46	0.56
<b>B<sub>1</sub></b>	0.058	0.060	0.064	1.47	1.52	1.63
<b>c</b>	0.008	0.010	0.014	0.20	0.25	0.36
<b>D</b>	—	0.360	0.380	—	9.14	9.65
<b>E</b>	0.290	0.300	0.310	7.37	7.62	7.87
<b>E<sub>1</sub></b>	0.245	0.250	0.255	6.22	6.35	6.48
<b>e<sub>1</sub></b>	0.090	0.100	0.110	2.29	2.54	2.79
<b>L</b>	0.120	0.130	0.140	3.05	3.30	3.56
<b><math>\alpha</math></b>	0	—	15	0	—	15
<b>e<sub>A</sub></b>	0.335	0.355	0.375	8.51	9.02	9.53
<b>S</b>	—	—	0.045	—	—	1.14

FIGURE 14 – 8L PDIP

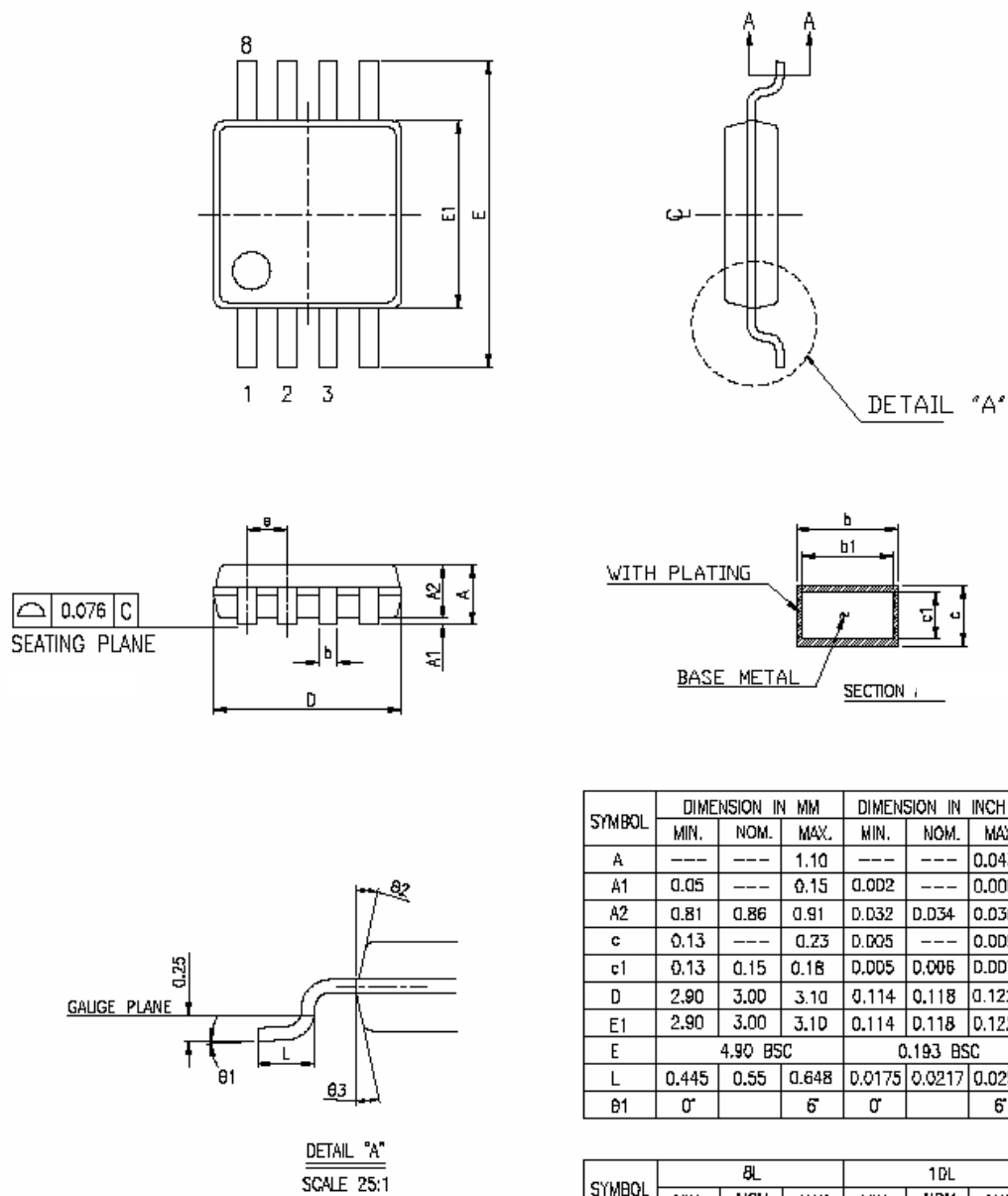
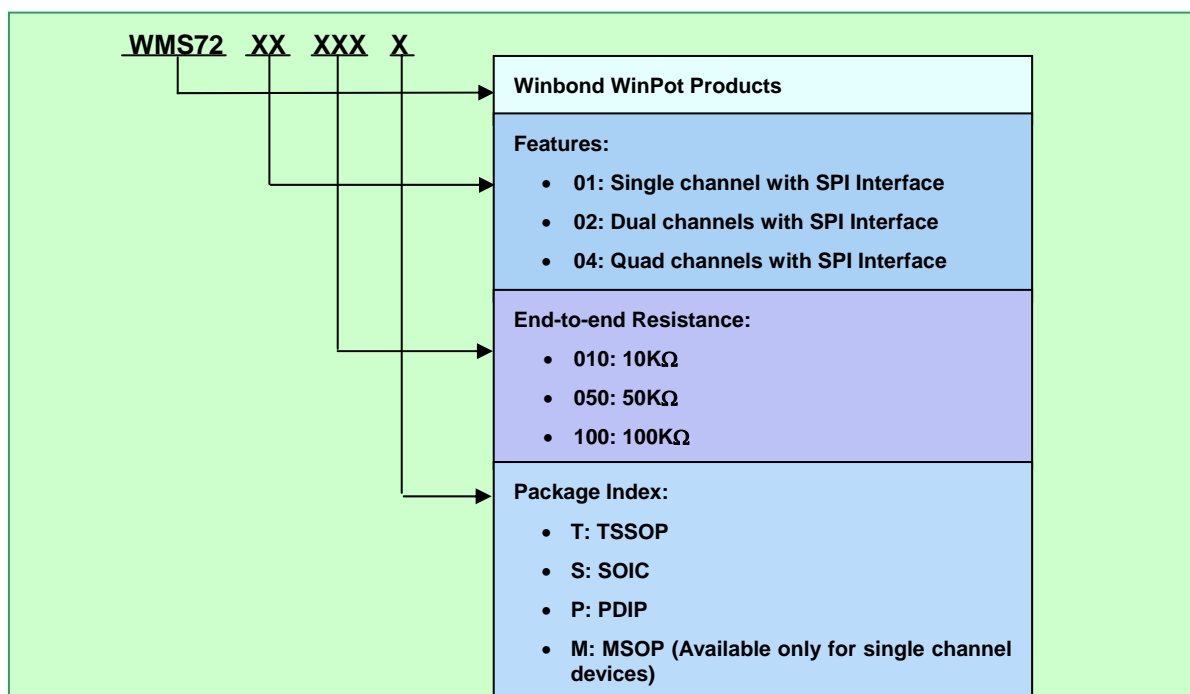


FIGURE 15 – 8L MSOP



### 13. ORDERING INFORMATION

Winbond's WinPot Part Number Description:



For the latest product information, access Winbond's worldwide website at <http://www.winbond-usa.com>

**14. VERSION HISTORY**

VERSION	DATE	DESCRIPTION
1.0	Jan. 2003	Initial issue
1.1	Jan. 2003	Correct typos
1.2	April. 2005	Revise disclaim section



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