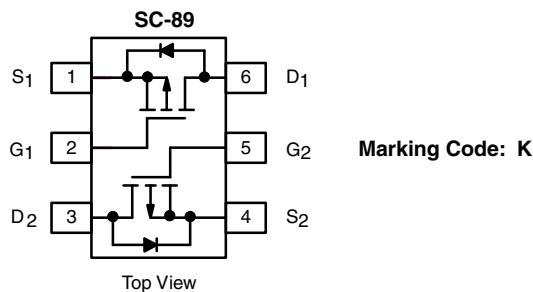


P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (mA)
- 20	8 at $V_{GS} = - 4.5$ V	- 150
	12 at $V_{GS} = - 2.5$ V	- 125
	15 at $V_{GS} = - 1.8$ V	- 100
	20 at $V_{GS} = - 1.5$ V	- 30



Ordering Information: Si1033X-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET: 1.5 V Rated
- High-Side Switching
- Low On-Resistance: 8 Ω
- Low Threshold: 0.9 V (typ.)
- Fast Switching Speed: 45 ns (typ.)
- 1.5 V Operation
- Gate-Source ESD Protected: 2000 V
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

BENEFITS

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation

APPLICATIONS

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	5 s	Steady State	Unit
Drain-Source Voltage	V_{DS}	- 20		V
Gate-Source Voltage	V_{GS}	± 5		
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	- 155	- 145	mA
		- 110	- 105	
Pulsed Drain Current ^b	I_{DM}	- 650		
Continuous Source Current (Diode Conduction) ^a	I_S	- 450	- 380	mW
Maximum Power Dissipation ^a	P_D	280	250	
		145	130	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		°C
Gate-Source ESD Rating (HBM, Method 3015)	ESD	2000		V

Notes:

a. Surface mounted on FR4 board.

b. Pulse width limited by maximum junction temperature.

SPECIFICATIONS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

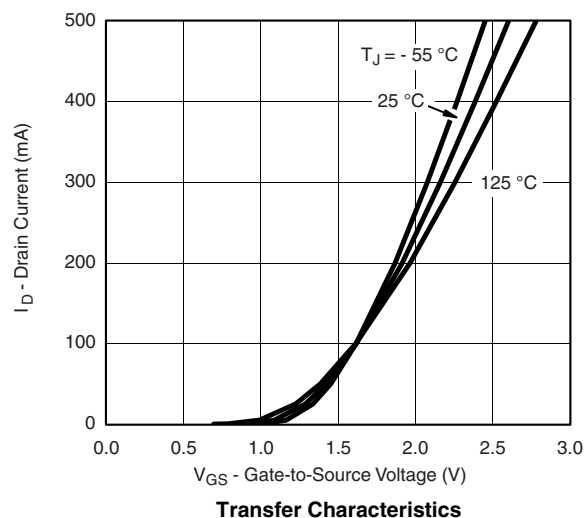
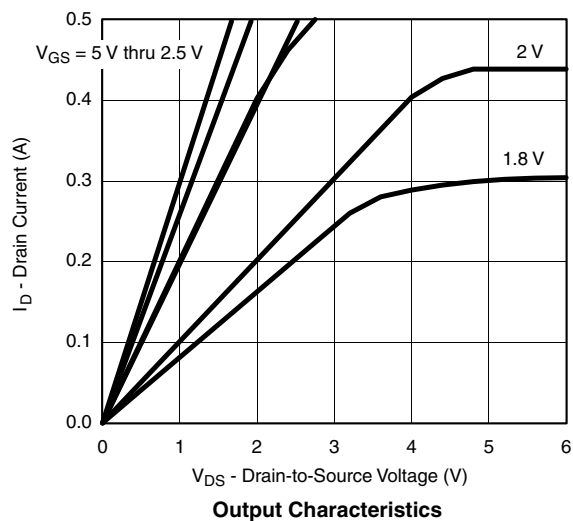
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-0.40		-1.20	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 2.8\text{ V}$		± 0.5	± 1	μA
		$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 4.5\text{ V}$		± 1	± 2	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16\text{ V}$, $V_{GS} = 0\text{ V}$		-1	-500	nA
		$V_{DS} = -16\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 85\text{ }^{\circ}\text{C}$			-10	μA
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\text{ V}$, $V_{GS} = -4.5\text{ V}$	-200			mA
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}$, $I_D = -150\text{ mA}$			8	Ω
		$V_{GS} = -2.5\text{ V}$, $I_D = -125\text{ mA}$			12	
		$V_{GS} = -1.8\text{ V}$, $I_D = -100\text{ mA}$			15	
		$V_{GS} = -1.5\text{ V}$, $I_D = -30\text{ mA}$			20	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}$, $I_D = -150\text{ mA}$		0.4		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -150\text{ mA}$, $V_{GS} = 0\text{ V}$			-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\text{ V}$, $V_{GS} = -4.5\text{ V}$, $I_D = -150\text{ mA}$		1500		pC
Gate-Source Charge	Q_{gs}			150		
Gate-Drain Charge	Q_{gd}			450		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}$, $R_L = 65\text{ }\Omega$ $I_D \cong -150\text{ mA}$, $V_{GEN} = -4.5\text{ V}$, $R_g = 10\text{ }\Omega$			55	ns
Rise Time	t_r				30	
Turn-Off Delay Time	$t_{d(off)}$				60	
Fall Time	t_f				30	

Notes:

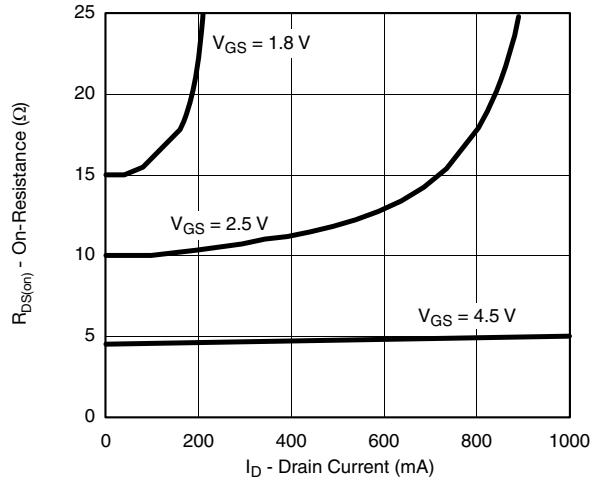
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

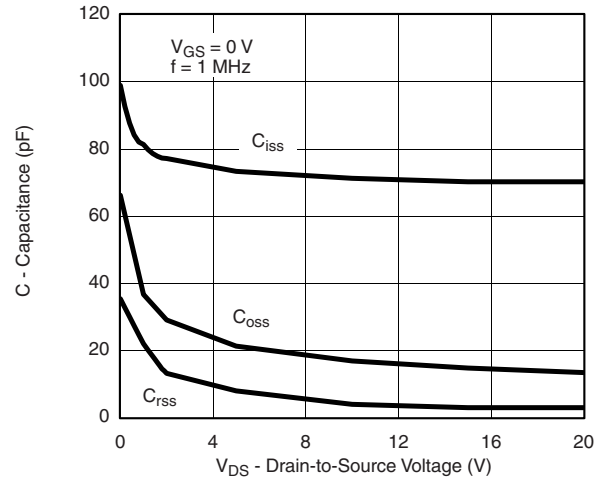
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

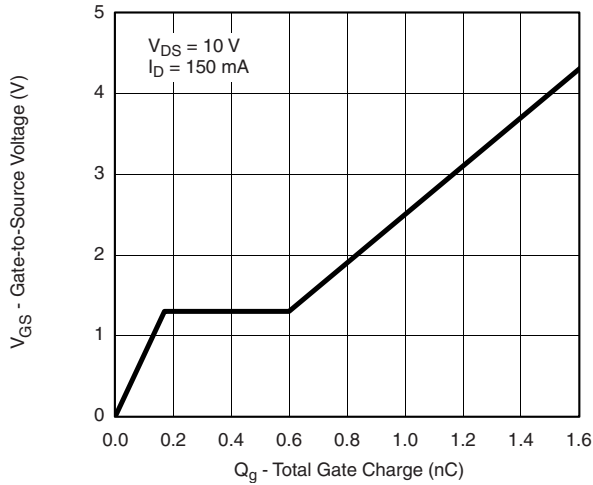
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



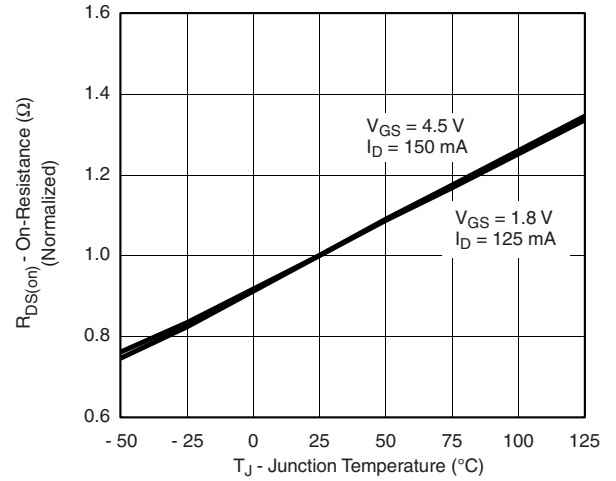
On-Resistance vs. Drain Current



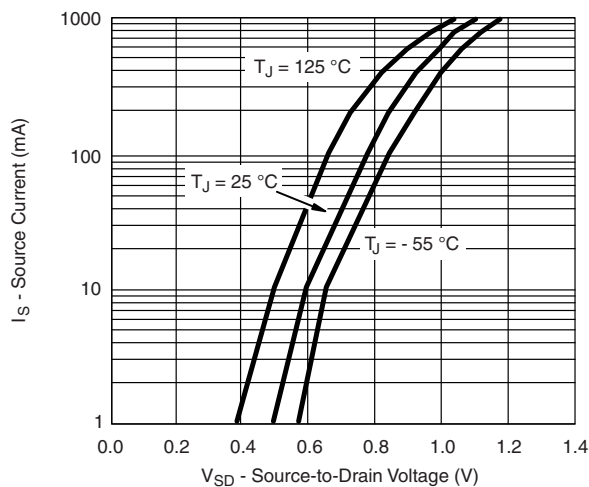
Capacitance



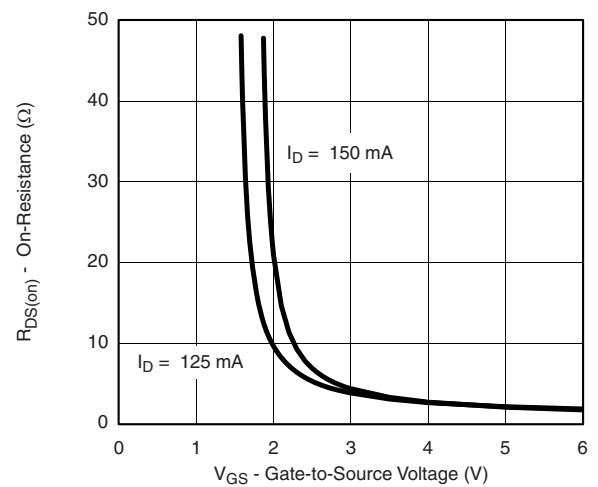
Gate Charge



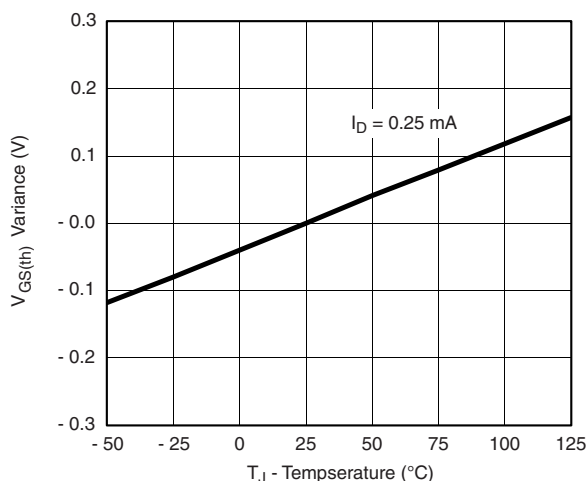
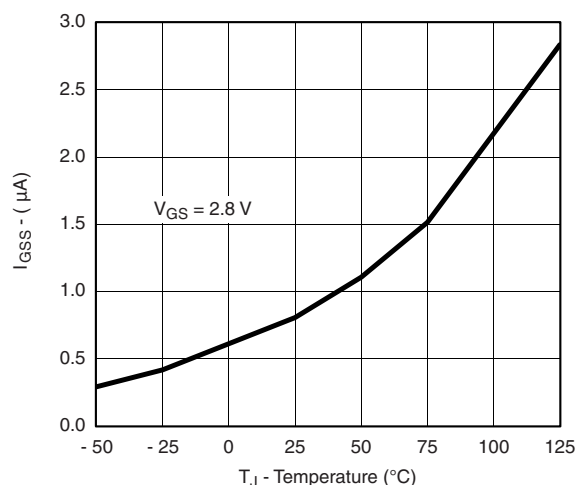
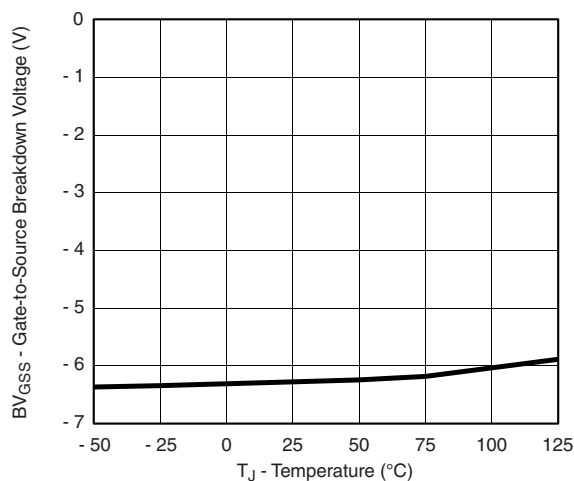
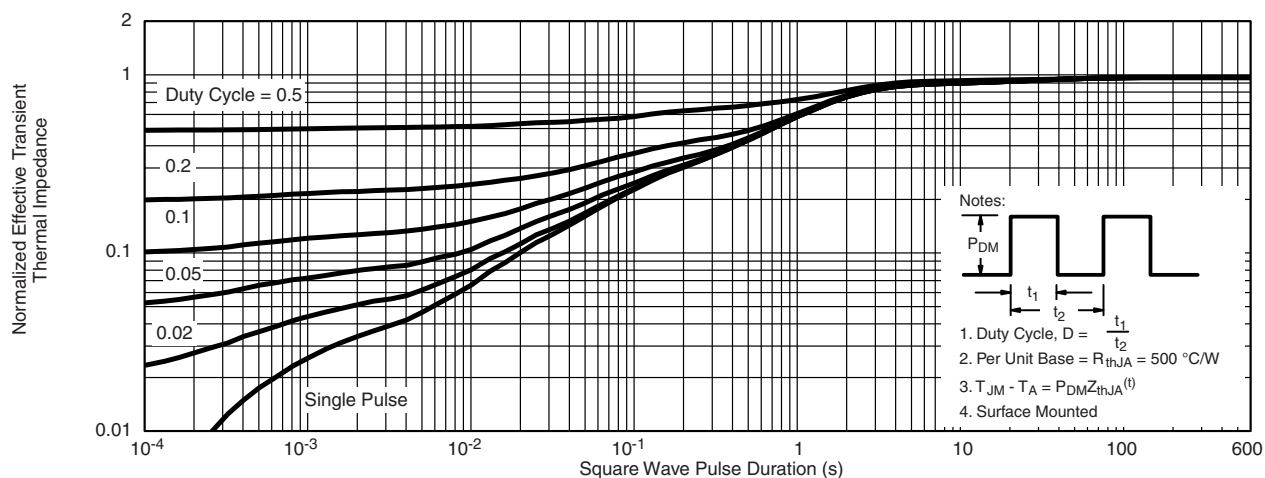
On-Resistance vs. Junction Temperature



Surge-Drain Diode Forward Voltage

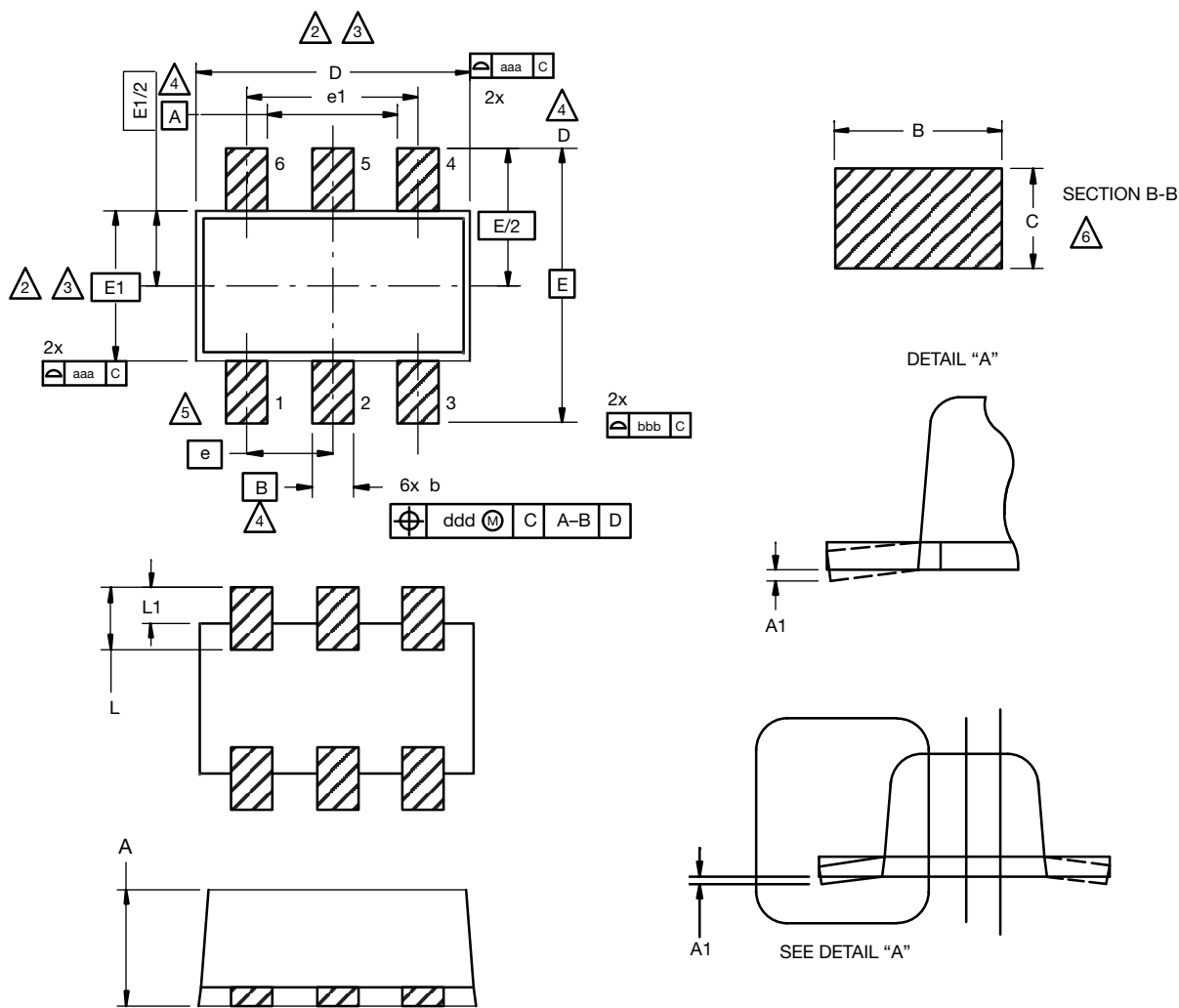


On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)**Threshold Voltage Variance vs. Temperature** **I_{GSS} vs. Temperature** **BV_{GSS} vs. Temperature****Normalized Thermal Transient Impedance, Junction-to-Ambient**

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SC-89 6-Leads (SOT-563F)



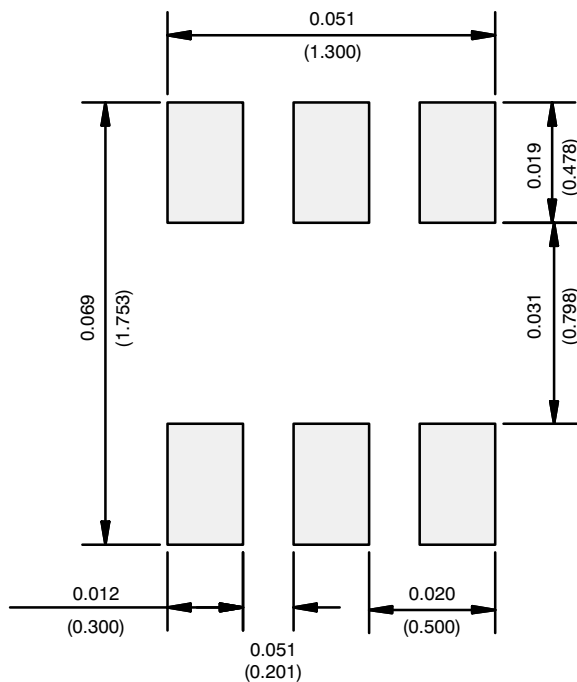
Notes

1. Dimensions in millimeters.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.
3. Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
4. Datums A, B and D to be determined 0.10 mm from the lead tip.
5. Terminal numbers are shown for reference only.
6. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.56	0.58	0.60
A1	0	0.02	0.10
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.15	1.20	1.25
e	0.45	0.50	0.55
e1	0.95	1.00	1.05
L	0.25	0.35	0.50
L1	0.10	0.20	0.30

C14-0439-Rev. C, 11-Aug-14
DWG: 5880

RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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