Enpirion® Power Datasheet

EP5358xUI 600mA PowerSoC Synchronous Buck Regulator with Integrated Inductor

Description

The EP5358xUI (x = L or H) is rated for up to 600mA of continuous output current. The EP5358xUI integrates MOSFET switches, control, compensation, and the magnetics in an advanced 2.5mm x 2.25mm micro-QFN Package.

Integrated magnetics enables a tiny solution footprint, low output ripple, low part-count, and high reliability, while maintaining high efficiency. The complete solution can be implemented in as little as $14mm^2$.

The EP5358xUI uses a 3-pin VID to easily select the output voltage setting. Output voltage settings are available in 2 optimized ranges providing coverage for typical V_{OUT} settings.

The VID pins can be changed on the fly for fast dynamic voltage scaling. EP5358LUI further has the option to use an external voltage divider.

The EP5358xUI is a perfect solution for noise sensitive and space constrained applications that require high efficiency.

Features

- Integrated Inductor Technology
- 2.5mm x 2.25mm x 1.1mm uQFN package
- Total Solution Footprint $14mm^2$
- Low V_{OUT} ripple for RF compatibility
- High efficiency, up to 93%
- Up to 600mA continuous output current
- Less than 1µA standby current
- 5 MHz switching frequency
- 3 pin VID for glitch free voltage scaling
- V_{OUT} Range 0.6V to V_{IN} – 0.25V
- Short circuit and over current protection
- UVLO and thermal protection
- IC level reliability in a PowerSOC solution

Application

- Wireless and RF applications
- Wireless broad band data cards
- Small form factor optical modules
- Low noise FPGA IO and Transceivers
- Advanced Low Power Processors, DSP, IO, Memory, Video, Multimedia Engines

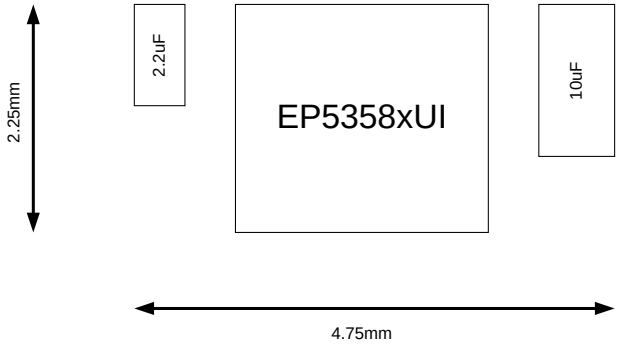


Figure 1: Total Solution Footprint.

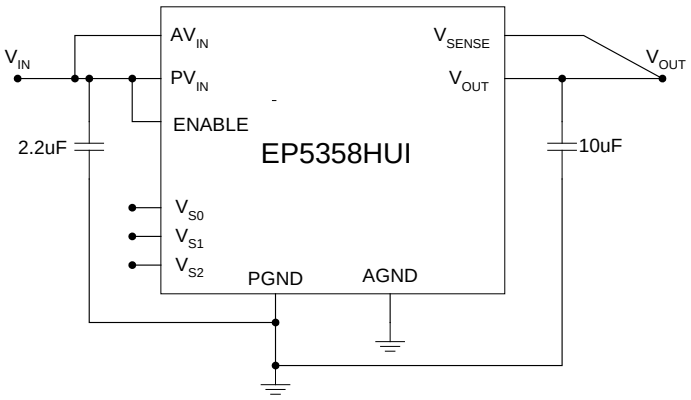


Figure 2: Typical Application Schematic

Ordering Information

Part Number	Comment	Package
EP5358LUI	LOW VID Range	16-pin QFN T&R
EP5358HUI	HIGH VID Range	16-pin QFN T&R
EVB-EP5358LUI	EP5358LUI Evaluation Board	
EVB-EP5358HUI	EP5358HUI Evaluation Board	

Pin Assignments (Top View)

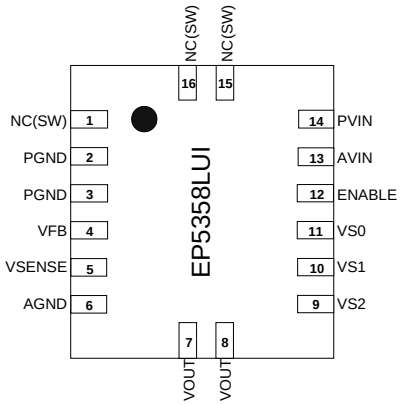


Figure 3: EP5358LUI Pin Out Diagram (Top View)

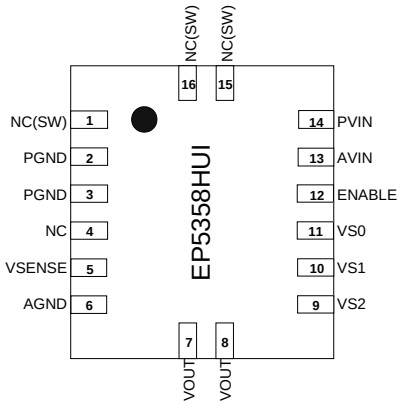


Figure 4: EP5358HUI Pin Out Diagram (Top View)

Pin Description

PIN	NAME	FUNCTION
1, 15, 16	NC(SW)	NO CONNECT – These pins are internally connected to the common switching node of the internal MOSFETs. NC (SW) pins are not to be electrically connected to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage to the device.
2,3	PGND	Power ground. Connect these pins together and to the ground electrode of the Input and output filter capacitors.
4	VFB/NC	EP5358LUI: Feed back pin for external divider option. EP5358HUI: No Connect
5	VSENSE	Sense pin for preset output voltages. Refer to application section for proper configuration.
6	AGND	Analog ground. This is the quiet ground for the internal control circuitry, and the ground return for external feedback voltage divider
7, 8	VOUT	Regulated Output Voltage. Refer to application section for proper layout and decoupling.
9, 10, 11	VS2, VS1, VS0	Output voltage select. VS2 = pin 9, VS1 = pin 10, VS0 = pin 11. EP5358LUI: Selects one of seven preset output voltages or an external resistor divider. EP5358HUI: Selects one of eight preset output voltages. (Refer to section on output voltage select for more details.)
12	ENABLE	Output Enable. Enable = logic high; Disable = logic low
13	AVIN	Input power supply for the controller circuitry.
14	PVIN	Input Voltage for the MOSFET switches.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage	V_{IN}	-0.3	6.0	V
Voltages on: ENABLE, V_{SENSE}, $V_{SO} – V_{S2}$		-0.3	V_{IN}+ 0.3	V
Voltages on: V_{FB} (EP5358LUI)		-0.3	2.7	V
Maximum Operating Junction Temperature	T_{J-ABS}		150	°C
Storage Temperature Range	T_{STG}	-65	150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020C			260	°C
ESD Rating (based on Human Body Mode)			2000	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.4	5.5	V
Operating Ambient Temperature	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient –0 LFM (**Note 1**)	θ_{JA}	85	°C/W
Thermal Overload Trip Point	T_{J-TP}	+155	°C
Thermal Overload Trip Point Hysteresis		25	°C

Note 1: Based on a four layer copper board and proper thermal design per JEDEC EIJ/JESD51 standards

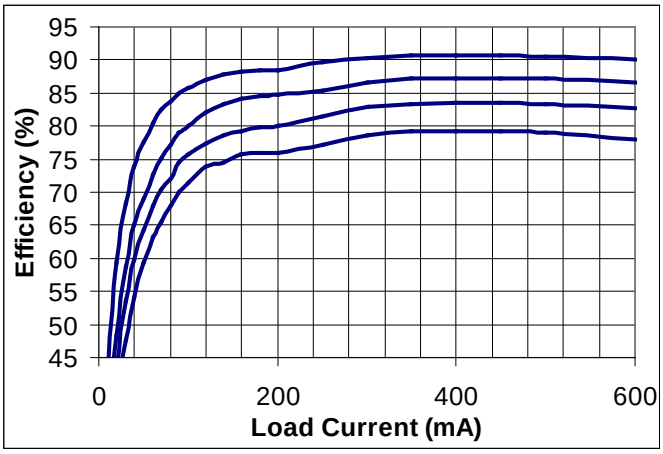
Electrical Characteristics

NOTE: T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C, VIN = 3.6V. C_{IN} = 4.7µF MLCC, C_{OUT} = 10µF

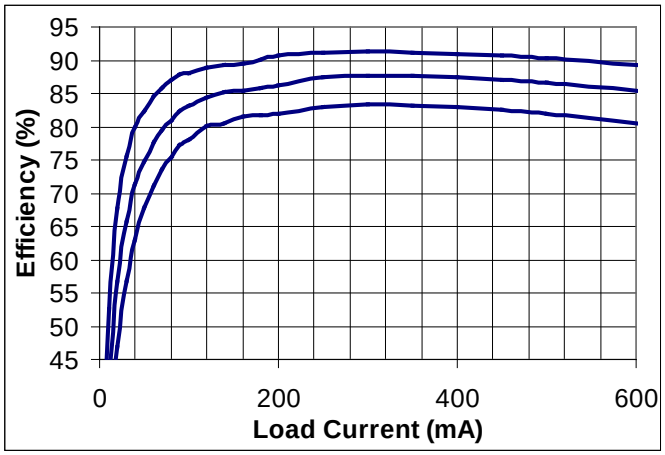
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage Range	V_{IN}		2.4		5.5	V
Under Voltage Lock-out – V_{IN} Rising	V_{UVLO_R}			2.0		V
Under Voltage Lock-out – V_{IN} Falling	V_{UVLO_F}			1.9		V
Drop Out Resistance	R_{DO}	Input to Output Resistance in 100% duty cycle operation.		350	500	mΩ
Output Voltage Range	V_{OUT}	EP5358LUI (V_{DO} = I_{LOAD} X R_{DO}) EP5358HUI	0.6 1.8		V_{IN}-V_{DO} 3.3	V
Dynamic Voltage Slew Rate (VID Change)	V_{SLEW}	EP5358LUI EP5358HUI		4 8		V/mS
VID Preset V_{OUT} Initial Accuracy	ΔV_{OUT}	T_A = 25°C, V_{IN} = 3.6V; I_{LOAD} = 100mA ; 0.8V ≤ V_{OUT} ≤ 3.3V	-2		+2	%
Line Regulation	ΔV_{OUT_LINE}	2.4V ≤ V_{IN} ≤ 5.5V		0.03		%/V
Load Regulation	ΔV_{OUT_LOAD}	0A ≤ I_{LOAD} ≤ 600mA		0.48		%/A
Temperature Variation	ΔV_{OUT_TEMPL}	-40°C ≤ T_A ≤ +85°C		24		ppm/°C
Output Current	I_{OUT}		600			mA
Shut-down Current	I_{SD}	Enable = Low		0.75		µA
OCP Threshold	I_{LIM}	2.4V ≤ V_{IN} ≤ 5.5V 0.6V ≤ V_{OUT} ≤ 3.3V	1.25	1.4		A
Feedback Pin Voltage Initial Accuracy	V_{FB}	T_A = 25°C, V_{IN} = 3.6V; I_{LOAD} = 100mA ; 0.8V ≤ V_{OUT} ≤ 3.3V	.588	0.6	0.612	V
Feedback Pin Input Current	I_{FB}	Note 1		<100		nA
VS0-VS2, Pin Logic Low	V_{VSLO}		0.0		0.3	V
VS0-VS2, Pin Logic High	V_{VSHI}		1.4		V_{IN}	V
VS0-VS2, Pin Input Current	I_{VSX}	Note 1		<100		nA
Enable Pin Logic Low	V_{ENLO}				0.3	V
Enable Pin Logic High	V_{ENHI}		1.4			V
Enable Pin Current	I_{ENABLE}	Note 1		<100		nA
Operating Frequency	F_{OSC}			5		MHz
Soft Start Operation						
Soft Start Slew Rate	ΔV_{SS}	EP5358LUI (VID MODE) EP5358HUI (VID MODE)	2.6 5.2	4 8	5.4 10.8	V/mS
V_{OUT} Rise Time	T_{RISE}	EP5358LUI VFB MODE	146	225	304	uSec

Note 1: Parameter guaranteed by design

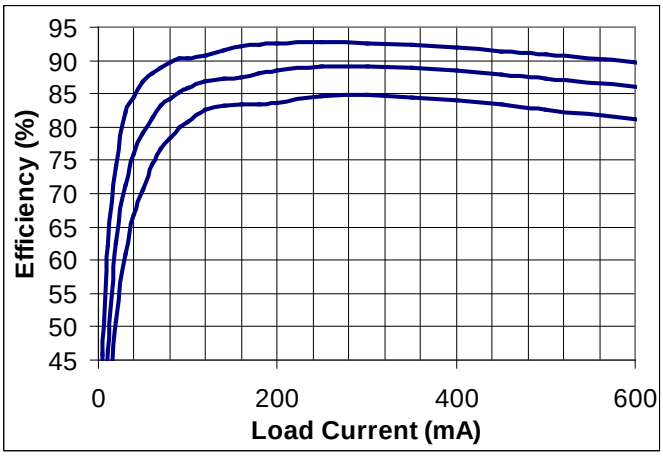
Typical Performance Characteristics



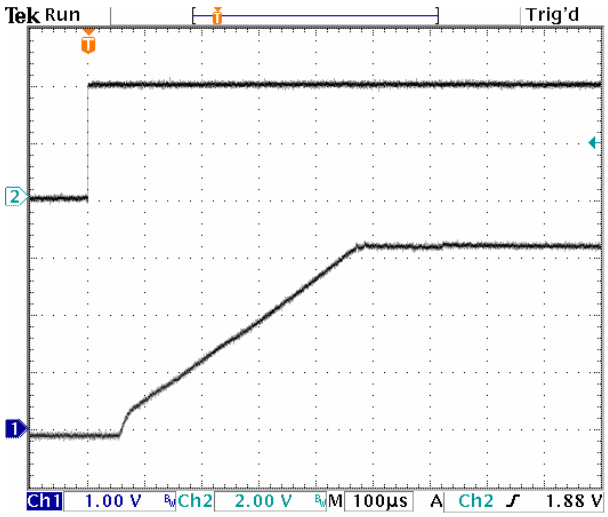
Efficiency vs. Load Current: V_{IN} = 5.0V, V_{OUT} (from top to bottom) = 3.3, 2.5, 1.8, 1.2V



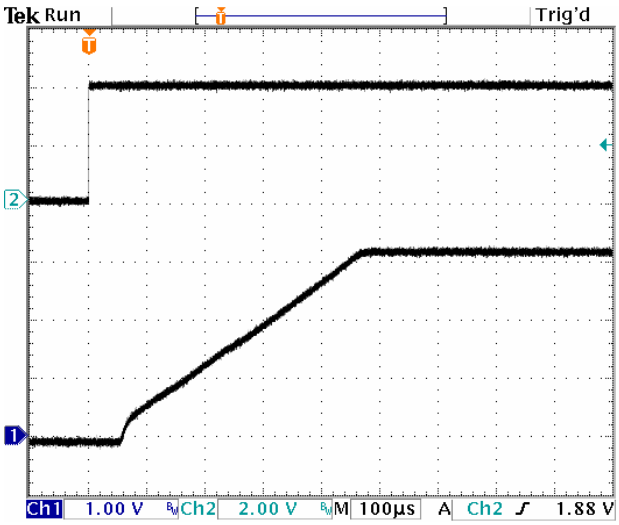
Efficiency vs. Load Current: V_{IN} = 3.7V, V_{OUT} (from top to bottom) = 2.5, 1.8, 1.2V



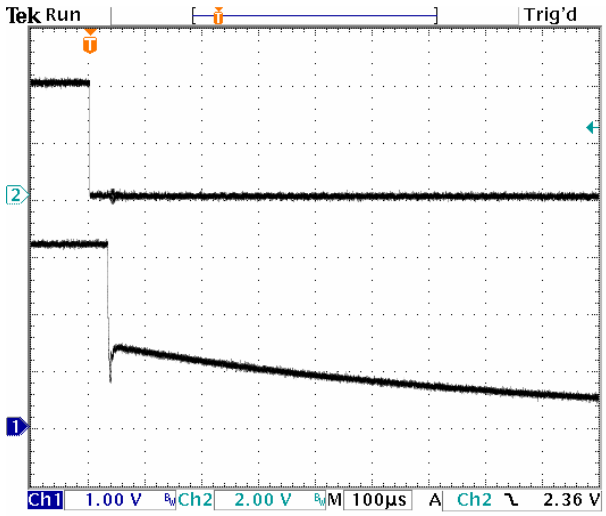
Efficiency vs. Load Current: V_{IN} = 3.3V, V_{OUT} (from top to bottom) = 2.5, 1.8, 1.2V



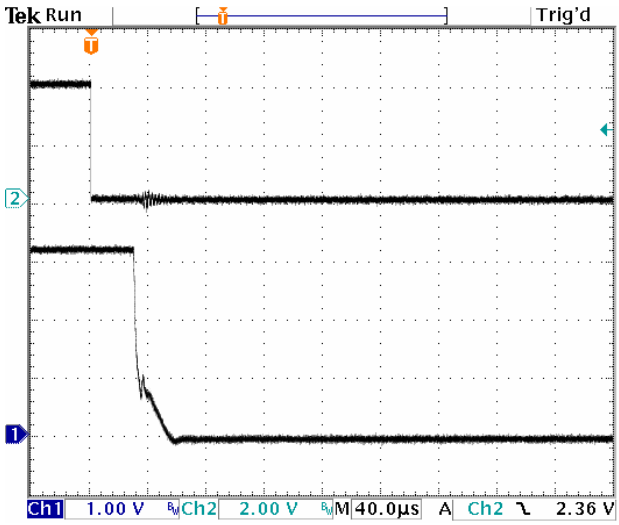
Start Up Waveform: V_{IN} = 5.0V, V_{OUT} = 3.3V; I_{LOAD} = 10mA (VID MODE)



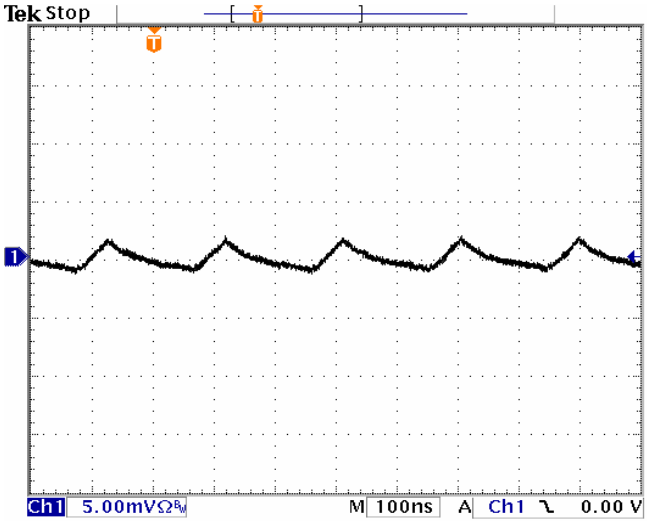
Start Up Waveform: V_{IN} = 5.0V, V_{OUT} = 3.3V; I_{LOAD} = 500mA (VID MODE)



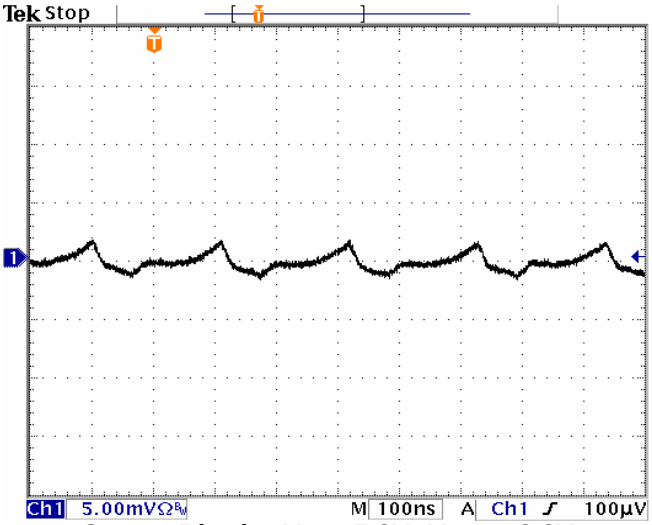
Shut-down Waveform: V_{IN} = 5.0V, V_{OUT} = 3.3V; I_{LOAD} = 10mA



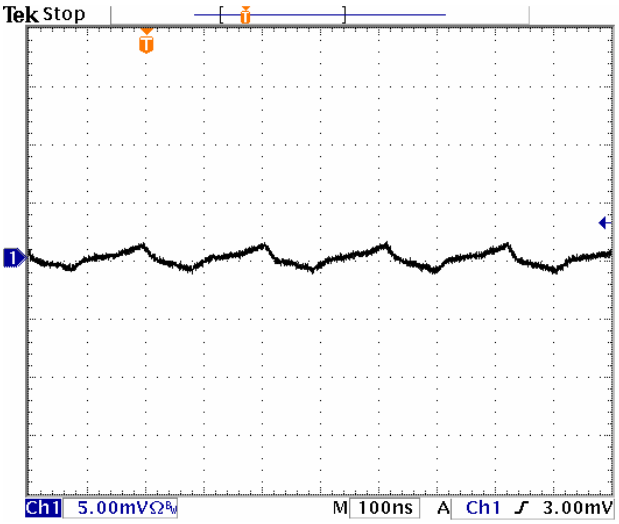
Shut-down Waveform: V_{IN} = 5.0V, V_{OUT} = 3.3V; I_{LOAD} = 500mA



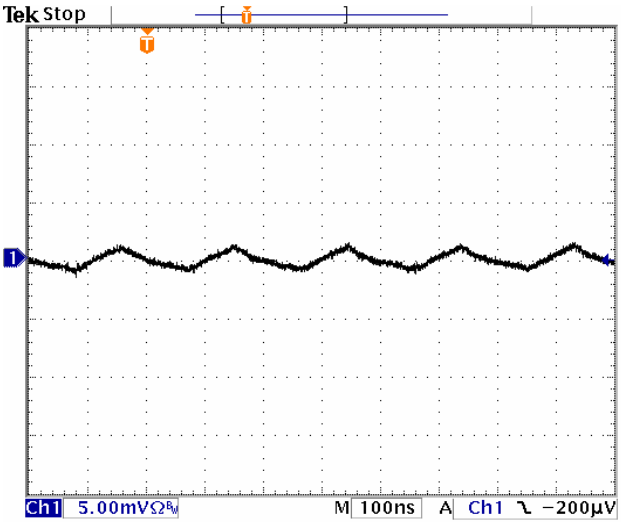
Output Ripple: V_{IN} = 5.0V, V_{OUT} = 1.2V, Load = 500mA



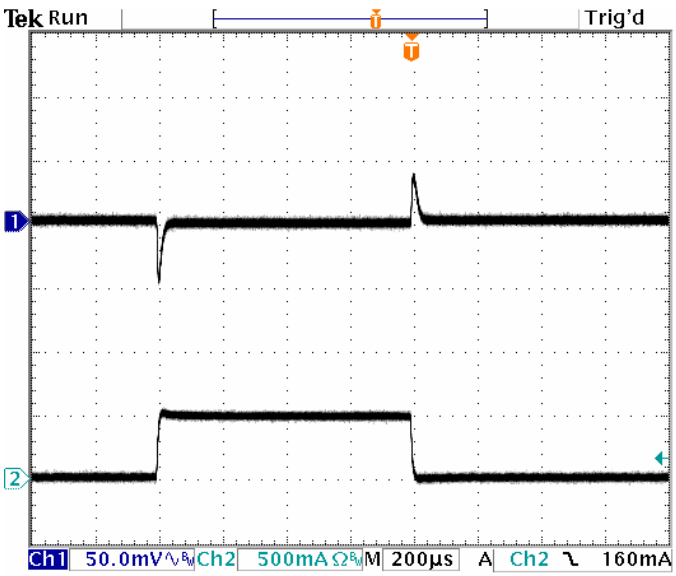
Output Ripple: V_{IN} = 5.0V, V_{OUT} = 3.3V Load = 500mA



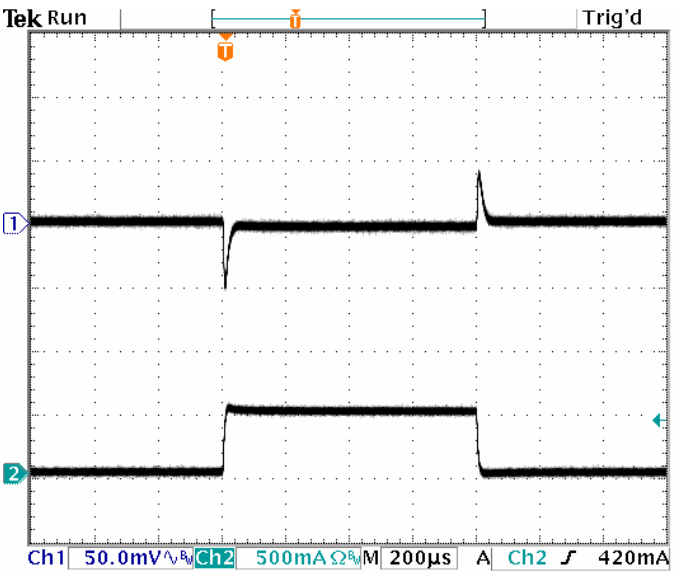
Output Ripple: V_{IN} = 3.3V, V_{OUT} = 1.8V Load = 500mA



Output Ripple: V_{IN} = 3.3V, V_{OUT} = 1.2V, Load = 500mA



Load Transient: V_{IN} = 5.0V, V_{OUT} = 1.2V
Load stepped from 10mA to 500mA



Load Transient: V_{IN} = 3.3V, V_{OUT} = 1.8V
Load stepped from 10mA to 500mA

Functional Block Diagram

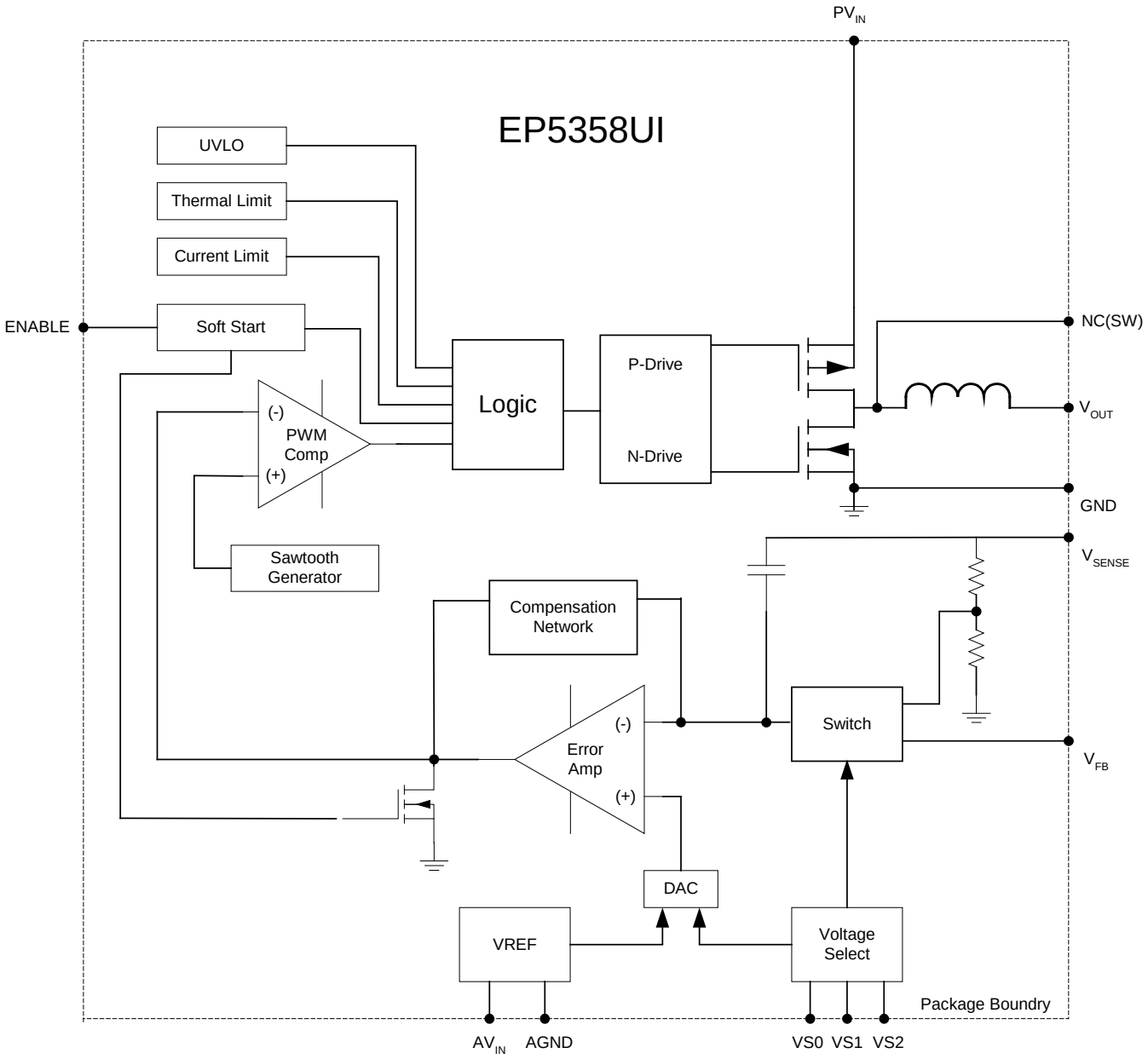


Figure 5: Functional Block Diagram

Detailed Description

Functional Overview

The EP5358xUI requires only 2 small MLCC capacitors for a complete DC-DC converter solution. The device integrates MOSFET switches, PWM controller, Gate-drive, compensation, and inductor into a tiny 2.5mm x 2.25mm x 1.1mm micro-QFN package. Advanced package design, along with the high level of integration, provides very low output ripple and noise. The EP5358xUI uses voltage mode control for high noise immunity and load matching to advanced ≤90nm loads. A 3-pin VID allows the user to choose from one of 8 output voltage settings. The EP5358xUI comes with two VID output voltage ranges. The EP5358HUI provides V_{OUT} settings from 1.8V to 3.3V, the EP5358LUI provides VID settings from 0.8V to 1.5V, and also has an external resistor divider option to program output setting over the 0.6V to V_{IN}-0.25V range. The EP5358xUI provides the industry's highest power density of any 600mA DCDC converter solution.

The key enabler of this revolutionary integration is Altera's proprietary power MOSFET technology. The advanced MOSFET switches are implemented in deep-submicron CMOS to supply very low switching loss at high switching frequencies and to allow a high level of integration. The semiconductor process allows seem-less integration of all switching, control, and compensation circuitry.

The proprietary magnetics design provides high-density/high-value magnetics in a very small footprint. Altera Enpirion magnetics are carefully matched to the control and compensation circuitry yielding an optimal solution with assured performance over the entire operating range.

Protection features include under-voltage lock-out (UVLO), over-current protection (OCP), short circuit protection, and thermal overload protection.

Integrated Inductor: Low-Noise Low-EMI

The EP5358xUI utilizes a proprietary low loss integrated inductor. The integration of the inductor greatly simplifies the power supply design process. The inherent shielding and compact construction of the integrated inductor reduces the conducted and radiated noise that can couple into the traces of the printed circuit board. Further, the package layout is optimized to reduce the electrical path length for the high di/dT input AC ripple currents that are a major source of radiated emissions from DC-DC converters. The integrated inductor provides the optimal solution to the complexity, output ripple, and noise that plague low power DCDC converter design.

Control Matched to sub 90nm Loads

The EP5358xUI utilizes an integrated type III compensation network. Voltage mode control is inherently impedance matched to the sub 90nm process technology that is used in today's advanced ICs. Voltage mode control also provides a high degree of noise immunity at light load currents so that low ripple and high accuracy are maintained over the entire load range. The very high switching frequency allows for a very wide control loop bandwidth and hence excellent transient performance.

Soft Start

Internal soft start circuits limit in-rush current when the device starts up from a power down condition or when the "ENABLE" pin is asserted "high". Digital control circuitry limits the V_{OUT} ramp rate to levels that are safe for the Power MOSFETS and the integrated inductor.

The EP5358HUI has a soft-start slew rate that is twice that of the EP5358LUI.

When the EP5358LUI is configured in external resistor divider mode, the device has a fixed VOUT ramp time. Therefore, the ramp rate will vary with the output voltage setting. Output voltage ramp time is given in the Electrical Characteristics Table.

Excess bulk capacitance on the output of the device can cause an over-current condition at startup. The maximum total capacitance on the output, including the output filter capacitor and bulk and decoupling capacitance, at the load, is given as:

EP5358LUI:

$C_{OUT\_TOTAL\_MAX} = C_{OUT\_Filter} + C_{OUT\_BULK} = 230uF$

EP5358HUI:

$C_{OUT\_TOTAL\_MAX} = C_{OUT\_Filter} + C_{OUT\_BULK} = 115uF$

EP5358LUI in external divider mode:

$C_{OUT\_TOTAL\_MAX} = 2.086x10^{-4}/V_{OUT}$ Farads

The above numbers and formula assume a no load condition.

Over Current/Short Circuit Protection

The current limit function is achieved by sensing the current flowing through a sense P-MOSFET which is compared to a reference current. When this level is exceeded the P-FET is turned off and the N-FET is turned on, pulling V_{OUT} low. This condition is maintained for approximately 0.5mS and then a normal soft start is initiated. If the over current condition still persists, this cycle will repeat.

Under Voltage Lockout

During initial power up an under voltage lockout circuit will hold-off the switching circuitry until the input voltage reaches a sufficient level to insure proper operation. If the voltage drops below the UVLO threshold the lockout circuitry will again disable the switching. Hysteresis is included to prevent chattering between states.

Enable

The ENABLE pin provides a means to shut down the converter or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation.

NOTE: The ENABLE pin must not be left floating.

Thermal Shutdown

When excessive power is dissipated in the chip, the junction temperature rises. Once the junction temperature exceeds the thermal shutdown temperature the thermal shutdown circuit turns off the converter output voltage thus allowing the device to cool. When the junction temperature decreases by 15C°, the device will go through the normal startup process.

Application Information

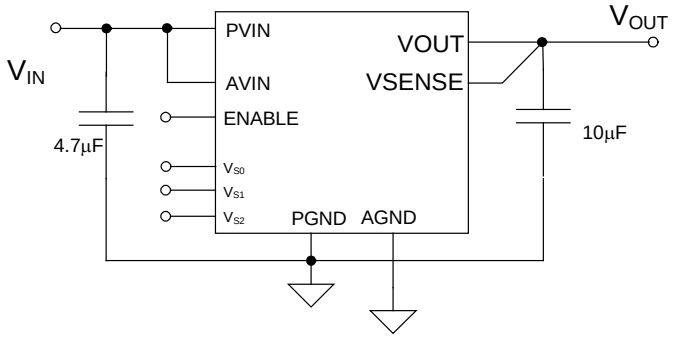


Figure 6: Application Circuit, EP5358HUI,.

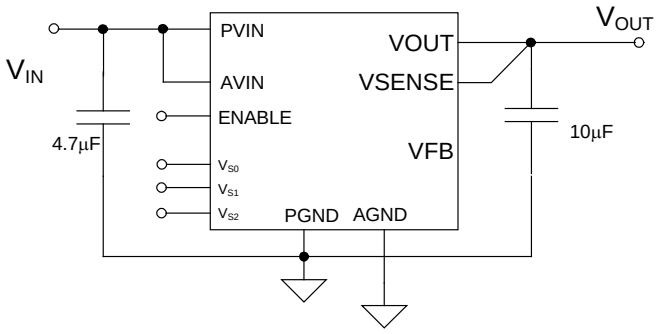


Figure 7: Application Circuit, EP5358LUI, showing the V_{FB} function.

Output Voltage Programming

The EP5358xUI utilizes a 3-pin VID to program the output voltage value. The VID is available in two sets of output VID programming ranges. The VID pins should be connected either to AVIN or to AGND to avoid noise coupling into the device.

The "Low" range is optimized for low voltage applications. It comes with preset VID settings ranging from 0.80V and 1.5V. This VID set also has an external divider option.

To specify this VID range, order part number EP5358LUI.

The "High" VID set provides output voltage settings ranging from 1.8V to 3.3V. This version does not have an external divider option. To specify this VID range, order part number EP5358HUI.

Internally, the output of the VID multiplexer sets the value for the voltage reference DAC, which in turn is connected to the non-inverting input of the error amplifier. This allows the use of a single feedback divider with constant loop gain and optimum compensation, independent of the output voltage selected.

NOTE: The VID pins must not be left floating.

EP5358L Low VID Range Programming

The EP5358LUI is designed to provide a high degree of flexibility in powering applications that require low V_{OUT} settings and dynamic voltage scaling (DVS). The device employs a 3-pin VID architecture that allows the user to choose one of seven (7) preset output voltage settings, or the user can select an external voltage divider option. The VID pin settings can be changed on the fly to implement glitch-free voltage scaling.

Table 1: EP5358LUI VID Voltage Select Settings

VS2	VS1	VS0	VOUT
0	0	0	1.50
0	0	1	1.45
0	1	0	1.20
0	1	1	1.15
1	0	0	1.10
1	0	1	1.05
1	1	0	0.8
1	1	1	EXT

Table 1 shows the VS2-VS0 pin logic states for the EP5358LUI and the associated output voltage levels. A logic "1" indicates a connection to AVIN or to a "high" logic voltage level. A logic "0" indicates a connection to AGND or to a "low" logic voltage level. These pins can be either hardwired to AVIN or AGND or alternatively can be driven by standard logic levels. Logic levels are defined in the electrical characteristics table. Any level between the logic high and logic low is indeterminate.

EP5358LUI External Voltage Divider

The external divider option is chosen by connecting VID pins VS2-VS0 to V_{IN} or a logic "1" or "high". The EP5358LUI uses a separate feedback pin, V_{FB}, when using the external divider. V_{SENSE} must be connected to V_{OUT} as indicated in figure 8.

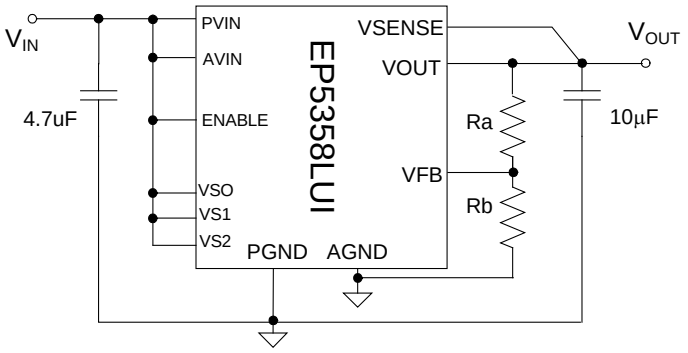


Figure 8: EP5358LUI using external divider

The output voltage is selected by the following formula:

$$V_{OUT} = 0.6V\left(1+\frac{Ra}{Rb}\right)$$

R_a must be chosen as 237KΩ to maintain loop gain. Then R_b is given as:

$$R_b = \frac{142.2x10^3}{V_{OUT}-0.6}\Omega$$

V_{OUT} can be programmed over the range of 0.6V to (V_{IN} – 0.25V).

NOTE: Dynamic Voltage Scaling is not allowed between internal preset voltages and external divider.

EP5358HUI High VID Range Programming

The EP5358HUI V_{OUT} settings are optimized for higher nominal voltages such as those required to power IO, RF, or IC memory. The preset voltages range from 1.8V to 3.3V. There are eight (8) preset output voltage settings. The EP5358HUI does not have an external divider option. As with the EP5358LUI, the VID pin settings can be changed while the device is enabled.

Table 2 shows the VS0-VS2 pin logic states for the EP5358HUI and the associated output voltage levels. A logic "1" indicates a connection to AVIN or to a "high" logic voltage level. A logic "0" indicates a connection to AGND or to a "low" logic voltage level. These pins can be either hardwired to AVIN or AGND or alternatively can be driven by standard logic levels. Logic levels are defined in the electrical characteristics table. Any level between the logic high and logic low is indeterminate. These pins must not be left floating.

Table 2: EP5358HUI VID Voltage Select Settings

VS2	VS1	VS0	VOUT
0	0	0	3.3
0	0	1	3.0
0	1	0	2.9
0	1	1	2.6
1	0	0	2.5
1	0	1	2.2
1	1	0	2.1
1	1	1	1.8

Custom VID Setting Adjustment

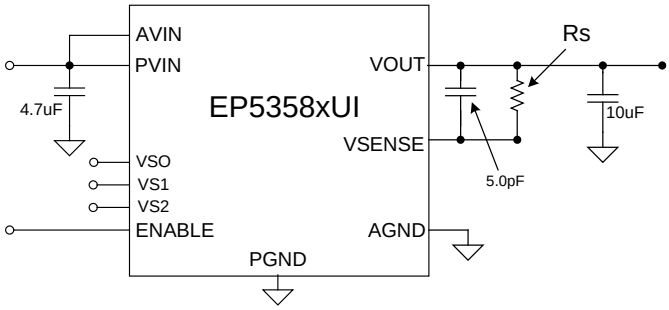


Figure 9: EP5358xUI with RC inserted in VSENSE path to modify VID output voltages.

It is possible to adjust VOUT for a given VID setting by inserting a parallel RC combination in the VSENSE path as shown in figure 9. The capacitor value is 5.0pF to ensure stability. Note that the value of VOUT can only be increased from its nominal setting ($VOUT_{NEW}$>$VOUT_{OLD}$):

For EP5358LUI:

$$Rs_L = 711*\left[\frac{VOUT_{NEW}}{VOUT_{OLD}}-1\right]kOhms$$

For EP5358HUI:

$$Rs_H = 356*\left[\frac{VOUT_{NEW}}{VOUT_{OLD}}-1\right]kOhms$$

$VOUT_{NEW}$ is the desired "new" VOUT.

$VOUT_{OLD}$ is the VID table output voltage.

For a given Rs Value, the $VOUT_{NEW}$ for VID settings is determined by the following equations:

EP5358LUI:

$$VOUT_{NEW} = VOUT_{OLD}\left[\left(\frac{Rs_L}{711}\right)+1\right]Volts$$

EP5358HUI:

$$VOUT_{NEW} = VOUT_{OLD}\left[\left(\frac{Rs_H}{356}\right)+1\right]Volts$$

NOTE: The amount of adjustment is limited to approximately 15% of the nominal VID setting.

NOTE: Adjusting VOUT using this method will increase the tolerance of the output voltage. The larger the adjustment, the greater the increase in tolerance.

Power-Up/Down Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. The PVIN should never be powered when AVIN is off. During power down, the AVIN should not be powered down before the PVIN. Tying PVIN and AVIN or all three pins (AVIN, PVIN, ENABLE) together during power up or power down meets these requirements.

Pre-Bias Start-up

The EP5358xUI does not support startup into a pre-biased condition. Be sure the output capacitors are not charged or the output of the EP5358xUI is not pre-biased when the EP5358xUI is first enabled.

Input Filter Capacitor

For $I_{LOAD} \leq 500mA$, $C_{IN} = 2.2uF$
For $I_{LOAD} > 500mA$ $C_{IN} = 4.7uF$.

0402 capacitor case size is acceptable.

The input capacitor must use a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and with temperature, and are not suitable for switch-mode DC-DC converter input filter applications.

Output Filter Capacitor

For VIN $\leq$ 4.3V, C_{OUT_MIN} = 10uF 0603 MLCC.

For VIN > 4.3V, C_{OUT_MIN} = 10uF 0805 MLCC.

Ripple performance can be improved by using 2x10µF 0603 MLCC capacitors (for any allowed VIN).

The maximum output filter capacitance next to the output pins of the device is 60µF low ESR MLCC capacitance. V_{OUT} has to be sensed at the last output filter capacitor next to the EP5358xUI.

Additional bulk capacitance for decoupling and bypass can be placed at the load as long as there is sufficient separation between the V_{OUT} Sense point and the bulk capacitance.

Excess total capacitance on the output (Output Filter + Bulk) can cause an over-current condition at startup. Refer to the section on Soft-Start for the maximum total capacitance on the output.

The output capacitor must use a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and temperature and are not suitable for switch-mode DC-DC converter output filter applications.

Layout Recommendation

Figure 10 shows critical components and layer 1 traces of a recommended minimum footprint EP5358LQI/EP5358HQI layout with ENABLE tied to V_{IN}. Alternate ENABLE configurations, and other small signal pins need to be connected and routed according to specific customer application. Please see the Gerber files on the Altera website www.altera.com/enpirion for exact dimensions and other layers. Please refer to Figure 10 while reading the layout recommendations in this section.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EP5358QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EP5358QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: Input and output grounds are separated until they connect at the PGND pins. The separation shown on Figure 10 between the input and output GND circuits helps minimize noise coupling between the converter input and output switching loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors. Please see the Gerber files on the Altera website www.altera.com/enpirion.

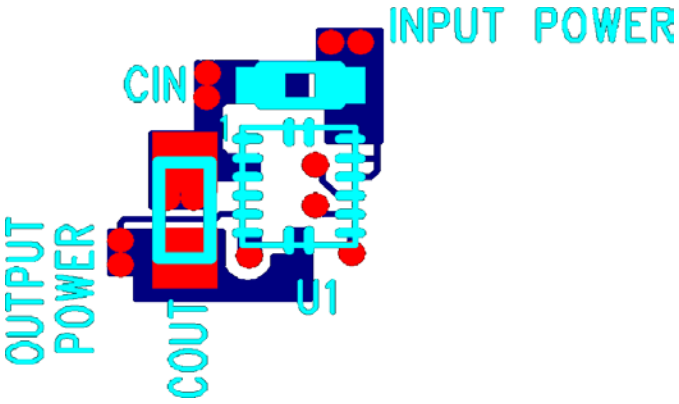


Figure 10:Top PCB Layer Critical Components and Copper for Minimum Footprint

Recommendation 4: Multiple small vias should be used to connect the ground traces under the device to the system ground plane on another layer for heat dissipation. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. It is preferred to put these vias under the capacitors along the edge of the GND copper closest to the +V copper. Please see Figure 10. These vias connect the input/output filter capacitors to the GND plane and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT}, then put them just outside the capacitors along the GND. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

Recommendation 5: AVIN is the power supply for the internal small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 10 this connection is made at the input capacitor close to the V_{IN} connection.

Recommended PCB Footprint

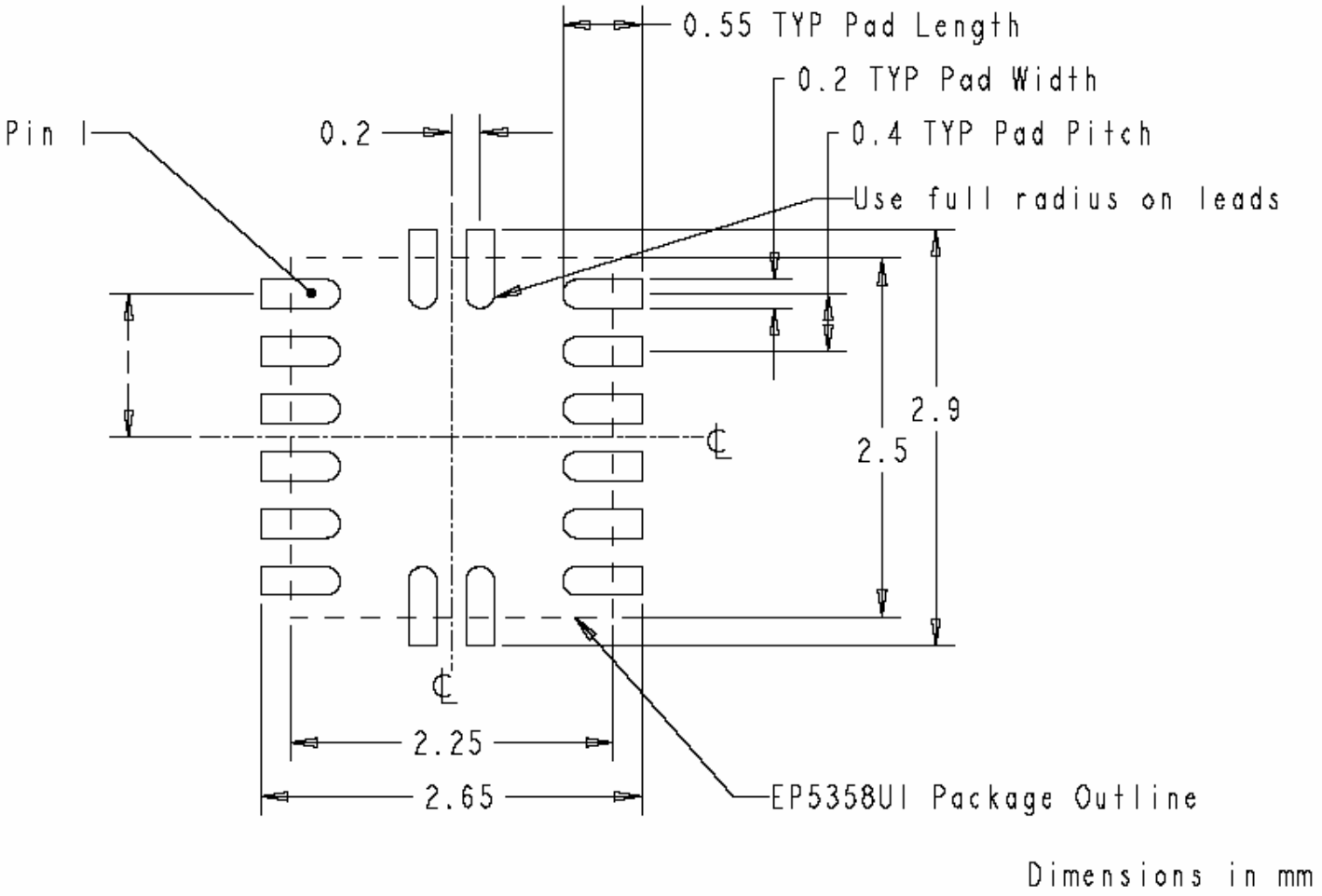


Figure 11: EP5358xUI Package PCB Footprint

Package and Mechanical

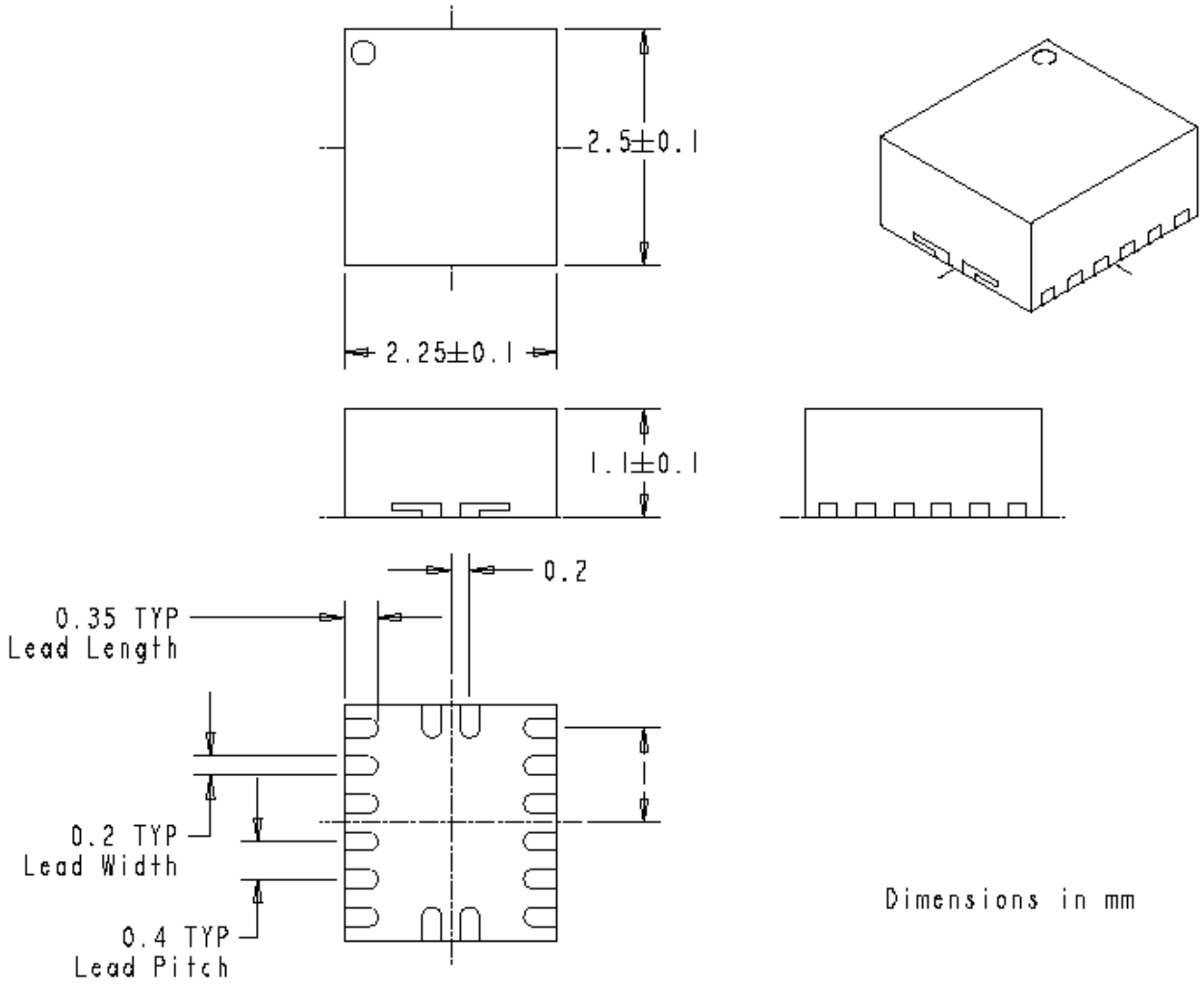


Figure 12: EN5358xUI Package Dimensions

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