19-5333; Rev 0; 6/10

EVALUATION KIT AVAILABLE

24-Bit, Single-Channel, Ultra-Low-Power, Delta Sigma ADC with 2-Wire Serial Interface

MAX11201

General Description

The MAX11201 is an ultra-low-power (< 320µA max active current), high-resolution, serial-output ADC. This device provides the highest resolution per unit power in the industry and is optimized for applications that require very high dynamic range with low power such as sensors on a 4mA to 20mA industrial control loop. The MAX11201 provides a high-accuracy internal oscillator that requires no external components.

When used with the specified data rates, the internal digital filter provides more than 100dB rejection of 50Hz or 60Hz line noise. The MAX11201 provides a simple 2-wire serial interface in the space-saving, 10-pin µMAX® package.

The MAX11201 operates over the -40°C to +85°C temperature range.

Applications

Sensor Measurement (Temperature and Pressure)

Portable Instrumentation

Battery Applications

Weigh Scales

Ordering Information

PART	PIN-PACKAGE	OUTPUT RATE (sps)
MAX11201AEUB+	10 µMAX	120
MAX11201BEUB+	10 µMAX	13.75

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.

Features

- **23.3-Bit ENOB**
  - **20.6-Bit Noise-Free Resolution at 13.75sps**
  - **19.1-Bit Noise-Free Resolution at 120sps**
- **700nV$_{RMS}$ Noise ±3.6V$_{FS}$ Input (MAX11201B)**
- **INL: 3ppm (typ), 10ppm (max)**
- **No Missing Codes**
- **Ultra-Low Power Dissipation**
  - **Operating Mode Current Drain < 320µA (max)**
  - **Sleep Mode Current Drain < 0.4µA**
- **2.7V to 3.6V Analog Supply Voltage Range**
- **1.7V to 3.6V Digital and I/O Supply Voltage Range**
- **Fully Differential Signal and Reference Inputs**
- **High-Impedance Inputs**
  - **Buffers on Signal Inputs**
- **Programmable Internal System Clock or External Clock**
  - **2.4576MHz (MAX11201A)**
  - **2.25275MHz (MAX11201B)**
- **> 100dB (min) 50Hz/60Hz Rejection (MAX11201B)**
- **Serial 2-Wire Interface (Clock Input and Data Output)**
- **On-Demand Offset and Gain Self-Calibration**
- **-40°C to +85°C Operating Temperature Range**
- **±2kV ESD Protection**
- **Lead(Pb)-Free and RoHS-Compliant µMAX Package**

Selector Guide

RESOLUTION (BITS)	4-WIRE SPI, 16-PIN QSOP, PROGRAMMABLE GAIN	4-WIRE SPI, 16-PIN QSOP	2-WIRE SERIAL, 10-PIN µMAX
24	MAX11210	MAX11200	MAX11201 (with buffers) MAX11202 (without buffers)
20	MAX11206	MAX11207	MAX11208
18	MAX11209	MAX11211	MAX11212
16	MAX11213	MAX11203	MAX11205

µMAX is a registered trademark of Maxim Integrated Products, Inc.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

24-Bit, Single-Channel, Ultra-Low-Power, Delta Sigma ADC with 2-Wire Serial Interface

ABSOLUTE MAXIMUM RATINGS

Any Pin to GND .....-0.3V to +3.9V
AVDD to GND.....-0.3V to +3.9V
DVDD to GND .....-0.3V to +3.9V
Analog Inputs (AINP, AINN, REFP, REFN)
to GND..... -0.3V to (V_{AVDD} + 0.3V)
Digital Inputs and Digital Outputs
to GND..... -0.3V to (V_{DVDD} + 0.3V)
ESD_{HB} (AVDD, AINP, AINN, REFP, REFN, DVDD, CLK, SCLK, $\overline{RDY}$/DOUT, GND) ..... ±2kV (Note 1)
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C).....444mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Human Body Model to specification MIL-STD-883 Method 3015.7.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = +3.6V, V_{DVDD} = +1.7V, V_{REFP} - V_{REFN} = V_{AVDD}; internal clock, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC PERFORMANCE						
Noise-Free Resolution (Notes 2, 3)	NFR	MAX11201A		19.1		Bits
		MAX11201B		20.6		
Noise (Notes 2, 3)	V_N	MAX11201A		2.0		μV_{RMS}
		MAX11201B		0.70		
Integral Nonlinearity	INL	(Note 4)	-10		+10	ppmFSR
Zero Error	V_{OFF}	After calibration, V_{REFP} - V_{REFN} = 2.5V	-10		+10	ppmFSR
Zero Drift				50		nV/°C
Full-Scale Error		After calibration, V_{REFP} - V_{REFN} = 2.5V (Note 5)	-20		+20	ppmFSR
Full-Scale Error Drift				0.05		ppmFSR/°C
Power-Supply Rejection		AVDD DC rejection	70	80		dB
		DVDD DC rejection	90	100		
ANALOG INPUTS/REFERENCE INPUTS						
Common-Mode Rejection	CMR	DC rejection	90	123		dB
		50Hz/60Hz rejection, MAX11201A	90			
		50Hz/60Hz rejection, MAX11201B	144			
Normal-Mode 50Hz Rejection	NMR_{50}	MAX11201B (Note 6)	100	144		dB
Normal-Mode 60Hz Rejection	NMR_{60}	MAX11201B (Note 6)	100	144		dB
Common-Mode Voltage Range			GND		V_{AVDD}	V
Absolute Input Voltage		Low input voltage		V_{GND} + 100mV		V
		High input voltage		V_{AVDD} - 100mV		
DC Input Leakage		Sleep mode (Note 2)		±1		µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = +3.6V, V_{DVDD} = +1.7V, V_{REFP} - V_{REFN} = V_{AVDD}; internal clock, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AIN_ Dynamic Input Current				±20		nA
REF_ Dynamic Input Current				±30		nA
AIN_ Input Capacitance				5		pF
REF_ Input Capacitance				7.5		pF
AIN_ Voltage Range		AINP - AINN	$-V_{REF}$		$+V_{REF}$	V
REF_ Voltage Range			0		V_{AVDD}	V
Input Sampling Rate	f_S	MAX11201A		246		kHz
		MAX11201B		225		
REF Sampling Rate		MAX11201A		246		kHz
		MAX11201B		225		
LOGIC INPUTS (SCLK, CLK)						
Input Current		Input leakage current		±1		µA
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Hysteresis	V_{HYS}			200		mV
External Clock		MAX11201A		2.4576		MHz
		MAX11201B		2.25275		
LOGIC OUTPUT ($\overline{RDY}$/DOUT)						
Output Low Level	V_{OL}	I_{OL} = 1mA; also tested for V_{DVDD} = 3.6V			0.4	V
Output High Level	V_{OH}	I_{OH} = 1mA; also tested for V_{DVDD} = 3.6V	0.9 x V_{DVDD}			V
Leakage Current		High-impedance state		±10		µA
Output Capacitance		High-impedance state		9		pF
POWER REQUIREMENTS						
Analog Supply Voltage	AVDD		2.7		3.6	V
Digital Supply Voltage	DVDD		1.7		3.6	V
Total Operating Current		AVDD + DVDD		245	320	µA
DVDD Operating Current				50	60	µA
AVDD Operating Current				195	265	µA
AVDD Sleep Current				0.15	2	µA
DVDD Sleep Current				0.25	2	µA
2-WIRE SERIAL-INTERFACE TIMING CHARACTERISTICS						
SCLK Frequency	f_{SCLK}				5	MHz
SCLK Pulse Width Low	t_1	60/40 duty cycle, 5MHz clock	80			ns
SCLK Pulse Width High	t_2	40/60 duty cycle, 5MHz clock	80			ns
SCLK Rising Edge to Data Valid Transition Time	t_3				40	ns

24-Bit, Single-Channel, Ultra-Low-Power, Delta Sigma ADC with 2-Wire Serial Interface

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = +3.6V, V_{DVDD} = +1.7V, V_{REFP} - V_{REFN} = V_{AVDD}; internal clock, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Rising Edge Data Hold Time	t_4	Allows for positive edge data read	3			ns
$\overline{RDY}$/DOUT Fall to SCLK Rising Edge	t_5		0			ns
Next Data Update Time; No Read Allowed	t_6	MAX11201A		155		µs
		MAX11201B		169		
Data Conversion Time	t_7	MAX11201A		8.6		ms
		MAX11201B		73		
Data Ready Time After Calibration Starts (CAL + CNV)	t_8	MAX11201A		208.3		ms
		MAX11201B		256.1		
SCLK High After $\overline{RDY}$/DOUT Goes Low to Activate Sleep Mode	t_9	MAX11201A	0		8.6	ms
		MAX11201B	0		73	
Time from $\overline{RDY}$/DOUT Low to SCLK High for Sleep-Mode Activation	t_{10}	MAX11201A	0		8.6	ms
		MAX11201B	0		73	
Data Ready Time After Wake-Up From Sleep Mode	t_{11}	MAX11201A		8.6		ms
		MAX11201B		73		
Data Ready Time After Calibration From Sleep Mode Wake-Up (CAL + CNV)	t_{12}	MAX11201A		208.4		ms
		MAX11201B		256.2		

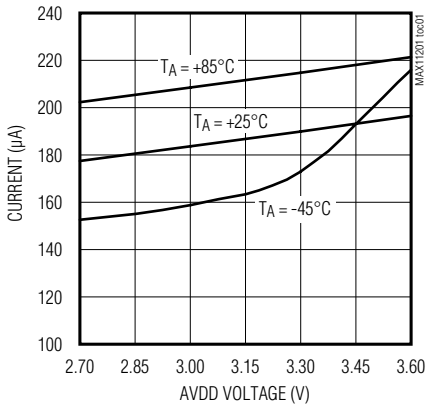
Note 2: These specifications are not fully tested and are guaranteed by design and/or characterization.
Note 3: V_{AINP} = V_{AINN}.
Note 4: ppmFSR is parts per million of full-scale range.
Note 5: Positive full-scale error includes zero-scale errors.
Note 6: The MAX11201A has no normal-mode rejection at 50Hz or 60Hz.

24-Bit, Single-Channel, Ultra-Low-Power, Delta Sigma ADC with 2-Wire Serial Interface

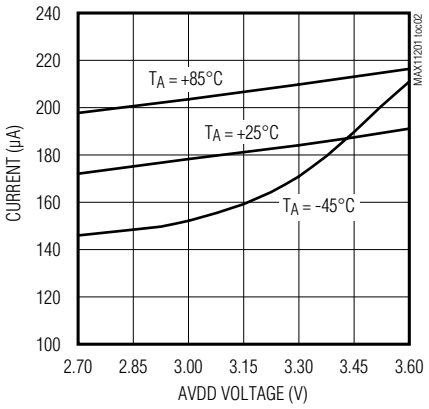
Typical Operating Characteristics

(V_{AVDD} = 3.6V, V_{DVDD} = 1.8V, V_{REFP} - V_{REFN} = AVDD; internal clock; T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

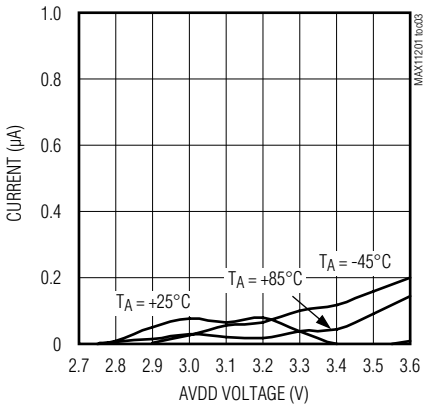
ANALOG ACTIVE CURRENT vs. AVDD VOLTAGE (MAX11201A)



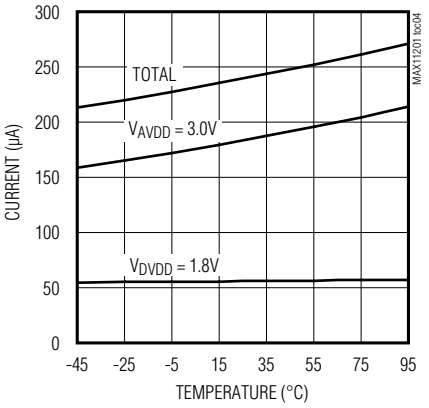
ANALOG ACTIVE CURRENT vs. AVDD VOLTAGE (MAX11201B)



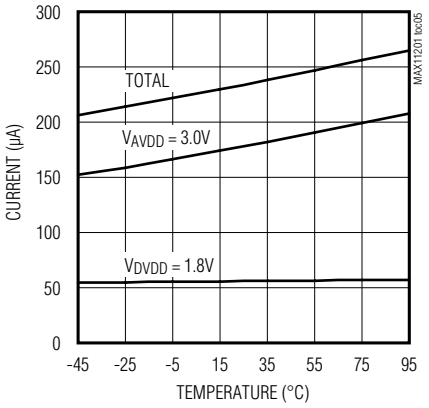
ANALOG SLEEP CURRENT vs. AVDD VOLTAGE



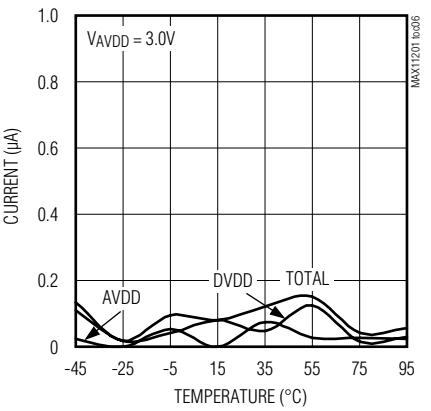
ACTIVE SUPPLY CURRENT vs. TEMPERATURE (MAX11201A)



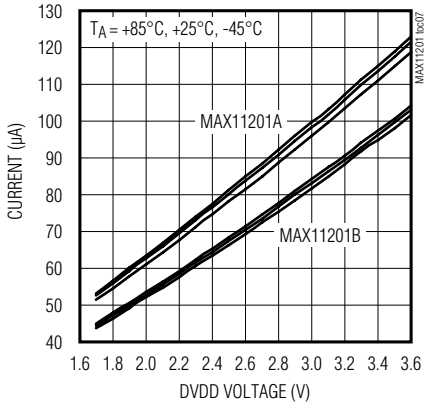
ACTIVE SUPPLY CURRENT vs. TEMPERATURE (MAX11201B)



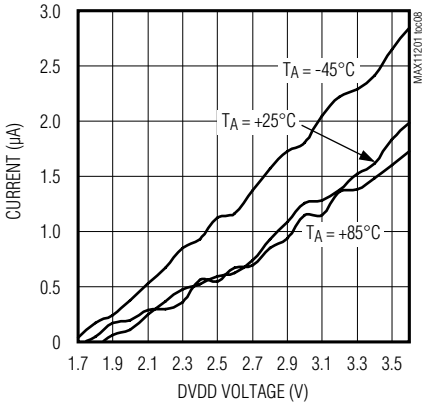
SLEEP CURRENT vs. TEMPERATURE



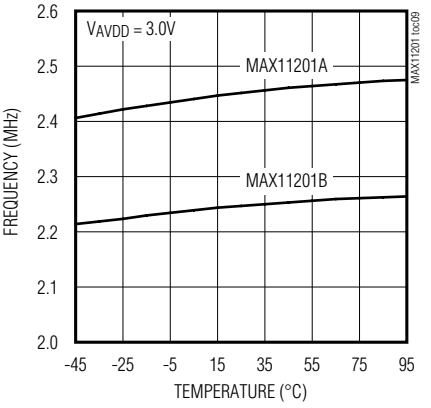
DIGITAL ACTIVE CURRENT vs. DVDD VOLTAGE



DIGITAL SLEEP CURRENT vs. DVDD VOLTAGE



INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE

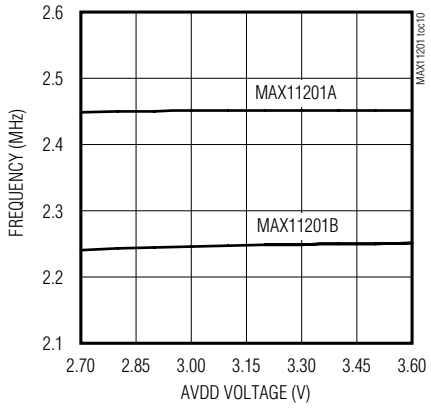


24-Bit, Single-Channel, Ultra-Low-Power, Delta Sigma ADC with 2-Wire Serial Interface

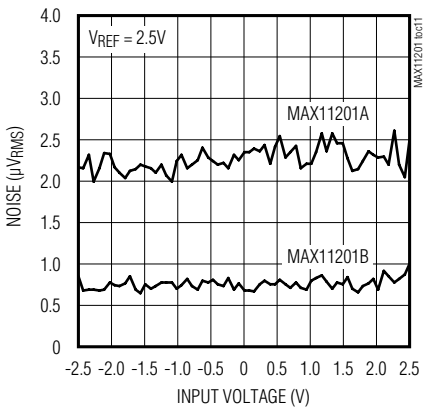
Typical Operating Characteristics (continued)

(V_{AVDD} = 3.6V, V_{DVDD} = 1.8V, V_{REFP} - V_{REFN} = AVDD; internal clock; T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

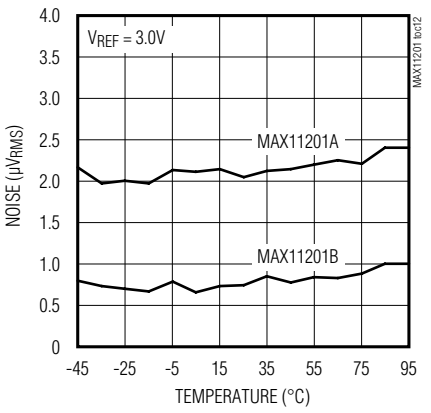
INTERNAL OSCILLATOR FREQUENCY vs. AVDD VOLTAGE



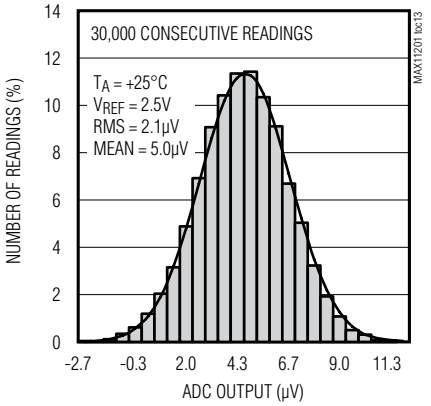
NOISE vs. INPUT VOLTAGE



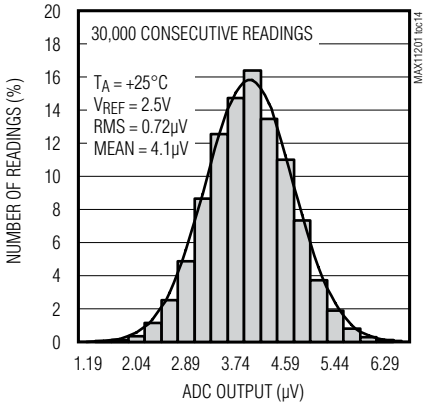
NOISE vs. TEMPERATURE



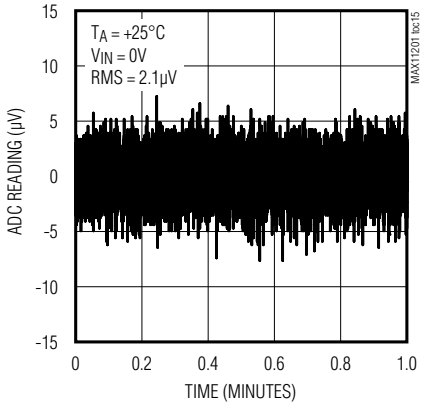
NOISE HISTOGRAM (MAX11201A, 120sps)



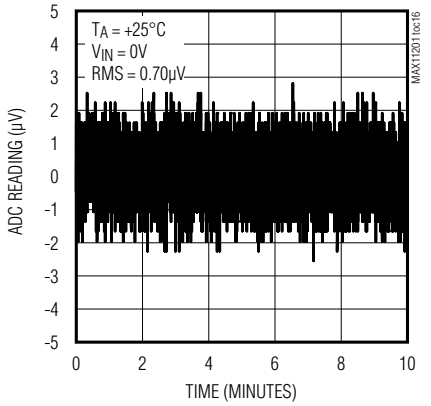
NOISE HISTOGRAM (MAX11201B, 13.75sps)



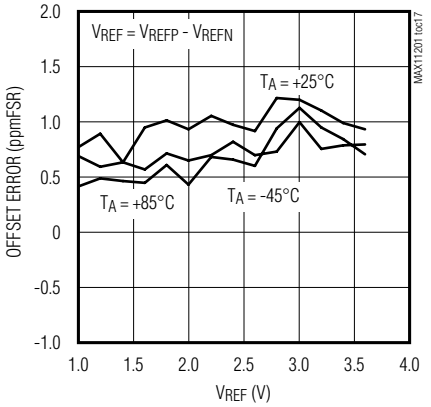
LONG-TERM ADC READINGS (MAX11201A)



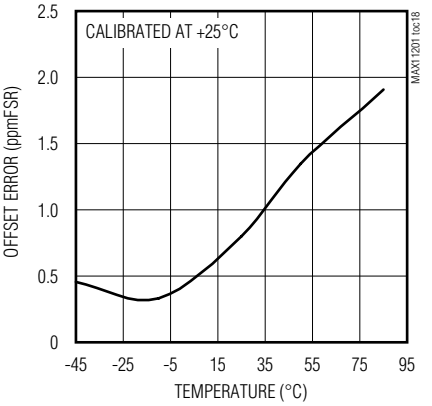
LONG-TERM ADC READINGS (MAX11201B)



OFFSET ERROR vs. V_{REF}



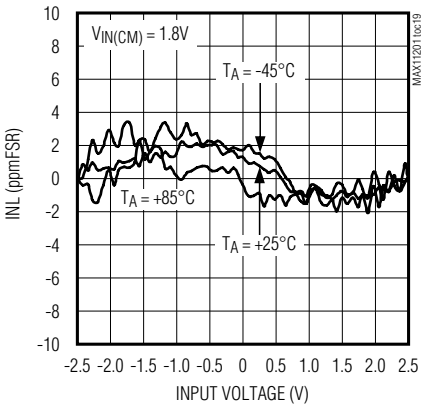
OFFSET ERROR vs. TEMPERATURE



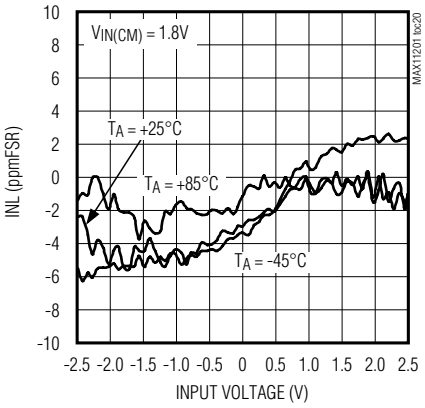
Typical Operating Characteristics (continued)

(V_{AVDD} = 3.6V, V_{DVDD} = 1.8V, V_{REFP} - V_{REFN} = AVDD; internal clock; T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

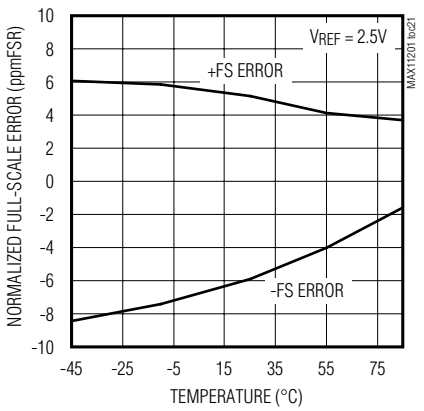
INL vs. INPUT VOLTAGE



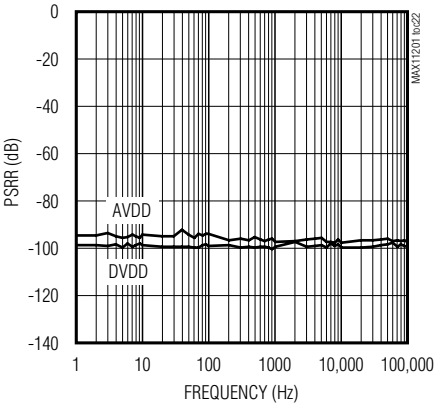
TUE vs. INPUT VOLTAGE



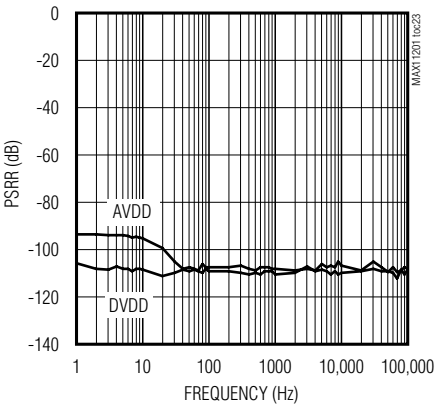
FULL-SCALE ERROR vs. TEMPERATURE



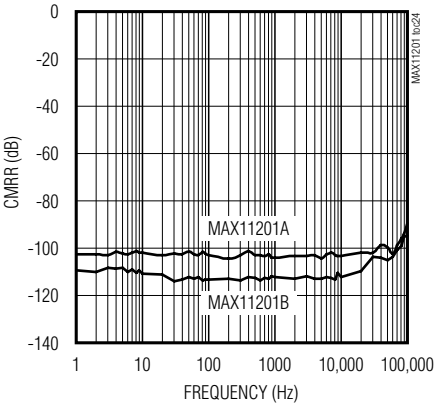
PSRR vs. FREQUENCY (MAX11201A)



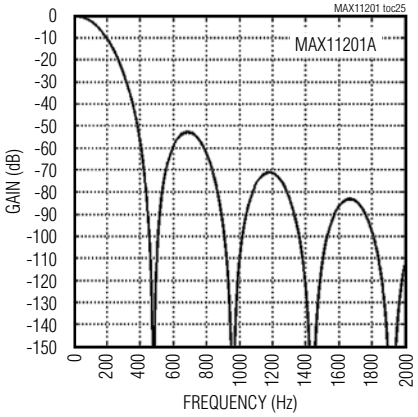
PSRR vs. FREQUENCY (MAX11201B)



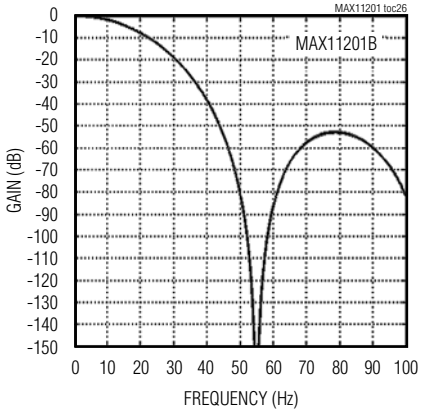
CMRR vs. FREQUENCY



NORMAL-MODE REJECTION DATA RATE 120.0SPS

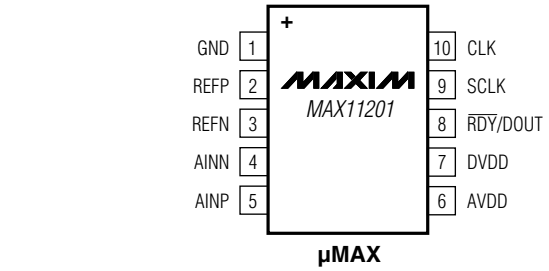


NORMAL-MODE REJECTION DATA RATE 13.750SPS



24-Bit, Single-Channel, Ultra-Low-Power, Delta Sigma ADC with 2-Wire Serial Interface

Pin Configuration

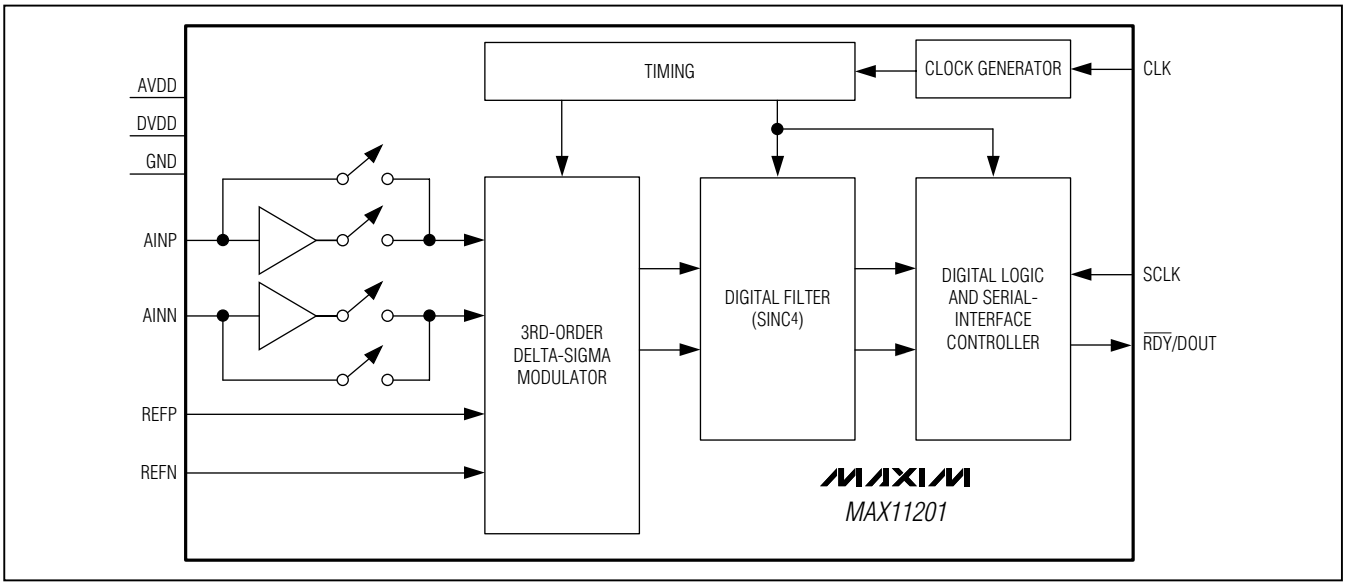


Pin Description

PIN	NAME	FUNCTION
1	GND	Ground. Ground reference for analog and digital circuitry.
2	REFP	Differential Reference Positive Input. REFP must be more positive than REFN. Connect REFP to a voltage between AVDD and GND.
3	REFN	Differential Reference Negative Input. REFN must be more negative than REFP. Connect REFN to a voltage between AVDD and GND.
4	AINN	Negative Fully Differential Analog Input
5	AINP	Positive Fully Differential Analog Input
6	AVDD	Analog Supply Voltage. Connect a supply voltage between +2.7V to +3.6V with respect to GND.
7	DVDD	Digital Supply Voltage. Connect a digital supply voltage between +1.7V to +3.6V with respect to GND.
8	$\overline{RDY}$/DOUT	Data Ready Output/Serial Data Output. This output serves a dual function. In addition to the serial data output function, the $\overline{RDY}$/DOUT also indicates that the data is ready when the $\overline{RDY}$ is logic-low. $\overline{RDY}$/DOUT changes on the rising edge of SCLK.
9	SCLK	Serial Clock Input. Apply an external serial clock to SCLK.
10	CLK	External Clock Signal Input. The internal clock shuts down when CLK is driven by an external clock. Use a 2.4576MHz oscillator (MAX11201A) or a 2.25275MHz oscillator (MAX11201B).

24-Bit, Single-Channel, Ultra-Low-Power, Delta Sigma ADC with 2-Wire Serial Interface

Functional Diagram



Detailed Description

The MAX11201 is an ultra-low-power (< 245µA active), high-resolution, low-speed, serial-output ADC. This device provides the highest resolution per unit power in the industry and is optimized for applications that require very high dynamic range with low power such as sensors on a 4mA to 20mA industrial control loop. The MAX11201 provides a high-accuracy internal oscillator, which requires no external components. When used with the specified data rates, the internal digital filter provides more than 100dB rejection of 50Hz or 60Hz line noise. The MAX11201 provides a simple, system-friendly, 2-wire serial interface in the space-saving, 10-pin µMAX package.

Power-On Reset (POR)

The MAX11201 utilizes power-on reset (POR) supply-monitoring circuitry on both the digital supply (DVDD) and the analog supply (AVDD). The POR circuitry ensures proper device default conditions after either a digital or analog power-sequencing event.

The MAX11201 performs a self-calibration operation as part of the startup initialization sequence whenever a digital POR is triggered. It is important to have a stable reference voltage available at the REFP and REFN pins to ensure an accurate calibration cycle. If the reference voltage is not stable during a POR event, the part should be calibrated once the reference has stabilized. The part can be programmed for calibration by using 26 SCLKs as shown in Figure 3.

The digital POR trigger threshold is approximately 1.2V and has 100mV of hysteresis. The analog POR trigger threshold is approximately 1.25V and has 100mV of hysteresis. Both POR circuits have lowpass filters that prevent high-frequency supply glitches from triggering the POR. The analog supply (AVDD) and the digital supply (DVDD) pins should be bypassed using 0.1µF capacitors placed as close as possible to the package pin.

Buffers

The MAX11201 includes signal input buffers capable of reducing the average input current from 1.4µA/V on the analog inputs to a constant 20nA. The MAX11201 analog inputs provide > 100MΩ input impedance for connecting directly to high-impedance sources.

Analog Inputs

The MAX11201 accepts two analog inputs (AINP and AINN). The modulator input range is bipolar ($-V_{REF}$ to $+V_{REF}$).

Internal Oscillator

The MAX11201 incorporates a highly stable internal oscillator that provides the system clock. The system clock runs the internal state machine and is trimmed to 2.4576MHz (MAX11201A) or 2.25275MHz (MAX11201B). The internal oscillator clock is divided down to run the digital and analog timing.

24-Bit, Single-Channel, Ultra-Low-Power, Delta Sigma ADC with 2-Wire Serial Interface

Reference

The MAX11201 provides differential inputs REFP and REFN for an external reference voltage. Connect the external reference directly across the REFP and REFN to obtain the differential reference voltage. The common-mode voltage range for V_{REFP} and V_{REFN} is between 0 and V_{AVDD}. The differential voltage range for REFP and REFN is 1.25V to V_{AVDD}.

Digital Filter

The MAX11201 contains an on-chip, digital lowpass filter that processes the 1-bit data stream from the modulator using a $SINC^4$ $(sinx/x)^4$ response. When the device is operating in single-cycle conversion mode, the filter is reset at the end of the conversion cycle. When operating in continuous conversion latent mode, the filter is not reset. The $SINC^4$ filter has a -3dB frequency equal to 24% of the data rate.

Data Output

The data output is clocked out on $\overline{RDY}$/DOUT. D23 is the MSB and D0 is the LSB. The data format is always two's complement. In two's complement format, the most negative value is 0x800000 (V_{AINP} - V_{AINN} = -V_{REF}), the midscale value is 0x000000 (AINP - AINN = 0), and the most positive value is 0x7FFFFF (V_{AINP} - V_{AINN} = V_{REF}). Any input exceeding the available input range is limited to the minimum or maximum data value.

Table 1. Output Data Format

INPUT VOLTAGE V_{AINP} - V_{AINN}	DIGITAL OUTPUT CODE
≥ V_{REF}	0x7FFFFF
$V_{REF} \times \left(1 - \frac{1}{2^{23}-1}\right)$	0x7FFFFE
$\frac{V_{REF}}{2^{23}-1}$	0x000001
0	0x000000
$\frac{-V_{REF}}{2^{23}-1}$	0xFFFFFF
$V_{REF} \times \left(1 - \frac{1}{2^{23}-1}\right)$	0x800001
≤ -V_{REF}	0x800000

Serial-Digital Interface

The MAX11201 communicates through a 2-wire interface, with a clock input and data output. The output rate is predetermined based on the package option (MAX11201A at 120sps and MAX11201B at 13.75sps).

2-Wire Interface

The MAX11201 is compatible with the 2-wire interface and uses SCLK and $\overline{RDY}$/DOUT for serial communications. In this mode, all controls are implemented by timing the high or low phase of the SCLK. The 2-wire serial interface only allows for data to be read out through the $\overline{RDY}$/DOUT output. Supply the serial clock to SCLK to shift the conversion data out.

The $\overline{RDY}$/DOUT is used to signal data ready, as well as reading the data out when SCLK pulses are applied. $\overline{RDY}$/DOUT is high by default. The MAX11201 pulls $\overline{RDY}$/DOUT low when data is available at the end of conversion, and stays low until clock pulses are applied at the SCLK input. On applying the clock pulses at SCLK, the $\overline{RDY}$/DOUT outputs the conversion data on every SCLK positive edge. To monitor data availability, pull $\overline{RDY}$/DOUT high after reading the 24 bits of data by supplying a 25th SCLK pulse.

The different operational modes using this 2-wire interface are described in the following sections.

Data Read Following Every Conversion

The MAX11201 indicates conversion data availability, as well as the retrieval of data through the $\overline{RDY}$/DOUT output. The $\overline{RDY}$/DOUT output idles at the value of the last bit read unless a 25th SCLK pulse is provided, causing $\overline{RDY}$/DOUT to idle high.

The timing diagram for the data read is shown in Figure 1. Once a low is detected on $\overline{RDY}$/DOUT, clock pulses at SCLK clock out the data. Data is shifted out MSB first and is in binary two's complement format. Once all the data has been shifted out, a 25th SCLK is required to pull the $\overline{RDY}$/DOUT output back to the idle high state. See Figure 2.

If the data is not read before the next conversion data is updated, the old data is lost, as the new data overwrites the old value.

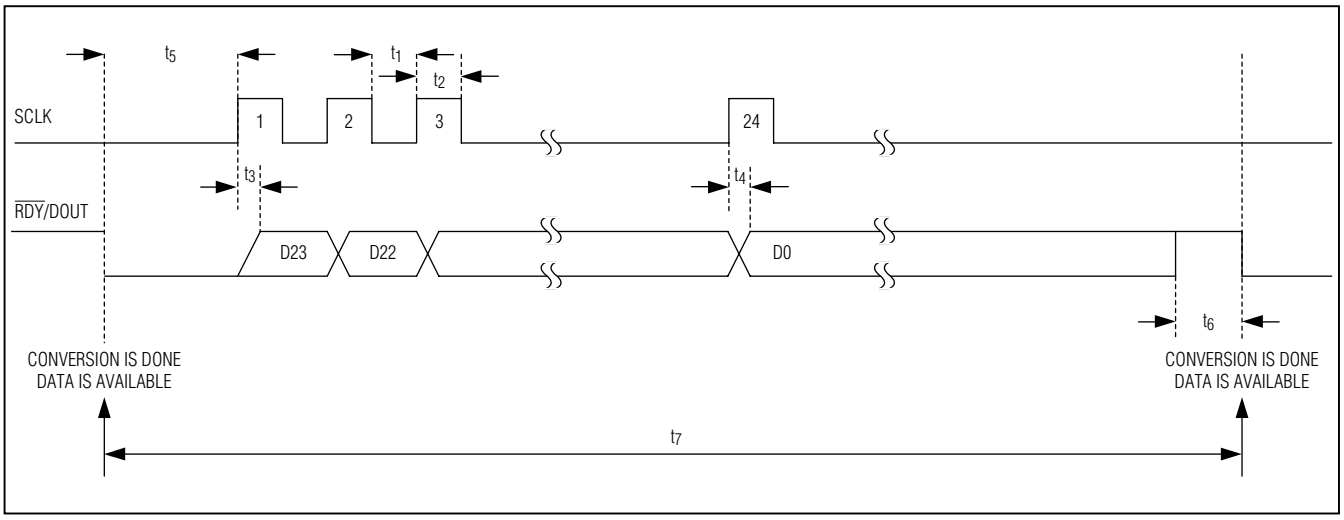


Figure 1. Timing Diagram for Data Read After Conversion

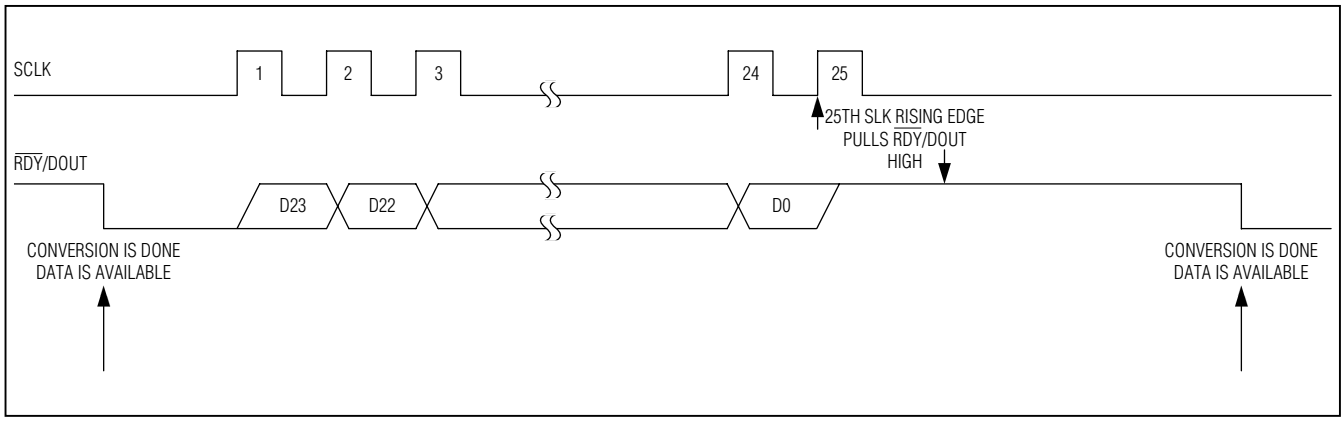


Figure 2. Timing Diagram for Data Read Followed by RDY/DOUT Being Asserted High Using 25th SCLK

Data Read Followed by Self-Calibration

To initiate self-calibration at the end of a data read, provide a 26th SCLK clock pulse. After reading the 24 bits of conversion data, a 25th positive edge on SCLK pulls the RDY/DOUT output back high, indicating the end of the data read. Provide a 26th SCLK clock pulse to initiate a self-calibration routine starting on the falling edge of the SCLK. A subsequent falling edge of RDY/DOUT indicates data availability at the end of calibration. The timing is illustrated in Figure 3.

Data Read Followed by Sleep Mode

The MAX11201 can be put into sleep mode to save power between conversions. To activate the sleep mode, idle the SCLK high any time after the RDY/DOUT output goes low (that is, after conversion data is available). It is not required to read out all 24 bits before putting the part in sleep mode. Sleep mode is activated after the SCLK is held high (see Figure 4). The RDY/DOUT output is pulled high once the device enters sleep mode. To come out of the sleep mode, pull SCLK low. After the sleep mode is deactivated (when the device wakes up), conversion starts again and RDY/DOUT goes low, indicating the next conversion data is available (see Figure 4).

Single-Conversion Mode

For operating the MAX11201 in single-conversion mode, activate and deactivate sleep mode between conversions as described in the *Data Read Followed by Sleep Mode* section). Single-conversion mode reduces power consumption by shutting down the device when idle between conversions. See Figure 4.

24-Bit, Single-Channel, Ultra-Low-Power, Delta Sigma ADC with 2-Wire Serial Interface

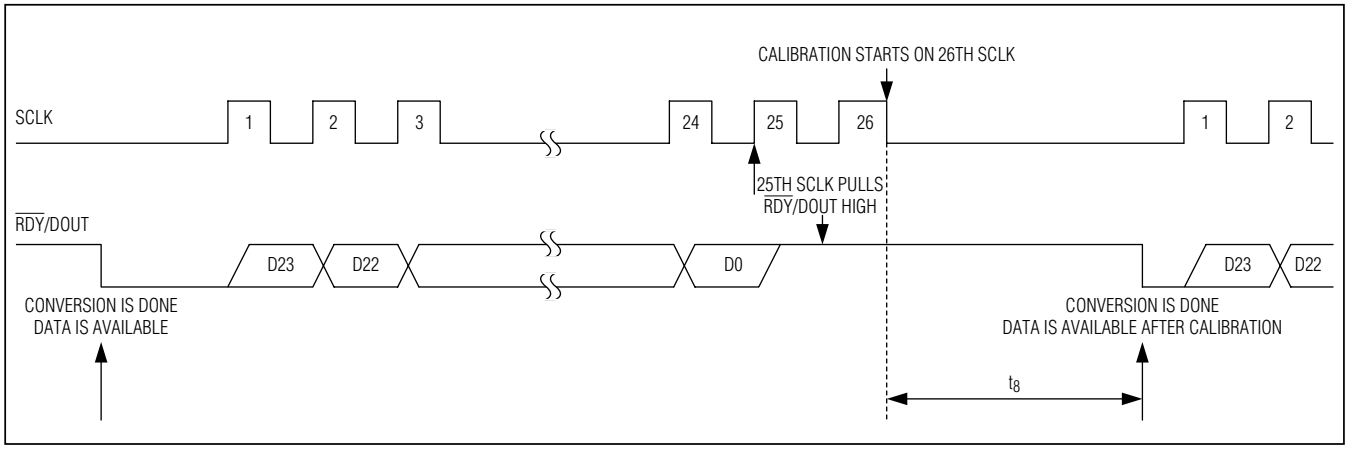


Figure 3. Timing Diagram for Data Read Followed by Two Extra Clock Cycles for Self-Calibration

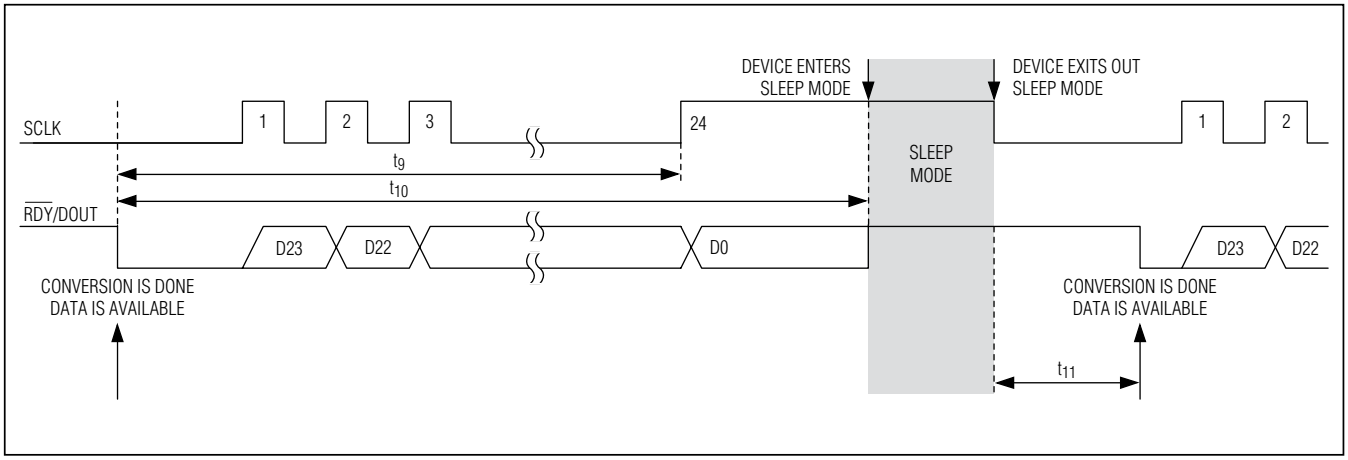


Figure 4. Timing Diagram for Data Read Followed by Sleep Mode Activation; Single Conversion Timing

Single-Conversion Mode with Self-Calibration at Wake-Up

The MAX11201 can be put in self-calibration mode immediately after wake-up from sleep mode. Self-calibration at wake-up helps to compensate for temperature or supply changes if the device is shut down for extensive periods. To automatically start self-calibration at the end of sleep mode, all the data bits must be shifted out followed by the 25th SCLK edge to pull $\overline{RDY}$/DOUT high. On the 26th SCLK, keep it high for as long as shutdown is desired. Once SCLK is pulled back low, the device automatically performs a self-calibration and, when the data is ready, the $\overline{RDY}$/DOUT output goes low. See Figure 5. This also achieves the purpose of single conversions with self-calibration.

24-Bit, Single-Channel, Ultra-Low-Power, Delta Sigma ADC with 2-Wire Serial Interface

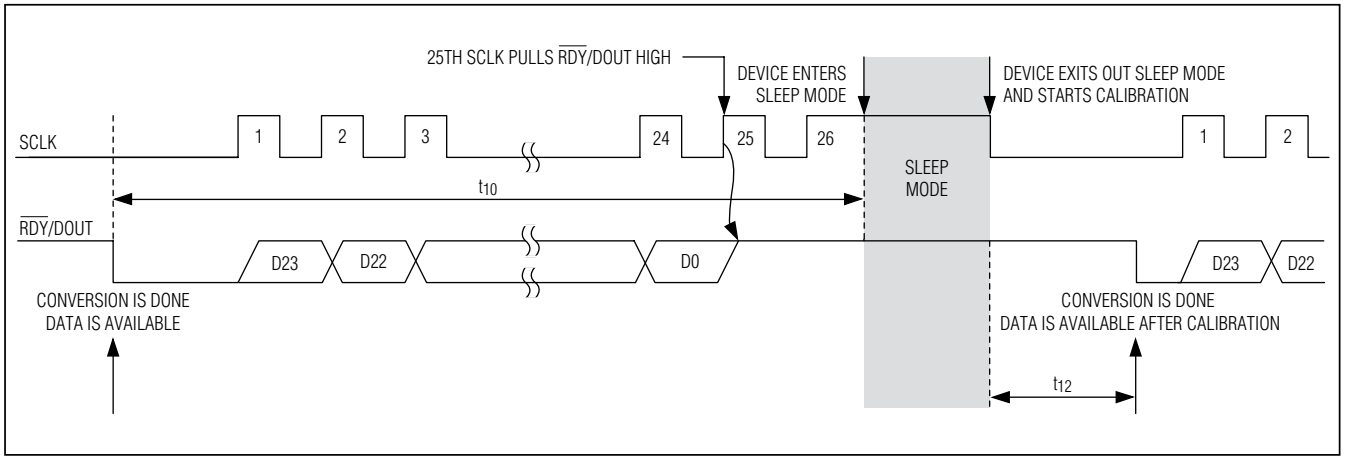


Figure 5. Timing Diagram for Sleep Mode Activation Followed by Self-Calibration at Wake-Up

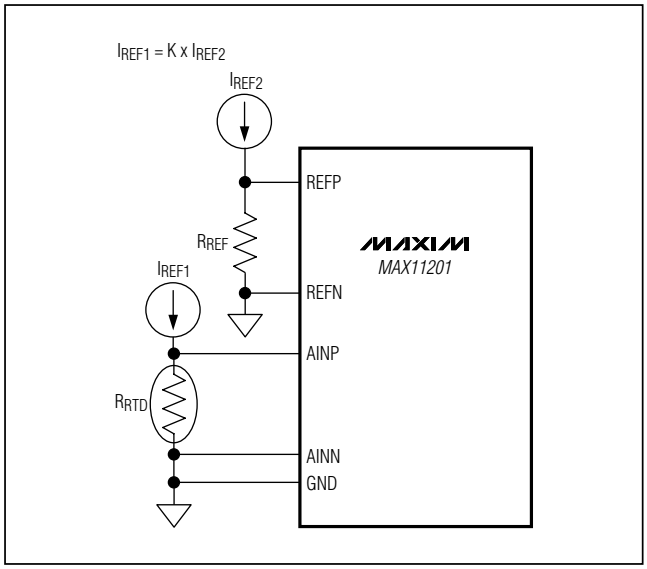


Figure 6. RTD Temperature Measurement Circuit

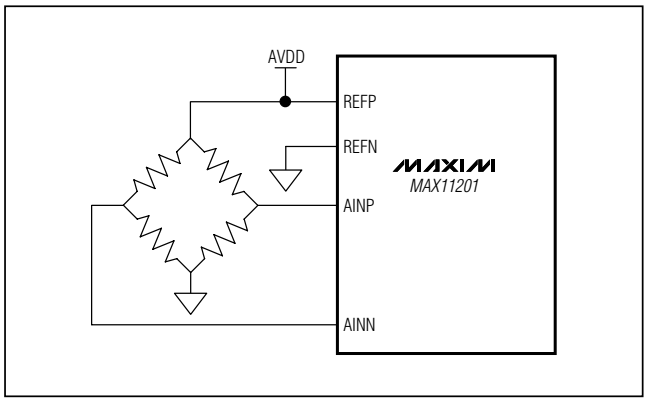


Figure 7. Resistive Bridge Measurement Circuit

Applications Information

See Figure 6 for the RTD temperature measurement circuit and Figure 7 for a resistive bridge measurement circuit.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 µMAX	U10+2	21-0061	90-0330

24-Bit, Single-Channel, Ultra-Low-Power, Delta Sigma ADC with 2-Wire Serial Interface

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/10	Initial release	—

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

© 2010 Maxim Integrated Products Maxim is a registered trademark of Maxim Integrated Products, Inc.

AMEYA360
Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com