

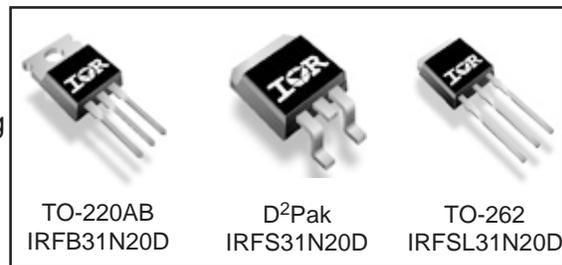
Applications

- High frequency DC-DC converters

| | | |
|------------------------|-------------------------------|----------------------|
| V_{DSS} | R_{DS(on)} max | I_D |
| 200V | 0.082Ω | 31A |

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{oss} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|------------------------|--------------|
| I _D @ T _C = 25°C | Continuous Drain Current, V _{GS} @ 10V | 31 | A |
| I _D @ T _C = 100°C | Continuous Drain Current, V _{GS} @ 10V | 21 | |
| I _{DM} | Pulsed Drain Current ① | 124 | |
| P _D @ T _A = 25°C | Power Dissipation ② | 3.1 | W |
| P _D @ T _C = 25°C | Power Dissipation | 200 | |
| | Linear Derating Factor | 1.3 | W/°C |
| V _{GS} | Gate-to-Source Voltage | ± 30 | V |
| dv/dt | Peak Diode Recovery dv/dt ③ | 2.1 | V/ns |
| T _J | Operating Junction and | -55 to + 175 | °C |
| T _{STG} | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |
| | Mounting torque, 6-32 or M3 screw④ | 10 lbf•in (1.1N•m) | |

Typical SMPS Topologies

- Telecom 48V Input Forward Converters

Notes ① through ④ are on page 11
 www.irf.com

IRFB/IRFS/IRFSL31N20D

International
IR Rectifier

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------------------|--------------------------------------|------|------|-------|----------|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 200 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.25 | — | V/°C | Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.082 | Ω | $V_{GS} = 10V, I_D = 18A$ ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 3.0 | — | 5.5 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 25 | μA | $V_{DS} = 200V, V_{GS} = 0V$ |
| | | — | — | 250 | | $V_{DS} = 160V, V_{GS} = 0V, T_J = 150^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 30V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = -30V$ |

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|------------------------|---------------------------------|------|------|------|-------|---|
| g_{fs} | Forward Transconductance | 17 | — | — | S | $V_{DS} = 50V, I_D = 18A$ |
| Q_g | Total Gate Charge | — | 70 | 110 | nC | $I_D = 18A$ |
| Q_{gs} | Gate-to-Source Charge | — | 18 | 27 | | $V_{DS} = 160V$ |
| Q_{gd} | Gate-to-Drain ("Miller") Charge | — | 33 | 49 | | $V_{GS} = 10V,$ ④ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 16 | — | ns | $V_{DD} = 100V$ |
| t_r | Rise Time | — | 38 | — | | $I_D = 18A$ |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 26 | — | | $R_G = 2.5\Omega$ |
| t_f | Fall Time | — | 10 | — | | $R_D = 5.4\Omega$ ④ |
| C_{iss} | Input Capacitance | — | 2370 | — | pF | $V_{GS} = 0V$ |
| C_{oss} | Output Capacitance | — | 390 | — | | $V_{DS} = 25V$ |
| C_{rss} | Reverse Transfer Capacitance | — | 78 | — | | $f = 1.0\text{MHz}$ |
| C_{oss} | Output Capacitance | — | 2860 | — | | $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$ |
| C_{oss} | Output Capacitance | — | 150 | — | | $V_{GS} = 0V, V_{DS} = 160V, f = 1.0\text{MHz}$ |
| $C_{oss \text{ eff.}}$ | Effective Output Capacitance | — | 170 | — | | $V_{GS} = 0V, V_{DS} = 0V \text{ to } 160V$ ⑤ |

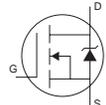
Avalanche Characteristics

| | Parameter | Typ. | Max. | Units |
|----------|--------------------------------|------|------|-------|
| E_{AS} | Single Pulse Avalanche Energy② | — | 420 | mJ |
| I_{AR} | Avalanche Current① | — | 18 | A |
| E_{AR} | Repetitive Avalanche Energy① | — | 20 | mJ |

Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|-----------------|---------------------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case | — | 0.75 | °C/W |
| $R_{\theta CS}$ | Case-to-Sink, Flat, Greased Surface ⑥ | 0.50 | — | |
| $R_{\theta JA}$ | Junction-to-Ambient⑥ | — | 62 | |
| $R_{\theta JA}$ | Junction-to-Ambient⑦ | — | 40 | |

Diode Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|--|---|------|------|---------|--|
| I_S | Continuous Source Current (Body Diode) | — | — | 31 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I_{SM} | Pulsed Source Current (Body Diode) ① | — | — | 124 | | |
| V_{SD} | Diode Forward Voltage | — | — | 1.3 | V | $T_J = 25^\circ\text{C}, I_S = 18A, V_{GS} = 0V$ ④ |
| t_{rr} | Reverse Recovery Time | — | 200 | 300 | ns | $T_J = 25^\circ\text{C}, I_F = 18A$ |
| Q_{rr} | Reverse Recovery Charge | — | 1.7 | 2.6 | μC | $di/dt = 100A/\mu s$ ④ |
| t_{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$) | | | | |

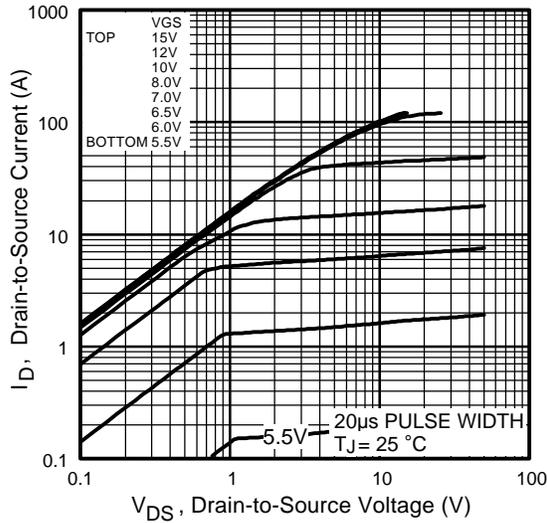


Fig 1. Typical Output Characteristics

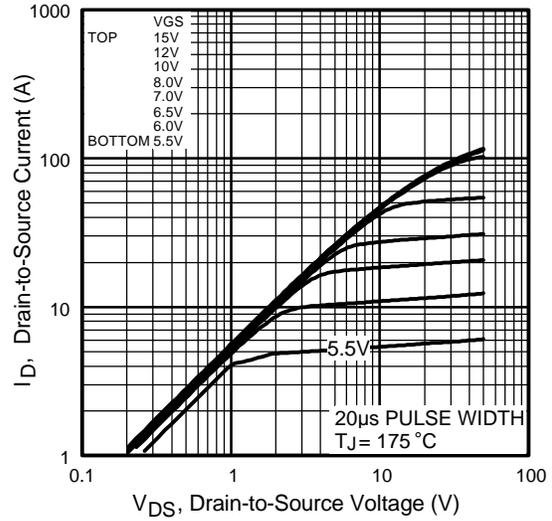


Fig 2. Typical Output Characteristics

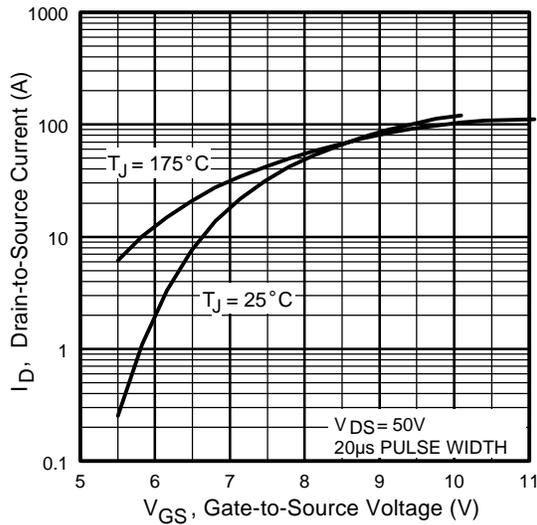


Fig 3. Typical Transfer Characteristics

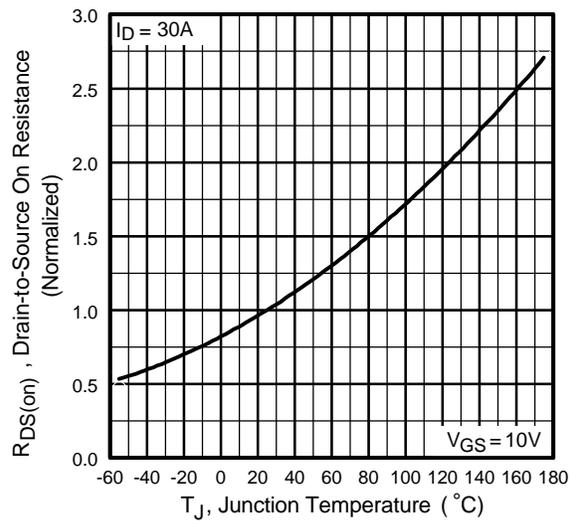


Fig 4. Normalized On-Resistance Vs. Temperature

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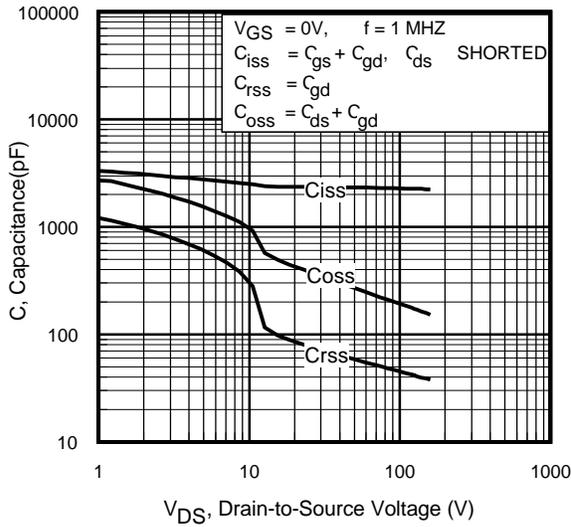


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

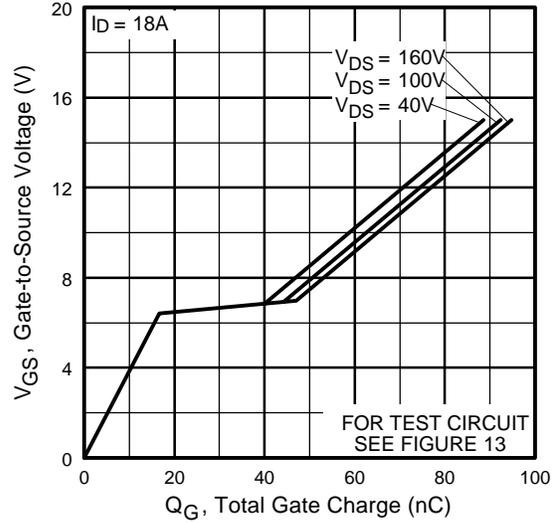


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

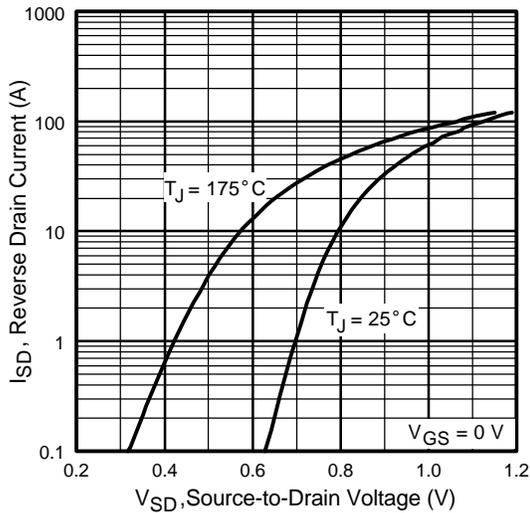


Fig 7. Typical Source-Drain Diode Forward Voltage

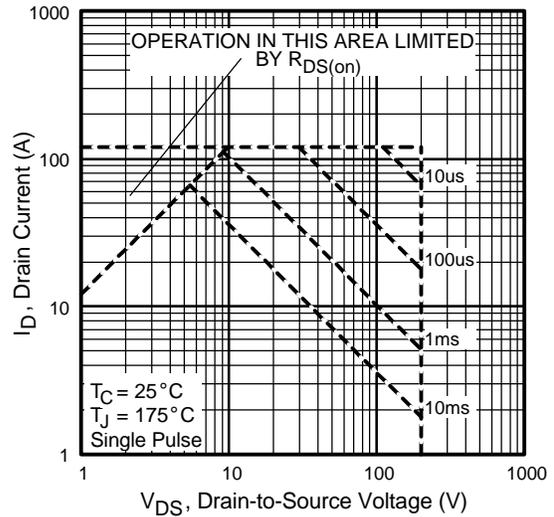


Fig 8. Maximum Safe Operating Area

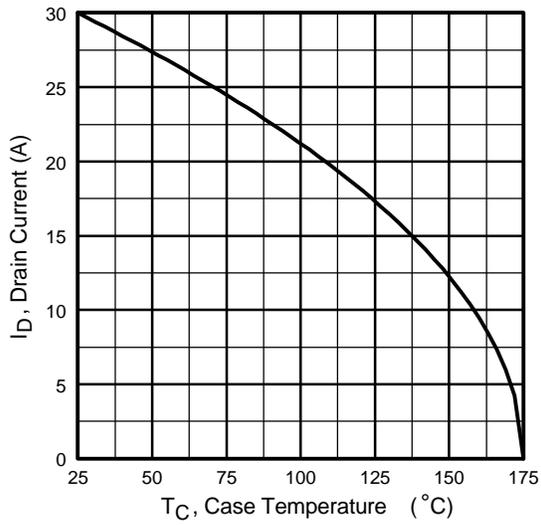


Fig 9. Maximum Drain Current Vs. Case Temperature

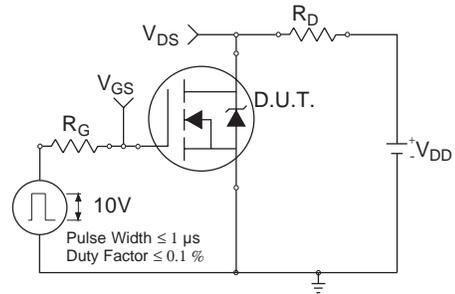


Fig 10a. Switching Time Test Circuit

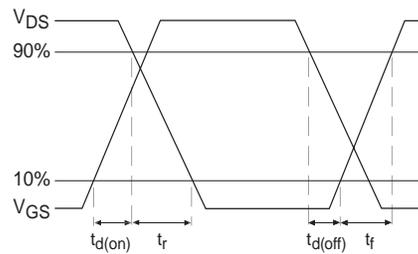


Fig 10b. Switching Time Waveforms

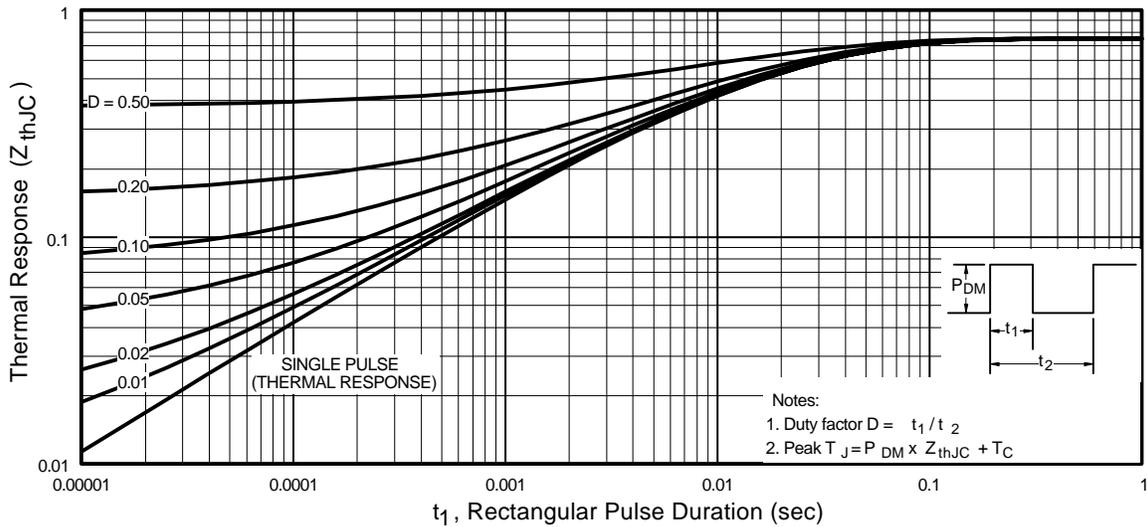


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRFB/IRFS/IRFSL31N20D

International
IR Rectifier

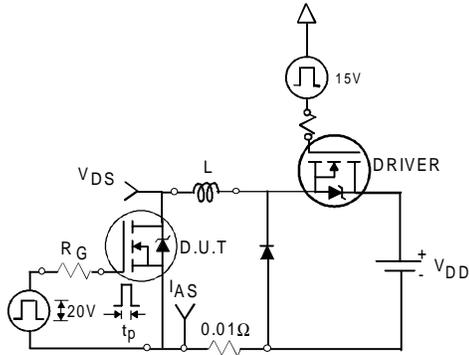


Fig 12a. Unclamped Inductive Test Circuit

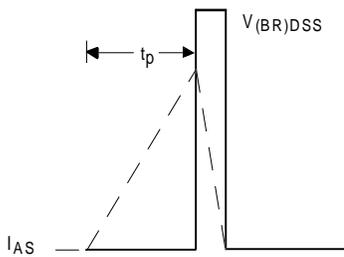


Fig 12b. Unclamped Inductive Waveforms

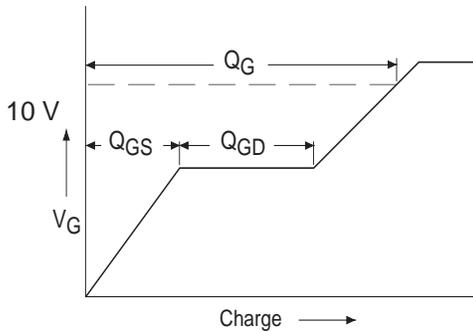


Fig 13a. Basic Gate Charge Waveform

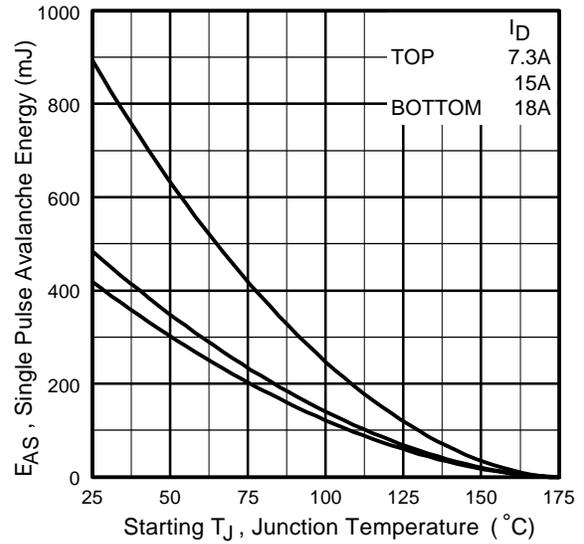


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

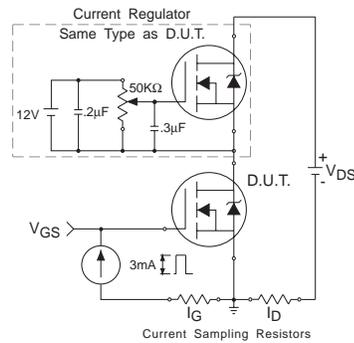
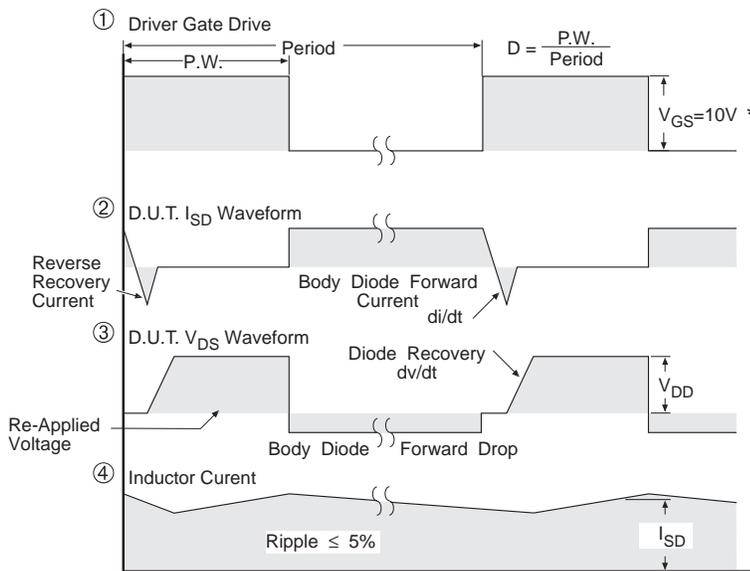
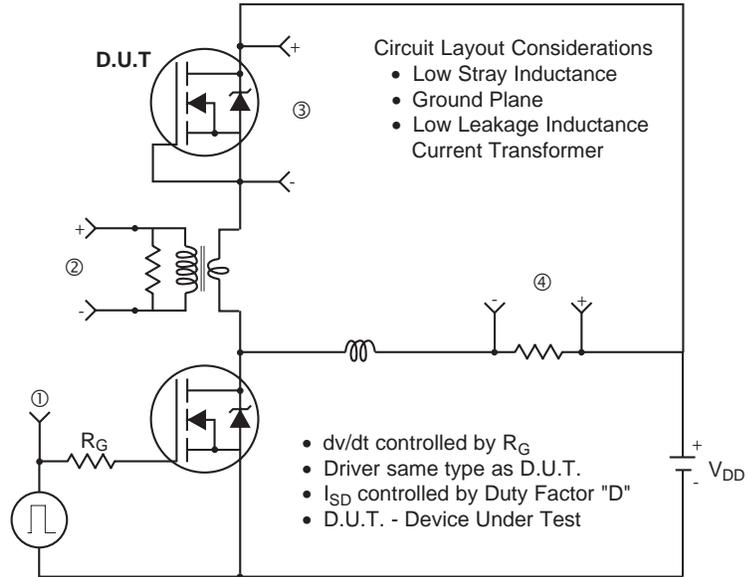


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

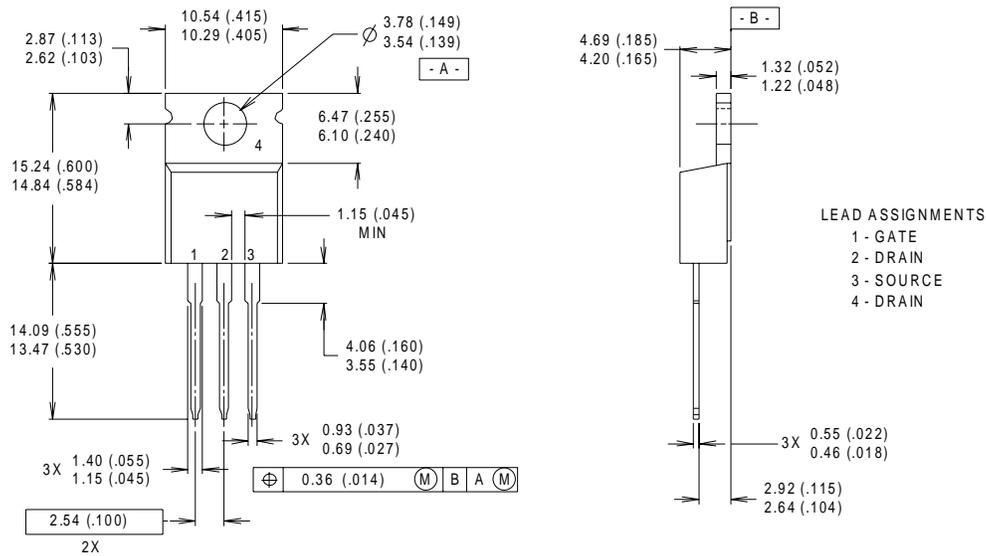
Fig 14. For N-channel HEXFET® Power MOSFETs

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TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

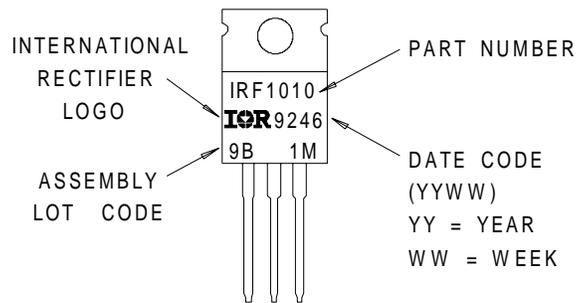


NOTES:

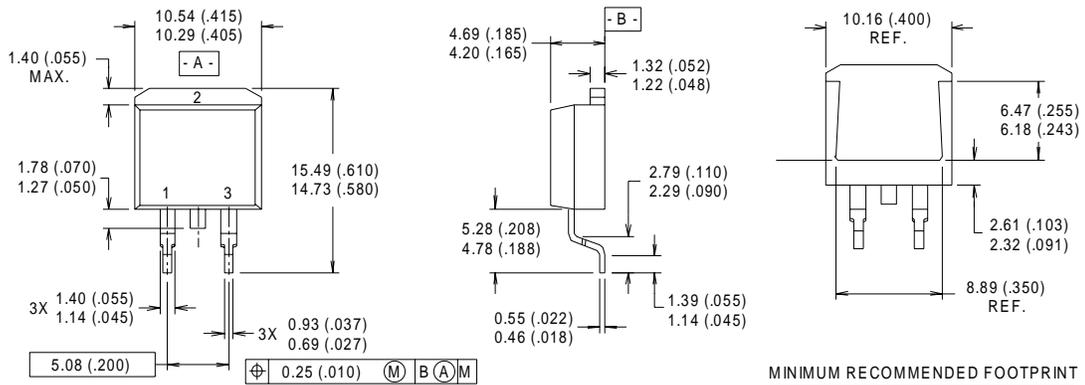
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



D²Pak Package Outline



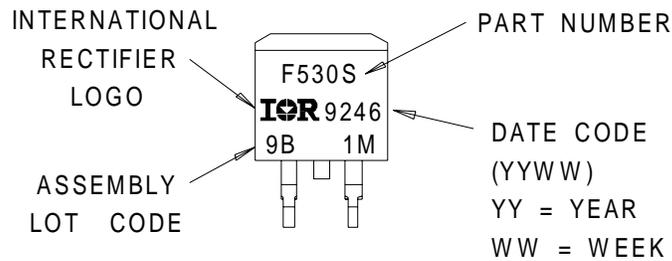
NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

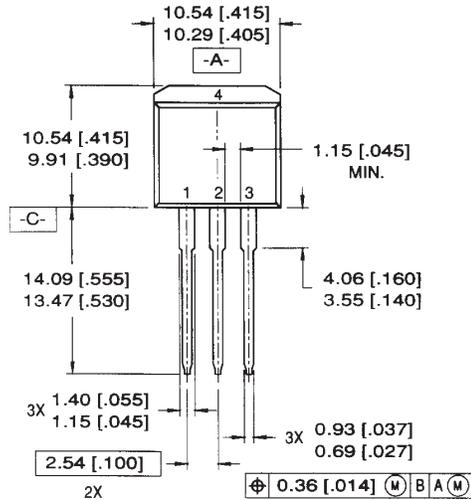
D²Pak Part Marking Information



IRFB/IRFS/IRFSL31N20D

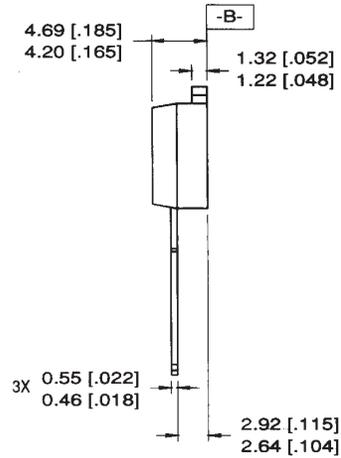


TO-262 Package Outline



LEAD ASSIGNMENTS

- 1 = GATE 3 = SOURCE
- 2 = DRAIN 4 = DRAIN

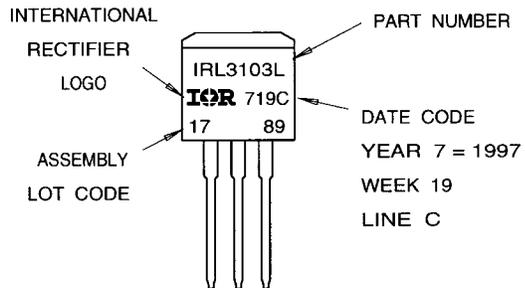


NOTES:

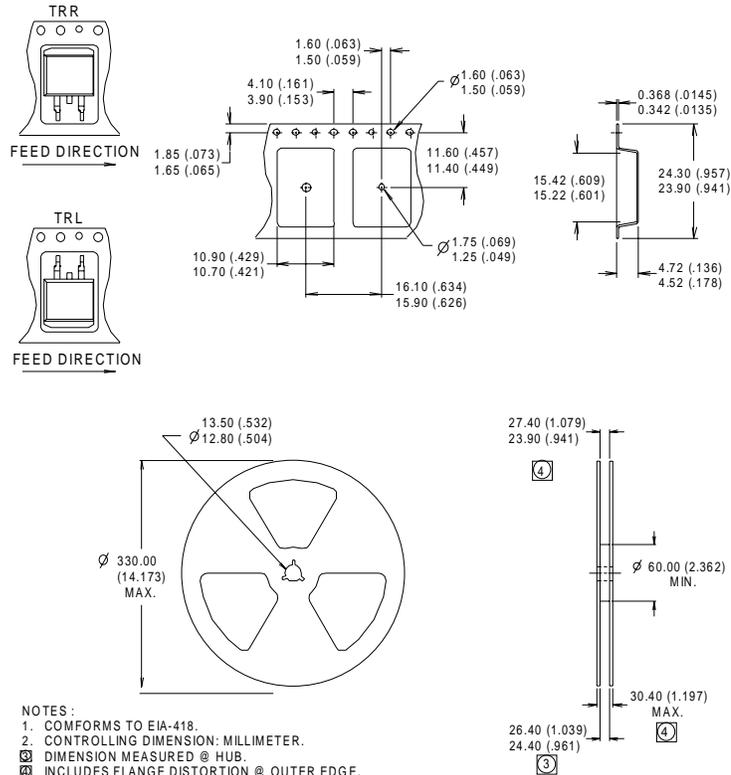
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



D²Pak Tape & Reel Information



- NOTES:
 1. CONFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 ③ DIMENSION MEASURED @ HUB.
 ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 3.8\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 18\text{A}$.
- ③ $I_{SD} \leq 18\text{A}$, $di/dt \leq 110\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ This is only applied to TO-220AB package
- ⑦ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
 For recommended footprint and soldering techniques refer to application note #AN-994.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

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