850 – 950 MHz RF Front End

Check for Samples: CC1190

FEATURES

- Seamless Interface to Sub-1 GHz Low Power RF Devices from Texas Instruments
- Up to 27 dBm (0.5 W) Output Power
- 6 dB Typical Sensitivity Improvement with CC11xx and CC430
- Few External Components
  - Integrated PA
  - Integrated LNA
  - Integrated Switches
  - Integrated Matching Network
  - Integrated Inductors
- Digital Control of LNA and PA Gain by HGM Pin
- 50-nA in Power Down (LNA_EN = PA_EN = 0)
- High Transmit Power Efficiency
  - PAE = 50% at 26 dBm Output Power
- Low Receive Current Consumption
  - 3 mA for High Gain Mode
  - 26 μA for Low Gain Mode
- 2.9 dB LNA Noise Figure, Including Switch and External Antenna Match
- RoHS Compliant 4-mm × 4-mm QFN-16 Package
- 2 V to 3.7 V Operation

APPLICATIONS

- 850 - 950 MHz ISM Bands Wireless Systems
- Wireless Sensor Networks
- Wireless Industrial Systems
- IEEE 802.15.4 Systems
- Wireless Consumer Systems
- Wireless Metering (AMR/AMI) Systems
- Smart Grid Wireless Networks

DESCRIPTION

CC1190 is a cost-effective and high-performance RF Front End for low-power and low-voltage wireless applications at 850 - 950 MHz.

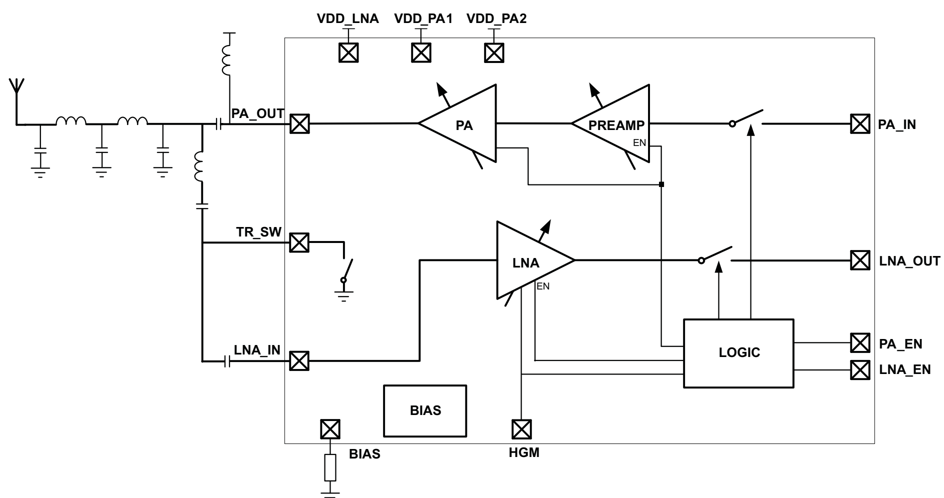
CC1190 is a range extender for the sub-1 GHz low-power RF transceivers, transmitters, and System-on-Chip devices from Texas Instruments.

CC1190 integrates a power amplifier (PA), a low-noise amplifier (LNA), switches, and RF matching for the design of a high-performance wireless systems.

CC1190 increases the link budget by providing a power amplifier for increased output power, and an LNA with low noise figure for improved receiver sensitivity.

CC1190 provides an efficient and easy-to-use range extender in a compact 4-mm × 4-mm QFN-16 package.

CC1190 BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

DEVICE	TEMPERATURE	PACKAGE (1)	TRANSPORTION MEDIA
CC1190RGVR	-40°C to 85°C	QFN (RVG) 16	Tape and Reel, 2500
CC1190RGVT			Tape and Reel, 250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Under no circumstances must the absolute maximum ratings be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

		VALUE	UNIT
Supply voltage, V_{DD}	All supply pins must have the same voltage	–0.3 to 3.8	V
Voltage on any digital pin		–0.3 to VDD + 0.3, max 3.8	V
Input RF level		10	dBm
Storage temperature range		–50 to 150	°C
ESD	Human-body model, non RF pins	2000	V
	Human-body model, RF pins: PA_IN, PA_OUT, TR_SW, LNA_IN, LNA_OUT	1500	V
	Charged device model	1000	V

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Ambient temperature range	–40	85	°C
Operating supply voltage	2	3.7	V
Operating frequency range	850	950	MHz

ELECTRICAL CHARACTERISTICS

T_C = 25°C, VDD = 3 V, f_{RF} = 915 MHz (unless otherwise noted). Measured on CC1190EM reference design including external matching components *optimized for 915 MHz operation*.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receive current	P_{IN} = -40 dBm, HGM = 1		3		mA
	P_{IN} = -40 dBm, HGM = 0		26		µA
Transmit current	P_{IN} = 5 dBm, POUT = 26.5 dBm, HGM = 1		302		mA
	No input signal, HGM = 1		56		
	No input signal, HGM = 0		29		
Power down current	LNA_EN = PA_EN = 0		50	200	nA
High input level (control pins)	HGM, LNA_EN, PA_EN	1.3		VDD	V
Low input level (control pins)	HGM, LNA_EN, PA_EN			0.3	V
Power down → Receive mode, switching time			300		ns
Power down → Transmit mode, switching time			600		ns

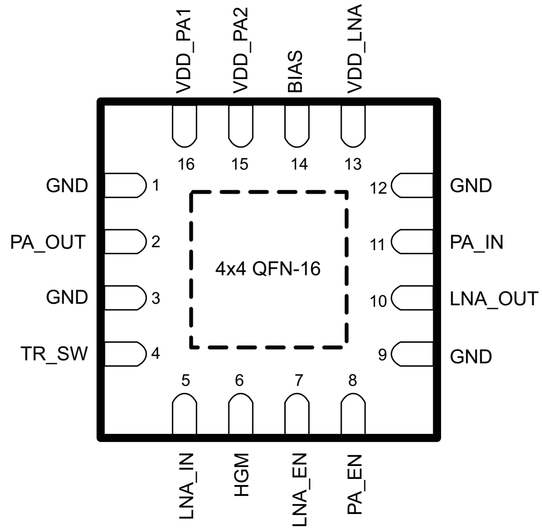
ELECTRICAL CHARACTERISTICS (continued)

T_C = 25°C, VDD = 3 V, f_{RF} = 915 MHz (unless otherwise noted). Measured on CC1190EM reference design including external matching components *optimized for 915 MHz operation*.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RF Receive					
Gain	P_{IN} = -40 dBm, HGM = 1		11.6		dB
	P_{IN} = -40 dBm, HGM = 0		-6		
Gain variation over frequency	850–950 MHz, P_{IN} = -40 dBm, HGM = 1		1.2		dB
Gain variation over power supply	2 – 3.7 V, P_{IN} = -40 dBm, HGM = 1		1		dB
Noise figure	HGM = 1, including internal switch and external antenna match		2.9		dB
	HGM = 0, including internal switch and external antenna match		6.2		dBm
Input 1 dB compression	HGM = 1		-12.3		dBm
	HGM = 0		11.2		
Input IP3, High Gain Mode	HGM = 1		-5		dBm
Input reflection coefficient, S11, High Gain Mode	HGM = 1, measured at antenna port, depends on external antenna and LNA match		-11.5		dB
RF Transmit					
Gain	P_{IN} = -20 dBm, HGM = 1		27.9		dB
	P_{IN} = -20 dBm, HGM = 0		24.6		
Maximum Output Power	P_{IN} = 5 dBm, HGM = 1, VDD = 3.7 V		27.7		dBm
Output power, POUT	P_{IN} = 5 dBm, HGM = 1		26.5		dBm
	P_{IN} = 0 dBm, HGM = 1		25.5		
	P_{IN} = -6 dBm, HGM = 1		22		
Power Added Efficiency, PAE	P_{IN} = 5 dBm, HGM = 1		48%		
Output 1 dB compression	HGM = 1		24		dBm
	HGM = 0		23.7		
Output power variation over frequency	850 – 950 MHz, PIN = 5 dBm, HGM = 1		1.7		dB
Output power variation over power supply	2 V – 3.7 V, PIN = 5 dBm, HGM = 1		4.5		dB
Output power variation over temperature	-40°C – 85°C, PIN = 5 dBm, HGM = 1		1		dB
2nd harmonic power	HGM = 1, PIN = 5 dBm See application note AN001 (SWRA090) for regulatory requirements.		2.5		dBm
3rd harmonic power			-37		
Input reflection coefficient, S11	HGM = 1, measured at SMA connector on PA_IN/LNA_OUT (TX active)		-10		dB

DEVICE INFORMATION

QFN-16 PACKAGE
TOP VIEW



NOTE

The exposed die attach pad *must* be connected to a solid ground plane as this is the primary ground connection for the chip. Inductance in vias to the pad should be minimized. *Following the CC1190EM reference layout is recommended*. Changes will alter the performance. Also see the PCB land pattern information in this data sheet.

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NO.	NAME		
-	GND	Ground	The exposed die attach pad must be connected to a solid ground plane. See CC1190EM (SWRR064) reference design for recommended layout.
1	GND	Ground	Secondary ground connection. Should be shorted to the die attach pad on the top PCB layer.
2	PA_OUT	RF	Output of PA.
3	GND	Ground	Secondary ground connection. Should be shorted to the die attach pad on the top PCB layer.
4	TR_SW	RF	RXTX switch pin.
5	LAN_IN	RF	Input of LNA.
6	HGM	Digital Input	Digital control pin. HGM = 1 → Device in High Gain Mode. HGM = 0 → Device in Low Gain Mode.
7	LNA_EN	Digital Input	Digital control pin. See Table 2 and Table 3 for details.
8	PA_EN	Digital Input	Digital control pin. See Table 2 and Table 3 for details.
9	GND	Ground	Secondary ground connection. Should be shorted to the die attach pad on the top PCB layer.
10	LNA_OUT	RF	Output of LNA.
11	PA_IN	RF	Input of PA.
12	GND	Ground	Secondary ground connection. Should be shorted to the die attach pad on the top PCB layer.
13	VDD_LNA	Power	2 – 3.7 V Supply Voltage.
14	BIAS	Analog	Biasing input. Resistor between this node and ground sets bias current.
15	VDD_PA2	Power	2 – 3.7 V Supply Voltage.
16	VDD_PA1	Power	2 – 3.7 V Supply Voltage.

CC1190EM Evaluation Module

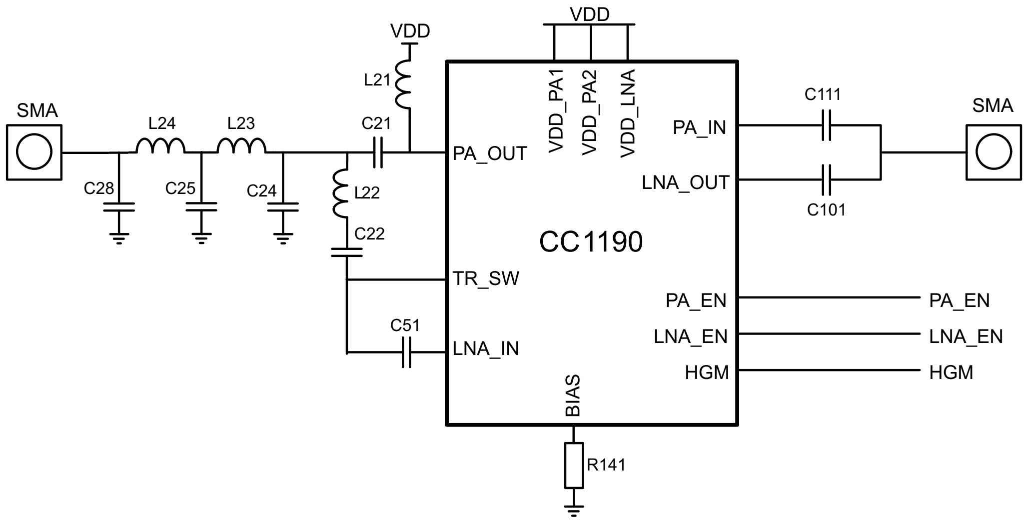


Figure 1. CC1190EM Evaluation Module

Table 1. List of Materials Optimized for 915 MHz Operation (See the CC1190EM Reference Design, SWRR064)

DEVICE	FUNCTION	VALUE
L21	PA load inductor	10 nH, LQW18AN10NG10 from Murata
L22	RXTX switch and LNA match	7.5 nH, LQW15AN7N5G00 from Murata
L23	Part of antenna match	2.2 nH, LQW15AN2N2C10D from Murata
L24	Part of antenna match	3.9 nH, LQW15AN3N9C00 from Murata
C21	DC block	47 pF, GRM1555C1H470JZ01D from Murata
C22	RXTX switch and LNA match	12 pF, GRM1555C1H120JZ01D from Murata
C24	Part of antenna match	3.3 pF: GRM1555C1H3R3CZ01D from Murata
C25	Part of antenna match	8.2 pF: GRM1555C1H8R2CZ01D from Murata
C28	Part of antenna match	0.5 pF, GRM1555C1HR50CZ01D from Murata
C51	Part of LNA match	12 pF, GRM1555C1H120JZ01D from Murata
C101	DC block	47 pF: GRM1555C1H470JZ01D from Murata
C111	DC block	47 pF: GRM1555C1H470JZ01D from Murata
R141	Bias resistor	3.3 kΩ, RK73H1ETTP3301F from Koa

TYPICAL CHARACTERISTICS

T_C = 25°C, V_{DD} = 3 V, f_{RF} = 915 MHz (unless otherwise noted). Measured on CC1190EM reference design including external matching components optimized for 915 MHz operation.

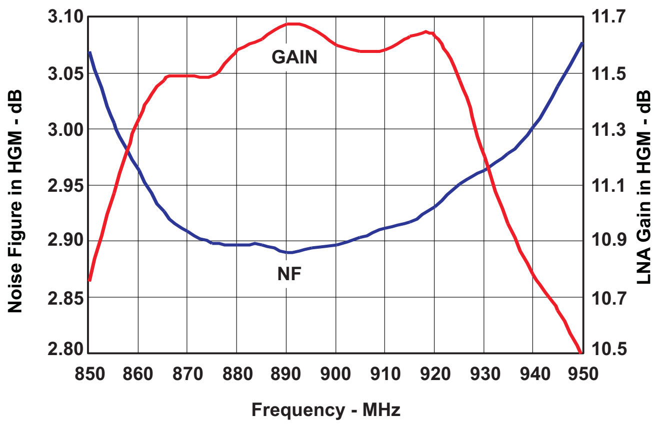


Figure 2. LNA Gain and Noise Figure vs Operating Frequency

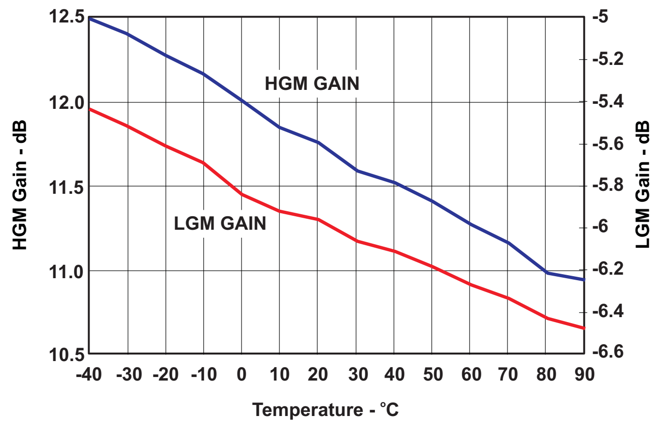


Figure 3. LNA Gain vs Temperature

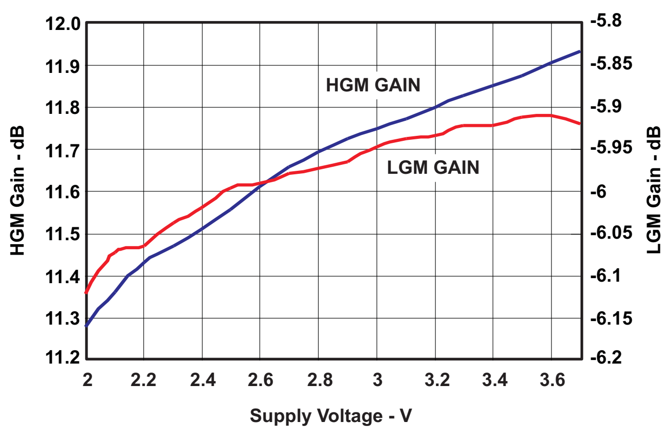


Figure 4. LNA Gain vs Supply Voltage

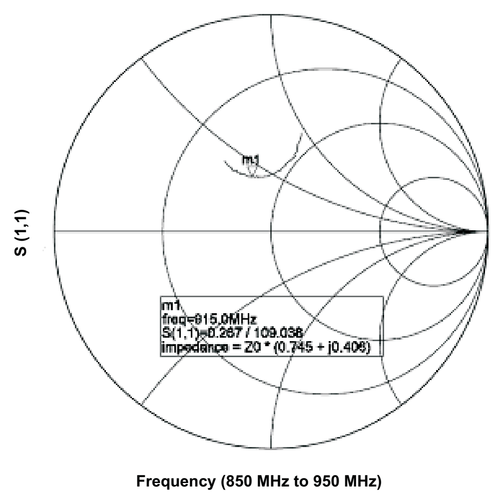


Figure 5. Input Impedance of LNA Measured from Antenna Port on CC1190EM (RX Active)

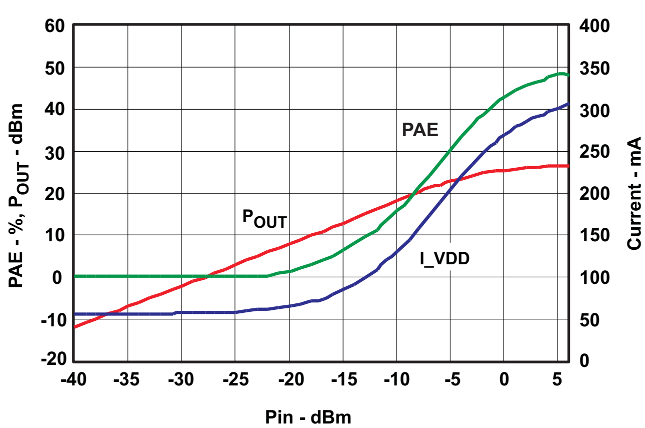


Figure 6. PA Output Power, PAE and Current Consumption vs Input Power

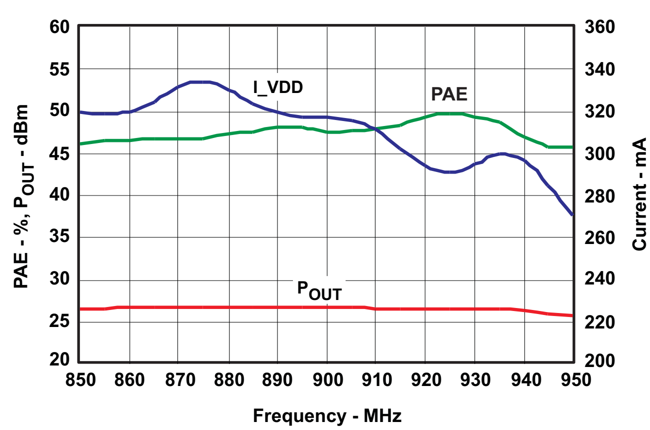


Figure 7. PA Output Power, PAE and Current Consumption vs Operating Frequency at 5 dBm Input Power

TYPICAL CHARACTERISTICS (continued)

T_C = 25°C, V_{DD} = 3 V, f_{RF} = 915 MHz (unless otherwise noted). Measured on CC1190EM reference design including external matching components optimized for 915 MHz operation.

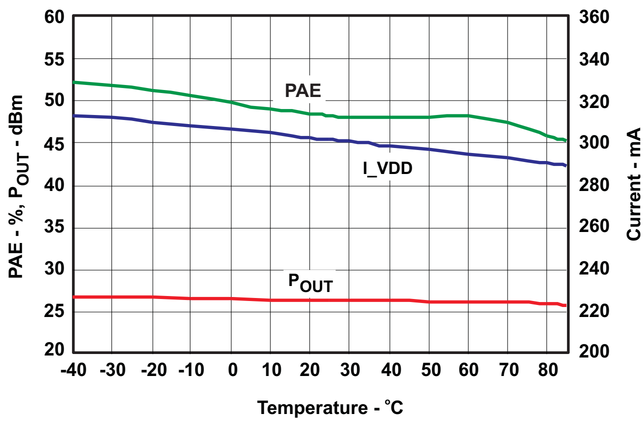


Figure 8. PA Output Power, PAE and Current Consumption vs Temperature at 5 dBm Input Power

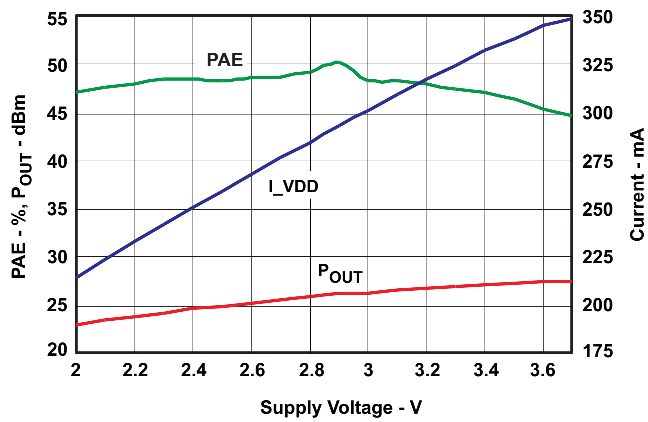


Figure 9. PA Output Power, PAE and Current Consumption vs Supply Voltage at 5 dBm Input Power

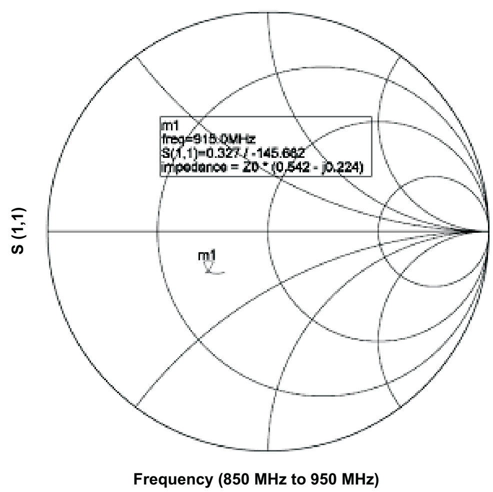


Figure 10. Input Impedance Measured at SMA connector on PA_IN/LNA_OUT on CC1190EM (TX Active)

INTERFACE AND CONTROL

Controlling the Output Power from CC1190

The output power of CC1190 is controlled by controlling the input power. The CC1190 PA is designed to work in compression (class AB), and the best efficiency is reached when a strong input signal is applied. The output power can be reduced by setting the pin HGM low. If a reduced maximum output power is wanted, the impedance seen by the PA should be increased, thus increasing the PA efficiency by changing the output matching network.

Input Levels on Control Pins

The three digital control pins (PA_EN, LNA_EN, HGM) have built-in level-shifting functionality, meaning that if CC1190 is operating from a 3.6 V supply voltage, the control pins will still sense 1.6 - 1.8 V signals as logical '1'.

An example of the above is that PA_EN is connected directly to the PA_EN pin on CC110x, but the global supply voltage is 3.6 V. The PA_EN pin on CC110x will switch between 0 V (RX) and 1.8 V (TX), and this is still a high enough voltage to control the operating mode of CC1190.

However, the input voltages should not have logical '1' level that is higher than the supply.

Connecting CC1190 to a CC102X Device

Table 2. Control Logic for Connecting CC1190 to a CC102X Device

PA_EN	LNA_EN	HGM	Mode Of Operation
0	0	don't care	Power Down
0	1	0	RX Low Gain Mode
0	1	1	RX High Gain Mode
1	0	0	TX Low Gain Mode
1	0	1	TX High Gain Mode

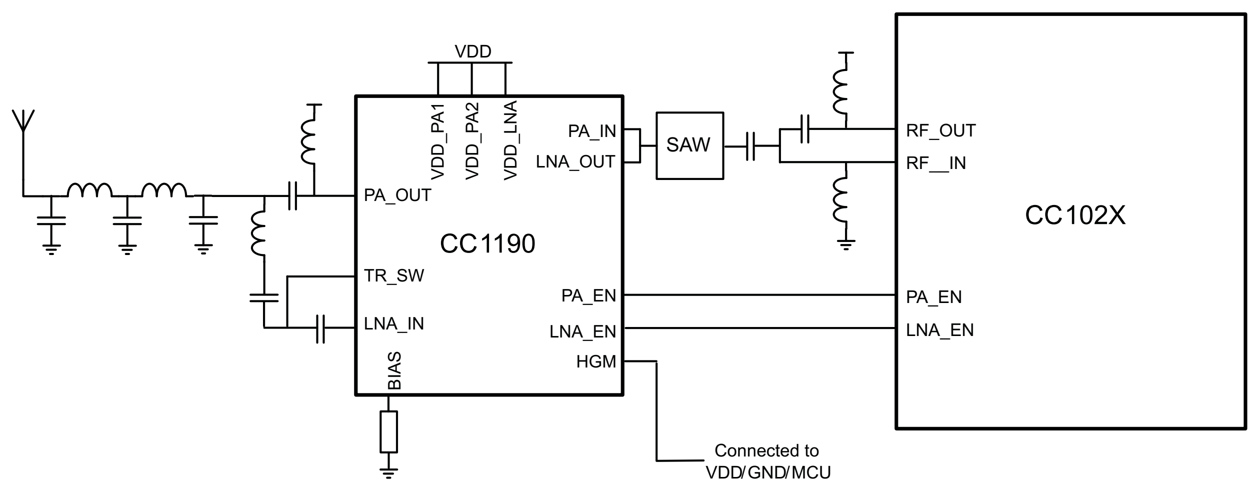


Figure 11. CC1190 + CC102X Application Circuit

Connecting CC1190 to a CC110X Device

Table 3. Control Logic for Connecting CC1190 to a CC110X Device

PA_EN	LNA_EN	HGM	Mode Of Operation
0	0	don't care	Power Down
0	1	0	RX Low Gain Mode
0	1	1	RX High Gain Mode
1	0	0	TX Low Gain Mode
1	0	1	TX High Gain Mode

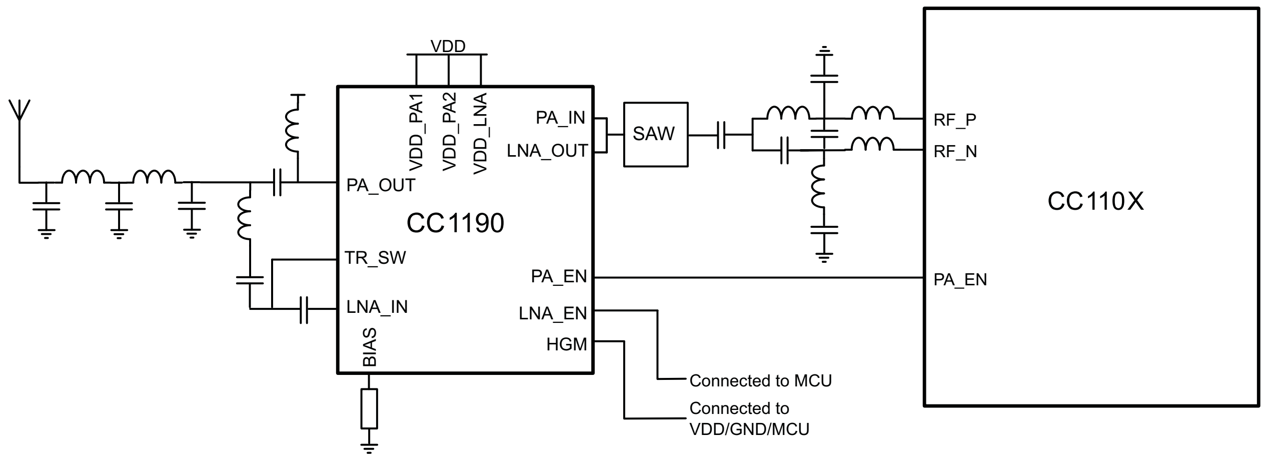


Figure 12. CC1190 + CC110X Application Circuit

Connecting CC1190 to a CC430 or CC111X Device

Table 4. Control Logic for Connecting CC1190 to a CC430 or CC111X Device

PA_EN	LNA_EN	HGM	Mode Of Operation
0	0	don't care	Power Down
0	1	0	RX Low Gain Mode
0	1	1	RX High Gain Mode
1	0	0	TX Low Gain Mode
1	0	1	TX High Gain Mode

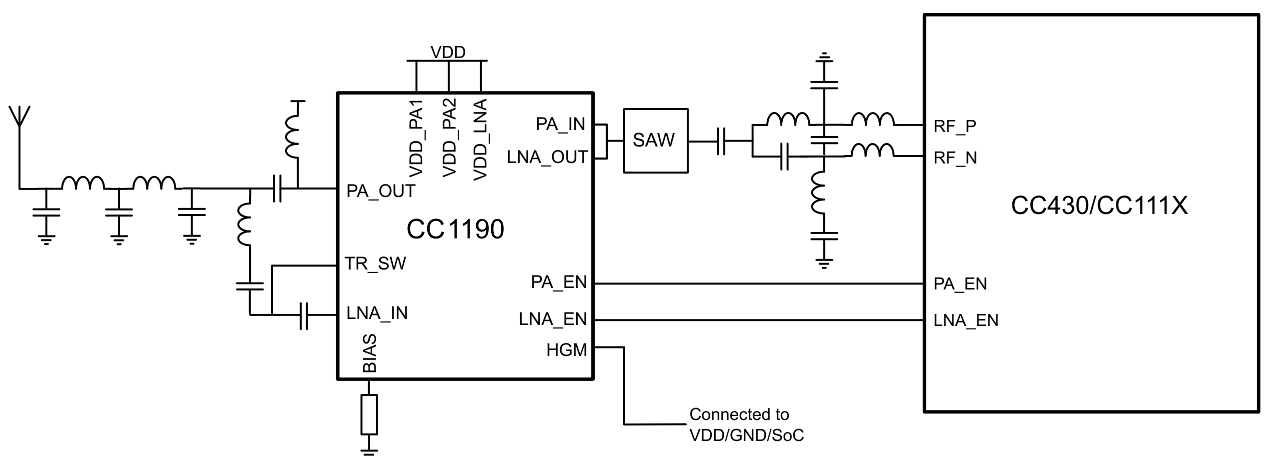


Figure 13. CC1190 + CC430/CC111X Application Circuit

REVISION HISTORY

Changes from Original (November 2009) to Revision A	Page
• Changed the data sheet from Product Preview to Production	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CC1190RGVR	ACTIVE	VQFN	RGV	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1190	Samples
CC1190RGVT	ACTIVE	VQFN	RGV	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1190	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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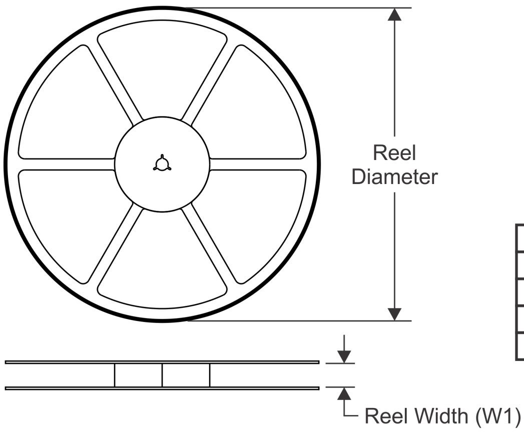
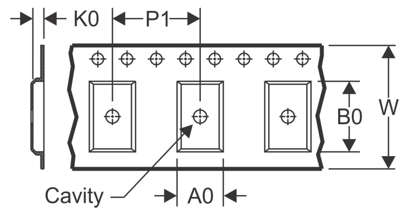
TAPE AND REEL INFORMATION

REEL DIMENSIONS

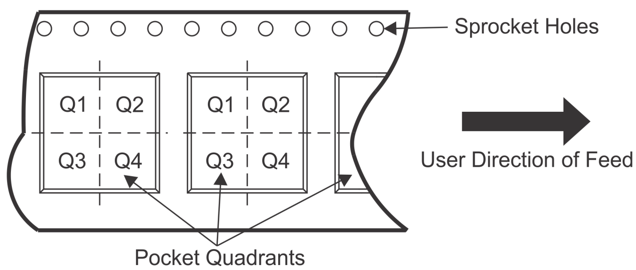


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

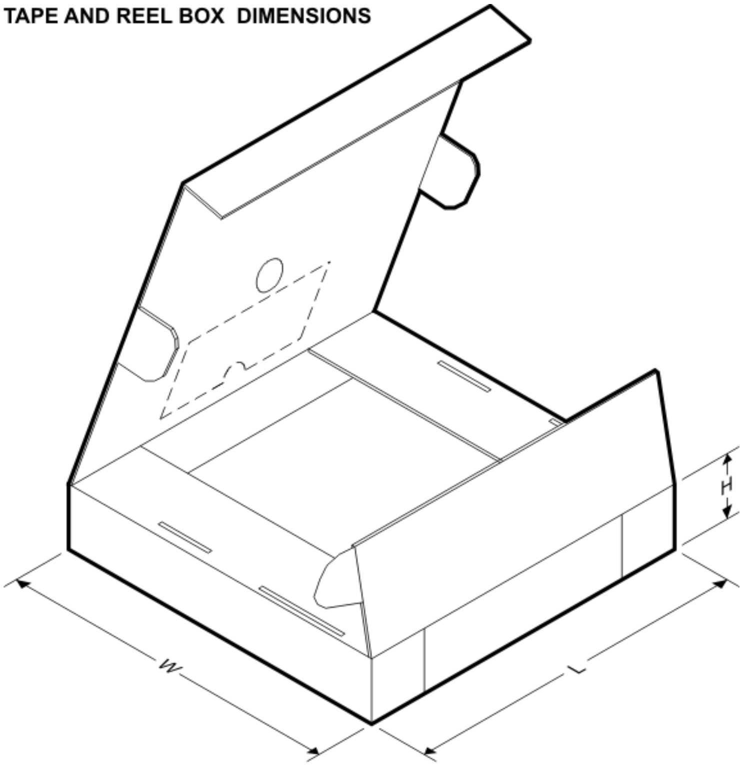
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC1190RGVR	VQFN	RGV	16	2500	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
CC1190RGVT	VQFN	RGV	16	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

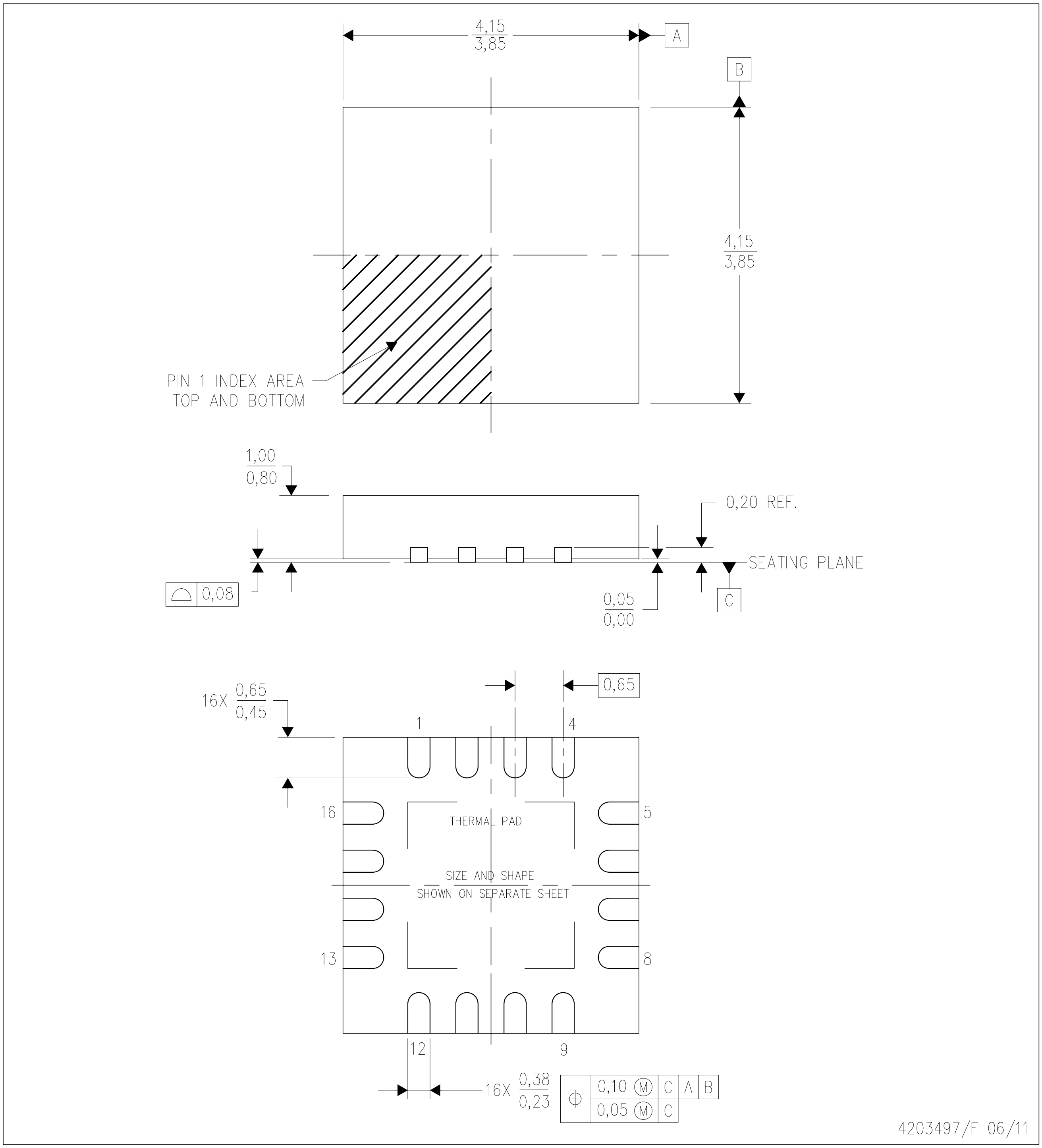
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC1190RGVR	VQFN	RGV	16	2500	338.1	338.1	20.6
CC1190RGVT	VQFN	RGV	16	250	210.0	185.0	35.0

RGV (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-220.

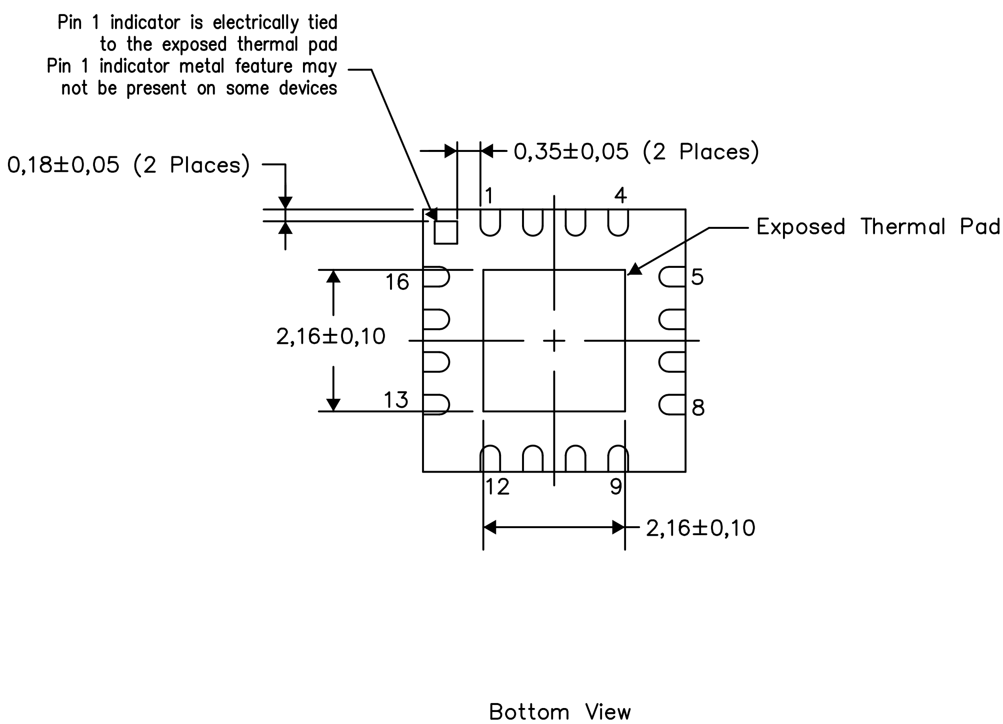
RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

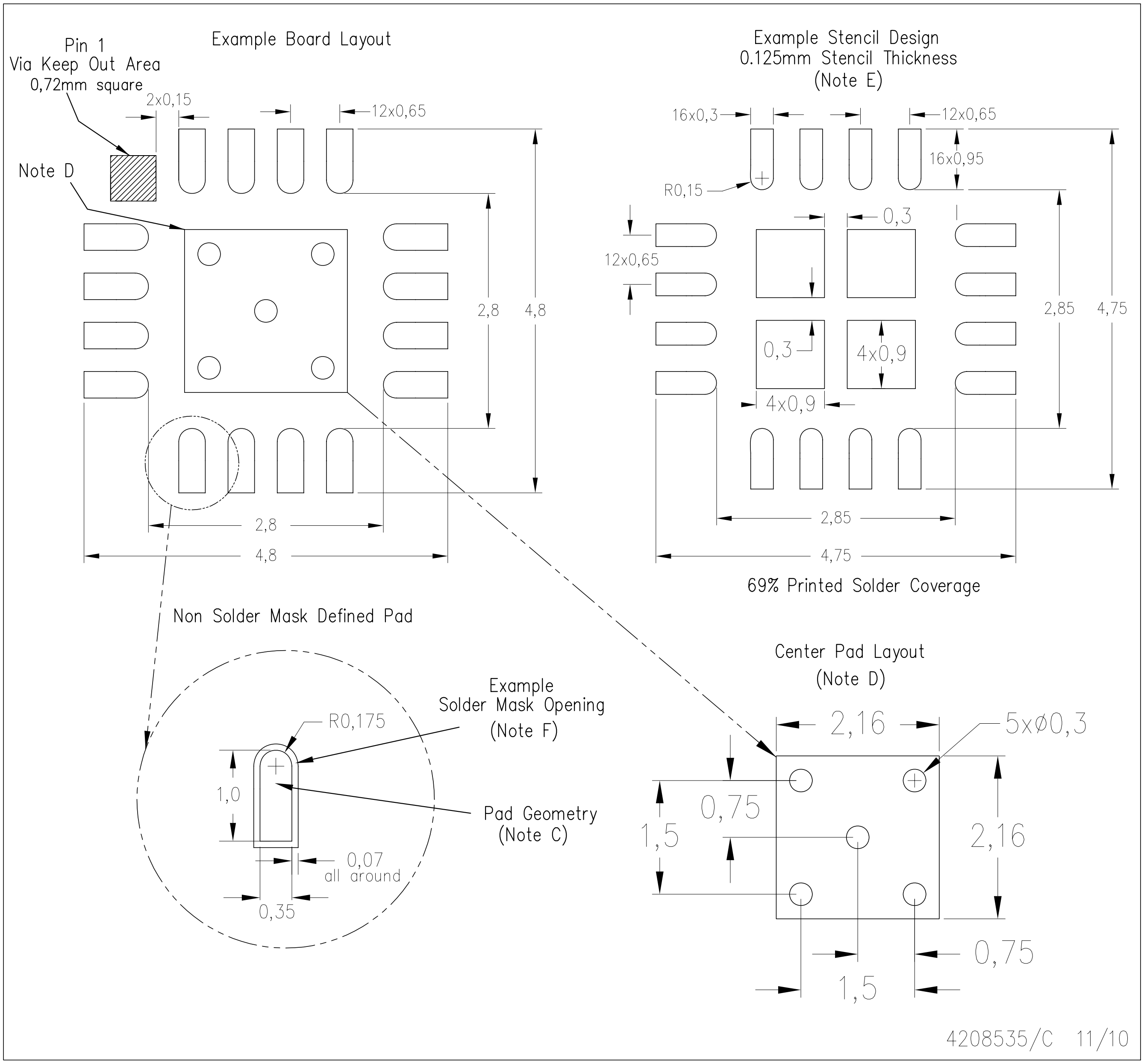


Exposed Thermal Pad Dimensions

4206351-2/K 03/13

NOTE: All linear dimensions are in millimeters

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

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Customer Service :

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Partnership :

Tel +86 (21) 64016692-8333

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